



National Semiconductor

400036

National Operational Amplifiers Databook

Operational Amplifiers

Buffers

Voltage Comparators

Active Matrix/LCD Display Drivers

Special Functions

Surface Mount



TRADEMARKS

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| ABICOM | EMBEDDED SYSTEM | MOLTE | 80CXX |
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| ALPHA | EP | MST | Series 3200 |
| ANALOG | E-2-LINK | Naked 8T | SIMPLE SWITCHER |
| APP | FACT | National | SN |
| ARM | FACT Quiet Series | National Semiconductor | SNIC |
| ASPECT | FAIRCAT | National Semiconductor | SoC |
| ATLANTIC | Falch | Corp. | SOIC |
| Auto-Chem Distributor | PAT | MAX 800 | SPK |
| BC | FAST | MAX 800 | SPR |
| BF | GEN | MAX 800 | Staggered Refresh |
| BFET | GNX | MAX 800 | STAR |
| BLIN | GTOM | MAX 800 | Starlink |
| BIP | HEX 3000 | MAX 800 | STARPLEX |
| BL | HIS | MAX 800 | ST-10 |
| BLX | HP | MAX 800 | SuperATTN |
| BMAC | Hyd | MAX 800 | Super-Block |
| Blue-Link | IL | MAX 800 | SuperChipt |
| BS | Intel | MAX 800 | SuperVOT |
| BSI-2 | Intel 128 | MAX 800 | SuperChipt |
| CDD | Intell | MAX 800 | SYST |
| CDL | Inter-ERIC | MAX 800 | Tap |
| CG | Inter-RIC | MAX 800 | TD |
| CIM | ISE | MAX 800 | Tel |
| CIMBUS | ISE 108 | MAX 800 | The National Antenna |
| CLAS | ISE 108 | MAX 800 | TinyP |
| COMBO | ISE 108 | MAX 800 | TL |
| COMBO 1 | ISE 108 | MAX 800 | Tri-Block |
| COMBO 11 | ISOP | MAX 800 | TRI-CODE |
| COPT microcontrollers | ISOP | MAX 800 | TRI-COL |
| COPT | LE | MAX 800 | TRI-SAFE |
| COPT | LM | MAX 800 | TRI-STATE |
| CROSS | MC | MAX 800 | TROPIC |
| CS | Mac | MAX 800 | Tropic Palm |
| CT | Mac | MAX 800 | Tropic Palm |
| CYCLO | MAC | MAX 800 | TURBO |
| DAT | MAR | MAX 800 | Twister |
| DEN | MAX | MAX 800 | VIP |
| DIB | Microbus data bus | MAX 800 | VR |
| DISC | MICRO-DAT | MAX 800 | WATCHDOG |
| DISTILL | Pol | MAX 800 | XMO |
| DIV | Pol | MAX 800 | XPU |
| DPV | Micro | MAX 800 | Z |
| ECMO | Micro | MAX 800 | 80386 |
| ELSTAR | Micro | MAX 800 | 80386 |

OPERATIONAL AMPLIFIERS DATABOOK

1995 Edition

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Appendices/Physical Dimensions

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| DS55451 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS55452 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS55453 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS55454 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS75451 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS75452 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS75453 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS75454 Series Dual Peripheral Driver | Section 3 | Application Specific Analog Products |
| DS75491 MOS-to-LED Quad Segment Driver | Section 4 | Application Specific Analog Products |
| DS75492 MOS-to-LED Hex Digit Driver | Section 4 | Application Specific Analog Products |
| DS75494 Hex Digit Driver | Section 4 | Application Specific Analog Products |
| Land Pattern Recommendations | Section 5 | Application Specific Analog Products |
| Land Pattern Recommendations | Section 5 | Power ICs |
| Land Pattern Recommendations | Section 9 | Data Acquisition |
| LF198 Monolithic Sample and Hold Circuit | Section 6 | Data Acquisition |
| LF298 Monolithic Sample and Hold Circuit | Section 6 | Data Acquisition |
| LF398 Monolithic Sample and Hold Circuit | Section 6 | Data Acquisition |
| LF11201 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF11202 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF11331 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF11332 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF11333 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF13006 Digital Gain Set | Section 6 | Data Acquisition |
| LF13007 Digital Gain Set | Section 6 | Data Acquisition |
| LF13201 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF13202 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF13331 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF13332 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF13333 Quad SPST JFET Analog Switch | Section 8 | Data Acquisition |
| LF13508 8-Channel Analog Multiplexer | Section 8 | Data Acquisition |
| LF13509 4-Channel Differential Analog Multiplexer | Section 8 | Data Acquisition |
| LH0070 Series BCD Buffered Reference | Section 4 | Data Acquisition |
| LH0071 Series Precision Buffered Reference | Section 4 | Data Acquisition |
| LH1605 5 Amp, High Efficiency Switching Regulator | Section 3 | Power ICs |
| LM12 80W Operational Amplifier | Section 4 | Power ICs |
| LM12H454 12-Bit + Sign Data Acquisition System with Self-Calibration | Section 1 | Data Acquisition |
| LM12H458 12-Bit + Sign Data Acquisition System with Self-Calibration | Section 1 | Data Acquisition |
| LM12L438 12-Bit + Sign Data Acquisition System with Serial I/O and Self-Calibration | Section 1 | Data Acquisition |
| LM12L454 12-Bit + Sign Data Acquisition System with Self-Calibration | Section 1 | Data Acquisition |

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| Self-Calibration | Section 1 | Data Acquisition |
| LM34 Precision Fahrenheit Temperature Sensor | Section 5 | Data Acquisition |
| LM35 Precision Centigrade Temperature Sensor | Section 5 | Data Acquisition |
| LM45 SOT-23 Precision Centigrade Temperature Sensor | Section 5 | Data Acquisition |
| LM50 Single Supply Precision Centigrade Temperature Sensor | Section 5 | Data Acquisition |
| LM78LXX Series 3-Terminal Positive Regulators | Section 1 | Power ICs |
| LM78MXX Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM78S40 Universal Switching Regulator Subsystem | Section 3 | Power ICs |
| LM78XX Series Voltage Regulators | Section 1 | Power ICs |
| LM79LXXAC Series 3-Terminal Negative Regulator | Section 1 | Power ICs |
| LM79MXX Series 3-Terminal Negative Regulators | Section 1 | Power ICs |
| LM79XX Series 3-Terminal Negative Regulators | Section 1 | Power ICs |
| LM105 Voltage Regulator | Section 1 | Power ICs |
| LM109 5-Volt Regulator | Section 1 | Power ICs |
| LM113 Reference Diode | Section 4 | Data Acquisition |
| LM117 3-Terminal Adjustable Regulator | Section 1 | Power ICs |
| LM117HV 3-Terminal Adjustable Regulator | Section 1 | Power ICs |
| LM120 Series 3-Terminal Negative Regulator | Section 1 | Power ICs |
| LM122 Precision Timer | Section 4 | Application Specific Analog Products |
| LM123 3-Amp, 5-Volt Positive Regulator | Section 1 | Power ICs |
| LM125 Dual Voltage Regulator | Section 1 | Power ICs |
| LM129 Precision Reference | Section 4 | Data Acquisition |
| LM131 Precision Voltage-to-Frequency Converter | Section 2 | Data Acquisition |
| LM133 3-Amp Adjustable Negative Regulator | Section 1 | Power ICs |
| LM134 3-Terminal Adjustable Current Source | Section 4 | Data Acquisition |
| LM134 3-Terminal Adjustable Current Source | Section 5 | Data Acquisition |
| LM135 Precision Temperature Sensor | Section 5 | Data Acquisition |
| LM136-2.5V Reference Diode | Section 4 | Data Acquisition |
| LM136-5.0V Reference Diode | Section 4 | Data Acquisition |
| LM137 3-Terminal Adjustable Negative Regulator | Section 1 | Power ICs |
| LM137HV 3-Terminal Adjustable Negative Regulator (High Voltage) | Section 1 | Power ICs |
| LM138 5-Amp Adjustable Regulator | Section 1 | Power ICs |
| LM140 Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM140L Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM145 Negative 3-Amp Regulator | Section 1 | Power ICs |
| LM150 3-Amp Adjustable Regulator | Section 1 | Power ICs |
| LM169 Precision Voltage Reference | Section 4 | Data Acquisition |
| LM185 Adjustable Micropower Voltage Reference | Section 4 | Data Acquisition |
| LM185-1.2 Micropower Voltage Reference Diode | Section 4 | Data Acquisition |
| LM185-2.5 Micropower Voltage Reference Diode | Section 4 | Data Acquisition |
| LM199 Precision Reference | Section 4 | Data Acquisition |
| LM205 Voltage Regulator | Section 1 | Power ICs |
| LM231 Precision Voltage-to-Frequency Converter | Section 2 | Data Acquisition |
| LM234 3-Terminal Adjustable Current Source | Section 4 | Data Acquisition |
| LM234 3-Terminal Adjustable Current Source | Section 5 | Data Acquisition |
| LM235 Precision Temperature Sensor | Section 5 | Data Acquisition |
| LM236-2.5V Reference Diode | Section 4 | Data Acquisition |

Additional Available Linear Devices (Continued)

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| LM236-5.0V Reference Diode | Section 4 | Data Acquisition |
| LM285 Adjustable Micropower Voltage Reference | Section 4 | Data Acquisition |
| LM285-1.2 Micropower Voltage Reference Diode | Section 4 | Data Acquisition |
| LM285-2.5 Micropower Voltage Reference Diode | Section 4 | Data Acquisition |
| LM299 Precision Reference | Section 4 | Data Acquisition |
| LM305 Voltage Regulator | Section 1 | Power ICs |
| LM309 5-Volt Regulator | Section 1 | Power ICs |
| LM313 Reference Diode | Section 4 | Data Acquisition |
| LM317 3-Terminal Adjustable Regulator | Section 1 | Power ICs |
| LM317HV 3-Terminal Adjustable Regulator | Section 1 | Power ICs |
| LM317L 3-Terminal Adjustable Regulator | Section 1 | Power ICs |
| LM320 Series 3-Terminal Negative Regulator | Section 1 | Power ICs |
| LM320L Series 3-Terminal Negative Regulator | Section 1 | Power ICs |
| LM322 Precision Timer | Section 4 | Application Specific Analog Products |
| LM323 3-Amp, 5-Volt Positive Regulator | Section 1 | Power ICs |
| LM325 Dual Voltage Regulator | Section 1 | Power ICs |
| LM329 Precision Reference | Section 4 | Data Acquisition |
| LM330 3-Terminal Positive Regulator | Section 2 | Power ICs |
| LM331 Precision Voltage-to-Frequency Converter | Section 2 | Data Acquisition |
| LM333 3-Amp Adjustable Negative Regulator | Section 1 | Power ICs |
| LM334 3-Terminal Adjustable Current Source | Section 4 | Data Acquisition |
| LM334 3-Terminal Adjustable Current Source | Section 5 | Data Acquisition |
| LM335 Precision Temperature Sensor | Section 5 | Data Acquisition |
| LM336-2.5V Reference Diode | Section 4 | Data Acquisition |
| LM336-5.0V Reference Diode | Section 4 | Data Acquisition |
| LM337 3-Terminal Adjustable Negative Regulator | Section 1 | Power ICs |
| LM337HV 3-Terminal Adjustable Negative Regulator (High Voltage) | Section 1 | Power ICs |
| LM337L 3-Terminal Adjustable Regulator | Section 1 | Power ICs |
| LM338 5-Amp Adjustable Regulator | Section 1 | Power ICs |
| LM340 Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM340L Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM341 Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM345 Negative 3-Amp Regulator | Section 1 | Power ICs |
| LM350 3-Amp Adjustable Regulator | Section 1 | Power ICs |
| LM368-2.5 Precision Voltage Reference | Section 4 | Data Acquisition |
| LM368-5.0 Precision Voltage Reference | Section 4 | Data Acquisition |
| LM368-10 Precision Voltage Reference | Section 4 | Data Acquisition |
| LM369 Precision Voltage Reference | Section 4 | Data Acquisition |
| LM376 Voltage Regulator | Section 1 | Power ICs |
| LM380 Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM383 7W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM384 5W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM385 Adjustable Micropower Voltage Reference | Section 4 | Data Acquisition |
| LM385-1.2 Micropower Voltage Reference Diode | Section 4 | Data Acquisition |
| LM385-2.5 Micropower Voltage Reference Diode | Section 4 | Data Acquisition |
| LM386 Low Voltage Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM387/LM387A Low Noise Dual Preamplifier | Section 1 | Application Specific Analog Products |
| LM388 1.5W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM389 Low-Voltage Audio Power Amplifier with NPN Transistor Array | Section 1 | Application Specific Analog Products |

Additional Available Linear Devices (Continued)

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| LM390 1W Battery Operated Audio Power Amplifier . . . | Section 1 | Application Specific Analog Products |
| LM391 Audio Power Driver . . . | Section 1 | Application Specific Analog Products |
| LM399 Precision Reference . . . | Section 4 | Data Acquisition |
| LM431A Adjustable Precision Zener Shunt Regulator . . | Section 3 | Power ICs |
| LM555 Timer . . . | Section 4 | Application Specific Analog Products |
| LM555C Timer . . . | Section 4 | Application Specific Analog Products |
| LM556 Dual Timer . . . | Section 4 | Application Specific Analog Products |
| LM556C Dual Timer . . . | Section 4 | Application Specific Analog Products |
| LM565 Phase Locked Loop . . . | Section 4 | Application Specific Analog Products |
| LM565C Phase Locked Loop . . . | Section 4 | Application Specific Analog Products |
| LM566C Voltage Controlled Oscillator . . . | Section 4 | Application Specific Analog Products |
| LM567 Tone Decoder . . . | Section 4 | Application Specific Analog Products |
| LM567C Tone Decoder . . . | Section 4 | Application Specific Analog Products |
| LM628 Precision Motion Controller . . . | Section 4 | Power ICs |
| LM629 Precision Motion Controller . . . | Section 4 | Power ICs |
| LM723 Voltage Regulator . . . | Section 1 | Power ICs |
| LM831 Low Voltage Audio Power Amplifier . . . | Section 1 | Application Specific Analog Products |
| LM833 Dual Audio Operational Amplifier . . . | Section 1 | Application Specific Analog Products |
| LM837 Low Noise Quad Operational Amplifier . . . | Section 1 | Application Specific Analog Products |
| LM903 Fluid Level Detector . . . | Section 3 | Application Specific Analog Products |
| LM1036 Dual DC Operated Tone/Volume/Balance Circuit . . . | Section 1 | Application Specific Analog Products |
| LM1042 Fluid Level Detector . . . | Section 3 | Application Specific Analog Products |
| LM1131 Dual Dolby B-Type Noise Reduction Processor . . . | Section 1 | Application Specific Analog Products |
| LM1201 Video Amplifier System . . . | Section 2 | Application Specific Analog Products |
| LM1202 230 MHz Video Amplifier System . . . | Section 2 | Application Specific Analog Products |
| LM1203 RGB Video Amplifier System . . . | Section 2 | Application Specific Analog Products |
| LM1203A 150 MHz RGB Video Amplifier System . . . | Section 2 | Application Specific Analog Products |
| LM1203B 100 MHz RGB Video Amplifier System . . . | Section 2 | Application Specific Analog Products |
| LM1204 150 MHz RGB Video Amplifier System . . . | Section 2 | Application Specific Analog Products |
| LM1205 130 MHz RGB Video Amplifier System with Blanking . . . | Section 2 | Application Specific Analog Products |
| LM1207 85 MHz RGB Video Amplifier System with Blanking . . . | Section 2 | Application Specific Analog Products |
| LM1208 130 MHz RGB Video Amplifier System with Blanking . . . | Section 2 | Application Specific Analog Products |
| LM1209 100 MHz RGB Video Amplifier System with Blanking . . . | Section 2 | Application Specific Analog Products |
| LM1212 230 MHz Video Amplifier System with OSD Blanking . . . | Section 2 | Application Specific Analog Products |
| LM1281 85 MHz RGB Video Amplifier System with On Screen Display (OSD) . . . | Section 2 | Application Specific Analog Products |
| LM1291 Video PLL System for Continuous Sync Monitors . . . | Section 2 | Application Specific Analog Products |
| LM1295 DC Controlled Geometry Correction System for Continuous Sync Monitors . . . | Section 2 | Application Specific Analog Products |
| LM1391 Phase-Locked Loop . . . | Section 2 | Application Specific Analog Products |
| LM1496 Balanced Modulator-Demodulator . . . | Section 4 | Application Specific Analog Products |
| LM1575 SIMPLE SWITCHER 1A Step-Down Voltage Regulator . . . | Section 3 | Power ICs |

Additional Available Linear Devices (Continued)

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| LM1575HV SIMPLE SWITCHER 1A Step-Down Voltage Regulator | Section 3 | Power ICs |
| LM1577 SIMPLE SWITCHER Step-Up Voltage Regulator | Section 3 | Power ICs |
| LM1577 SIMPLE SWITCHER Step-Up Voltage Regulator | Section 3 | Application Specific Analog Products |
| LM1578A Switching Regulator | Section 3 | Power ICs |
| LM1596 Balanced Modulator-Demodulator | Section 4 | Application Specific Analog Products |
| LM1815 Adaptive Variable Reluctance Sensor Amplifier | Section 3 | Application Specific Analog Products |
| LM1819 Air-Core Meter Driver | Section 3 | Application Specific Analog Products |
| LM1823 Video IF Amplifier/PLL Detector System | Section 2 | Application Specific Analog Products |
| LM1830 Fluid Detector | Section 3 | Application Specific Analog Products |
| LM1851 Ground Fault Interrupter | Section 4 | Application Specific Analog Products |
| LM1865 Advanced FM IF System | Section 4 | Application Specific Analog Products |
| LM1868 AM/FM Radio System | Section 4 | Application Specific Analog Products |
| LM1875 20W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM1876 Dual 20W Audio Power Amplifier with Mute and Standby Modes | Section 1 | Application Specific Analog Products |
| LM1877 Dual Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM1881 Video Sync Separator | Section 2 | Application Specific Analog Products |
| LM1882 Programmable Video Sync Generator | Section 2 | Application Specific Analog Products |
| LM1893 Carrier-Current Transceiver | Section 4 | Application Specific Analog Products |
| LM1894 Dynamic Noise Reduction System DNR® | Section 1 | Application Specific Analog Products |
| LM1896 Dual Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM1921 1 Amp Industrial Switch | Section 3 | Application Specific Analog Products |
| LM1946 Over/Under Current Limit Diagnostic Circuit | Section 3 | Application Specific Analog Products |
| LM1949 Injector Drive Controller | Section 3 | Application Specific Analog Products |
| LM1950 750 mA High Side Switch | Section 3 | Application Specific Analog Products |
| LM1951 Solid State 1 Amp Switch | Section 3 | Application Specific Analog Products |
| LM1971 μ Pot 62 dB Digitally Controlled Audio Attenuator with Mute | Section 1 | Application Specific Analog Products |
| LM1972 μ Pot 2-Channel 78 dB Audio Attenuator with Mute | Section 1 | Application Specific Analog Products |
| LM1973 μ Pot 3-Channel 76 dB Audio Attenuator with Mute | Section 1 | Application Specific Analog Products |
| LM2416 Triple 50 MHz CRT Driver | Section 2 | Application Specific Analog Products |
| LM2416C Triple 50 MHz CRT Driver | Section 2 | Application Specific Analog Products |
| LM2418 Triple 30 MHz CRT Driver | Section 2 | Application Specific Analog Products |
| LM2419 Triple 65 MHz CRT Driver | Section 2 | Application Specific Analog Products |
| LM2427 Triple 80 MHz CRT Driver | Section 2 | Application Specific Analog Products |
| LM2524D Regulating Pulse Width Modulator | Section 3 | Power ICs |
| LM2574 SIMPLE SWITCHER 0.5A Step-Down Voltage Regulator | Section 3 | Power ICs |
| LM2574HV SIMPLE SWITCHER 0.5A Step-Down Voltage Regulator | Section 3 | Power ICs |
| LM2575 SIMPLE SWITCHER 1A Step-Down Voltage Regulator | Section 3 | Power ICs |
| LM2575HV SIMPLE SWITCHER 1A Step-Down Voltage Regulator | Section 3 | Power ICs |

Additional Available Linear Devices (Continued)

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| LM2576 SIMPLE SWITCHER 3A Step-Down Voltage Regulator | Section 3 | Power ICs |
| LM2576HV SIMPLE SWITCHER 3A Step-Down Voltage Regulator | Section 3 | Power ICs |
| LM2577 SIMPLE SWITCHER Step-Up Voltage Regulator | Section 3 | Power ICs |
| LM2577 SIMPLE SWITCHER Step-Up Voltage Regulator | Section 3 | Power ICs |
| LM2578A Switching Regulator | Section 3 | Application Specific Analog Products |
| LM2587 SIMPLE SWITCHER 5A Flyback Regulator | Section 3 | Power ICs |
| LM2876 High-Performance 40W Audio Power Amplifier with Mute | Section 1 | Application Specific Analog Products |
| LM2877 Dual 4W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM2878 Dual 5W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM2879 Dual 8W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM2889 TV Video Modulator | Section 2 | Application Specific Analog Products |
| LM2893 Carrier-Current Transceiver | Section 4 | Application Specific Analog Products |
| LM2896 Dual Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM2907 Frequency to Voltage Converter | Section 3 | Application Specific Analog Products |
| LM2917 Frequency to Voltage Converter | Section 3 | Application Specific Analog Products |
| LM2925 Low Dropout Regulator with Delayed Reset | Section 3 | Application Specific Analog Products |
| LM2925 Low Dropout Regulator with Delayed Reset | Section 2 | Power ICs |
| LM2926 Low Dropout Regulator with Delayed Reset | Section 3 | Application Specific Analog Products |
| LM2927 Low Dropout Regulator with Delayed Reset | Section 3 | Application Specific Analog Products |
| LM2927 Low Dropout Regulator with Delayed Reset | Section 2 | Power ICs |
| LM2930 3-Terminal Positive Regulator | Section 2 | Power ICs |
| LM2931 Series Low Dropout Regulators | Section 2 | Power ICs |
| LM2931 Series Low Dropout Regulators | Section 3 | Application Specific Analog Products |
| LM2935 Low Dropout Dual Regulator | Section 3 | Application Specific Analog Products |
| LM2935 Low Dropout Dual Regulator | Section 2 | Power ICs |
| LM2936 Ultra-Low Quiescent Current 5V Regulator | Section 2 | Power ICs |
| LM2936 Ultra-Low Quiescent Current 5V Regulator | Section 3 | Application Specific Analog Products |
| LM2937 500 mA Low Dropout Regulator | Section 3 | Application Specific Analog Products |
| LM2937 500 mA Low Dropout Regulator | Section 2 | Power ICs |
| LM2940/LM2940C 1A Low Dropout Regulators | Section 2 | Power ICs |
| LM2940/LM2940C 1A Low Dropout Regulators | Section 3 | Application Specific Analog Products |
| LM2941/LM2941C 1A Low Dropout Adjustable Regulators | Section 2 | Power ICs |
| LM2984 Microprocessor Power Supply System | Section 2 | Power ICs |
| LM2984 Microprocessor Power Supply System | Section 3 | Application Specific Analog Products |
| LM2990 Negative Low Dropout Regulator | Section 2 | Power ICs |
| LM2991 Negative Low Dropout Adjustable Regulator | Section 2 | Power ICs |
| LM3001 Primary-Side PWM Driver | Section 3 | Power ICs |
| LM3101 Secondary-Side PWM Controller | Section 3 | Power ICs |
| LM3411 Precision Secondary Regulator/Driver | Section 3 | Power ICs |
| LM3420-4.2, -8.4, -12.6 Lithium-Ion Battery Charge Controller | Section 2 | Power ICs |
| LM3524D Regulating Pulse Width Modulator | Section 3 | Power ICs |
| LM3578A Switching Regulator | Section 3 | Power ICs |

Additional Available Linear Devices (Continued)

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| LM3875 High Performance 56W Audio Power Amplifier | Section 1 | Application Specific Analog Products |
| LM3876 High Performance 56W Audio Power Amplifier with Mute | Section 1 | Application Specific Analog Products |
| LM3886 High-Performance 68W Audio Power Amplifier with Mute | Section 1 | Application Specific Analog Products |
| LM3905 Precision Timer | Section 4 | Application Specific Analog Products |
| LM3909 LED Flasher/Oscillator | Section 4 | Application Specific Analog Products |
| LM3914 Dot/Bar Display Driver | Section 4 | Application Specific Analog Products |
| LM3915 Dot/Bar Display Driver | Section 4 | Application Specific Analog Products |
| LM3916 Dot/Bar Display Driver | Section 4 | Application Specific Analog Products |
| LM3940 1A Low Dropout Regulator for 5V to 3.3V Conversion | Section 2 | Power ICs |
| LM3999 Precision Reference | Section 4 | Data Acquisition |
| LM4040 Precision Micropower Shunt Voltage Reference | Section 4 | Data Acquisition |
| LM4041 Precision Micropower Shunt Voltage Reference | Section 4 | Data Acquisition |
| LM4431 Micropower Shunt Voltage Reference | Section 4 | Data Acquisition |
| LM4700 Overture™ 30W Audio Power Amplifier with Mute and Standby Modes | Section 1 | Application Specific Analog Products |
| LM4860 1W Audio Power Amplifier with Shutdown Mode | Section 1 | Application Specific Analog Products |
| LM4861 1/2W Audio Power Amplifier with Shutdown Mode | Section 1 | Application Specific Analog Products |
| LM4862 350 mW Audio Power Amplifier with Shutdown Mode | Section 1 | Application Specific Analog Products |
| LM4880 Dual 200 mW Audio Power Amplifier with Shutdown Mode | Section 1 | Application Specific Analog Products |
| LM6104 Quad Gray Scale Current Feedback Amplifier | Section 2 | Application Specific Analog Products |
| LM6121 High Speed Buffer | Section 2 | Application Specific Analog Products |
| LM6125 High Speed Buffer | Section 2 | Application Specific Analog Products |
| LM6142 Dual High Speed/Low Power 17 MHz Rail-to-Rail Input-Output Operational Amplifier | Section 1 | Application Specific Analog Products |
| LM6144 Quad High Speed/Low Power 17 MHz Rail-to-Rail Input-Output Operational Amplifier | Section 1 | Application Specific Analog Products |
| LM6152 Dual High Speed/Low Power 45 MHz Rail-to-Rail I/O Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6154 Quad High Speed/Low Power 45 MHz Rail-to-Rail I/O Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6161 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6162 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6164 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6165 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6171 Voltage Feedback Low Distortion Low Power Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6181 100 mA, 100 MHz Current Feedback Amplifier | Section 2 | Application Specific Analog Products |
| LM6182 Dual 100 mA Output, 100 MHz Dual Current Feedback Amplifier | Section 2 | Application Specific Analog Products |

Additional Available Linear Devices (Continued)

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| LM6221 High Speed Buffer | Section 2 | Application Specific Analog Products |
| LM6225 High Speed Buffer | Section 2 | Application Specific Analog Products |
| LM6261 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6262 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6264 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6265 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6321 High Speed Buffer | Section 2 | Application Specific Analog Products |
| LM6325 High Speed Buffer | Section 2 | Application Specific Analog Products |
| LM6361 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6362 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6364 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM6365 High Speed Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM7131 Tiny High Speed Single Supply Operational Amplifier | Section 2 | Application Specific Analog Products |
| LM7171 Very High Speed High Output Current Voltage Feedback Amplifier | Section 2 | Application Specific Analog Products |
| LM7800C Series 3-Terminal Positive Regulator | Section 1 | Power ICs |
| LM8305 STN LCD Display Bias Voltage Source | Section 2 | Application Specific Analog Products |
| LM9044 Lambda Sensor Interface Amplifier | Section 3 | Application Specific Analog Products |
| LM9061 Power MOSFET Driver with Lossless Protection | Section 3 | Application Specific Analog Products |
| LM9140 Precision Micropower Shunt Voltage Reference | Section 4 | Data Acquisition |
| LM12434 12-Bit + Sign Data Acquisition System with Serial I/O and Self-Calibration | Section 1 | Data Acquisition |
| LM12454 12-Bit + Sign Data Acquisition System with Self-Calibration | Section 1 | Data Acquisition |
| LM12458 12-Bit + Sign Data Acquisition System with Self-Calibration | Section 1 | Data Acquisition |
| LM18293 Four Channel Push-Pull Driver | Section 4 | Power ICs |
| LMC555 CMOS Timer | Section 4 | Application Specific Analog Products |
| LMC567 Low Power Tone Decoder | Section 4 | Application Specific Analog Products |
| LMC568 Low Power Phase-Locked Loop | Section 4 | Application Specific Analog Products |
| LMC835 Digital Controlled Graphic Equalizer | Section 1 | Application Specific Analog Products |
| LMC1982 Digitally-Controlled Stereo Tone and Volume Circuit with Two Selectable Stereo Inputs | Section 1 | Application Specific Analog Products |
| LMC1983 Digitally-Controlled Stereo Tone and Volume Circuit with Three Selectable Stereo Inputs | Section 1 | Application Specific Analog Products |
| LMC1992 Digitally-Controlled Stereo Tone and Volume Circuit with Four-Channel Input-Selector | Section 1 | Application Specific Analog Products |
| LMC6008 8 Channel Buffer | Section 2 | Application Specific Analog Products |
| LMC7660 Switched Capacitor Voltage Converter | Section 3 | Power ICs |
| LMD18200 3A, 55V H-Bridge | Section 4 | Power ICs |
| LMD18201 3A, 55V H-Bridge | Section 4 | Power ICs |
| LMD18245 3A, 55V DMOS Full-Bridge Motor Driver | Section 4 | Power ICs |
| LMD18400 Quad High Side Driver | Section 3 | Application Specific Analog Products |
| LMF40 High Performance 4th-Order Switched Capacitor Butterworth Low-Pass Filter | Section 7 | Data Acquisition |
| LMF60 High Performance 6th-Order Switched Capacitor Butterworth Low-Pass Filter | Section 7 | Data Acquisition |
| LMF90 4th-Order Elliptic Notch Filter | Section 7 | Data Acquisition |

Additional Available Linear Devices (Continued)

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| LMF100 High Performance Dual Switched Capacitor Filter | Section 7 | Data Acquisition |
| LMF380 Triple One-Third Octave Switched Capacitor Active Filter | Section 7 | Data Acquisition |
| LP2950/A-XX Series of Adjustable Micropower Voltage Regulators | Section 3 | Application Specific Analog Products |
| LP2950/A-XX Series of Adjustable Micropower Voltage Regulators | Section 2 | Power ICs |
| LP2951/A-XX Series of Adjustable Micropower Voltage Regulators | Section 2 | Power ICs |
| LP2951/A-XX Series of Adjustable Micropower Voltage Regulators | Section 3 | Application Specific Analog Products |
| LP2952 Adjustable Micropower Low-Dropout Voltage Regulator | Section 2 | Power ICs |
| LP2953 Adjustable Micropower Low-Dropout Voltage Regulator | Section 2 | Power ICs |
| LP2954 5V Micropower Low-Dropout Voltage Regulator | Section 2 | Power ICs |
| LP2956 Dual Micropower Low-Dropout Voltage Regulator | Section 2 | Power ICs |
| LP2957 5V Low-Dropout Regulator for μ P Applications | Section 2 | Power ICs |
| LP2980 Micropower SOT, 50 mA Ultra Low-Dropout Regulator | Section 2 | Power ICs |
| MF4 4th Order Switched Capacitor Butterworth Lowpass Filter | Section 7 | Data Acquisition |
| MF5 Universal Monolithic Switched Capacitor Filter | Section 7 | Data Acquisition |
| MF6 6th Order Switched Capacitor Butterworth Lowpass Filter | Section 7 | Data Acquisition |
| MF8 4th Order Switched Capacitor Bandpass Filter | Section 7 | Data Acquisition |
| MF10 Universal Monolithic Dual Switched Capacitor Filter | Section 7 | Data Acquisition |
| MM5368 CMOS Oscillator Divider Circuit | Section 4 | Application Specific Analog Products |
| MM5369 17 Stage Oscillator/Divider | Section 4 | Application Specific Analog Products |
| MM5450 LED Display Driver | Section 4 | Application Specific Analog Products |
| MM5451 LED Display Driver | Section 4 | Application Specific Analog Products |
| MM5452 Liquid Crystal Display Driver | Section 4 | Application Specific Analog Products |
| MM5453 Liquid Crystal Display Driver | Section 4 | Application Specific Analog Products |
| MM5480 LED Display Driver | Section 4 | Application Specific Analog Products |
| MM5481 LED Display Driver | Section 4 | Application Specific Analog Products |
| MM5483 Liquid Crystal Display Driver | Section 4 | Application Specific Analog Products |
| MM5484 16-Segment LED Display Driver | Section 4 | Application Specific Analog Products |
| MM5486 LED Display Driver | Section 4 | Application Specific Analog Products |
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| MM58341 High Voltage Display Driver | Section 4 | Application Specific Analog Products |
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Packing Considerations (Methods, Materials and Recycling)

Recommended Soldering Profiles—Surface Mount

Recommended Soldering Profiles—Surface Mount

Recommended Soldering Profiles—Surface Mount

Data Acquisition

Data Acquisition

Power ICs

Application Specific Analog Products

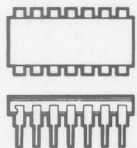
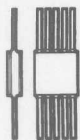

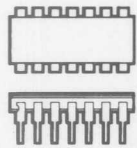
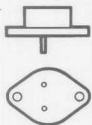
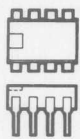
| NSC | NSC A ₁₁ | Signetics | Motorola | TI | AND | Specials | |
|-----|---------------------|-------------|----------|------|-----|----------|---|
| D | D | I | L | | D | R | 4-16 Lead Glass/Metal DIP |
| F | F | Q | F | F, S | F | | Glass/Metal Flat Pack |
| H | H | T, K, L, DB | G | L | H | | TO-66, TO-100, TO-8 |
| J | R, D | F | U | J | D | H | 8-, 14- and 16-Lead Low Temperature Ceramic DIP |
| K | K | KS | K | K | | | TO-3 (Steel) |
| KC | K | DA | K | | | | TO-3 (Aluminum) |
| N | T, P | N, V | P | P, N | P | A, B, M | 8-, 14- and 16-Lead Plastic DIP |

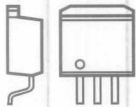
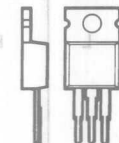
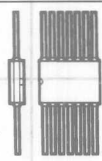

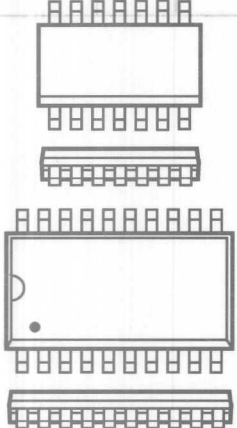

Inquiry package cross-reference guide



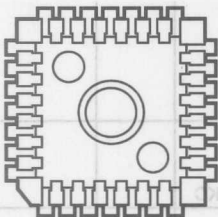
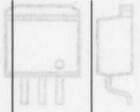
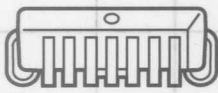

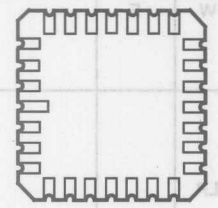

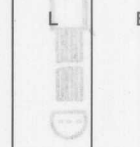




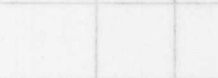

National Semiconductor

Industry Package Cross-Reference Guide

| | NSC | NSC μ A | Signetics | Motorola | TI | AMD | Sprague |
|--|-----|----------------|----------------------|----------|---------|-----|---------------|
|  4/16 Lead Glass/Metal DIP | D | D | I | L | | D | R |
|  Glass/Metal Flat Pack | F | F | Q | F | F, S | F | |
|  TO-99, TO-100, TO-5 | H | H | T, K, L, DB | G | L | H | |
|  8-, 14- and 16-Lead Low Temperature Ceramic DIP | J | R, D | F | U | J | D | H |
|  TO-3 (Steel) (Aluminum) | K | | | KS | | | |
| | KC | K | DA | K | K | | |
|  8-, 14- and 16-Lead Plastic DIP | N | T, P | N, V | P | P, N | P | A, B, M |

| Sprague | AMD | TI | Motorola | NSC | NSC μ A | Signetics | Motorola | TI | AMD | Sprague |
|---|-----|----|--|-----|----------------|-----------|----------|----|-----|---------|
|  | | | TO-263 3- & 5-Lead | S | | | | | | |
|  | | | TO-220 3- & 5-Lead | T | U | U | | KC | | |
| | | | TO-220 11-, 15- & 23-Lead | T | | | | | | |
|  | | | Low Temperature Glass Hermetic Flat Pack | W | F | | F | W | F | |
|  | | | TO-92 (Plastic) | Z | W | S | P | LP | | |
|  | | | SO (Narrow Body) | M | S | S, D | D | D | | L |
| | | | (Wide Body) | WM | | | | DW | | LW |
|  | | | SOT-23 5-Lead | M5 | | | | | | |

Industry Package Cross-Reference

| | | | | | | | | | |
|---|---|--|---|----|---|----|--------------|---|----|
|  | PCC | | V | Q | A | FN | FN |  | EP |
| | | | | | | | | | |
|  | LCC Leadless Ceramic Chip Carrier | | E | L1 | G | U | FK/ FG/FH |  | EK |
|  | | | | | | | | | |
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Section 1 Operational Amplifiers



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Operational Amplifiers

Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental. % harmonic distortion =

$$\frac{(V_2^2 + V_3^2 + V_4^2 + \dots)^{1/2}}{V_1} (100)$$

where V_1 is the rms amplitude of the fundamental and V_2 , V_3 , V_4 , ... are the rms amplitudes of the individual harmonics.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Output Impedance: The ratio of output voltage to output current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Unity Gain Bandwidth: The frequency range from dc to the frequency where the amplifier open loop gain rolls off to one.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).



General Purpose Operational Amplifier Selection Guide

Automotive Temperature Range (-40°C to $+85^{\circ}\text{C}$) Specs at $T_A = 25^{\circ}\text{C}$ (Note 1)

| Part # | V_{OS} mV (Max) | I_B nA (Max) | GBW MHz (Typ) | Slew Rate $V/\mu\text{s}$ (Typ) | Supply Current (Note 3) mA (Max) | Specified Supply Voltage | | Special Features |
|---------|----------------------|-------------------|------------------|---------------------------------------|---|--------------------------------|----------|---------------------|
| | | | | | | Min V | Max V | |
| LM6142A | 1 | 250 | 17 | 25 | 0.8 | 2.7 | 24 | R-R In-Out Dual |
| LM6144A | 1 | 250 | 17 | 25 | 0.8 | 2.7 | 24 | R-R In-Out Quad |
| LM6142B | 2.5 | 300 | 17 | 25 | 0.8 | 2.7 | 24 | R-R In-Out Dual |
| LM6144B | 2.5 | 300 | 17 | 25 | 0.8 | 2.7 | 24 | R-R In-Out Quad |
| LM833 | 5 | 1000 | 15 | 7 | 4 | 10 | 30 | Dual Low Noise |
| LP2902 | 4 | 20 | 0.1 | 0.05 | 0.031 | 3 | 26 | Quad |
| LM2902 | 7 | 250 | 1 | 0.5 | 0.75 | 5 | 26 | Quad |
| LM2904 | 7 | 250 | 1 | 0.5 | 1.0 | 5 | 26 | Dual |
| LM2924 | 7 | 250 | 1 | 0.5 | 1.0 | 5 | 26 | Comparator + Op Amp |

Industrial Temperature Range (-25°C to $+85^{\circ}\text{C}$) Specs at $T_A = 25^{\circ}\text{C}$ (Note 1)

| Part # | V_{OS} mV (Max) | I_B nA (Max) | GBW MHz (Typ) | Slew Rate $V/\mu\text{s}$ (Typ) | Supply Current (Note 3) mA (Max) | Specified Supply Voltage | | Special Features |
|----------|----------------------|-------------------|------------------|---------------------------------------|---|--------------------------------|----------|---------------------|
| | | | | | | Min V | Max V | |
| LM208A | 0.5 | 2 | 1 | 0.3 | 0.6 | 10 | 40 | |
| LM10B(L) | 2 | 20 | 0.09 | 0.1 | 0.4 | (Note 4) | | Op Amp + Reference |
| LM201A | 2 | 75 | 1 | 0.5 | 2.5 | 10 | 40 | |
| LM207 | 2 | 75 | 1 | 0.5 | 2.5 | 10 | 40 | Compensated LM201A |
| LM208 | 2 | 2 | 1 | 0.3 | 0.6 | 10 | 40 | |
| LM224A | 3 | 80 | 1 | 0.5 | 0.75 | 5 | 30 | Quad |
| LM258A | 3 | 80 | 1 | 0.5 | 1.0 | 3 | 32 | Dual |
| LF255 | 5 | 0.1 | 2.5 | 5 | 4 | 30 | 40 | |
| LF256 | 5 | 0.1 | 5 | 12 | 7 | 30 | 40 | |
| LF257 | 5 | 0.1 | 20 | 50 | 7 | 30 | 40 | Minimum Gain of 5 |
| LM224 | 5 | 150 | 1 | 0.5 | 0.75 | 5 | 30 | Quad |
| LM258 | 5 | 150 | 1 | 0.5 | 1.0 | 5 | 30 | Dual |
| LM246 | 6 | 250 | 1.2 | 0.4 | 0.625 | 3 | 30 | (Note 5) |
| LM248 | 6 | 200 | 1 | 0.5 | 1.13 | 10 | 30 | Quad |
| LH0042C | 20 | 0.05 | 1 | 3 | 4 | 10 | 40 | |
| LM6132 | 0.25 | 110 | 7 | 22 | 0.4 | 2.7 | 24 | R-R In-Out Dual |
| LM6134 | 0.25 | 110 | 7 | 22 | 0.4 | 2.7 | 24 | R-R In-Out Quad |

General Purpose Operational Amplifier Selection Guide (Continued)

Commercial Temperature Range (0°C to +70°C) Specs at $T_A = 25^\circ\text{C}$ (Notes 1 and 2)

| Part # | V_{OS} mV (Max) | I_B nA (Max) | GBW MHz (Typ) | Slew Rate $V/\mu\text{s}$ (Typ) | Supply Current (Note 3) mA (Max) | Specified Supply Voltage | | Special Features |
|----------|----------------------|-------------------|------------------|---------------------------------------|---|--------------------------------|----------|------------------------------------|
| | | | | | | Min V | Max V | |
| LF411A | 0.5 | 0.2 | 4.0 | 15 | 2.8 | 10 | 40 | |
| LF441A | 0.5 | 0.05 | 1 | 1.0 | 0.25 | 10 | 40 | |
| LM308A | 0.5 | 7 | 19.0 | 0.3 | 0.8 | 10 | 40 | |
| LM11C | 0.6 | 0.1 | 0.8 | 0.3 | 0.8 | 5 | 40 | |
| LF412A | 1 | 0.2 | 4 | 15 | 2.8 | 12 | 40 | Dual |
| LF442A | 1 | 0.05 | 1.5 | 1.0 | 0.2 | 10 | 32 | Dual |
| LM604AC | 1 | 50 | 7.5 | 3 | 9 | 10 | 32 | Multiplexed Op Amp |
| LF355A | 2 | 0.05 | 2.5 | 5.0 | 4.0 | 30 | 36 | |
| LF356A | 2 | 0.05 | 5.0 | 12 | 10 | 30 | 36 | |
| LF357A | 2 | 0.05 | 20 | 50 | 10 | 30 | 36 | Minimum Gain of 5 |
| LF411 | 2 | 0.2 | 4 | 15 | 3.4 | 10 | 30 | |
| LF412 | 3 | 0.2 | 4 | 15 | 3.3 | 12 | 30 | Dual |
| LM324A | 3 | 100 | 1.0 | 0.5 | 0.75 | 5 | 30 | Quad |
| LM358A | 3 | 100 | 1 | 0.5 | 1.0 | 5 | 30 | Dual |
| LM604C | 3 | 80 | 7.5 | 7 | 4.5 | 10 | 32 | Multiplexed Op Amp |
| LM741E | 3 | 80 | 1.5 | 0.7 | 2.8 | 10 | 40 | |
| LM10C(L) | 4 | 30 | 0.09 | 0.1 | 0.5 | (Note 4) | | Op Amp + Reference |
| LP324 | 4 | 10 | 0.1 | 0.05 | 0.0375 | 5 | 30 | |
| LF347B | 5 | 0.2 | 4 | 13 | 2.8 | 10 | 30 | Quad |
| LF355B | 5 | 0.1 | 2.5 | 5 | 4 | 30 | 40 | |
| LF356B | 5 | 0.1 | 5 | 12 | 4 | 30 | 40 | |
| LF357B | 5 | 0.1 | 20 | 50 | 7 | 30 | 40 | |
| LF441 | 5 | 0.1 | 1.5 | 1 | 0.25 | 10 | 30 | |
| LF442 | 5 | 0.1 | 1 | 1 | 0.25 | 10 | 30 | Dual |
| LM11CL | 5 | 0.2 | 0.8 | 0.3 | 0.8 | 5 | 40 | |
| LF451 | 5 | 0.2 | 4 | 13 | 3.4 | 10 | 32 | SO Pkg |
| LF453 | 5 | 0.2 | 4 | 13 | 3.25 | 10 | 32 | SO Pkg Dual |
| LM611 | 5 | 35 | 0.8 | 0.7 | 0.35 | 2.8 | 32 | Op Amp + Ref |
| LM613 | 5 | 35 | 0.8 | 0.7 | 0.25 | 2.8 | 32 | 2 Op Amps + 2 Comparators + Ref |

General Purpose Operational Amplifier Selection Guide (Continued)

Commercial Temperature Range (0°C to +70°C) (Notes 1 and 2) (Continued)

| Part # | V _{OS} mV (Max) | I _B nA (Max) | GBW MHz (Typ) | Slew Rate V/μs (Typ) | Supply Current (Note 3) mA (Max) | Specified Supply Voltage | | Special Features |
|---------|-----------------------------|----------------------------|------------------|----------------------------|---|--------------------------------|----------|-----------------------------------|
| | | | | | | Min V | Max V | |
| LM614 | 5 | 35 | 0.8 | 0.7 | 0.25 | 2.8 | 32 | Quad Op Amp + Ref |
| LM392 | 5 | 250 | 1 | 0.5 | 1 | 5 | 30 | |
| LM346 | 6 | 250 | 1.2 | 0.4 | 0.63 | 3 | 30 | (Note 5) |
| LM348 | 6 | 200 | 1 | 0.5 | 1.13 | 10 | 30 | |
| LM349 | 6 | 200 | 4 | 2 | 1.13 | 10 | 30 | |
| LM741C | 6 | 500 | 1.5 | 0.5 | 2.8 | 10 | 40 | |
| LM1458 | 6 | 500 | * | * | 2.8 | 30 | 30 | |
| LM4250C | 6 | 75 | 0.2 | 0.2 | 0.15 | 3 | 30 | (Note 5) |
| LM324 | 7 | 250 | 1 | 0.5 | 0.75 | 5 | 30 | Quad, Low Cost |
| LM358 | 7 | 250 | 1 | 0.5 | 1.0 | 5 | 30 | Dual |
| LM301A | 7.5 | 250 | 1 | 0.5 | 3 | 10 | 30 | V _{CM} to V ⁺ |
| LM307 | 7.5 | 250 | 1 | 0.5 | 3 | 10 | 30 | Compensated LM301A |
| LM308 | 7.5 | 7 | 0.3 | 0.3 | 0.8 | 10 | 36 | |
| LM343 | 8 | 40 | 1 | 2.5 | 5 | 56 | 68 | |
| LF347 | 10 | 0.2 | 4 | 13 | 2.75 | 10 | 30 | Quad |
| LF351 | 10 | 0.2 | 4 | 13 | 3.4 | 10 | 30 | |
| LF353 | 10 | 0.2 | 4 | 13 | 5.4 | 10 | 30 | Dual |
| LF355 | 10 | 0.2 | 2.5 | 5 | 4 | 30 | 30 | |
| LF356 | 10 | 0.2 | 5 | 12 | 10 | 30 | 30 | |
| LF357 | 10 | 0.2 | 20 | 50 | 10 | 30 | 30 | Minimum Gain of 5 |
| LF444 | 10 | 0.1 | 1 | 1 | 0.25 | 10 | 30 | Quad |
| TL081C | 15 | 0.2 | 4 | 13 | 2.8 | 10 | 30 | |
| TL082C | 15 | 0.2 | 4 | 13 | 2.8 | 12 | 30 | Dual |

*Not Specified.

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: Those looking for a commercial part should also look at the Industrial Temp Range guide as many Hybrids are listed there.

Note 3: Supply current is per amplifier.

Note 4: The LM10 has 2 versions: one a high voltage part, good to 45V and a low voltage part, good to 7V. Refer to the datasheet for more information.

Note 5: The LM146 and LM4250 are programmable amplifiers. The data shown is for V_S = ±15V and I_{SET} = 10 μA. Refer to the datasheets for more information.

General Purpose Operational Amplifier Selection Guide (Continued)

Military Temperature Range (-55°C to $+125^{\circ}\text{C}$) Specs at $T_A = 25^{\circ}\text{C}$ (Note 1)

| Part # | V_{OS} mV (Max) | I_B nA (Max) | GBW MHz (Typ) | Slew Rate $V/\mu\text{s}$ (Typ) | Supply Current (Note 3) mA (Max) | Specified Supply Voltage | | Special Features |
|---------|----------------------|-------------------|------------------|---------------------------------------|---|--------------------------------|----------|---------------------|
| | | | | | | Min V | Max V | |
| LF411AM | 0.5 | 0.2 | 4 | 15 | 2.8 | 10 | 40 | |
| LF441AM | 0.5 | 0.05 | 1 | 1 | 0.2 | 10 | 40 | |
| LM108A | 0.5 | 2 | 1 | 0.3 | 0.6 | 10 | 40 | |
| LF412A | 1 | 0.2 | 4 | 15 | 2.8 | 12 | 40 | Dual |
| LF442A | 1 | 0.05 | 1 | 1 | 0.2 | 12 | 40 | Dual |
| LH0004 | 1 | 100 | 10 | * | 0.15 | 10 | 80 | High Voltage |
| LM604A | 1 | 50 | 7 | 2 | 4.5 | 10 | 32 | Multiplexed Op Amp |
| LF155A | 2 | 0.05 | 2.5 | 5 | 4 | 30 | 40 | |
| LF156A | 2 | 0.05 | 5 | 12 | 7 | 30 | 40 | |
| LF157A | 2 | 0.05 | 20 | 50 | 7 | 30 | 40 | Minimum Gain of 5 |
| LF411M | 2 | 0.2 | 4 | 15 | 3.4 | 10 | 30 | |
| LM10 | 2 | 20 | 0.09 | 0.1 | 0.4 | 1.2 | 40 | Op Amp + Reference |
| LM101A | 2 | 75 | 1 | 0.5 | 3 | 10 | 40 | V_{CM} to V^+ |
| LM107 | 2 | 100 | 1 | 0.5 | 3 | 10 | 40 | Compensated LM101A |
| LM108 | 2 | 2 | 1 | 0.3 | 0.6 | 10 | 40 | |
| LM124A | 2 | 50 | 1 | 0.5 | 0.75 | 5 | 30 | Quad |
| LM158A | 2 | 50 | 1 | 0.5 | 0.5 | 5 | 30 | Dual |
| LP124 | 2 | 4 | 0.1 | 0.05 | 0.035 | 5 | 30 | Quad |
| LF412 | 3 | 0.2 | 4 | 15 | 3.25 | 12 | 30 | Dual |
| LM741A | 3 | 80 | 1.5 | 0.7 | 2.8 | 10 | 40 | |
| LF155 | 5 | 0.1 | 2.5 | 5 | 4 | 30 | 40 | |
| LF156 | 5 | 0.1 | 5 | 12 | 7 | 30 | 40 | |
| LF157 | 5 | 0.1 | 20 | 50 | 7 | 30 | 40 | Minimum Gain of 5 |
| LF147 | 5 | 0.2 | 4 | 13 | 2.75 | 10 | 40 | Quad |
| LF442 | 5 | 0.1 | 1 | 1 | 0.25 | 10 | 40 | Dual |
| LF444A | 5 | 50 | 1 | 1 | 0.20 | 10 | 40 | Quad |
| LM124 | 5 | 150 | 1 | 0.5 | 0.75 | 5 | 30 | Quad |

General Purpose Operational Amplifier Selection Guide (Continued)

Military Temperature Range (-55°C to +125°C) Specs at T_A = 25°C (continued)

| Part # | V _{OS} mV (Max) | I _B nA (Max) | GBW MHz (Typ) | Slew Rate V/μs (Typ) | Supply Current (Note 3) mA (Max) | Specified Supply Voltage | | Special Features |
|--------|-----------------------------|----------------------------|------------------|----------------------------|---|--------------------------------|----------|-----------------------------------|
| | | | | | | Min V | Max V | |
| LM143 | 5 | 20 | 1 | 2.5 | 4 | 56 | 80 | High Voltage |
| LM146 | 5 | 100 | 1.2 | 0.4 | 0.55 | 3 | 30 | (Note 5) |
| LM148 | 5 | 100 | 1 | 0.5 | 0.9 | 10 | 30 | Quad |
| LM149 | 5 | 100 | 4 | 2 | 0.9 | 10 | 30 | Minimum Gain of 5, Quad |
| LM158 | 5 | 150 | 1 | 0.5 | 1 | 5 | 30 | Dual |
| LM741 | 5 | 500 | 1 | 0.5 | 2.8 | 10 | 40 | |
| LM1558 | 5 | 500 | * | * | 2.5 | 30 | 30 | Dual |
| LM4250 | 5 | 50 | 0.2 | 0.2 | 0.1 | 3 | 30 | (Note 5) |
| LH0042 | 20 | 0.025 | 1 | 3 | 3.5 | 10 | 40 | |
| LM157A | 5 | 30 | 7 | 50 | 20 | 0.05 | 5 | |
| LM141M | 5 | 10 | 3.4 | 15 | 4 | 0.5 | 2 | |
| LM10 | 5 | 40 | 0.4 | 0.1 | 0.09 | 50 | 2 | Op Amp + Reference |
| LM101A | 5 | 10 | 3 | 0.5 | 1 | 75 | 2 | V _{CM} to V ⁺ |
| LM107 | 5 | 10 | 3 | 0.5 | 1 | 100 | 2 | Compensated LM101A |
| LM108 | 5 | 10 | 0.8 | 0.3 | 1 | 2 | 2 | |
| LM124A | 5 | 30 | 0.75 | 0.5 | 1 | 50 | 2 | Quad |
| LM188A | 5 | 30 | 0.5 | 0.5 | 1 | 50 | 2 | Dual |
| LP124 | 5 | 30 | 0.035 | 0.02 | 0.1 | 4 | 2 | Quad |
| LP412 | 3 | 30 | 0.55 | 15 | 4 | 0.5 | 2 | Dual |
| LM124A | 3 | 10 | 0.3 | 0.3 | 1.5 | 50 | 2 | |
| LP125 | 2 | 30 | 4 | 5 | 5.5 | 0.1 | 2 | |
| LP126 | 2 | 30 | 7 | 15 | 5 | 0.1 | 2 | |
| LP127 | 2 | 30 | 7 | 50 | 20 | 0.1 | 2 | Minimum Gain of 5 |
| LP147 | 2 | 40 | 2.75 | 13 | 4 | 0.5 | 2 | Quad |
| LP442 | 2 | 40 | 0.55 | 1 | 1 | 0.1 | 2 | Dual |
| LP444A | 2 | 40 | 0.50 | 1 | 1 | 50 | 2 | Quad |
| LM124 | 2 | 30 | 0.75 | 0.5 | 1 | 150 | 2 | Quad |

Low Input Current Selection Guide

| < 25 fA | < 100 fA | ≤ 5 pA* | ≤ 20 pA | ≤ 50 pA | ≤ 100 pA | ≤ 200 pA | ≤ 500 pA |
|-----------------------------|------------|----------|---------|-------------|-------------|----------------|----------|
| T_A = 25°C | | | | | | | |
| LMC6001A** | LMC6001B** | LMC660* | LH0042 | LH0032A | LH0032 | TL081 | LH0032C |
| | | LMC662* | LH0042C | LF155A/156A | LF155/156 | LH0032AC | LH4004 |
| | | LMC6041* | | LF157A | LF157 | LF351 | |
| | | LMC6042* | | LF355A/356A | LF255/256 | LF411A/411 | |
| | | LMC6044* | | LF357A | LF257 | LF355/356 | |
| | | LMC6062* | | LF441A | LF355B/356B | LF357 | |
| | | LMC6082* | | LF442A | LF357B | LF147/347B/347 | |
| | | LPC660* | | LF444A | LF441 | LF353 | |
| | | LPC661* | | LM11 | LF442 | LF412A/412 | |
| | | LPC662* | | | LF444 | LM11CL | |
| | | LMC6061* | | | LM11C | LMC6022* | |
| | | LMC6081* | | | LH0101 | LMC6024* | |
| | | LMC6064* | | | | LMC6032* | |
| | | LMC6084* | | | | LMC6034* | |
| | | LMC6482* | | | | LH4104 | |
| | | LMC6484* | | | | LH4104C | |
| | | LMC6001C | | | | | |
| | | LMC6462 | | | | | |
| | | LMC6464 | | | | | |
| | | LMC6492 | | | | | |
| | | LMC6494 | | | | | |
| | | LMC6572 | | | | | |
| | | LMC6574 | | | | | |
| | | LMC6584 | | | | | |
| | | LMC6681 | | | | | |
| | | LMC6682 | | | | | |
| | | LMC6684 | | | | | |
| | | LMC7101 | | | | | |
| | | LMC7111 | | | | | |

Note: Datasheet should be referred to for conditions and more detailed information.

*Guaranteed over industrial temperature range (–40°C to +85°C). Typical value is ≤ 40 fA.

**100 percent tested and guaranteed.



High Speed Operational Amplifier Selection Guide

| Part # | Slew Rate V/ μ s (Typ) | GBW MHz (Typ) | V _{os} mV (Max) | I _s mA (Max) (Note 1) | Notes |
|--|-------------------------------|------------------|-----------------------------|--|---------------------------------------|
| GBW \geq 4 MHz, T_A = 25°C | | | | | |
| LM7171A | 4100 | 200 | 1 | 8.5 | High Output Current, Voltage Feedback |
| LM6171A | 3600 | 100 | 3 | 4 | Low Power, Voltage Feedback |
| LM7171 | 4100 | 200 | 3 | 8.5 | High Output Current, Voltage Feedback |
| LM6171 | 3600 | 100 | 6 | 4 | Low Power, Voltage Feedback |
| LM6172 | 3600 | 100 | 1 | 4 | Dual Low Power, Voltage Feedback |
| LM6181 | 2000 | 100 | 7.0 | 10 | Current Feedback, VIP |
| LM7121A | 1000 | 200 | 3 | 5 | Low Power, Voltage Feedback |
| LM7121 | 1000 | 200 | 6 | 5 | Low Power, Voltage Feedback |
| LH0024 | 500 | 70 | 4 | 15 | |
| LH0032 | 500 | 70 | 5 | 20 | FET Input |
| LM6161 | 300 | 50 | 7 | 6.8 | Unity Gain Stable, VIP™ |
| LM6162 | 300 | 100 | 5 | 6.8 | Min Gain of 2, VIP |
| LM6164 | 300 | 175 | 4 | 6.8 | Min Gain of 5, VIP |
| LM6165 | 300 | 725 | 3 | 6.8 | Min Gain of 25, VIP |
| LM6313 | 250 | 35 | 20 | 11.5 | Hi Speed Hi Power, Dual |
| LM6218A | 140 | 17 | 1 | 3.5 | Fast Settling Dual, VIP |
| LM6218 | 140 | 17 | 3 | 3.5 | Fast Settling Dual, VIP |
| LH0003 | 2-70 | 10-30 | 3 | 3 | External Compensation |
| LM118 | 70 | 15 | 4 | 7 | |
| LF157A | 50 | 20 | 2 | 7 | Min Gain of 5, JFET |
| LM359 | 30 | 30 | * | 11 | Dual Current Mode (Norton) Amp |
| LM6152 | 30 | 45 | 2.5 | 1.5 | R-R In-Out, Dual |
| LM6154 | 30 | 45 | 2.5 | 1.5 | R-R In-Out, Quad |
| LM6142A | 25 | 17 | 1.0 | 0.8 | Low Power, R-R In-Out, Dual |
| LM6144A | 25 | 17 | 1.0 | 0.8 | Low Power, R-R In-Out, Quad |
| LF411A | 15 | 4 | 0.5 | 1.4 | JFET |
| LF412A | 15 | 4 | 1.0 | 2.8 | Dual JFET |
| LF147 | 13 | 4 | 5 | 2.75 | Quad JFET |
| LF451 | 13 | 4 | 5 | 3.4 | SO Pkg |
| LF453 | 13 | 4 | 5 | 3.25 | SO Pkg Dual |
| LF351 | 13 | 4 | 10 | 3.4 | JFET |
| LF353 | 13 | 4 | 10 | 3.3 | Dual JFET |
| LF156A | 12 | 5 | 2 | 7 | JFET |
| LM833 | 7 | 15 | 5 | 4 | Dual Low Noise |

*Not specified.

Note 1: Supply current is per amplifier in a package.

Precision Operational Amplifier Selection Guide

| Part # | V _{os} mV (Max) | I _B nA (Max) | GBW MHz (typ) | Slew Rate V/μs (Typ) | Supply Current (Note 1) mA (Max) | Notes |
|----------------|-----------------------------|----------------------------|------------------|----------------------------|---|---------------------------|
| Singles | | | | | | |
| LMC6081A | 0.35 | 0.00001* | 1.3 | 1.5 | 0.750 | Low power |
| LMC6061A | 0.35 | 0.00001* | 0.1 | 0.035 | 0.024 | Micropower |
| LM308A | 0.5 | 7 | 1 | 0.3 | 0.8 | |
| LM208A | 0.5 | 2 | 1 | 0.3 | 0.6 | |
| LM108A | 0.5 | 2 | 1 | 0.3 | 0.6 | |
| LF441A | 0.5 | 0.05 | 1 | 1 | 0.2 | |
| LF411A | 0.5 | 0.2 | 4 | 15 | 2.8 | |
| LM11C | 0.6 | 0.1 | 0.8 | 0.3 | 0.8 | |
| LMC6081 | 0.8 | 0.00001* | 1.3 | 1.5 | 0.750 | Low power |
| LMC6061 | 0.8 | 0.00001* | 0.1 | 0.035 | 0.032 | Micropower |
| Duals | | | | | | |
| LMC6082A | 0.35 | 0.00001* | 1.3 | 0.75 | 0.75 | Dual LMC6081A |
| LMC6062A | 0.35 | 0.00001* | 0.1 | 0.019 | 0.019 | Dual LMC6061A |
| LMC6482A | 0.5 | 0.00002* | 1.3 | 1 | 0.50 | Rail to Rail Input/Output |
| LMC6082 | 0.8 | 0.00001* | 1.3 | 1.5 | 0.75 | Dual LMC6081 |
| LMC6062 | 0.8 | 0.00001* | 0.1 | 0.035 | 0.023 | Dual LMC6061 |
| Quads | | | | | | |
| LMC6084A | 0.35 | 0.00001* | 1.3 | 1.5 | 0.75 | Quad LMC6081A |
| LMC6064A | 0.35 | 0.00001* | 0.1 | 0.035 | 0.019 | Quad LMC6061A |
| LMC6484A | 0.5 | 0.00002* | 1.3 | 1 | 0.50 | Rail to Rail Input/Output |
| LMC6084 | 0.8 | 0.00001* | 1.3 | 1.5 | 0.75 | Quad LMC6081 |
| LMC6064 | 0.8 | 0.00001* | 0.1 | 0.35 | 0.029 | Quad LMC6061 |

*Typical Value

Note 1: Supply current is per amplifier.



National Semiconductor

MicroPower/Low Power Operational Amplifier Selection Guide

| Part # | Is μA Typ (per Amp) | Vos mV Max | Ib fA Typ | VCM V Typ | Output Swing V Typ with RL = 100 kΩ | GBW MHz Typ | Specified Supply Voltage | |
|---------------------------------|------------------------------|------------------|-----------------|-----------------|---|-------------------|--------------------------------|----------|
| | | | | | | | Min V | Max V |
| | | | | | | | | |
| Specs at TA = 25°C and Vs = +5V | | | | | | | | |
| Singles | | | | | | | | |
| LMC6041A | 14 | 3 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.075 | 5 | 15 |
| LMC6041 | 14 | 6 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.075 | 5 | 15 |
| LMC6061A | 20 | 0.35 | 10 | −0.4 to 3.1 | 0.005 to 4.995 | 0.1 | 5 | 15 |
| LMC6061 | 20 | 0.8 | 10 | −0.4 to 3.1 | 0.005 to 4.995 | 0.1 | 5 | 15 |
| LPC661A | 55 | 3 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LPC661 | 55 | 6 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LMC6081A | 450 | 0.35 | 10 | −0.4 to 3.1 | 0.02 to 4.98 | 1.3 | 5 | 15 |
| LMC6081 | 450 | 0.8 | 10 | −0.4 to 3.1 | 0.02 to 4.98 | 1.3 | 5 | 15 |
| LMC6681A | 700 | 1 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6681 | 700 | 3 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| Duals | | | | | | | | |
| LMC6042A | 10 | 3 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.1 | 5 | 15 |
| LMC6042 | 10 | 6 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.1 | 5 | 15 |
| LMC6062A | 16 | 0.35 | 10 | −0.4 to 3.1 | 0.005 to 4.995 | 0.1 | 5 | 15 |
| LMC6062 | 16 | 0.8 | 10 | −0.4 to 3.1 | 0.005 to 4.995 | 0.1 | 5 | 15 |
| LMC6462A | 20 | 0.5 | 150 | −0.2 to 5.3 | 0.005 to 4.995 | 0.05 | 73 | 15 |
| LMC6462 | 20 | 3 | 150 | −0.2 to 5.3 | 0.005 to 4.995 | 0.05 | 3 | 15 |
| LPC662A | 43 | 3 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LPC662 | 43 | 6 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LMC6022 | 43 | 9 | 40 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LMC662A | 375 | 3 | 2 | −0.4 to 3.1 | 0.02 to 4.98 | 1.4 | 5 | 15 |
| LMC662 | 375 | 6 | 2 | −0.4 to 3.1 | 0.02 to 4.98 | 1.4 | 5 | 15 |
| LMC6032 | 375 | 9 | 40 | −0.4 to 3.1 | 0.02 to 4.98 | 1.4 | 5 | 15 |
| LMC6082A | 450 | 0.35 | 10 | −0.4 to 3.1 | 0.02 to 4.98 | 1.3 | 5 | 15 |
| LMC6082 | 450 | 0.8 | 10 | −0.4 to 3.1 | 0.02 to 4.98 | 1.3 | 5 | 15 |
| LMC6482A | 500 | 0.5 | 20 | 0 to 5 | 0.03 to 4.97 | 1.3 | 3 | 15 |
| LMC6482 | 500 | 3 | 20 | 0 to 5 | 0.03 to 4.97 | 1.3 | 3 | 15 |
| LMC6492A | 500 | 3 | 150 | −0.3 to 5.3 | 0.02 to 4.98 | 1.5 | 2.5 | 15.5 |
| LMC6492 | 500 | 6 | 150 | −0.3 to 5.3 | 0.02 to 4.98 | 1.5 | 2.5 | 15.5 |

MicroPower/Low Power Operational Amplifier Selection Guide (Continued)

| Part # | Is μA Typ (per Amp) | Vos mV Max | IB fA Typ | VCM V Typ | Output Swing V Typ with RL = 100 kΩ | GBW MHz Typ | Specified Supply Voltage | |
|---------------------------------|------------------------------|------------------|-----------------|-----------------|---|-------------------|--------------------------------|----------|
| | | | | | | | Min V | Max V |
| Specs at TA = 25°C and Vs = +5V | | | | | | | | |
| Duals Continued | | | | | | | | |
| LMC6582A | 700 | 1 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6582 | 700 | 3 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6682A | 700 | 1 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6682 | 700 | 3 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6142A | 650 | 1 | 170* | | 0.005 to 4.995 | 17 | 2.7 | 24 |
| Quads | | | | | | | | |
| LMC6044A | 10 | 3 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.1 | 5 | 15 |
| LMC6044 | 10 | 6 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.1 | 5 | 15 |
| LMC6064A | 16 | 0.35 | 10 | −0.4 to 3.1 | 0.005 to 4.995 | 0.1 | 5 | 15 |
| LMC6064 | 16 | 0.8 | 10 | −0.4 to 3.1 | 0.005 to 4.995 | 0.1 | 5 | 15 |
| LMC6464 | 20 | 3 | 150 | −0.2 to 5.3 | 0.05 to 4.995 | 0.05 | 3 | 15 |
| LMC6464A | 20 | 0.5 | 150 | −0.2 to 5.3 | 0.05 to 4.995 | 0.05 | 3 | 15 |
| LPC660A | 40 | 3 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LPC660 | 40 | 6 | 2 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LMC6024 | 40 | 9 | 40 | −0.4 to 3.1 | 0.004 to 4.987 | 0.35 | 5 | 15 |
| LMC660A | 375 | 3 | 2 | −0.4 to 3.1 | 0.02 to 4.98 | 1.4 | 5 | 15 |
| LMC660 | 375 | 6 | 2 | −0.4 to 3.1 | 0.02 to 4.98 | 1.4 | 5 | 15 |
| LMC6034 | 375 | 9 | 40 | −0.4 to 3.1 | 0.02 to 4.98 | 1.4 | 5 | 15 |
| LMC6084A | 450 | 0.35 | 10 | −0.4 to 3.1 | 0.02 to 4.98 | 1.3 | 5 | 15 |
| LMC6084 | 450 | 0.8 | 10 | −0.4 to 3.1 | 0.02 to 4.98 | 1.3 | 5 | 15 |
| LMC6484A | 500 | 0.5 | 20 | 0 to 5 | 0.03 to 4.97 | 1.3 | 3 | 15 |
| LMC6484 | 500 | 3 | 20 | 0 to 5 | 0.03 to 4.97 | 1.3 | 3 | 15 |
| LMC6494A | 500 | 3 | 150 | −0.3 to 5.3 | 0.02 to 4.98 | 1.5 | 5 | 15 |
| LMC6494 | 500 | 3 | 150 | −0.3 to 5.3 | 0.02 to 4.98 | 1.5 | 5 | 15 |
| LMC6144A | 650 | 1 | 170* | −0.25 to 5.3 | 0.005 to 4.995 | 1.7 | 2.7 | 24 |
| LMC6584A | 700 | 1 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6584 | 700 | 3 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6684A | 700 | 1 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |
| LMC6684 | 700 | 3 | 80 | −0.3 to 5.3 | 0.05 to 4.9 | 1.2 | 1.8 | 10 |

*nA



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Medium and High Power Operational Amplifier Selection Guide ($\geq 0.1A$ Output) ($T_A = 25^\circ C$, Note 1)

| Part # | I_{OUT} A (Typ) | V_{OS} mV (Max) | I_S mA (Max) | Slew Rate V/ μ S (Typ) | PBW (Typ) |
|----------|----------------------|----------------------|-------------------|-------------------------------|-----------|
| LM6181 | 0.1 | 7.0 | 10 | 2000 | 60 MHz |
| LM6182 | 0.1 (Dual) | 7.0 | 20 | 2000 | 60 MHz |
| LH0041 | 0.2 | 3 | 3.5 | 3 | 20 kHz |
| LH0101A | 2.2 | 3 | 35 | 10 | 300 kHz |
| LH0101 | 2.2 | 10 | 35 | 10 | 300 kHz |
| LM675 | 3 | 10 | 50 | 8 | |
| LM12(L) | (Note 2) | 7 | 80 | 9 | 60 kHz |
| LM12C(L) | (Note 2) | 15 | 120 | 9 | 60 kHz |
| LM7171A | 0.1 | 1 | 8.5 | 4100 | 33 MHz |
| LM7171 | 0.1 | 3 | 8.5 | 4100 | 33 MHz |
| LM6171A | 0.1 | 3 | 4 | 3600 | 28 MHz |
| LM6171 | 0.1 | 6 | 4 | 3600 | 28 MHz |

*Not Specified

Note 1: Refer to Datasheet for conditions and more detailed information.

Note 2: I_{OUT} for the LM12 is dependent on the amount of power dissipated in the output transistor. The datasheet should be referred to, to determine amount of current available.

Low Voltage Selection Guide

| Part # | Minimum Supply Voltage | Typical Supply Current (per Device) | Description |
|---------|------------------------|-------------------------------------|---|
| LMC6482 | 3V | 500 μ A | Dual 1 MHz Rail-to-Rail Amp |
| LMC6484 | 3V | 500 μ A | Quad 1 MHz Rail-to-Rail Amp |
| LMC7101 | 2.7V | 500 μ A | Tiny Pak™ SOT23 1 MHz Rail-to-Rail Amp |
| LMC7111 | 2.2V | 25 μ A | Tiny Pak SOT23 35 kHz Rail-to-Rail Amp |
| LMC6582 | 1.8V | 700 | Dual Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifier |
| LMC6584 | 1.8V | 700 | Quad Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifiers |
| LMC6681 | 1.8V | 700 μ A | Single Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifier with Powerdown |
| LMC6682 | 1.8V | 700 μ A | Dual Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Op Amp with Powerdown |
| LMC6684 | 1.8V | 700 μ A | Quad Low-Voltage, 1.2 MHz Rail-to-Rail Input and Output CMOS Amplifiers with Powerdown |
| LM6142 | 1.8V | 650 μ A | Dual 17 MHz Gain-Bandwidth Rail-to-Rail Amp |
| LM6144 | 1.8V | 650 μ A | Quad 17 MHz Gain-Bandwidth Rail-to-Rail Amp |
| LM7131 | 3V | 7 mA | Video Amp in SOT23 Tiny Pak, 70 MHz Gain-Bandwidth |
| LM6132 | 1.8V | 360 μ A | Dual 7 MHz Gain-Bandwidth Rail-to-Rail Amplifier |
| LM6134 | 1.8V | 360 μ A | Quad 7 MHz Gain-Bandwidth Rail-to-Rail Amplifier |
| LM6152 | 1.8V | 1500 μ A | Dual 45 MHz Gain-Bandwidth Rail-to-Rail Amplifier |
| LM6154 | 1.8V | 1500 μ A | Dual 45 MHz Gain-Bandwidth Rail-to-Rail Amplifier |



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Audio Op Amp Selection Guide

| Part # | Description Precision Op Amp | Input Referred Noise Voltage | THD | Slew Rate | GBW | PSRR | Supply Range | Single/ Dual/Quad | Package (Pin Count) |
|--------|---------------------------------|---------------------------------|---------|--------------------|--------|--------|--------------------------|----------------------|------------------------|
| LM833 | Dual Audio Amplifier | 4.5 nV/ $\sqrt{\text{Hz}}$ | 0.002% | 7V/ μs | 15 MHz | 100 dB | $\pm 18\text{V}$ | Dual | SO(8), DIP(8) |
| LM837 | Quad Audio Amplifier | 4.5 nV/ $\sqrt{\text{Hz}}$ | 0.0015% | 10V/ μs | 25 MHz | 100 dB | $\pm 18\text{V}$ | Quad | SO(14), DIP(14) |
| LF347 | Wide Bandwidth JFET | 20 nV/ $\sqrt{\text{Hz}}$ | 0.02% | 13V/ μs | 4 MHz | 100 dB | $\pm 18\text{V}$ | Quad | DIP(14), SO(14) |
| LF351 | Wide Bandwidth JFET | 25 nV/ $\sqrt{\text{Hz}}$ | 0.02% | 13V/ μs | 4 MHz | 100 dB | $\pm 18\text{V}$ | Single | SO(8), DIP(8) |
| LF353 | Dual LF351 | 16 nV/ $\sqrt{\text{Hz}}$ | 0.02% | 13V/ μs | 4 MHz | 100 dB | $\pm 18\text{V}$ | Dual | SO(14), DIP(14) |
| LF411 | Low Offset, Low Drift JFET | 25 nV/ $\sqrt{\text{Hz}}$ | 0.02% | 15V/ μs | 3 MHz | 100 dB | $\pm 18\text{V}$ | Single | DIP(8) |
| LF412 | Dual LF411 | 25 nV/ $\sqrt{\text{Hz}}$ | 0.02% | 15V/ μs | 3 MHz | 100 dB | $\pm 18\text{V}$ | Dual | DIP(8) |
| LF444 | Low Power JFET Quad | 35 nV/ $\sqrt{\text{Hz}}$ | 0.02% | 1V/ μs | 1 MHz | 100 dB | $\pm 18\text{V}$ | Quad | DIP(14), SO(14) |
| LM6142 | High-Speed/Low Power Dual | 16 nV/ $\sqrt{\text{Hz}}$ | 0.03% | 5V/ μs | 17 MHz | 87 dB | $\pm 1.8\text{V}$ to 24V | Dual | DIP(8), SO(8) |
| LM6144 | High-Speed/Low Power Quad | 16 nV/ $\sqrt{\text{Hz}}$ | 0.03% | 5V/ μs | 17 MHz | 87 dB | $\pm 1.8\text{V}$ to 24V | Quad | DIP(14), SO(14) |
| | CMOS Amplifiers with Powerdown | | | | | | | | |
| | Dual 17 MHz Gain-Bandwidth | | | | | | | | |
| | Quad 17 MHz Gain-Bandwidth | | | | | | | | |
| | Video Amp in SOT23 Tiny Pak | | | | | | | | |
| | Dual 7 MHz Gain-Bandwidth | | | | | | | | |
| | Quad 7 MHz Gain-Bandwidth | | | | | | | | |
| | Dual 45 MHz Gain-Bandwidth | | | | | | | | |
| | Dual 45 MHz Gain-Bandwidth | | | | | | | | |

Audio Power Amp Selection Guide

| Users Supply Voltage | Part # | Power [THD ≤ 1% (Typ)] | | | Power [THD ≤ 10% (Typ)] | | |
|---|--------|-----------------------------------|-------|-------|-----------------------------------|-------|-------|
| | | Power Specified as Continuous RMS | | | Power Specified as Continuous RMS | | |
| | | 4Ω | 8Ω | 16Ω | 4Ω | 8Ω | 16Ω |
| 5V ($V_S = 6V$) | LM1896 | 0.7W | 0.45W | NA | 1.1W | 1.3W | NA |
| 12V | LM1877 | 1.5W | 1.0W | 0.55W | 1.75W | 1.3W | 0.75W |
| | LM2877 | 1.5W | 1.0W | 0.55W | 1.75W | 1.3W | 0.75W |
| | LM2878 | 1.5W | 1.0W | 0.55W | 2.0W | 1.3W | 0.75W |
| 14V | LM1877 | 2.0W | 1.3W | 0.85W | 2.5W | 1.75W | 1.0W |
| | LM2877 | 2.0W | 1.3W | 0.85W | 2.75W | 1.75W | 1.0W |
| | LM2878 | 2.0W | 1.3W | 0.85W | 2.75W | 1.75W | 1.0W |
| | LM2879 | NA | 1.25W | NA | NA | 2W | NA |
| 20V and Above ($V_S = 20V$) ($V_S = 20V$) ($V_S = 20V$) ($V_S = 28V$) ($V_S = \pm 25V$) ($V_S = \pm 35V$) ($V_S = \pm 35V$) ($V_S = \pm 35V$) | LM1877 | 2.0W | 2.0W | NA | 2.5W | 3.0W | NA |
| | LM2877 | 2.5W | 3.0W | 1.75W | 3.7 | 4.25W | 2.3W |
| | LM2878 | NA | 4.0W | NA | NA | 4.75W | NA |
| | LM2879 | NA | 7.0W | NA | NA | 8W | NA |
| | LM1875 | 20W | 20W | NA | 25W | 30W | NA |
| | LM3875 | 45W ($V_S = \pm 25V$) | 56W | 30W | 56W ($V_S = \pm 25V$) | 70W | 39W |
| | LM3876 | 45W ($V_S = \pm 25V$) | 56W | 30W | 56W ($V_S = \pm 25V$) | 70W | 39W |
| | LM3886 | 68W ($V_S = \pm 28V$) | 63W | 33W | 87W ($V_S = \pm 28V$) | 78W | 41W |



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Typical THD Ratings

| Typical THD Ratings | THD Measurements Conditions | Supply Range (V) | Single/Dual | Package (Pin Count) |
|--------------------------------|----------------------------------|------------------|-------------|---------------------|
| 0.72% | Po = 1W @ V _S = 5V | 2.7V to 5.5V | Single | SO(16) |
| 0.45% | Po = 0.5W @ V _S = 5V | 2.7V to 5.5V | Single | SO(8) |
| 0.72% | Po = 1W @ V _S = 5V | 2.7V to 5.5V | Single | SO(16) |
| 0.45% | Po = 0.5W @ V _S = 5V | 2.7V to 5.5V | Single | SO(8) |
| 0.11% | Po = 0.5W @ V _S = 6V | 3V to 10V | Dual | DIP(14) |
| 0.055% | Po = 1W @ V _S = 14V | 6V to 24V | Dual | DIP(14), SO(14) |
| 0.07% | Po = 1W @ V _S = 14V | 6V to 24V | Dual | SIP(11) |
| 0.14% | Po = 2W @ V _S = 22V | 6V to 32V | Dual | SIP(11) |
| 0.14% | Po = 1W @ V _S = 12V | 3V to 15V | Dual | SIP(11) |
| 0.055% | Po = 1W @ V _S = 14V | 6V to 24V | Dual | DIP(14), SO(14) |
| 0.07% | Po = 1W @ V _S = 1W | 6V to 24V | Dual | SIP(11) |
| 0.15% | Po = 2W @ V _S = 22V | 6V to 32V | Dual | SIP(11) |
| 0.05% | Po = 1W @ V _S = 12V | 6V to 32V | Dual | TO-220(11) |
| 0.02% | Po = 20W @ V _S = ±25V | 16V to 60V | Single | TO-220(5) |
| 0.06% | Po = 25W @ V _S = ±30V | 20V to 60V | Single | TO-220(11)** |
| 0.06% | Po = 40W @ V _S = ±35V | 20V to 84V | Single | TO-220(11)** |
| 0.06% | Po = 40W @ V _S = ±35V | 20V to 84V | Single | TO-220(11)** |
| 0.03% | Po = 60W @ V _S = ±28V | 20V to 84V | Single | TO-220(11)** |
| **Isolated packages available. | | | | |

Special Amplifier Selection Guide

Amplifiers with Added Functions

Featuring the new Super-Block™ family, these amplifiers have additional special functions within their packages which help minimize the number of components required in an application. These devices are often used in control circuits, power supplies, and automatic test systems.

| | |
|-------|--|
| LM10 | Op Amp and Adjustable Voltage Reference |
| LM392 | Op Amp and Comparator |
| LM611 | Super-Block Op Amp and Adjustable Voltage Reference |
| LM613 | Super-Block Dual Op Amp, Dual Comparator, and Adjustable Voltage Reference |
| LM614 | Super-Block Quad Op Amp and Adjustable Voltage Reference |

Transconductance Amplifiers (Voltage In, Current Out)

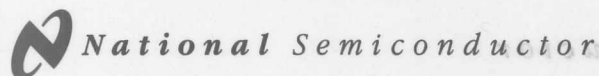
These amplifiers provide a transconductance (g_m) proportional to their bias current, which is controlled externally. This programmable gain makes the amplifiers useful in applications such as voltage-controlled amplifiers, current-controlled amplifiers, AGC circuits, and voltage multipliers.

| | |
|---------|--|
| LM3080 | Operational Transconductance Amplifier |
| LM13600 | Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers |
| LM13700 | Improved Dual Operational Transconductance Amplifier with Linearizing Diodes and Buffers |

Transimpedance Amplifiers (Current In, Voltage Out)

Transimpedance amplifiers are widely used to amplify photo-diode signals, and to ground-reference differential voltage signals which have high common-mode voltages. The LH0082 was designed to receive and amplify analog and digital signals transmitted by fiber optics. Like the LM359, the LH0082 can also be used as a video amplifier. The LM2900 series has found popularity in filter applications, as well as general-purpose amplifiers.

| | |
|--------|--------------------------------------|
| LM359 | Dual Current Mode (Norton) Amplifier |
| LM2900 | Quad Current Mode (Norton) Amplifier |
| LM3900 | |
| LM3301 | |
| LM3401 | |



LF147/LF347 Wide Bandwidth Quad JFET Input Operational Amplifiers

General Description

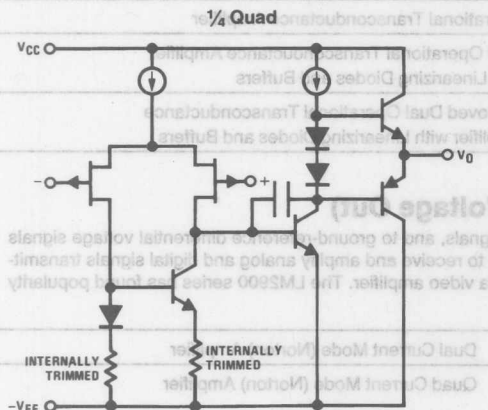
The LF147 is a low cost, high speed quad JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET IITM technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF147 is pin compatible with the standard LM148. This feature allows designers to immediately upgrade the overall performance of existing LF148 and LM124 designs.

The LF147 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift.

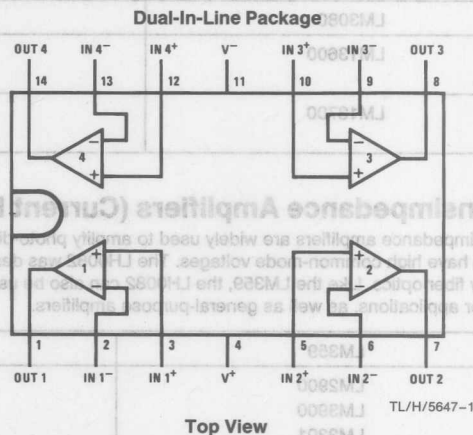
Features

- Internally trimmed offset voltage 5 mV max
- Low input bias current 50 pA
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 7.2 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz – 20 kHz < 0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Simplified Schematic



Connection Diagram



Order Number LF147J, LF347M, LF347BN,
LF347N, LF147D/883 or LF147J/883*
See NS Package Number D14E, J14A, M14A or N14A

*Available per SMD #8102306, JM38510/11906.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | LF147 | LF347B/LF347 |
|--|------------|--------------|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous |
| Power Dissipation (Notes 3 and 9) | 900 mW | 1000 mW |
| T _J max | 150°C | 150°C |
| θ _{JA} | | |
| Cavity DIP (D) Package | | 80°C/W |
| Ceramic DIP (J) Package | | 70°C/W |
| Plastic DIP (N) Package | | 75°C/W |
| Surface Mount Narrow (M) | | 100°C/W |
| Surface Mount Wide (WM) | | 85°C/W |

Operating Temperature Range

Storage Temperature Range

Lead Temperature (Soldering, 10 sec.)

Soldering Information

Dual-In-Line Package

Soldering (10 seconds)

Small Outline Package

Vapor Phase (60 seconds)

Infrared (15 seconds)

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10)

LF147

(Note 4)

LF347B/LF347

(Note 4)

−65°C ≤ T_A ≤ 150°C

260°C

260°C

260°C

215°C

220°C

900V

DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|----------------------|------------------------------------|--|------------------|------------|-----|------------------|------------|-----|------------------|------------|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S = 10 kΩ, T _A = 25°C Over Temperature | 1 | 5 | 8 | 3 | 5 | 7 | 5 | 10 | 13 | mV |
| ΔV _{OS} /ΔT | Average TC of Input Offset Voltage | R _S = 10 kΩ | 10 | | | 10 | | | 10 | | | μV/°C |
| I _{OS} | Input Offset Current | T _J = 25°C, (Notes 5, 6) Over Temperature | 25 | 100 | 25 | 25 | 100 | 4 | 25 | 100 | 4 | pA |
| I _B | Input Bias Current | T _J = 25°C, (Notes 5, 6) Over Temperature | 50 | 200 | 50 | 50 | 200 | 8 | 50 | 200 | 8 | pA |
| R _{IN} | Input Resistance | T _J = 25°C | 10 ¹² | | | 10 ¹² | | | 10 ¹² | | | Ω |
| A _{VOL} | Large Signal Voltage Gain | V _S = ±15V, T _A = 25°C V _O = ±10V, R _L = 2 kΩ Over Temperature | 50 | 100 | 25 | 50 | 100 | 25 | 25 | 100 | 15 | V/mV |
| V _O | Output Voltage Swing | V _S = ±15V, R _L = 10 kΩ | ±12 | ±13.5 | | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| V _{CM} | Input Common-Mode Voltage Range | V _S = ±15V | ±11 | +15 −12 | | ±11 | +15 −12 | | ±11 | +15 −12 | | V |
| CMRR | Common-Mode Rejection Ratio | R _S ≤ 10 kΩ | 80 | 100 | | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | 80 | 100 | | 80 | 100 | | 70 | 100 | | dB |
| I _S | Supply Current | | 7.2 | 11 | | 7.2 | 11 | | 7.2 | 11 | | mA |

AC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF147 | | | LF347B | | | LF347 | | | Units |
|--------|---------------------------------|---|-------|------|-----|--------|------|-----|-------|------|-----|------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25^\circ\text{C}$, $f = 1\text{ Hz} - 20\text{ kHz}$ (Input Referred) | | -120 | | | -120 | | | -120 | | dB |
| SR | Slew Rate | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 8 | 13 | | 8 | 13 | | 8 | 13 | | V/ μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 2.2 | 4 | | 2.2 | 4 | | 2.2 | 4 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ\text{C}$, $R_S = 100\Omega$, $f = 1000\text{ Hz}$ | | 20 | | | 20 | | | 20 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $T_j = 25^\circ\text{C}$, $f = 1000\text{ Hz}$ | | 0.01 | | | 0.01 | | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} .

Note 4: The LF147 is available in the military temperature range $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, while the LF347B and the LF347 are available in the commercial temperature range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$. Junction temperature can rise to $T_j \text{ max} = 150^\circ\text{C}$.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20\text{V}$ for the LF147 and for $V_S = \pm 15\text{V}$ for the LF347B/LF347. V_{OS} , I_B , and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_j = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

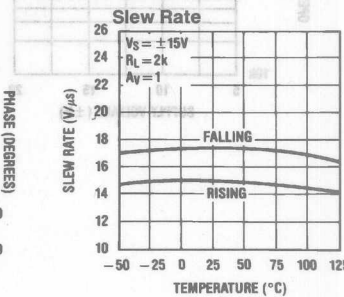
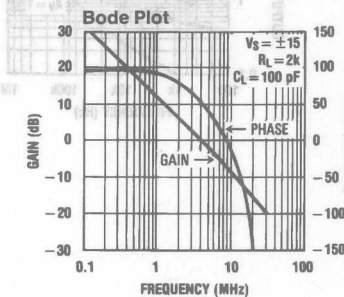
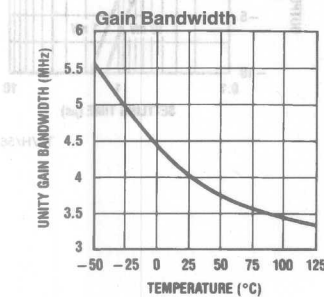
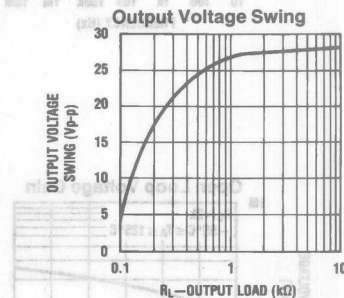
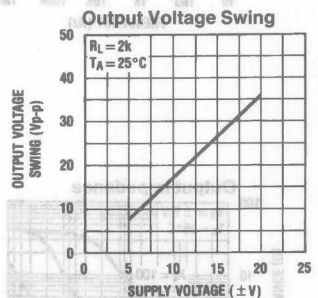
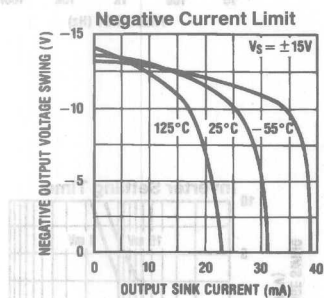
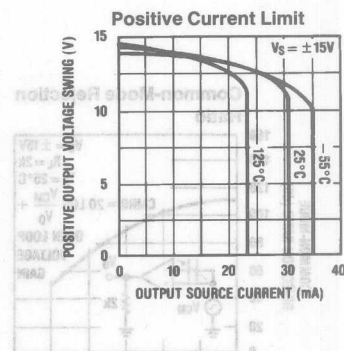
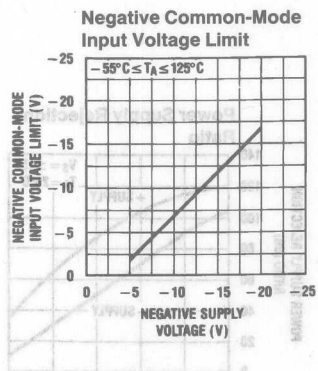
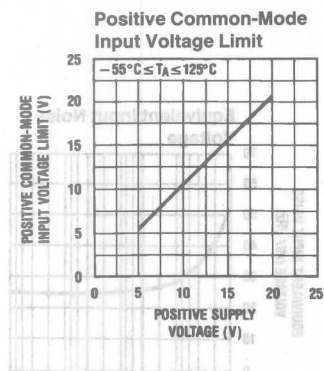
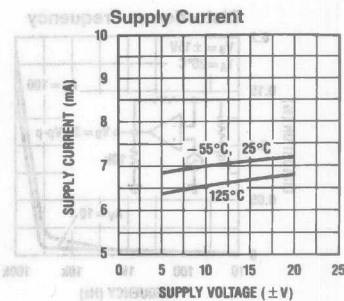
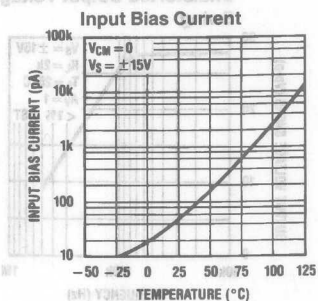
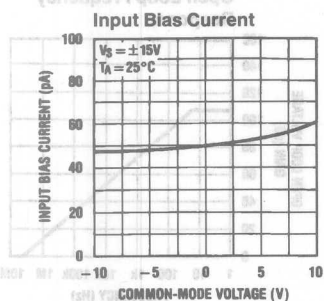
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_S = \pm 5\text{V}$ to $\pm 15\text{V}$ for the LF347 and LF347B and from $V_S = \pm 20\text{V}$ to $\pm 5\text{V}$ for the LF147.

Note 8: Refer to RETS147X for LF147D and LF147J military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 10: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

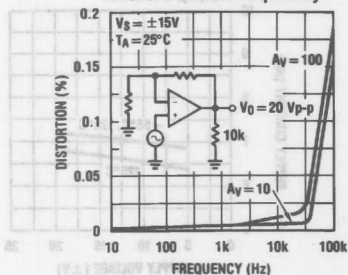
Typical Performance Characteristics



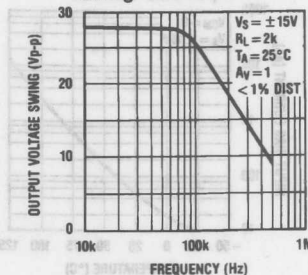
TL/H/5647-2

Typical Performance Characteristics (Continued)

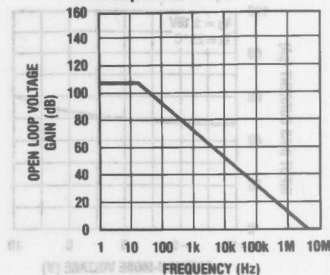
Distortion vs Frequency



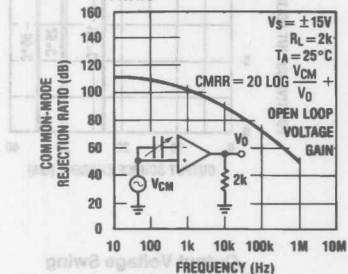
Undistorted Output Voltage Swing



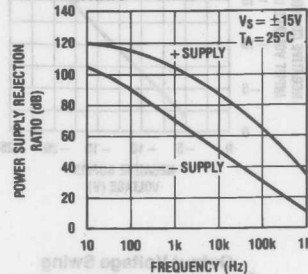
Open Loop Frequency Response



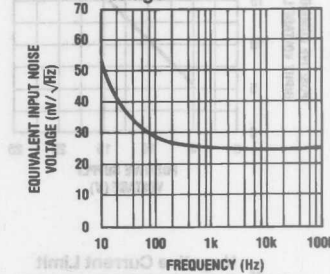
Common-Mode Rejection Ratio



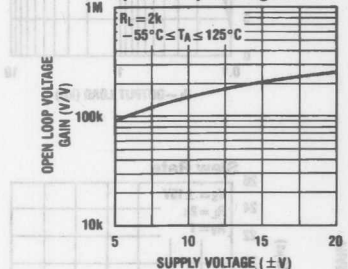
Power Supply Rejection Ratio



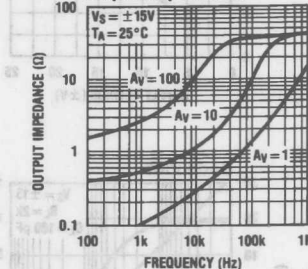
Equivalent Input Noise Voltage



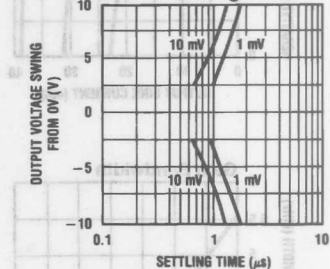
Open Loop Voltage Gain



Output Impedance



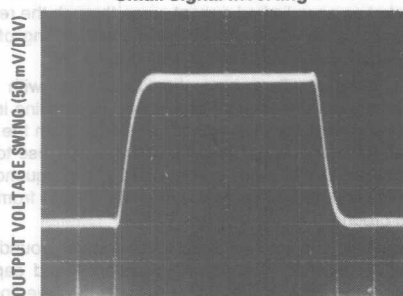
Inverter Settling Time



TL/H/5647-3

Pulse Response $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$

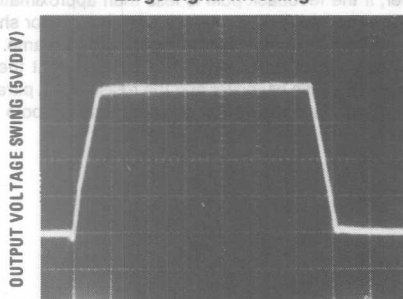
Small Signal Inverting



TIME (0.2 $\mu\text{s}/\text{DIV}$)

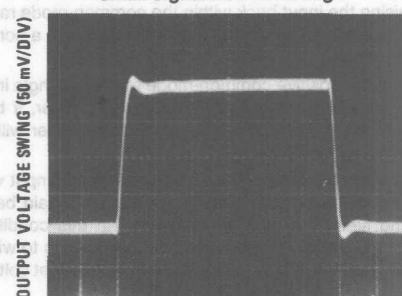
TL/H/5647-4

Large Signal Inverting



TIME (2 $\mu\text{s}/\text{DIV}$)

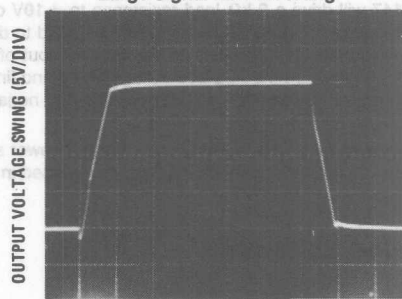
Small Signal Non-Inverting



TIME (0.2 $\mu\text{s}/\text{DIV}$)

TL/H/5647-5

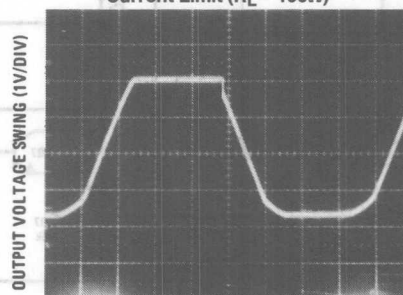
Large Signal Non-Inverting



TIME (2 $\mu\text{s}/\text{DIV}$)

TL/H/5647-7

Current Limit ($R_L = 100\Omega$)



TIME (5 $\mu\text{s}/\text{DIV}$)

TL/H/5647-8

Application Hints

The LF147 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages

should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier

Application Hints (Continued)

output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 4.5\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF147 will drive a $2\text{ k}\Omega$ load resistance to $\pm 10\text{V}$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

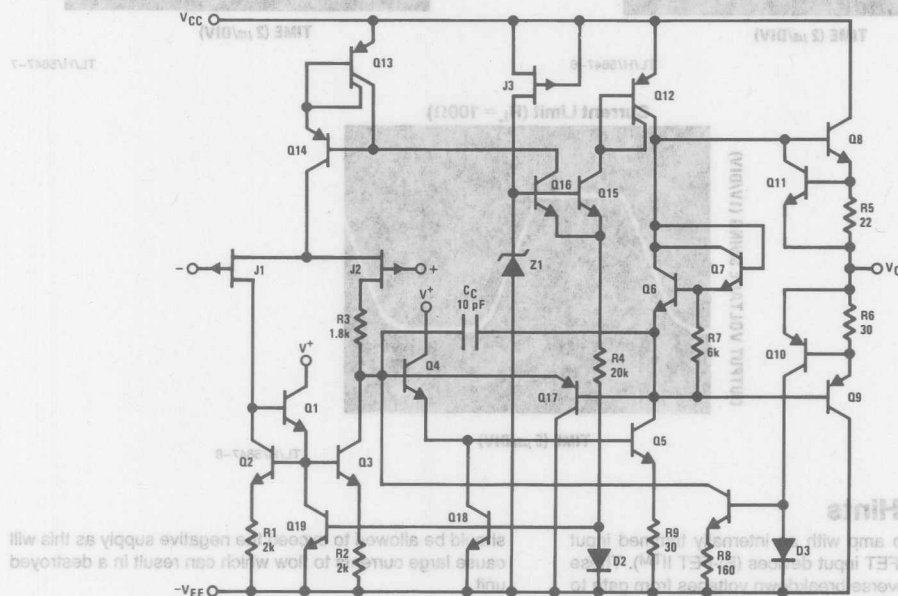
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in po-

larity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

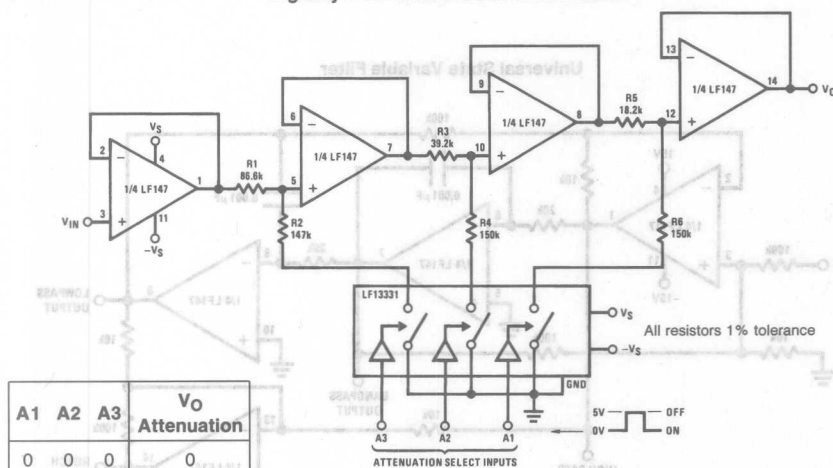
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



Typical Applications

Digitally Selectable Precision Attenuator

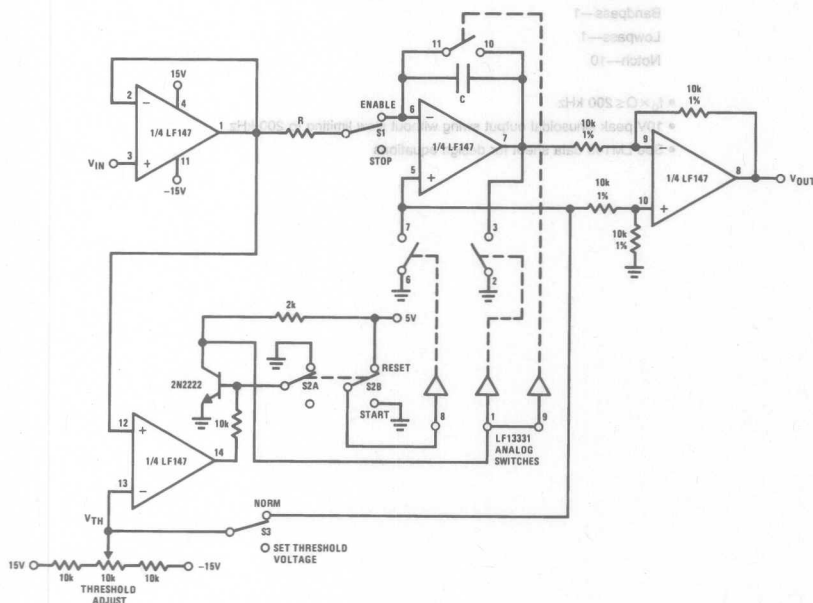


| A1 | A2 | A3 | V ₀ Attenuation |
|----|----|----|----------------------------|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | -1 dB |
| 0 | 1 | 0 | -2 dB |
| 0 | 1 | 1 | -3 dB |
| 1 | 0 | 0 | -4 dB |
| 1 | 0 | 1 | -5 dB |
| 1 | 1 | 0 | -6 dB |
| 1 | 1 | 1 | -7 dB |

- Accuracy of better than 0.4% with standard 1% value resistors
- No offset adjustment necessary
- Expandable to any number of stages
- Very high input impedance

TL/H/5647-10

Long Time Integrator with Reset, Hold and Starting Threshold Adjustment



- V_{OUT} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

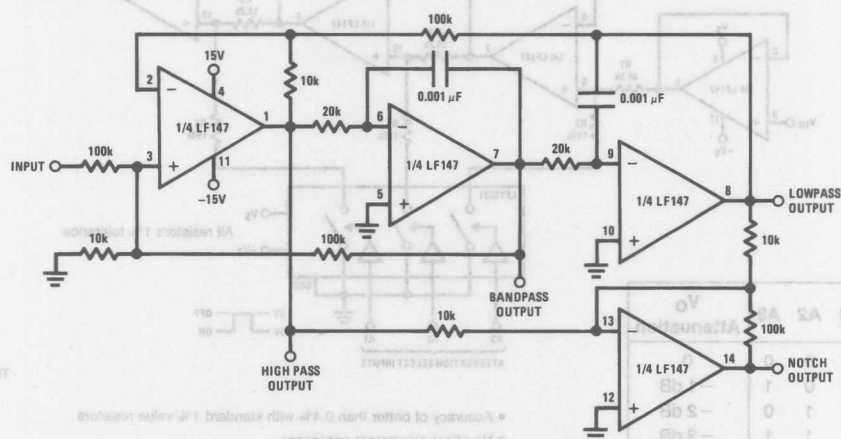
$$V_{OUT} = \frac{1}{RC} \int_0^t (V_{IN} - V_{TH}) dt$$

- Output starts when V_{IN} ≥ V_{TH}
- Switch S1 permits stopping and holding any output value
- Switch S2 resets system to zero

TL/H/5647-11

Typical Applications (Continued)

Universal State Variable Filter



For circuit shown:

$f_0 = 3 \text{ kHz}$, $f_{\text{NOTCH}} = 9.5 \text{ kHz}$
 $Q = 3.4$

Passband gain:

Highpass—0.1
 Bandpass—1
 Lowpass—1
 Notch—10

- $f_0 \times Q \leq 200 \text{ kHz}$
- 10V peak sinusoidal output swing without slew limiting to 200 kHz
- See LM148 data sheet for design equations

TL/H/5647-12

156/LF157

These are the first monolithic JFET input operational amplifiers to incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BI-FET™ Technology). These amplifiers feature low input bias and offset currents/low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low $1/f$ corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (5,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers

- (LF155A, LF156A, LF157A)

- Low input bias current
- Low Input Offset Current
- High input impedance
- Low input offset voltage
- Low input offset voltage temp. drift
- Low input noise current
- High common-mode rejection ratio
- Large dc voltage gain

| | LF155A | LF156A | LF157A ($A_V = 5$) | Units |
|---|--------|--------|-------------------------|-----------------|
| ■ Extremely fast settling time to 0.01% | 4 | 1.5 | 1.5 | μs |
| ■ Fast slew rate | 5 | 12 | 50 | V/ μs |
| ■ Wide gain bandwidth | 2.5 | 5 | 20 | MHz |
| ■ Low input noise voltage | 20 | 12 | 12 | nV/ \sqrt{Hz} |

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 8)

| | LF155A/6A/7A | LF155/6/7 | LF355B/6B/7B | LF355/6/7 | LF355A/6A/7A |
|---|-----------------|-----------------|-----------------|-----------------|--------------|
| Supply Voltage | ±22V | ±22V | ±22V | ±18V | |
| Differential Input Voltage | ±40V | ±40V | ±40V | ±30V | |
| Input Voltage Range (Note 2) | ±20V | ±20V | ±20V | ±16V | |
| Output Short Circuit Duration | Continuous | Continuous | Continuous | Continuous | |
| T _{JMAX} | | | | | |
| H-Package | 150°C | 150°C | 115°C | 115°C | |
| N-Package | | | 100°C | 100°C | |
| M-Package | | | 100°C | 100°C | |
| Power Dissipation at T _A = 25°C (Notes 1 and 9) | | | | | |
| H-Package (Still Air) | 560 mW | 560 mW | 400 mW | 400 mW | |
| H-Package (400 LF/Min Air Flow) | 1200 mW | 1200 mW | 1000 mW | 1000 mW | |
| N-Package | | | 670 mW | 670 mW | |
| M-Package | | | 380 mW | 380 mW | |
| Thermal Resistance (Typical) θ_{JA} | | | | | |
| H-Package (Still Air) | 160°C/W | 160°C/W | 160°C/W | 160°C/W | |
| H-Package (400 LF/Min Air Flow) | 65°C/W | 65°C/W | 65°C/W | 65°C/W | |
| N-Package | | | 130°C/W | 130°C/W | |
| M-Package | | | 195°C/W | 195°C/W | |
| (Typical) θ_{JC} | | | | | |
| H-Package | 23°C/W | 23°C/W | 23°C/W | 23°C/W | |
| Storage Temperature Range | -65°C to +150°C | -65°C to +150°C | -65°C to +150°C | -65°C to +150°C | |
| Soldering Information (Lead Temp.) | | | | | |
| Metal Can Package | | | | | |
| Soldering (10 sec.) | 300°C | 300°C | 300°C | 300°C | |
| Dual-In-Line Package | | | | | |
| Soldering (10 sec.) | | 260°C | 260°C | 260°C | |
| Small Outline Package | | | | | |
| Vapor Phase (60 sec.) | | | 215°C | 215°C | |
| Infrared (15 sec.) | | | 220°C | 220°C | |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | | | |
| ESD tolerance | | | | | |
| (100 pF discharged through 1.5 k Ω) | 1000V | 1000V | 1000V | 1000V | |

DC Electrical Characteristics (Note 3) T_A = T_J = 25°C

| Symbol | Parameter | Conditions | LF155A/6A/7A | | | LF355A/6A/7A | | | Units |
|---------------------------|--|--|----------------------|----------------------|----------|----------------------|----------------------|----------|-----------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S = 50 Ω , T _A = 25°C Over Temperature | | 1 | 2 2.5 | | 1 | 2 2.3 | mV mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | R _S = 50 Ω | | 3 | 5 | | 3 | 5 | $\mu V/^{\circ}C$ |
| $\Delta TC/\Delta V_{OS}$ | Change in Average TC with V _{OS} Adjust | R _S = 50 Ω , (Note 4) | | 0.5 | | | 0.5 | | $\mu V/^{\circ}C$ per mV |
| I _{OS} | Input Offset Current | T _J = 25°C, (Notes 3, 5) T _J \leq T _{HIGH} | | 3 | 10 10 | | 3 | 10 1 | pA nA |
| I _B | Input Bias Current | T _J = 25°C, (Notes 3, 5) T _J \leq T _{HIGH} | | 30 | 50 25 | | 30 | 50 5 | pA nA |
| R _{IN} | Input Resistance | T _J = 25°C | | 10 ¹² | | | 10 ¹² | | Ω |
| A _{VOL} | Large Signal Voltage Gain | V _S = $\pm 15V$, T _A = 25°C V _O = $\pm 10V$, R _L = 2k Over Temperature | 50 25 | 200 | | 50 25 | 200 | | V/mV V/mV |
| V _O | Output Voltage Swing | V _S = $\pm 15V$, R _L = 10k V _S = $\pm 15V$, R _L = 2k | ± 12 ± 10 | ± 13 ± 12 | | ± 12 ± 10 | ± 13 ± 12 | | V V |

DC Electrical Characteristics (Note 3) $T_A = T_j = 25^\circ\text{C}$ (Continued)

| Symbol | Parameter | Conditions | LF155A/6A/7A | | | LF355A/6A/7A | | | Units |
|----------|---------------------------------|------------------------|--------------|------------------|-----|--------------|------------------|-----|--------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{CM} | Input Common-Mode Voltage Range | $V_S = \pm 15\text{V}$ | ± 11 | $+15.1$ -12 | | ± 11 | $+15.1$ -12 | | V V |
| CMRR | Common-Mode Rejection Ratio | | 85 | 100 | | 85 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 85 | 100 | | 85 | 100 | | dB |

AC Electrical Characteristics $T_A = T_j = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

| Symbol | Parameter | Conditions | LF155A/355A | | | LF156A/356A | | | LF157A/357A | | | Units |
|----------|--------------------------------|--|-------------|--------------|-----|-------------|--------------|-----|-------------|--------------|-----|--|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| SR | Slew Rate | LF155A/6A; $A_V = 1$, LF157A; $A_V = 5$ | 3 | 5 | | 10 | 12 | | 40 | 50 | | V/ μs V/ μs |
| GBW | Gain Bandwidth Product | | | 2.5 | | 4 | 4.5 | | 15 | 20 | | MHz |
| t_s | Settling Time to 0.01% | (Note 7) | | 4 | | | 1.5 | | | 1.5 | | μs |
| e_n | Equivalent Input Noise Voltage | $R_S = 100\Omega$ $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$ | | 25 20 | | | 15 12 | | | 15 12 | | nV/ $\sqrt{\text{Hz}}$ nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$ | | 0.01 0.01 | | | 0.01 0.01 | | | 0.01 0.01 | | pA/ $\sqrt{\text{Hz}}$ pA/ $\sqrt{\text{Hz}}$ |
| C_{IN} | Input Capacitance | | | 3 | | | 3 | | | 3 | | pF |

DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | LF155/6/7 | | | LF255/6/7 LF355B/6B/7B | | | LF355/6/7 | | | Units |
|---------------------------|---|---|----------------------|----------------------|-----------|---------------------------|----------------------|----------|----------------------|----------------------|----------|--|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25^\circ\text{C}$ Over Temperature | | 3 | 5 7 | | 3 | 5 6.5 | | 3 | 10 13 | mV mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 50\Omega$ | | 5 | | | 5 | | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| $\Delta TC/\Delta V_{OS}$ | Change in Average TC with V_{OS} Adjust | $R_S = 50\Omega$, (Note 4) | | 0.5 | | | 0.5 | | | 0.5 | | $\mu\text{V}/^\circ\text{C}$ per mV |
| I_{OS} | Input Offset Current | $T_j = 25^\circ\text{C}$, (Notes 3, 5) $T_j \leq T_{HIGH}$ | | 3 | 20 20 | | 3 | 20 1 | | 3 | 50 2 | pA nA |
| I_B | Input Bias Current | $T_j = 25^\circ\text{C}$, (Notes 3, 5) $T_j \leq T_{HIGH}$ | | 30 | 100 50 | | 30 | 100 5 | | 30 | 200 8 | pA nA |
| R_{IN} | Input Resistance | $T_j = 25^\circ\text{C}$ | | 10^{12} | | | 10^{12} | | | 10^{12} | | Ω |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}$ Over Temperature | 50 | 200 | | 50 | 200 | | 25 | 200 | | V/mV V/mV |
| V_O | Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{k}$ $V_S = \pm 15\text{V}$, $R_L = 2\text{k}$ | ± 12 ± 10 | ± 13 ± 12 | | ± 12 ± 10 | ± 13 ± 12 | | ± 12 ± 10 | ± 13 ± 12 | | V V |
| V_{CM} | Input Common-Mode Voltage Range | $V_S = \pm 15\text{V}$ | ± 11 | $+15.1$ -12 | | ± 11 | $+15.1$ -12 | | $+10$ | $+15.1$ -12 | | V V |
| CMRR | Common-Mode Rejection Ratio | | 85 | 100 | | 85 | 100 | | 80 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 85 | 100 | | 85 | 100 | | 80 | 100 | | dB |

DC Electrical Characteristics $T_A = T_j = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

| Parameter | LF155A/155, LF255, LF355A/355B | | LF355 | | LF156A/156, LF256/356B | | LF356A/356 | | LF157A/157 LF257/357B | | LF357A/357 | | Units |
|----------------|--------------------------------------|-----|-------|-----|---------------------------|-----|------------|-----|--------------------------|-----|------------|-----|-------|
| | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | Typ | Max | |
| Supply Current | 2 | 4 | 2 | 4 | 5 | 7 | 5 | 10 | 5 | 7 | 5 | 10 | mA |

AC Electrical Characteristics $T_A = T_j = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$

| Symbol | Parameter | Conditions | LF155/255/ 355/355B | LF156/256, LF356B | LF156/256/ 356/356B | LF157/257, LF357B | LF157/257/ 357/357B | Units |
|----------|--------------------------------|--|------------------------|----------------------|------------------------|----------------------|------------------------|--|
| | | | Typ | Min | Typ | Min | Typ | |
| SR | Slew Rate | LF155/6: $A_V = 1$, LF157: $A_V = 5$ | 5 | 7.5 | 12 | 30 | 50 | $\text{V}/\mu\text{s}$ $\text{V}/\mu\text{s}$ |
| GBW | Gain Bandwidth Product | | 2.5 | | 5 | | 20 | MHz |
| t_s | Settling Time to 0.01% | (Note 7) | 4 | | 1.5 | | 1.5 | μs |
| e_n | Equivalent Input Noise Voltage | $R_S = 100\Omega$ $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$ | 25 20 | | 15 12 | | 15 12 | $\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Current Noise | $f = 100\text{ Hz}$ $f = 1000\text{ Hz}$ | 0.01 0.01 | | 0.01 0.01 | | 0.01 0.01 | $\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$ |
| C_{IN} | Input Capacitance | | 3 | | 3 | | 3 | pF |

Notes for Electrical Characteristics

Note 1: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by $T_{j\text{MAX}}$, θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_d = (T_{j\text{MAX}} - T_A)/\theta_{JA}$ or the 25°C $P_{d\text{MAX}}$, whichever is less.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: Unless otherwise stated, these test conditions apply:

| | LF155A/6A/7A LF155//6/7 | LF255//6/7 | LF355A/6A/7A | LF355B/6B/7B | LF355//6/7 |
|-----------------------|--|---|---|---|---|
| Supply Voltage, V_S | $\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$ | $\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$ | $\pm 15\text{V} \leq V_S \leq \pm 18\text{V}$ | $\pm 15\text{V} \leq V_S \leq \pm 20\text{V}$ | $V_S = \pm 15\text{V}$ |
| T_A | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ |
| T_{HIGH} | $+125^\circ\text{C}$ | $+85^\circ\text{C}$ | $+70^\circ\text{C}$ | $+70^\circ\text{C}$ | $+70^\circ\text{C}$ |

and V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0$.

Note 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount ($0.5\mu\text{V}/^\circ\text{C}$ typically) for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.

Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_d . $T_j = T_A + \theta_{JA} P_d$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

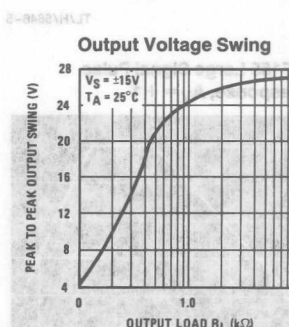
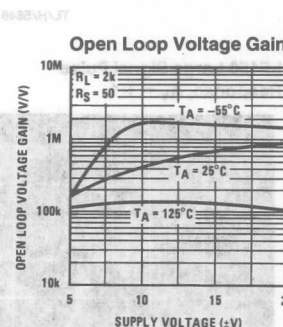
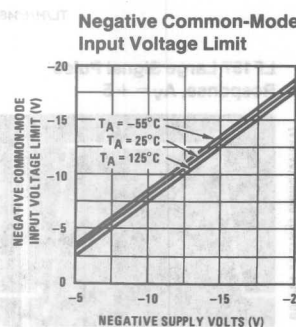
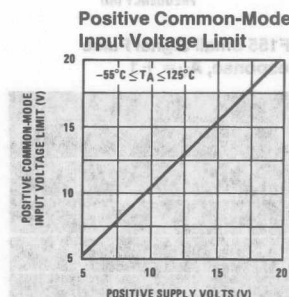
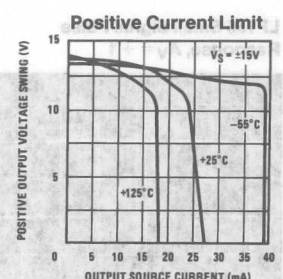
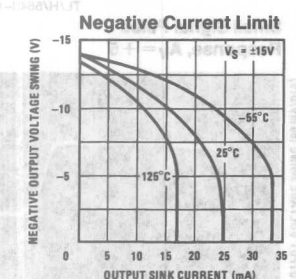
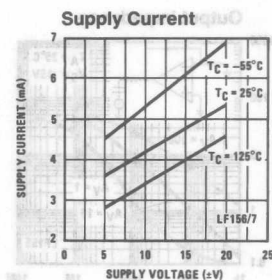
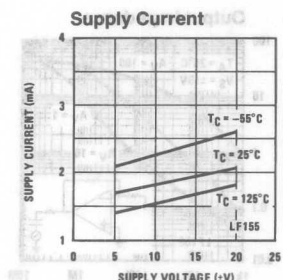
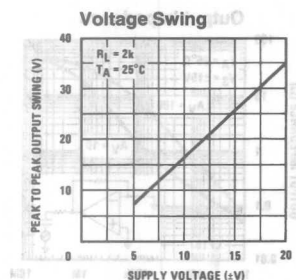
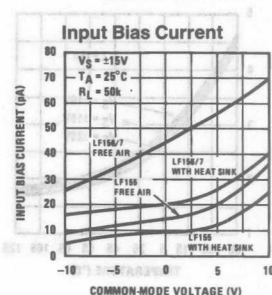
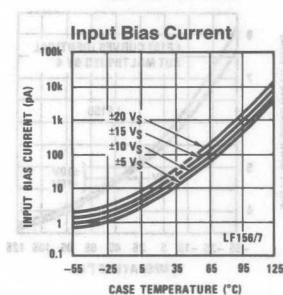
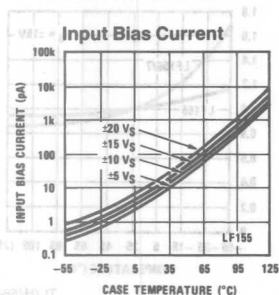
Note 7: Settling time is defined here, for a unity gain inverter connection using $2\text{ k}\Omega$ resistors for the LF155/6. It is the time required for the error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is $2\text{ k}\Omega$ and the output step is 10V (See Settling Time Test Circuit).

Note 8: Refer to RETS155AX for LF155A, RETS155X for LF155, RETS156AX for LF156A, RETS156X for LF156, RETS157A for LF157A and RETS157X for LF157 military specifications.

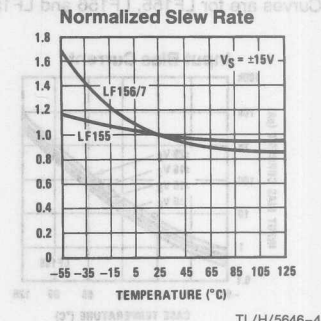
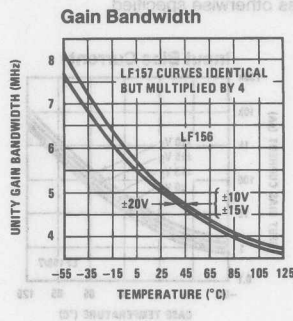
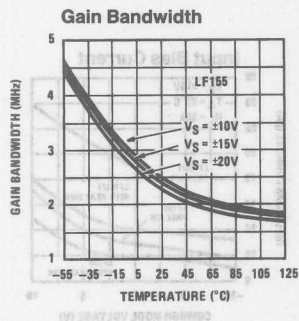
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical DC Performance Characteristics

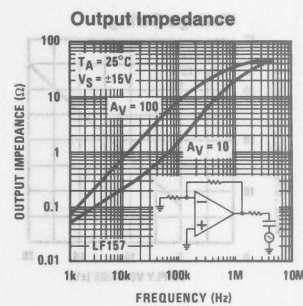
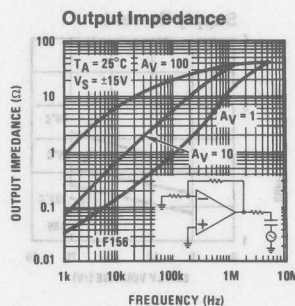
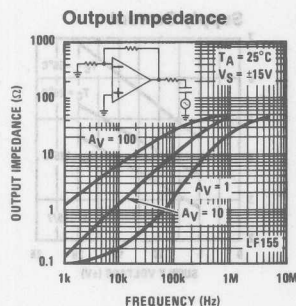
Curves are for LF155, LF156 and LF157 unless otherwise specified.



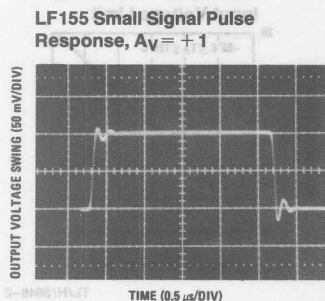
Typical AC Performance Characteristics



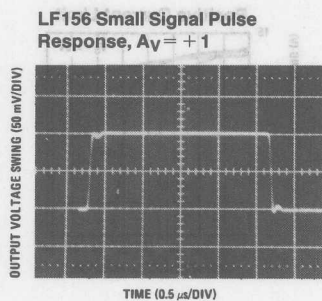
TL/H/5646-4



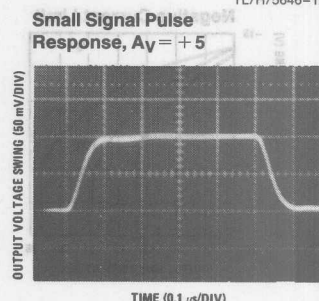
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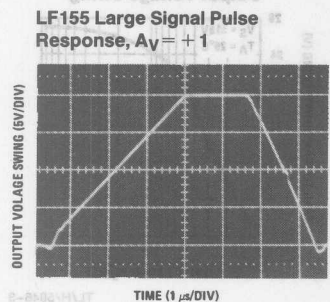
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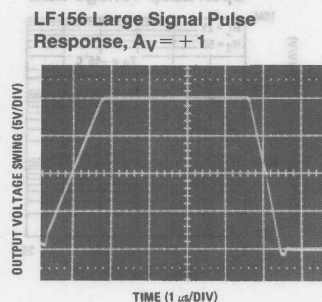
TL/H/5646-6



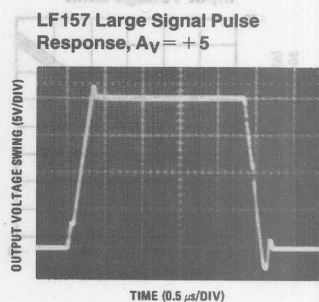
TL/H/5646-7



TL/H/5646-8

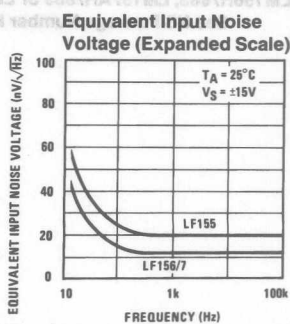
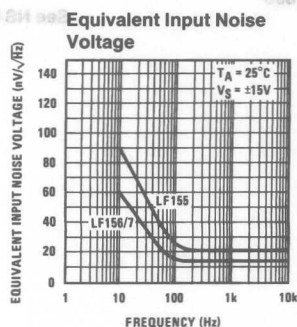
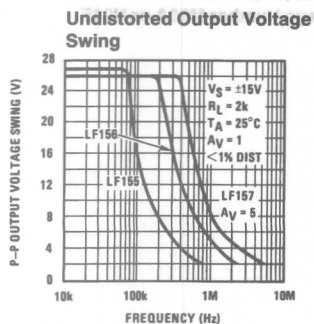
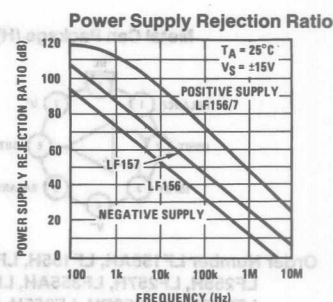
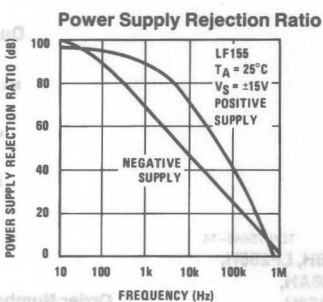
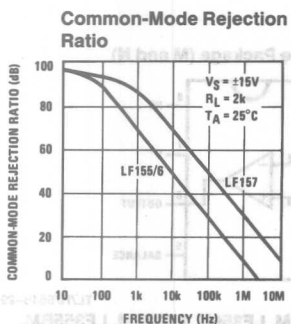
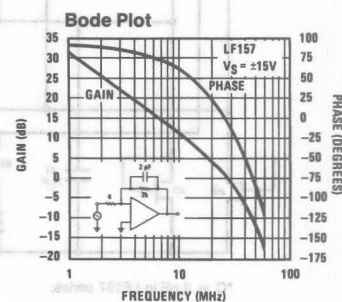
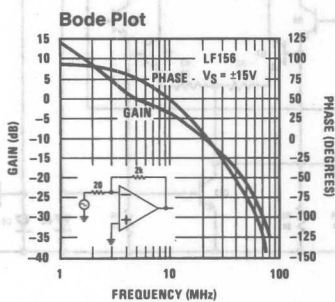
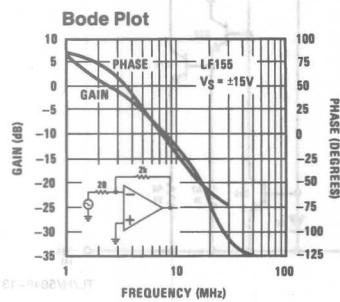
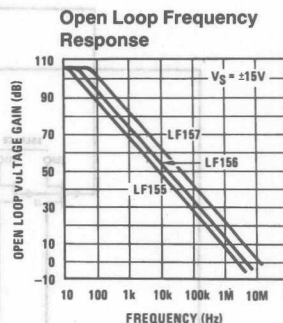
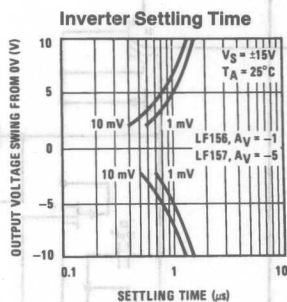
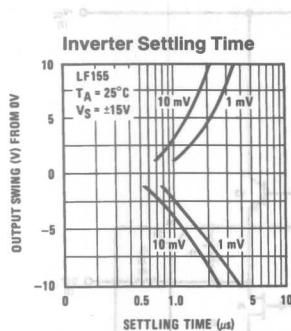


TL/H/5646-9



TL/H/5646-10

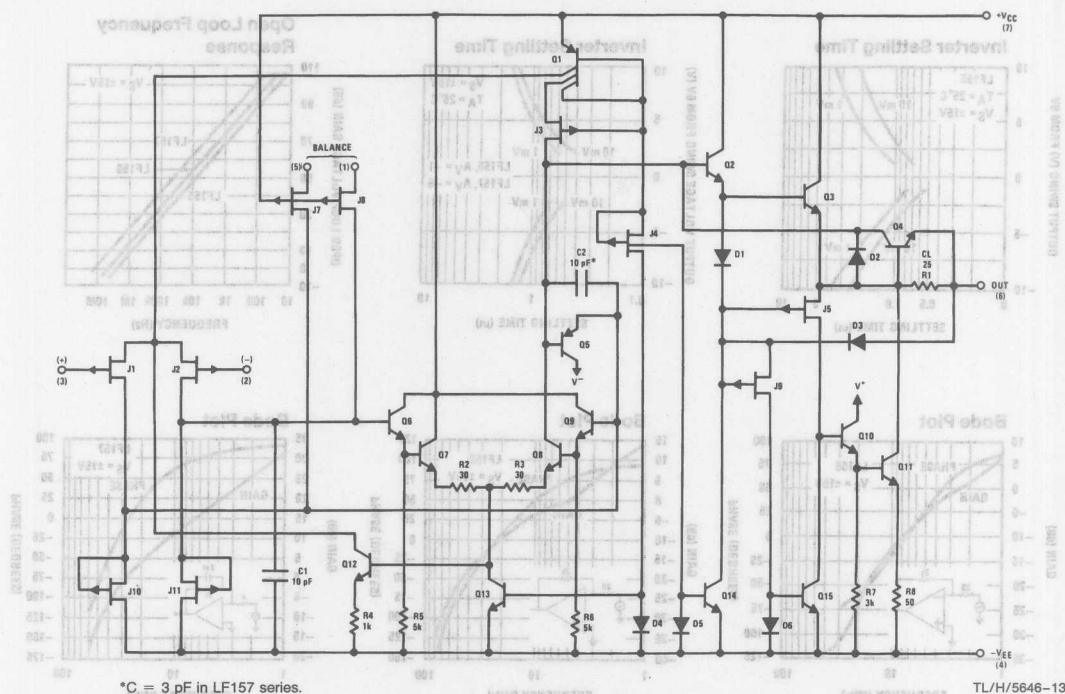
Typical AC Performance Characteristics (Continued)



LF155/LF156/LF157

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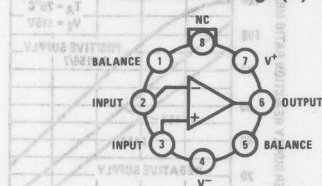
Detailed Schematic



*C = 3 pF in LF157 series.

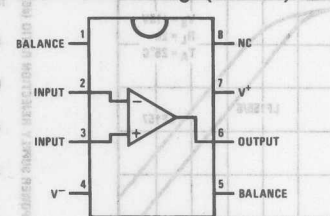
Connection Diagrams (Top Views)

Metal Can Package (H)



TL/H/5646-14

Dual-In-Line Package (M and N)



TL/H/5646-29

Order Number LF156AH, LF155H, LF156H, LF255H, LF256H, LF257H, LF355AH, LF356AH, LF357AH, LF356BH, LF355H, LF356H, LF357H, LM155AH/883, LM155H/883, LM156AH/883, LM156H/883, LM157AH/883 or LM157H/883*

See NS Package Number H08C

Order Number LF355M, LF356M, LF357M, LF355BM, LF356BM, LF355BN, LF356BN, LF357BN, LF355N, LF356N or LF357N

See NS Package Number M08A or N08E

*Available per JM38510/11401 or JM38510/11402

Application Hints

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

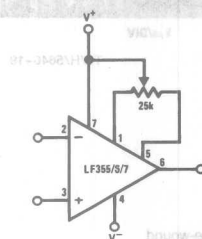
All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

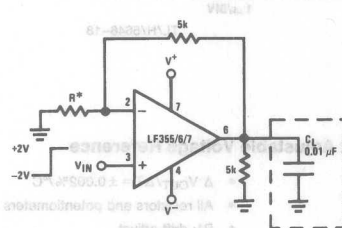
Typical Circuit Connections

V_{OS} Adjustment



- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V⁺
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is $\approx 0.5 \mu\text{V}/^\circ\text{C}/\text{mV}$ of adjustment
- Typical overall drift: $5 \mu\text{V}/^\circ\text{C} \pm (0.5 \mu\text{V}/^\circ\text{C}/\text{mV of adj.})$

Driving Capacitive Loads



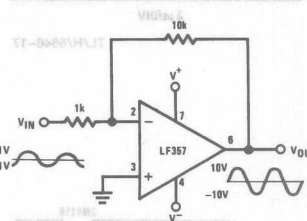
*LF155/6 R = 5k
LF157 R = 1.25k

Due to a unique output stage design, these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_L(\text{MAX}) \approx 0.01 \mu\text{F}$.

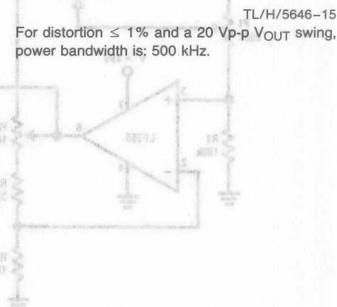
Overshoot $\leq 20\%$

Settling time (t_s) $\approx 5 \mu\text{s}$

LF157. A Large Power BW Amplifier

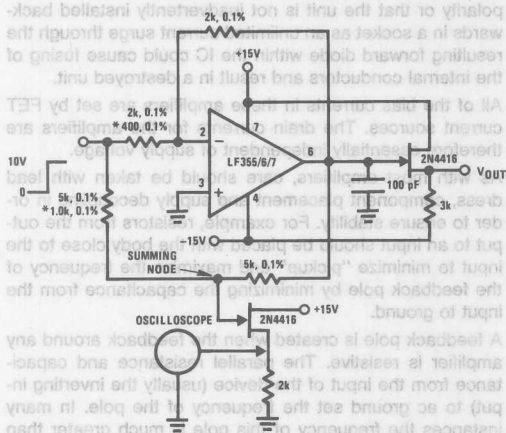


For distortion $\leq 1\%$ and a 20 Vp-p V_{OUT} swing, power bandwidth is: 500 kHz.



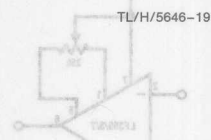
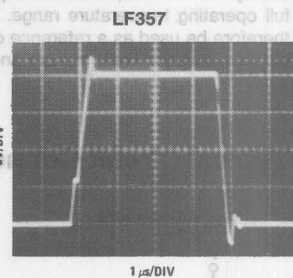
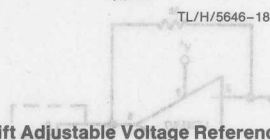
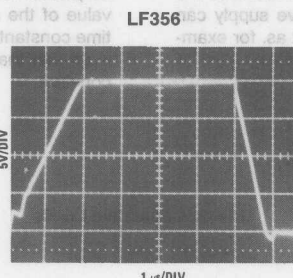
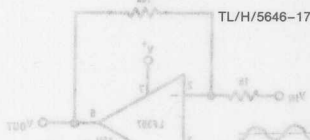
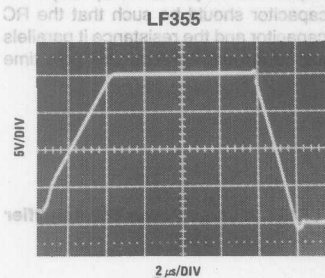
Typical Applications

Settling Time Test Circuit



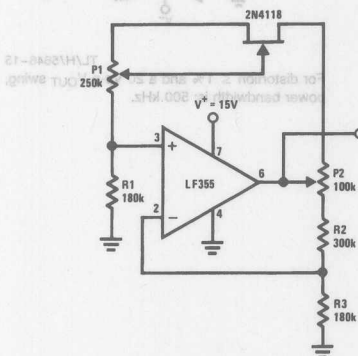
- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_v = -5$
- FET used to isolate the probe capacitance
- Output = 10V step
- $A_v = 5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)



Low Drift Adjustable Voltage Reference

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/^{\circ}\text{C}$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
 - Low I_B
 - Low drift
 - Low supply current



TL/H/5646-20

Application Hints

The LF155/6/7 series are op amps with JFET input stages. These JFETs have large reverse breakdown voltages and drain eliminating the need for clamping across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the positive common-mode limit on a single input will force the output to a high state. Exceeding the negative common-mode limit on a single input will force the output to a low state. Exceeding the common-mode limit on both inputs will force the output to a high state. Exceeding the common-mode limit on both inputs will force the output to a low state.

TL/H/5646-16

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply and over the full operating range. The positive supply can be as low as 10V and the negative supply can be as low as -10V.

TL/H/5646-18

• V_{OS} is adjusted with a 50k potentiometer

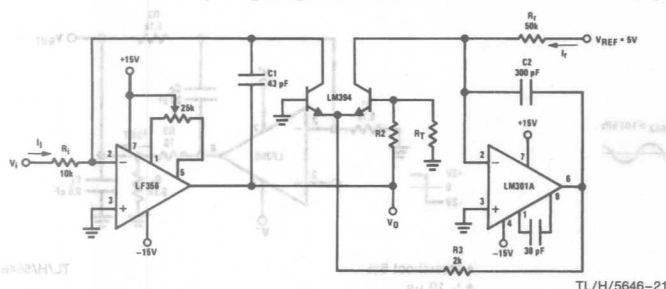
• The potentiometer wiper is connected to V_{+}

• For potentiometers with temperature coefficients of 100 ppm/°C or less the additional drift with adjustment is $\pm 0.5 \text{ } \mu\text{V}/^{\circ}\text{C}$ per 10V of adjustment

• Typical overall drift: $\pm 0.5 \text{ } \mu\text{V}/^{\circ}\text{C}$ (to 10V of adjustment)

Typical Applications (Continued)

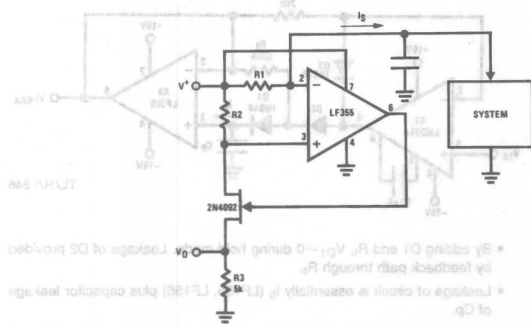
Fast Logarithmic Converter



- Dynamic range: $100 \mu A \leq I_i \leq 1 \text{ mA}$ (5 decades), $|V_O| = 1V/\text{decade}$
- Transient response: $3 \mu s$ for $\Delta I_i = 1 \text{ decade}$
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T : Tel Labs type Q81 + $0.3\%/^{\circ}C$

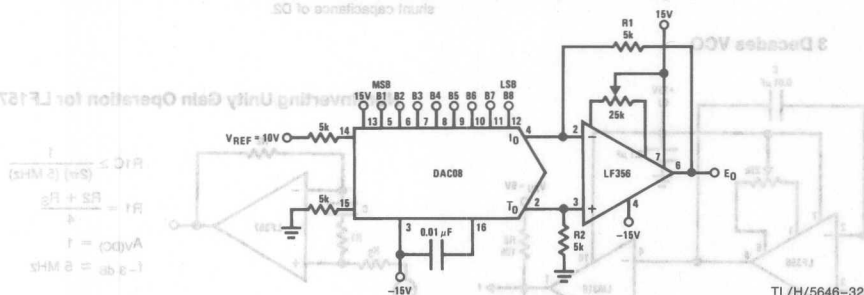
$$|V_{out}| = \left[1 + \frac{R_2}{R_T} \right] \frac{kT}{q} \ln V_i \left[\frac{R_f}{V_{REF} R_i} \right] = \log V_i \frac{1}{R_{f/R_i}} R_2 = 15.7k, R_T = 1k, 0.3\%/^{\circ}C \text{ (for temperature compensation)}$$

Precision Current Monitor



- $V_O = 5 R_1/R_2$ (V/mA of I_g)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
 - Common-mode range to supply range
 - Low I_B
 - Low V_{OS}
 - Low Supply Current

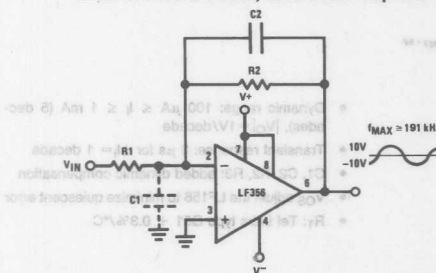
8-Bit D/A Converter with Symmetrical Offset Binary Operation



- R1, R2 should be matched within $\pm 0.05\%$
- Full-scale response time: $3 \mu s$

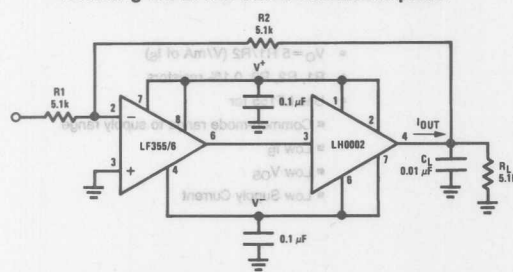
| E_0 | B1 | B2 | B3 | B4 | B5 | B6 | B7 | B8 | Comments |
|--------|----|----|----|----|----|----|----|----|---------------------|
| +9.920 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Positive Full-Scale |
| +0.040 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | (+) Zero-Scale |
| -0.040 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | (-) Zero-Scale |
| -9.920 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Negative Full-Scale |

Wide BW Low Noise, Low Drift Amplifier



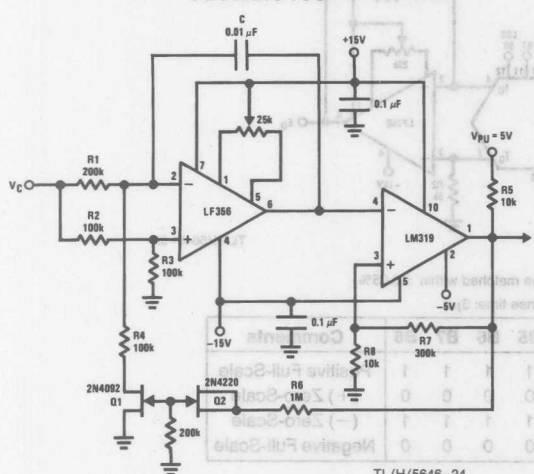
- Power BW: $f_{MAX} = \frac{S_T}{2\pi V_P} \approx 191 \text{ kHz}$
- Parasitic input capacitance $C_1 \approx (3 \text{ pF for LF155, LF156 and LF157 plus any additional layout capacitance})$ interacts with feedback elements and creates undesirable high frequency pole. To compensate add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

Boosting the LF156 with a Current Amplifier



- $I_{OUT(MAX)} \approx 150 \text{ mA}$ (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = \frac{0.15}{10^{-2}} \text{ V}/\mu\text{s}$ (with C_L shown)
- No additional phase shift added by the current amplifier.

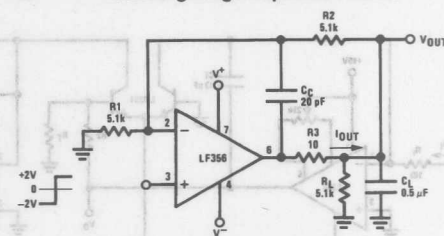
3 Decades VCO



- $f = \frac{V_C (R_8 + R_7)}{(8 V_{PU} R_8 R_1) C}$ $0 \leq V_C \leq 30V$, $10 \text{ Hz} \leq f \leq 10 \text{ kHz}$
 R_1, R_4 matched. Linearity 0.1% over 2 decades.

TL/H/5646-24

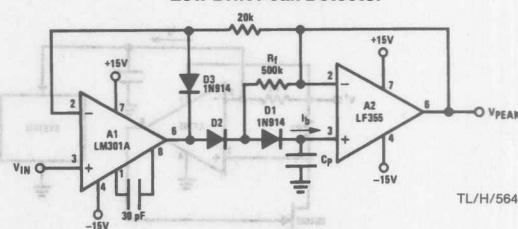
Isolating Large Capacitive Loads



- Overshoot 6%
- $t_s 10 \mu\text{s}$
- When driving large C_L , the V_{OUT} slew rate determined by C_L and $I_{OUT(MAX)}$:
 $\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \approx \frac{0.02}{0.5} \text{ V}/\mu\text{s} = 0.04 \text{ V}/\mu\text{s}$ (with C_L shown)

TL/H/5646-22

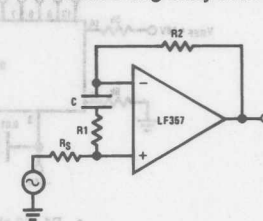
Low Drift Peak Detector



- By adding D_1 and R_f , $V_{D1} = 0$ during hold mode. Leakage of D_2 provided by feedback path through R_f .
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_p .
- Diode D_3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D_2 .
- Maximum input frequency should be $\ll \frac{1}{2\pi R_f C_{D2}}$ where C_{D2} is the shunt capacitance of D_2 .

TL/H/5646

Non-Inverting Unity Gain Operation for LF157



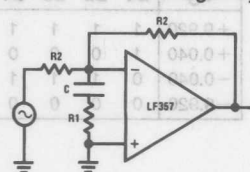
$$R_1 C \geq \frac{1}{(2\pi) (5 \text{ MHz})}$$

$$R_1 = \frac{R_2 + R_S}{4}$$

$$A_V(DC) = 1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

Inverting Unity Gain for LF157



$$R_1 C \geq \frac{1}{(2\pi) (5 \text{ MHz})}$$

$$R_1 = \frac{R_2}{4}$$

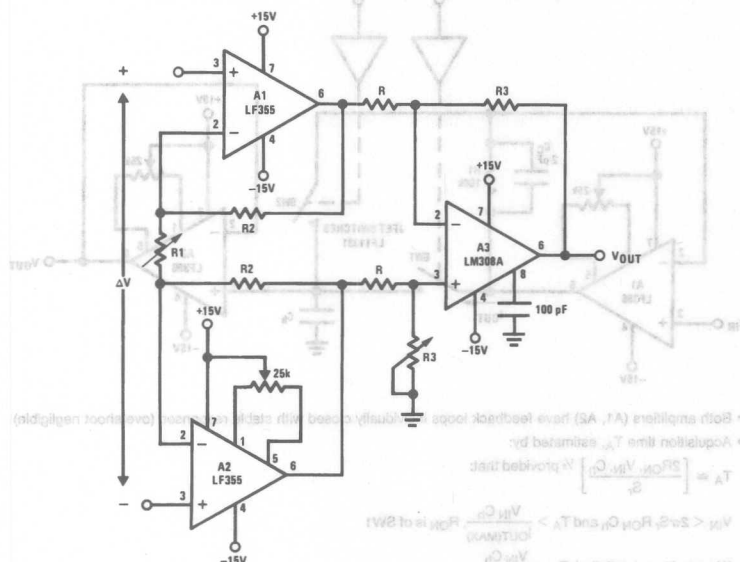
$$A_V(DC) = -1$$

$$f_{-3 \text{ dB}} \approx 5 \text{ MHz}$$

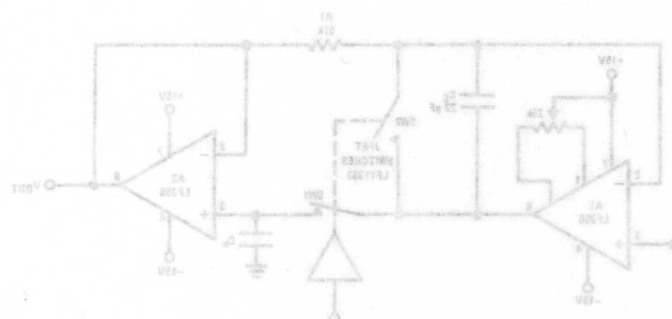
TL/H/5646-25

Typical Applications (Continued)

High Impedance, Low Drift Instrumentation Amplifier



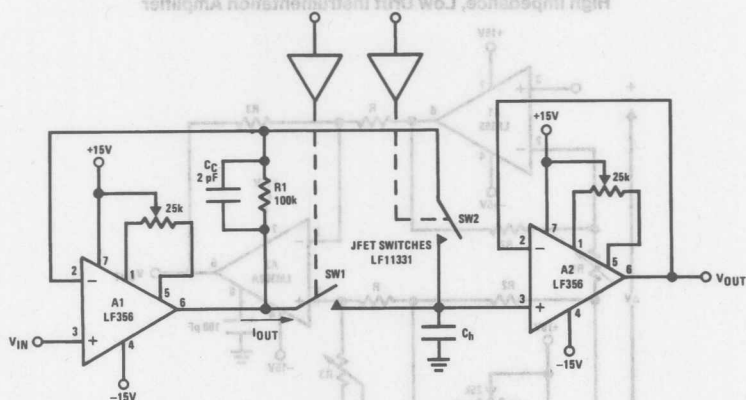
- $V_{OUT} = \frac{R_3}{R} \left[\frac{2R_2}{R_1} + 1 \right] \Delta V$, $V^- + 2V \leq V_{IN \text{ common-mode}} \leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier resistor array recommended for best accuracy and lowest drift



- By closing the loop through A2, the V_{OUT} accuracy will be determined mainly by A1.
- The V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously, but, because of the added propagation delay in the feedback loop (A2), the overvoltage is not negligible.
- Overall system slower than test sample and hold.
- R1, C1: additional compensation.
- Use LF155 for
- Fast settling time
- Low V_{OS}

Typical Applications (Continued)

Fast Sample and Hold



TL/H/5646-33

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time T_A , estimated by:

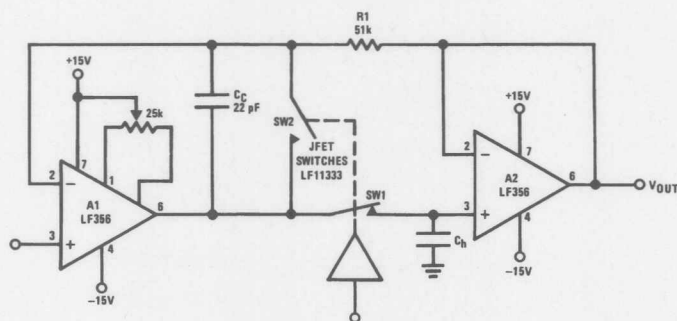
$$T_A \approx \left[\frac{2R_{ON} \cdot V_{IN} \cdot C_H}{S_r} \right]^{1/2} \text{ provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_H \text{ and } T_A > \frac{V_{IN} C_H}{I_{OUT(MAX)}} \text{, } R_{ON} \text{ is of SW1}$$

$$\text{If inequality not satisfied: } T_A \approx \frac{V_{IN} C_H}{20 \text{ mA}}$$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

High Accuracy Sample and Hold

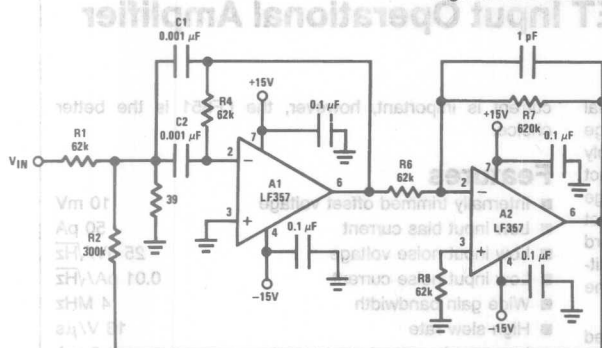


TL/H/5646-27

- By closing the loop through A2, the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but, because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C : additional compensation
- Use LF156 for
 - Fast settling time
 - Low V_{OS}

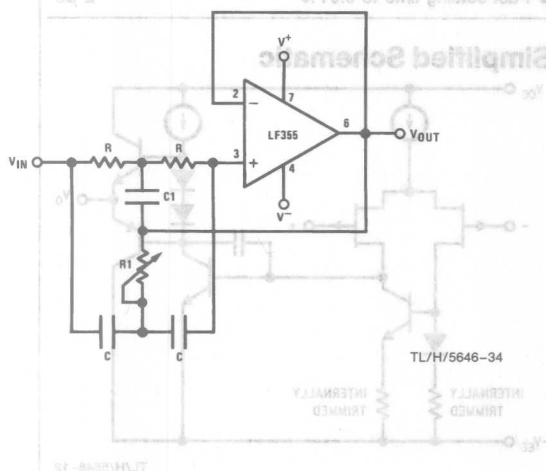
Typical Applications (Continued)

High Q Band Pass Filter



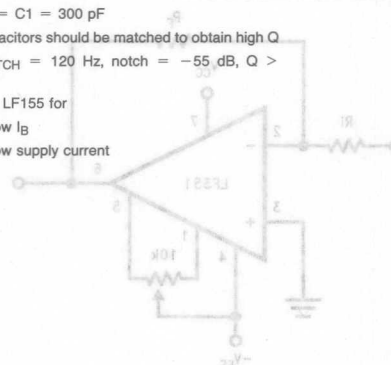
- By adding positive feedback (R2)
Q increases to 40
- $f_{BP} = 100 \text{ kHz}$
- $V_{OUT} = 10/V_{IN}$
- Clean layout recommended
- Response to a 1 Vp-p tone burst:
300 μs

High Q Notch Filter

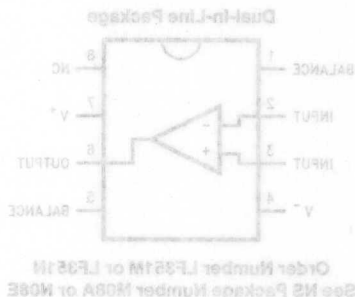


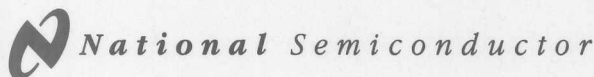
- $2R1 = R = 10 \text{ M}\Omega$
- $2C = C1 = 300 \text{ pF}$
- Capacitors should be matched to obtain high Q
- $f_{NOTCH} = 120 \text{ Hz}$, notch = -55 dB, $Q > 100$
- Use LF155 for
 - Low I_B
 - Low supply current

Typical Connection



Connection Diagrams





LF351 Wide Bandwidth JFET Input Operational Amplifier

General Description

The LF351 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET II™ technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF351 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

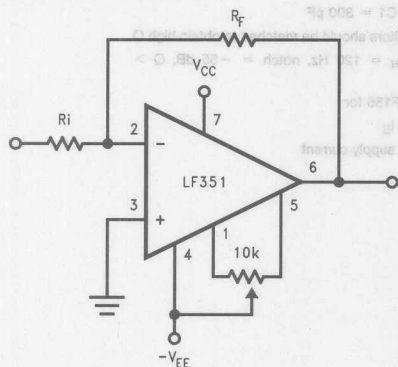
The LF351 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements are critical, the LF356 is recommended. If maximum supply

current is important, however, the LF351 is the better choice.

Features

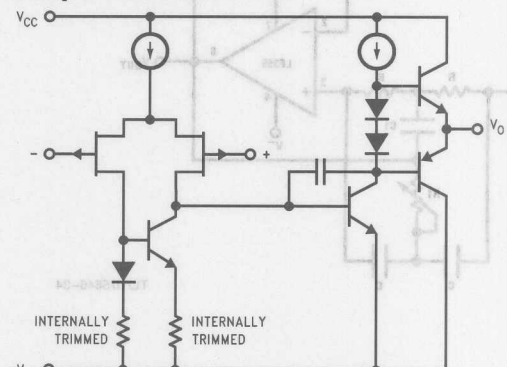
- Internally trimmed offset voltage 10 mV
- Low input bias current 50 pA
- Low input noise voltage 25 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 1.8 mA
- High input impedance 10¹²Ω
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, BW = 20 Hz–20 kHz < 0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection



TL/H/5648-11

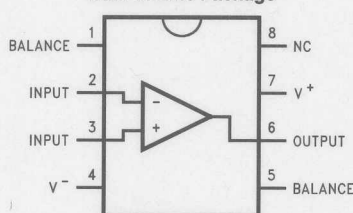
Simplified Schematic



TL/H/5648-12

Connection Diagrams

Dual-In-Line Package



Order Number LF351M or LF351N
See NS Package Number M08A or N08E

TL/H/5648-13

Absolute Maximum Ratings

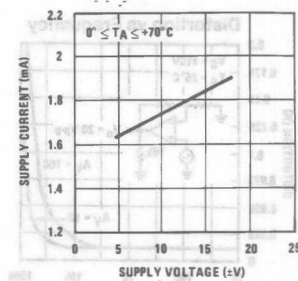
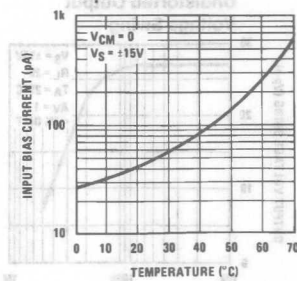
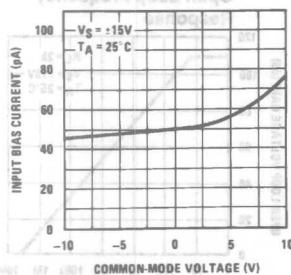
If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | | | |
|-----------------------------------|---|---|-----------------------|
| Supply Voltage | $\pm 18\text{V}$ | Soldering Information | |
| Power Dissipation (Notes 1 and 6) | 670 mW | Dual-In-Line Package | |
| Operating Temperature Range | 0°C to $+70^{\circ}\text{C}$ | Soldering (10 sec.) | 260°C |
| $T_{\text{J}}(\text{MAX})$ | 115°C | Small Outline Package | |
| Differential Input Voltage | $\pm 30\text{V}$ | Vapor Phase (60 sec.) | 215°C |
| Input Voltage Range (Note 2) | $\pm 15\text{V}$ | Infrared (15 sec.) | 220°C |
| Output Short Circuit Duration | Continuous | See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | |
| Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ | ESD rating to be determined. | |
| Lead Temp. (Soldering, 10 sec.) | | | |
| Metal Can | 300°C | | |
| DIP | 260°C | | |

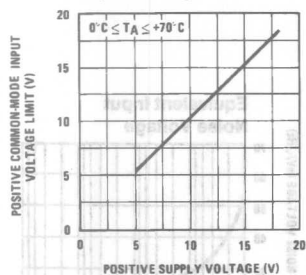
DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | LF351 | | | Units |
|---------------------------------|------------------------------------|--|----------|------------|-----|--------------------------------|
| | | | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_{\text{S}} = 10\text{ k}\Omega$, $T_{\text{A}} = 25^{\circ}\text{C}$ Over Temperature | | 5 | 10 | mV |
| $\Delta V_{\text{OS}}/\Delta T$ | Average TC of Input Offset Voltage | $R_{\text{S}} = 10\text{ k}\Omega$ | | 10 | 13 | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{OS} | Input Offset Current | $T_{\text{J}} = 25^{\circ}\text{C}$, (Notes 3, 4) $T_{\text{J}} \leq 70^{\circ}\text{C}$ | | 25 | 100 | pA |
| I_{B} | Input Bias Current | $T_{\text{J}} = 25^{\circ}\text{C}$, (Notes 3, 4) $T_{\text{J}} \leq \pm 70^{\circ}\text{C}$ | | 50 | 200 | pA |
| R_{IN} | Input Resistance | $T_{\text{J}} = 25^{\circ}\text{C}$ | | 10^{12} | | Ω |
| A_{VOL} | Large Signal Voltage Gain | $V_{\text{S}} = \pm 15\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$ $V_{\text{O}} = \pm 10\text{V}$, $R_{\text{L}} = 2\text{ k}\Omega$ Over Temperature | 25 | 100 | | V/mV |
| V_{O} | Output Voltage Swing | $V_{\text{S}} = \pm 15\text{V}$, $R_{\text{L}} = 10\text{ k}\Omega$ | ± 12 | ± 13.5 | | V |
| V_{CM} | Input Common-Mode Voltage Range | $V_{\text{S}} = \pm 15\text{V}$ | ± 11 | +15 -12 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_{\text{S}} \leq 10\text{ k}\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 5) | 70 | 100 | | dB |
| I_{S} | Supply Current | | | 1.8 | 3.4 | mA |

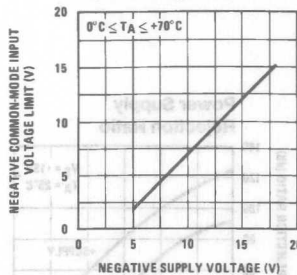
| | | | Min | Typ | Max | |
|--|---|---|-----|------|-----|-----------------|
| SR | Slew Rate | $V_S = \pm 15V, T_A = 25^\circ C$ | | 13 | | V/ μs |
| GBW | Gain Bandwidth Product | $V_S = \pm 15V, T_A = 25^\circ C$ | | 4 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ C, R_S = 100\Omega, f = 1000 Hz$ | | 25 | | nV/ \sqrt{Hz} |
| i_n | Equivalent Input Noise Current | $T_j = 25^\circ C, f = 1000 Hz$ | | 0.01 | | pA/ \sqrt{Hz} |
| <p>Note 1: For operating at elevated temperature, the device must be derated based on the thermal resistance, θ_{JA}.</p> <p>Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.</p> <p>Note 3: These specifications apply for $V_S = \pm 15V$ and $0^\circ C \leq T_A \leq +70^\circ C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.</p> <p>Note 4: The input bias currents are junction leakage currents which approximately double for every $10^\circ C$ increase in the junction temperature, T_j. Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.</p> <p>Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From $\pm 15V$ to $\pm 5V$.</p> <p>Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.</p> | | | | | | |
| V_{OS} | Input Offset Voltage | $R_F = 10 k\Omega, T_A = 25^\circ C$ | | | | |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_F = 10 k\Omega$ | | | | |
| I_{OS} | Input Offset Current | $T = 25^\circ C$ (Notes 3, 4) $T \leq 70^\circ C$ | | | | |
| I_B | Input Bias Current | $T = 25^\circ C$ (Notes 3, 4) $T \leq \pm 70^\circ C$ | | | | |
| R_{IN} | Input Resistance | $T = 25^\circ C$ | | | | |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15V, T_A = 25^\circ C$ $V_O = \pm 10V, R_L = 2 k\Omega$ Over Temperature | | | | |
| V_O | Output Voltage Swing | $V_S = \pm 15V, R_L = 10 k\Omega$ | | | | |
| V_{CM} | Input Common-Mode Voltage Range | $V_S = \pm 15V$ | | | | |
| CMRR | Common-Mode Rejection Ratio | $R_F \leq 10 k\Omega$ | | | | |
| PSRR | Supply Voltage Rejection Ratio (Note 5) | | | | | |
| I_S | Supply Current | | | | | |



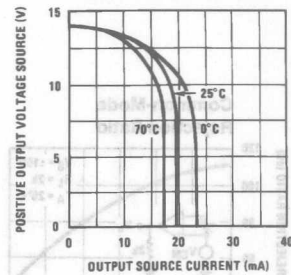
Positive Common-Mode Input Voltage Limit



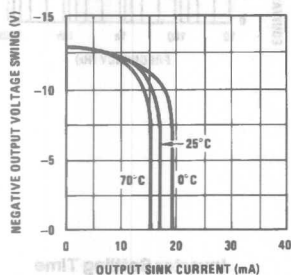
Negative Common-Mode Input Voltage Limit



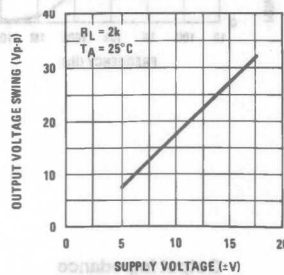
Positive Current Limit



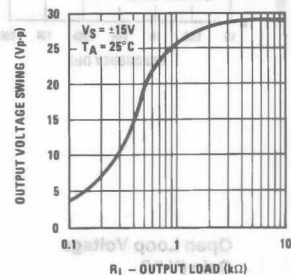
Negative Current Limit



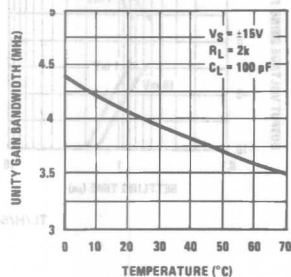
Voltage Swing



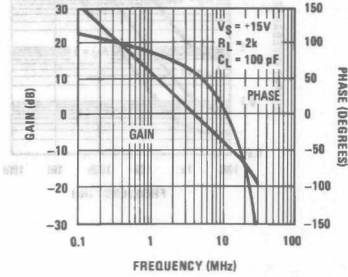
Output Voltage Swing



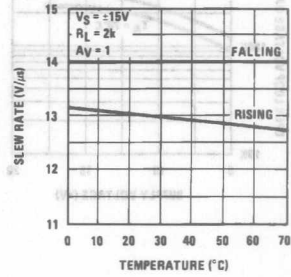
Gain Bandwidth



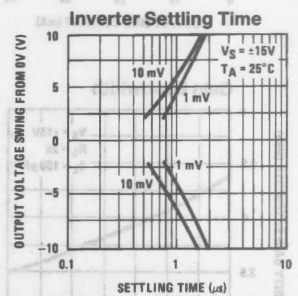
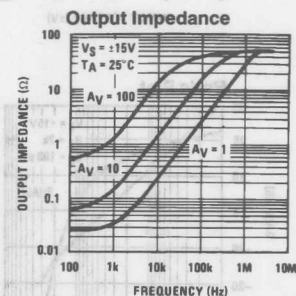
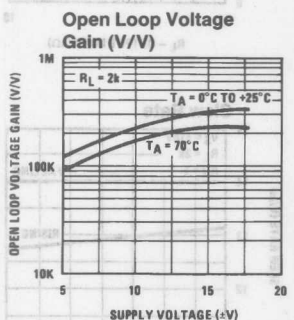
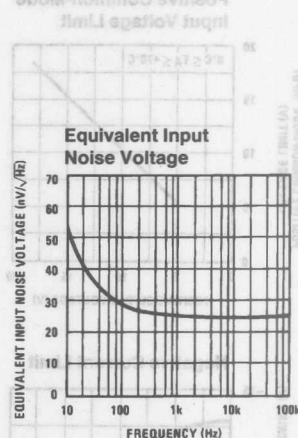
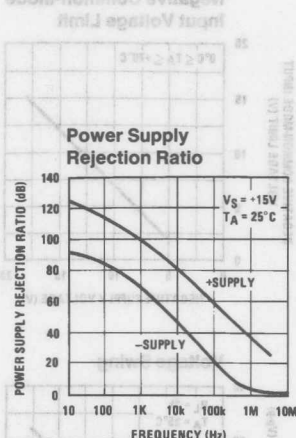
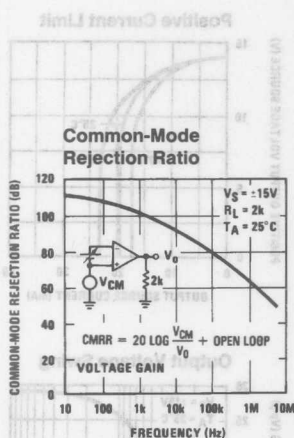
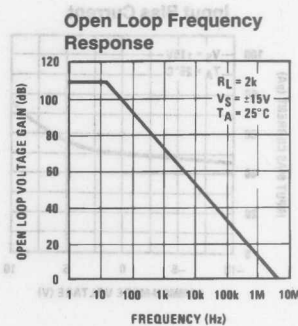
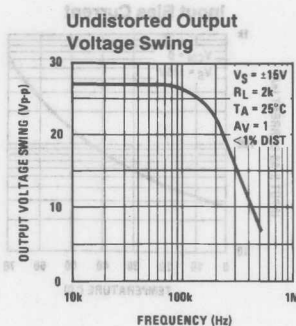
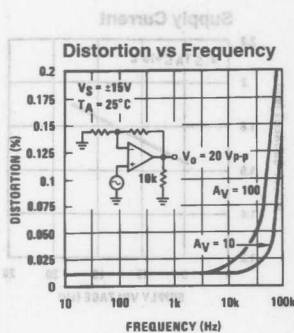
Bode Plot



Slew Rate



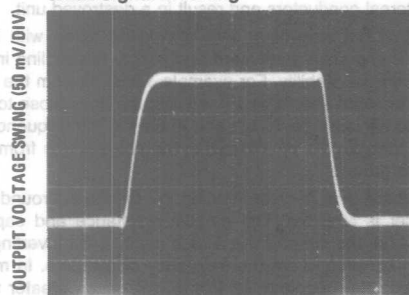
Typical Performance Characteristics (Continued)



TL/H/5648-3

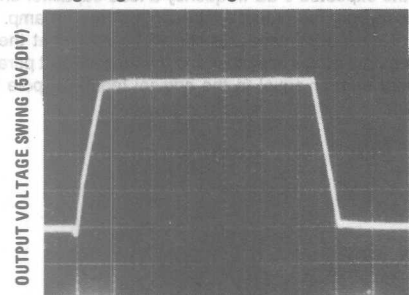
Pulse Response

Small Signal Inverting



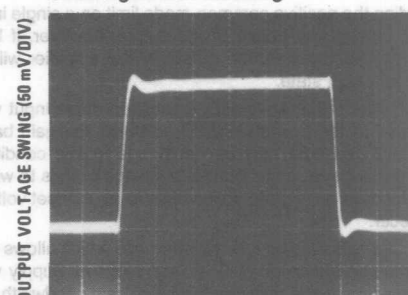
TIME (0.2 μs/DIV)

Large Signal Inverting



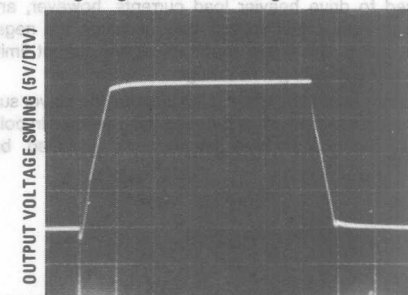
TIME (2 μs/DIV)

Small Signal Non-Inverting



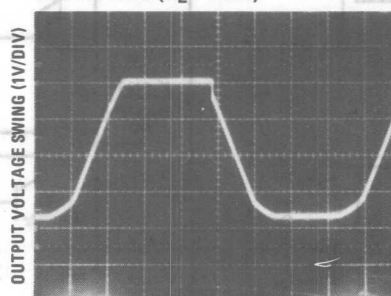
TIME (0.2 μs/DIV)

Large Signal Non-Inverting



TIME (2 μs/DIV)

Current Limit ($R_L = 100\Omega$)



TIME (5 μs/DIV)

Application Hints

The LF351 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET IITM). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will

cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF351 is biased by a zener reference which allows normal circuit operation on $\pm 4V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF351 will drive a 2 k Ω load resistance to $\pm 10V$ over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

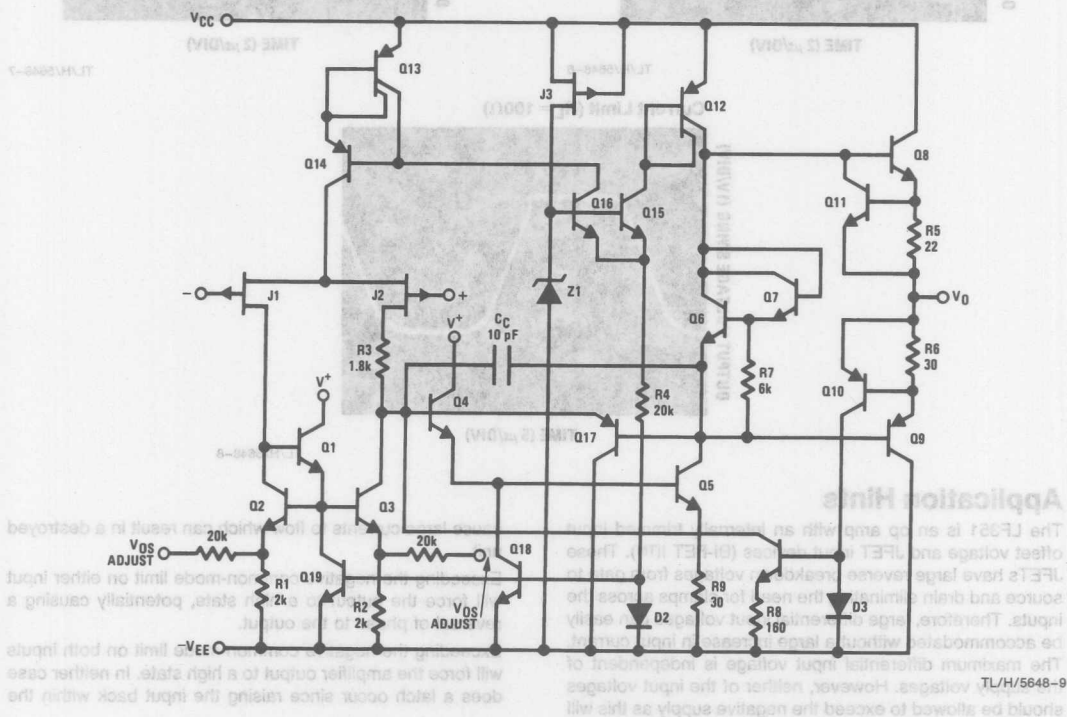
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed back-

resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

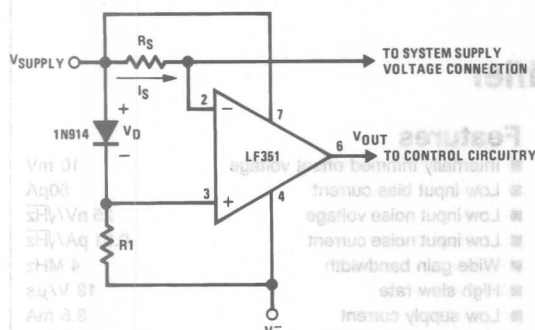
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



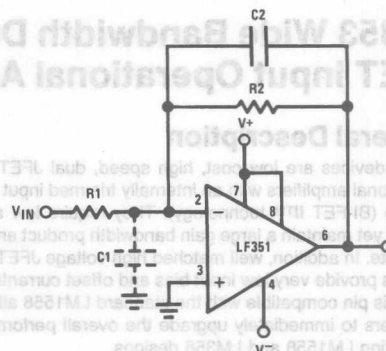
Typical Applications

Supply Current Indicator/Limiter



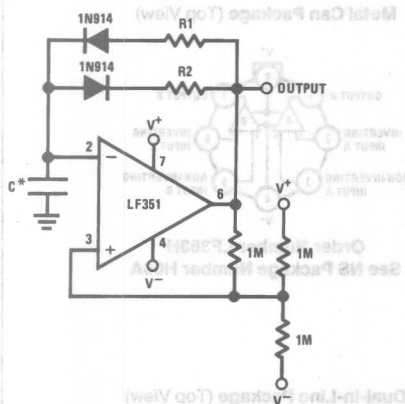
* V_{OUT} switches high when $R_S I_S > V_D$

Hi- Z_{IN} Inverting Amplifier



Parasitic input capacitance $C_1 \approx (3 \text{ pF for LF351 plus any additional layout capacitance})$ interacts with feedback elements and creates undesirable high frequency pole. To compensate, add C_2 such that: $R_2 C_2 \approx R_1 C_1$.

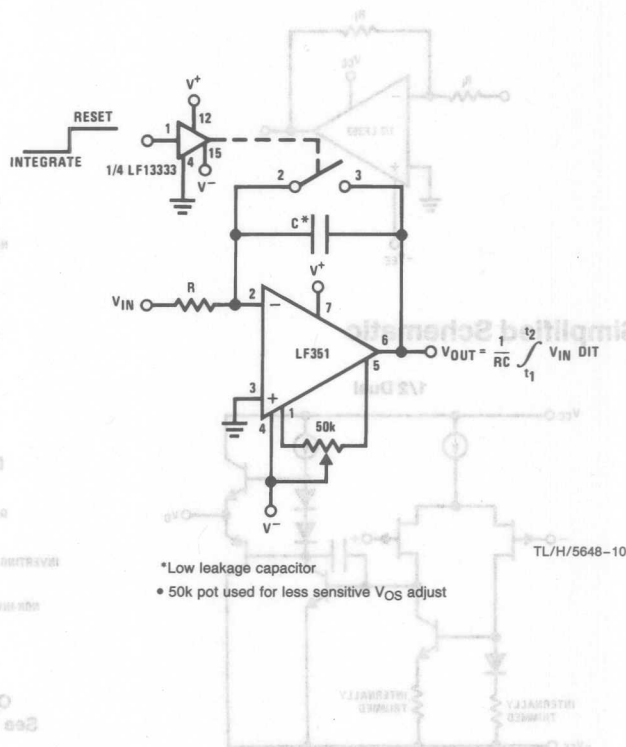
Ultra-Low (or High) Duty Cycle Pulse Generator



* $t_{\text{OUTPUT HIGH}} \approx R_1 C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$
 * $t_{\text{OUTPUT LOW}} \approx R_2 C \ln \frac{2V_S - 7.8}{V_S - 7.8}$
 where $V_S = V^+ + |V^-|$

*low leakage capacitor

Long Time Integrator



*Low leakage capacitor

* 50k pot used for less sensitive V_{OS} adjust

LF353 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

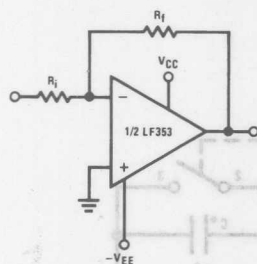
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET IITM technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF353 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

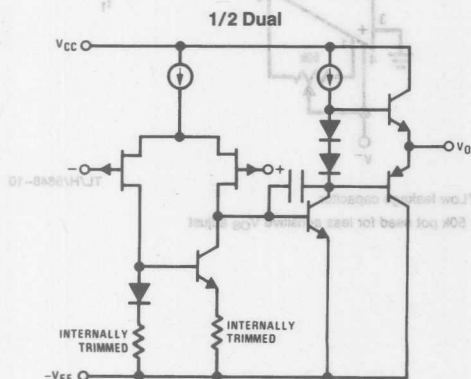
Features

- Internally trimmed offset voltage 10 mV
- Low input bias current 50pA
- Low input noise voltage 25 nV/√Hz
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 4 MHz
- High slew rate 13 V/μs
- Low supply current 3.6 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20Vp-p$, BW = 20 Hz-20 kHz < 0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection

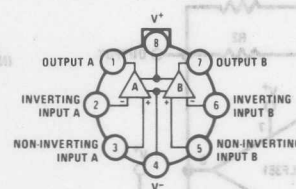


Simplified Schematic



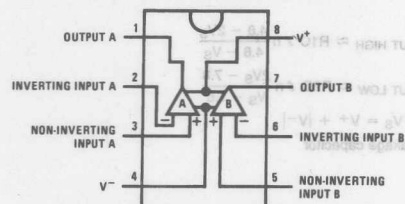
Connection Diagrams

Metal Can Package (Top View)



Order Number LF353H
See NS Package Number H08A

Dual-In-Line Package (Top View)



Order Number LF353M or LF353N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-------------------------------|---|
| Supply Voltage | $\pm 18\text{V}$ |
| Power Dissipation | (Note 1) |
| Operating Temperature Range | 0°C to $+70^{\circ}\text{C}$ |
| $T_J(\text{MAX})$ | 150°C |
| Differential Input Voltage | $\pm 30\text{V}$ |
| Input Voltage Range (Note 2) | $\pm 15\text{V}$ |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ |

Lead Temp. (Soldering, 10 sec.)

260°C

Soldering Information

Dual-In-Line Package

Soldering (10 sec.)

260°C

Small Outline Package

Vapor Phase (60 sec.)

215°C

Infrared (15 sec.)

220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7)

1700V

θ_{JA} M Package

TBD

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF353 | | | Units |
|--------------------------|------------------------------------|---|----------|------------|----------|--------------------------------|
| | | | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_S = 10\text{k}\Omega$, $T_A = 25^{\circ}\text{C}$ Over Temperature | | 5 | 10 13 | mV mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\text{k}\Omega$ | | 10 | | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{OS} | Input Offset Current | $T_J = 25^{\circ}\text{C}$, (Notes 4, 5) $T_J \leq 70^{\circ}\text{C}$ | | 25 | 100 4 | pA nA |
| I_B | Input Bias Current | $T_J = 25^{\circ}\text{C}$, (Notes 4, 5) $T_J \leq 70^{\circ}\text{C}$ | | 50 | 200 8 | pA nA |
| R_{IN} | Input Resistance | $T_J = 25^{\circ}\text{C}$ | | 10^{12} | | Ω |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{k}\Omega$ Over Temperature | 25 15 | 100 | | V/mV V/mV |
| V_O | Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{k}\Omega$ | ± 12 | ± 13.5 | | V |
| V_{CM} | Input Common-Mode Voltage Range | $V_S = \pm 15\text{V}$ | ± 11 | +15 -12 | | V V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\text{k}\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 70 | 100 | | dB |
| I_S | Supply Current | | | 3.6 | 6.5 | mA |

AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF353 | | | Units |
|--------|---------------------------------|--|-------|------|-----|------------------------|
| | | | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25^{\circ}\text{C}$, $f = 1\text{ Hz} - 20\text{ kHz}$ (Input Referred) | | -120 | | dB |
| SR | Slew Rate | $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$ | 8.0 | 13 | | V/ μs |
| GBW | Gain Bandwidth Product | $V_S = \pm 15\text{V}$, $T_A = 25^{\circ}\text{C}$ | 2.7 | 4 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^{\circ}\text{C}$, $R_S = 100\Omega$, $f = 1000\text{ Hz}$ | | 16 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $T_J = 25^{\circ}\text{C}$, $f = 1000\text{ Hz}$ | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: For operating at elevated temperatures, the device must be derated based on a thermal resistance of $115^{\circ}\text{C}/\text{W}$ typ junction to ambient for the N package, and $158^{\circ}\text{C}/\text{W}$ typ junction to ambient for the H package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

Note 4: These specifications apply for $V_S = \pm 15\text{V}$ and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$. V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0$.

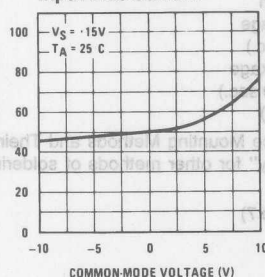
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6\text{V}$ to $\pm 15\text{V}$.

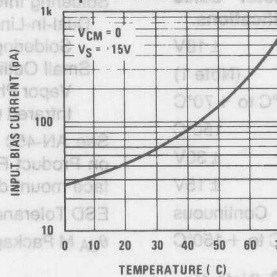
Note 7: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Typical Performance Characteristics

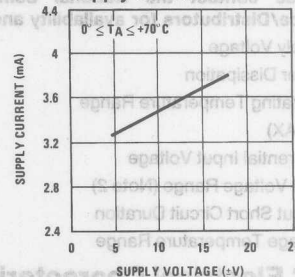
Input Bias Current



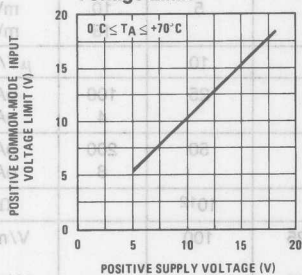
Input Bias Current



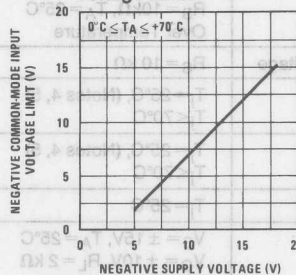
Supply Current



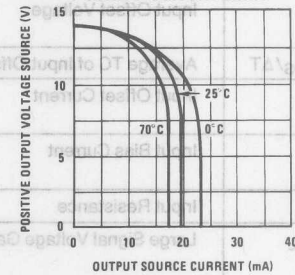
Positive Common-Mode Input Voltage Limit



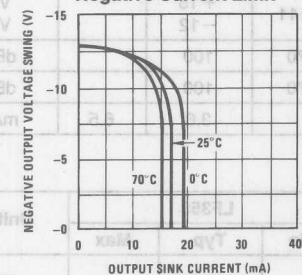
Negative Common-Mode Input Voltage Limit



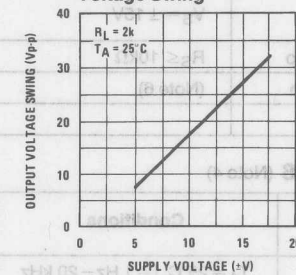
Positive Current Limit



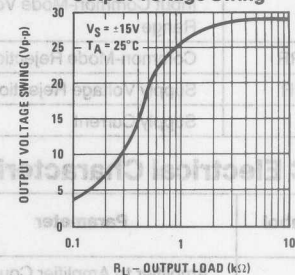
Negative Current Limit



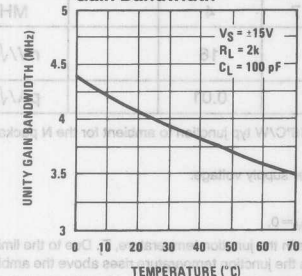
Voltage Swing



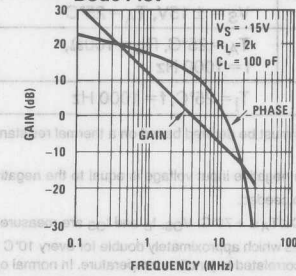
Output Voltage Swing



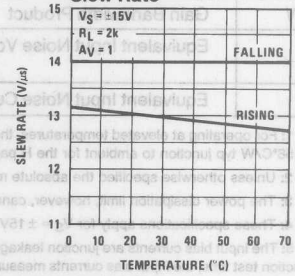
Gain Bandwidth



Bode Plot

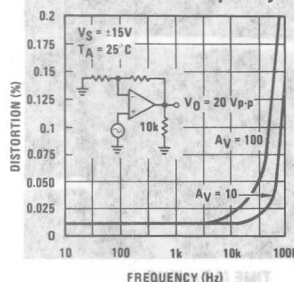


Slew Rate

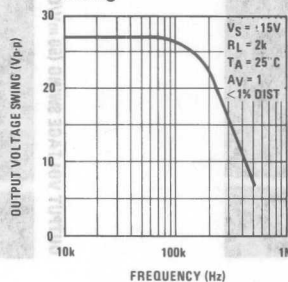


Typical Performance Characteristics (Continued)

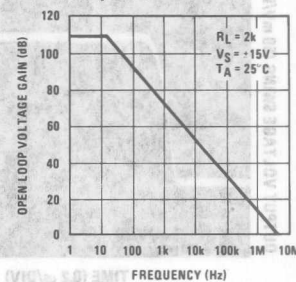
Distortion vs Frequency



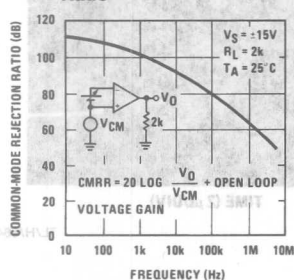
Undistorted Output Voltage Swing



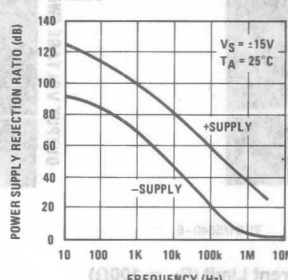
Open Loop Frequency Response



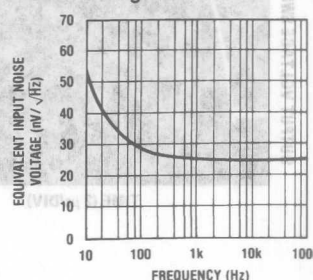
Common-Mode Rejection Ratio



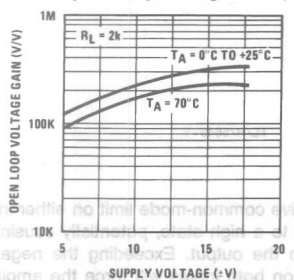
Power Supply Rejection Ratio



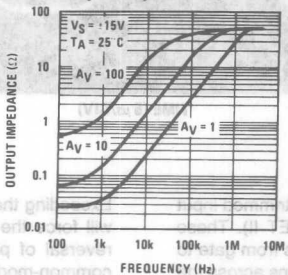
Equivalent Input Noise Voltage



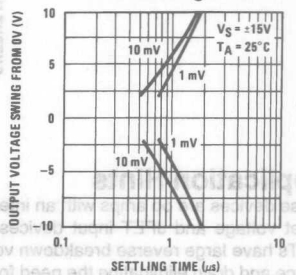
Open Loop Voltage Gain (V/V)



Output Impedance



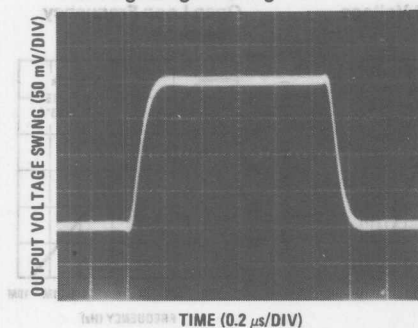
Inverter Settling Time



TL/H/5649-3

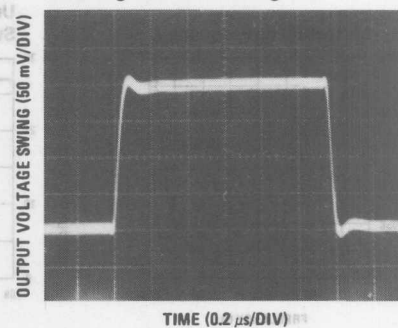
Pulse Response

Small Signaling Inverting



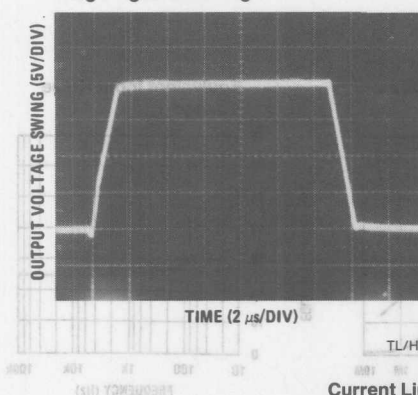
TL/H/5649-4

Small Signal Non-Inverting



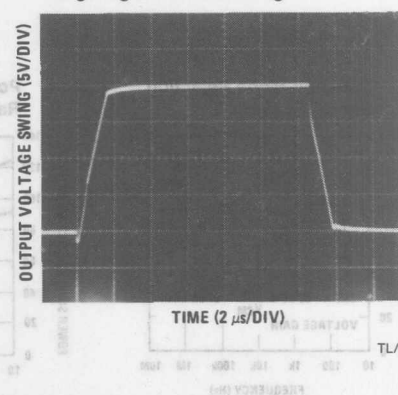
TL/H/5649-5

Large Signal Inverting



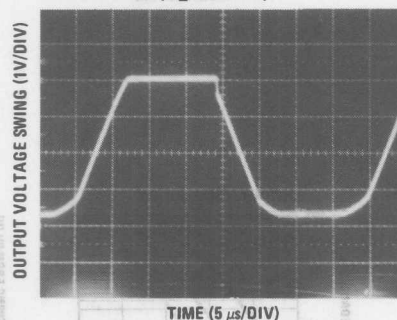
TL/H/5649-6

Large Signal Non-Inverting

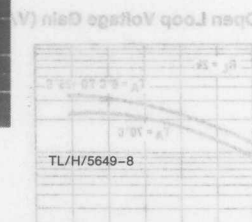


TL/H/5649-7

Current Limit ($R_L = 100\Omega$)



TIME (5 μs/DIV)



TL/H/5649-8

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 6V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a 2 k Ω load resistance to $\pm 10V$ over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

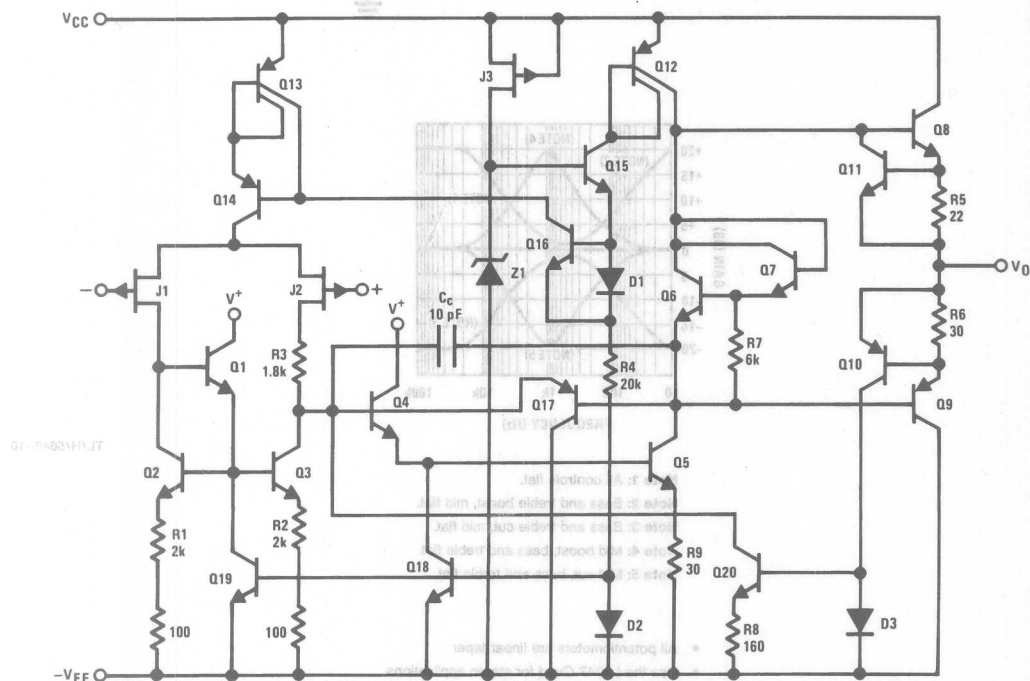
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards

in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic

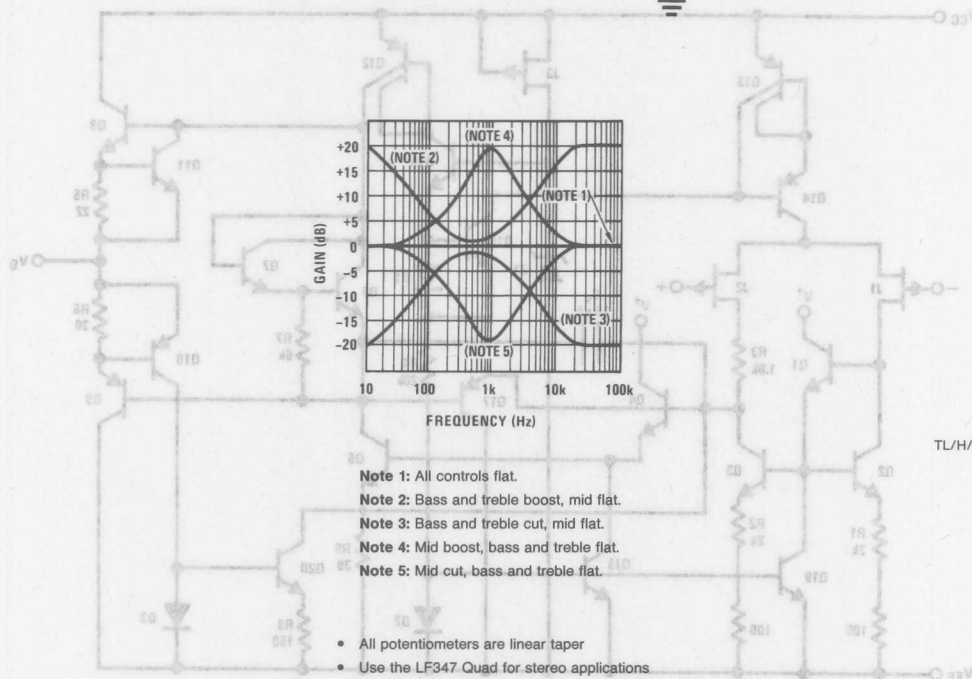
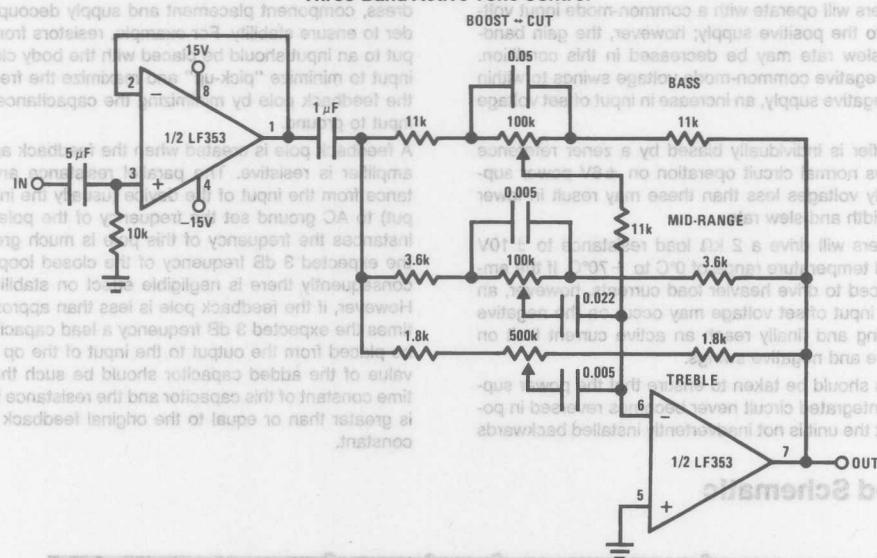


TL/H/5649-9

Typical Applications

However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be added from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance in parallel with the feedback pole is greater than or equal to the original feedback pole time constant.

Three-Band Active Tone Control

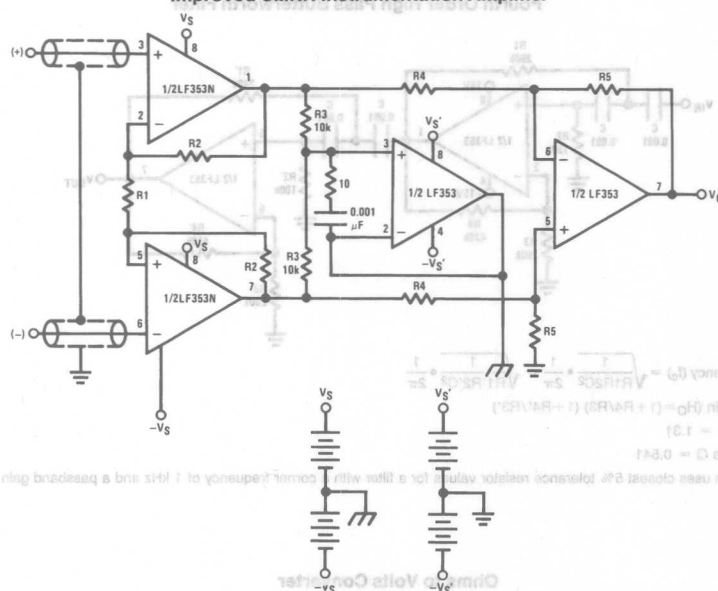


- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

The diagram shows a two-stage amplifier. The first stage is a voltage divider with a 500k resistor and a 100k resistor, with a 0.022 capacitor in parallel with the 100k resistor. The output of this stage is connected to a 0.005 capacitor, which is in series with a 11k resistor. The second stage is a common-emitter amplifier with a 3.6k collector resistor and an 1.8k emitter resistor. The circuit is powered by a 10V supply.

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



$$A_V = \left(\frac{2R_2}{R_1} + 1 \right) \frac{R_5}{R_4}$$

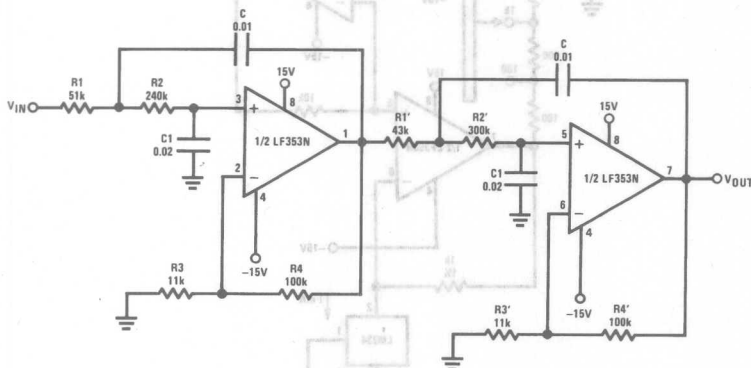
--- and --- are separate isolated grounds

Matching of R2's, R4's and R5's control CMRR

With $A_{VT} = 1400$, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

Fourth Order Low Pass Butterworth Filter

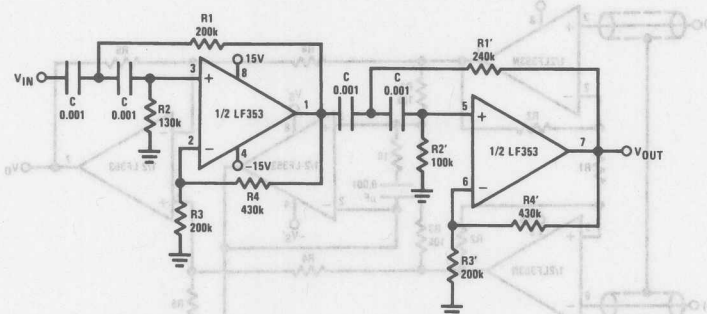


$$\text{Corner frequency } (f_c) = \frac{1}{\sqrt{R_1 R_2 C C_1}} \cdot \frac{1}{2\pi} = \frac{1}{\sqrt{R_1' R_2' C C_1}} \cdot \frac{1}{2\pi}$$

- Passband gain (H_0) = $(1 + R_4/R_3) (1 + R_4'/R_3')$
- First stage Q = 1.31
- Second stage Q = 0.541
- Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100
- Offset nulling necessary for accurate DC performance

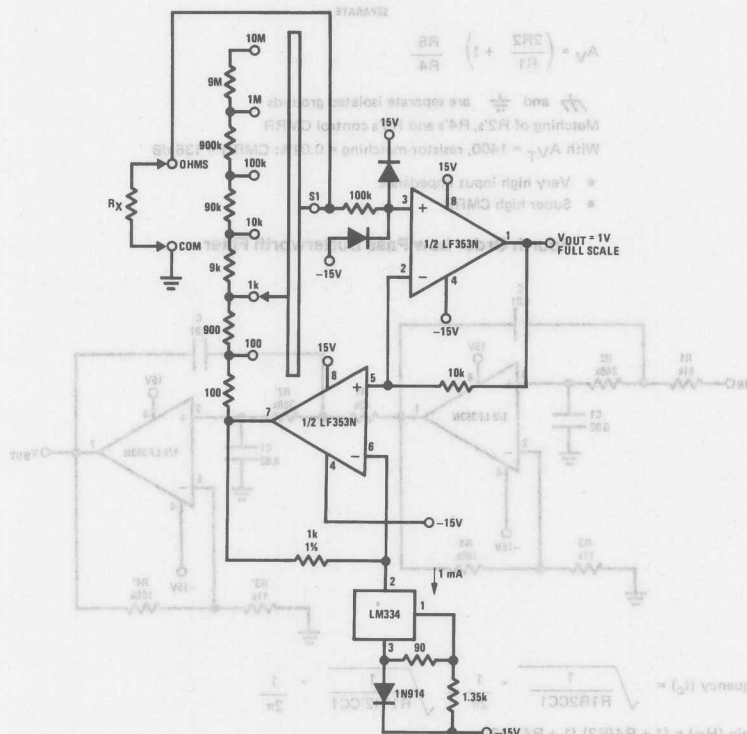
Typical Applications (Continued)

Fourth Order High Pass Butterworth Filter



- Corner frequency (f_c) = $\frac{1}{\sqrt{R_1 R_2 C^2}} \cdot \frac{1}{2\pi} = \frac{1}{\sqrt{R_1' R_2' C^2}} \cdot \frac{1}{2\pi}$
- Passband gain ($H_0 = (1 + R_4/R_3) (1 + R_4'/R_3')$)
- First stage $Q = 1.31$
- Second stage $Q = 0.541$
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10.

Ohms to Volts Converter



$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the LF353.

TL/H/5649-13

LF411 Low Offset, Low Drift JFET Input Operational Amplifier

General Description

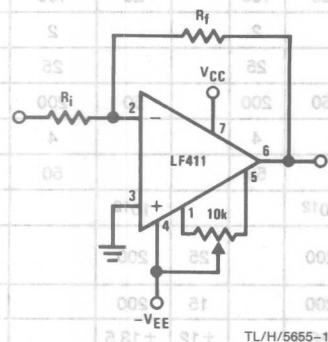
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage 0.5 mV(max)
- Input offset voltage drift $10 \mu\text{V}/^\circ\text{C}(\text{max})$
- Low input bias current 50 pA
- Low input noise current 0.01 pA/√Hz
- Wide gain bandwidth 3 MHz(min)
- High slew rate $10\text{V}/\mu\text{s}(\text{min})$
- Low supply current 1.8 mA
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V=10$, $R_L=10\text{k}$, $V_O=20\text{Vp-p}$, $\text{BW}=20\text{Hz}-20\text{kHz}$ <0.02%
- Low 1/f noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection



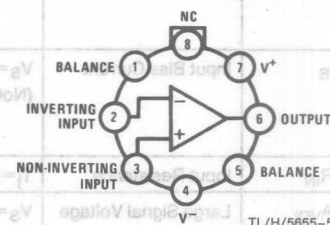
Ordering Information

LF411XYZ

- X indicates electrical grade
- Y indicates temperature range
- "M" for military
- "C" for commercial
- Z indicates package type
- "H" or "N"

Connection Diagrams

Metal Can Package



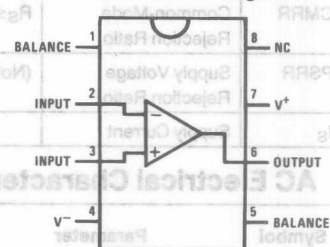
Top View

Note: Pin 4 connected to case.

Order Number LF411ACH
or LF411MH/883*

See NS Package Number H08A

Dual-In-Line Package

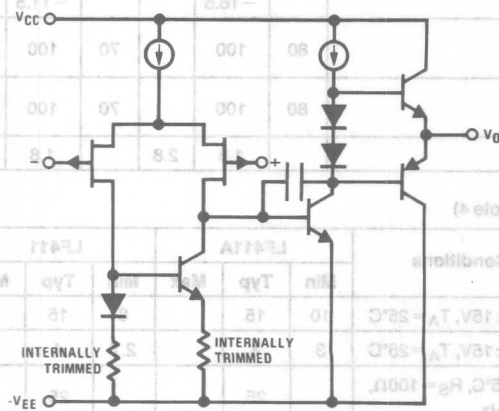


Top View

Order Number LF411ACN,
LF411CN or LF411MJ/883*

See NS Package Number
N08E or J08A

Simplified Schematic



please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 8)

| | LF411A | LF411 |
|-------------------------------|------------|------------|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous |

| | | |
|-----------------------------------|------------------------------|--------------------------|
| Power Dissipation (Notes 2 and 9) | 670 mW | 670 mW |
| T_{jmax} | 150°C | 115°C |
| θ_{JA} | 162°C/W (Still Air) | 120°C/W |
| | 65°C/W (400 LF/min Air Flow) | |
| θ_{JC} | 20°C/W | |
| Operating Temp. Range (Note 3) | | (Note 3) |
| Storage Temp. Range | –65°C ≤ T_A ≤ 150°C | –65°C ≤ T_A ≤ 150°C |
| Lead Temp. (Soldering, 10 sec.) | 260°C | 260°C |
| ESD Tolerance | | Rating to be determined. |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF411A | | | LF411 | | | Units |
|----------------------|------------------------------------|---|------------------------|------------------|-----|------------------|-------|----------------|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S = 10 kΩ, T _A = 25°C | | 0.3 | 0.5 | | 0.8 | 2.0 | mV |
| ΔV _{OS} /ΔT | Average TC of Input Offset Voltage | R _S = 10 kΩ (Note 5) | | 7 | 10 | | 7 | 20 (Note 5) | μV/°C |
| I _{OS} | Input Offset Current | V _S = ±15V (Notes 4, 6) | T _J = 25°C | 25 | 100 | | 25 | 100 | pA |
| | | | T _J = 70°C | | 2 | | 2 | | nA |
| | | | T _J = 125°C | | 25 | | 25 | | nA |
| I _B | Input Bias Current | V _S = ±15V (Notes 4, 6) | T _J = 25°C | 50 | 200 | | 50 | 200 | pA |
| | | | T _J = 70°C | | 4 | | 4 | | nA |
| | | | T _J = 125°C | | 50 | | 50 | | nA |
| R _{IN} | Input Resistance | T _J = 25°C | | 10 ¹² | | 10 ¹² | | Ω | |
| A _{VOL} | Large Signal Voltage Gain | V _S = ±15V, V _O = ±10V, R _L = 2k, T _A = 25°C | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | 25 | 200 | | 15 | 200 | | V/mV |
| V _O | Output Voltage Swing | V _S = ±15V, R _L = 10k | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| V _{CM} | Input Common-Mode Voltage Range | | ±16 | +19.5 | | ±11 | +14.5 | | V |
| | | | | −16.5 | | | −11.5 | | V |
| CMRR | Common-Mode Rejection Ratio | R _S ≤ 10k | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | 80 | 100 | | 70 | 100 | | dB |
| I _S | Supply Current | | | 1.8 | 2.8 | | 1.8 | 3.4 | mA |

AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF411A | | | LF411 | | | Units |
|--------|--------------------------------|---|--------|------|-----|-------|------|-----|------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| SR | Slew Rate | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 10 | 15 | | 8 | 15 | | V/ μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 3 | 4 | | 2.7 | 4 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ\text{C}$, $R_S = 100\Omega$, $f = 1\text{ kHz}$ | | 25 | | | 25 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $T_A = 25^\circ\text{C}$, $f = 1\text{ kHz}$ | | 0.01 | | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} .

Note 3: These devices are available in both the commercial temperature range $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and the military temperature range $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20\text{V}$ for the LF411A and for $V_S = \pm 15\text{V}$ for the LF411. V_{OS} , I_B , and I_{OS} are measured at $V_{CM} = 0$.

Note 5: The LF411A is 100% tested to this specification. The LF411 is sample tested to insure at least 90% of the units meet this specification.

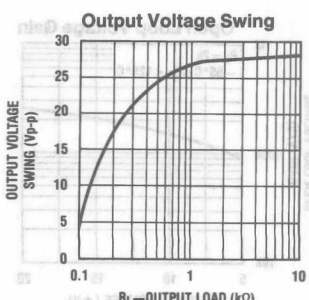
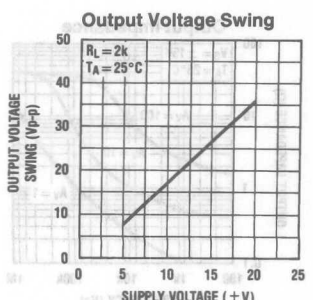
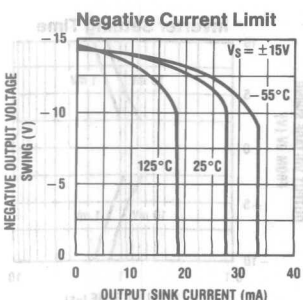
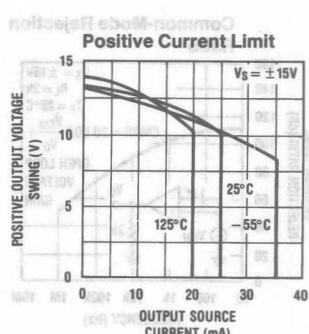
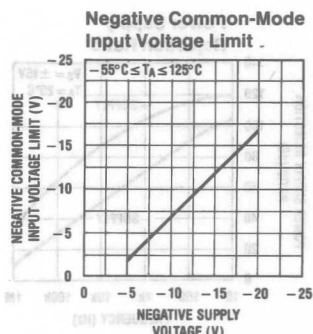
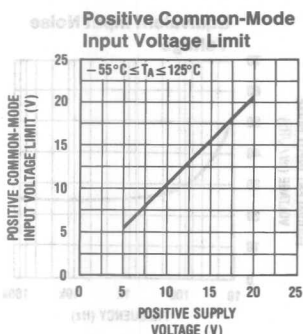
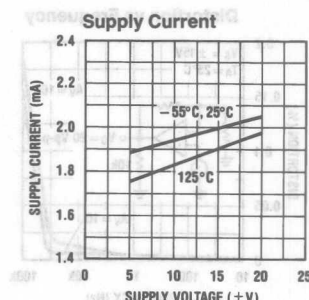
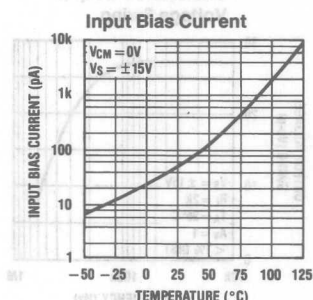
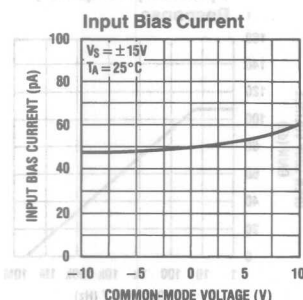
Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from $\pm 15\text{V}$ to $\pm 5\text{V}$ for the LF411 and from $\pm 20\text{V}$ to $\pm 5\text{V}$ for the LF411A.

Note 8: RETS 411X for LF411MH and LF411MJ military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

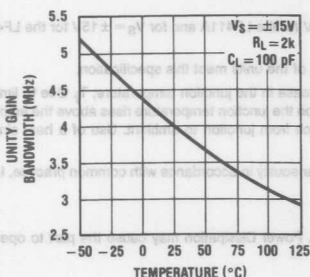
Typical Performance Characteristics



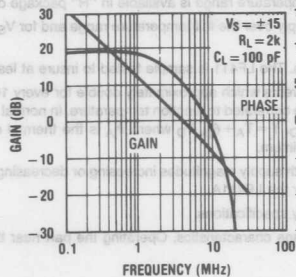
TL/H/5655-2

Typical Performance Characteristics (Continued)

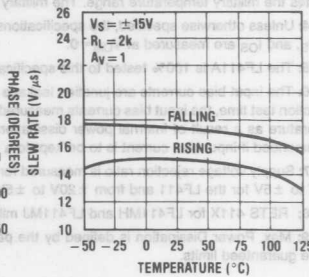
Gain Bandwidth



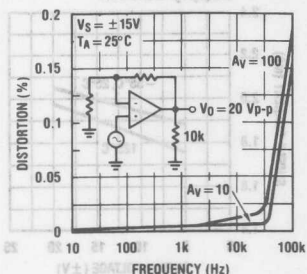
Gain Plot



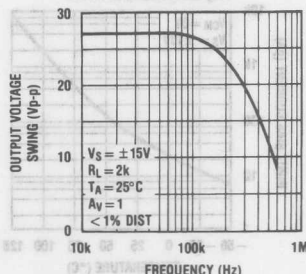
Slew Rate



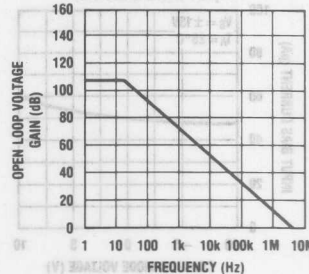
Distortion vs Frequency



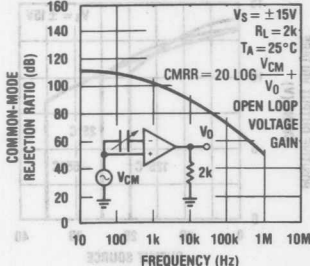
Undistorted Output Voltage Swing



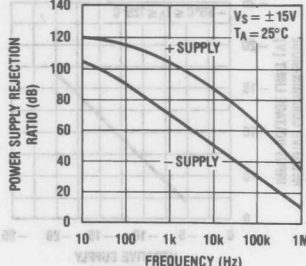
Open Loop Frequency Response



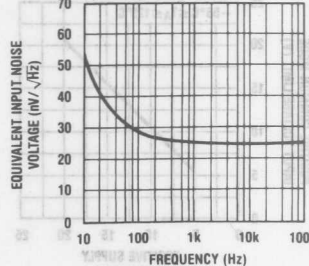
Common-Mode Rejection Ratio



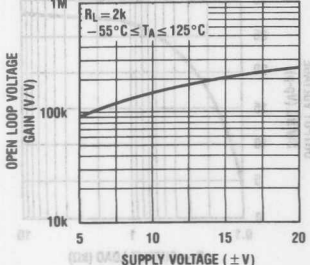
Power Supply Rejection Ratio



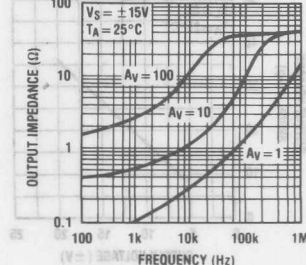
Equivalent Input Noise Voltage



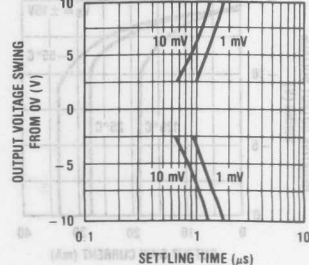
Open Loop Voltage Gain



Output Impedance



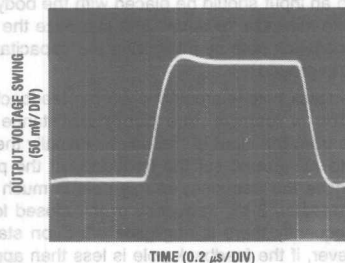
Inverter Settling Time



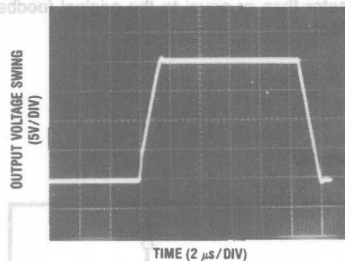
Pulse Response $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stable operation. The LF411 is a unity-gain buffer and its output impedance is very low. This means that the output voltage will be close to the input voltage. The frequency of the output signal will be the same as the input signal. The LF411 will operate with a common-mode input voltage equal to the positive supply, however, the gain bandwidth and slew rate may be affected. When the negative input is driven to the negative supply, the output will follow the input. The LF411 is a precision op amp and its output voltage will be close to the input voltage. The LF411 will operate with a common-mode input voltage equal to the positive supply, however, the gain bandwidth and slew rate may be affected. When the negative input is driven to the negative supply, the output will follow the input. The LF411 is a precision op amp and its output voltage will be close to the input voltage.

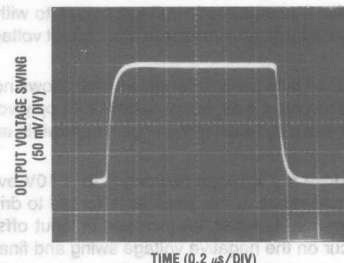
Small Signal Inverting



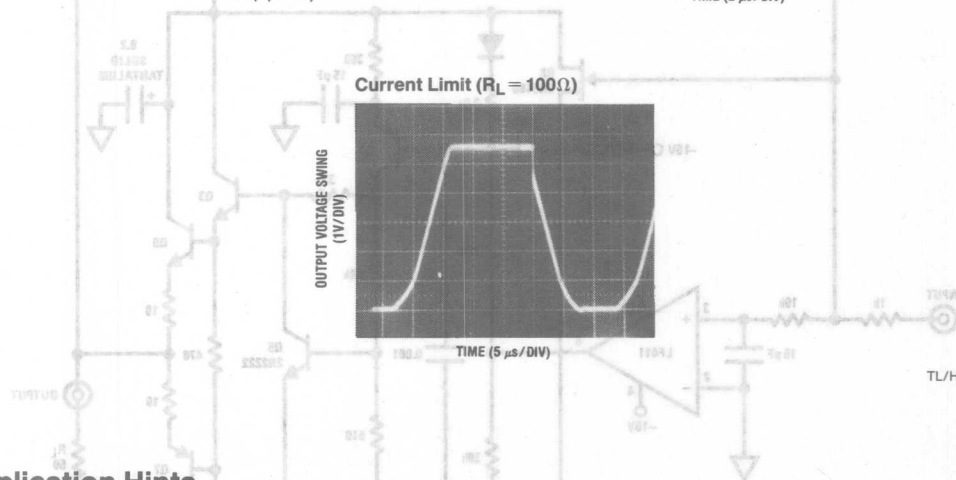
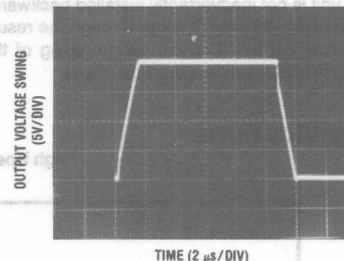
Large Signal Inverting



Small Signal Non-Inverting



Large Signal Non-Inverting



Application Hints

The LF411 series of internally trimmed JFET input op amps (BI-FET IITM) provide very low input offset voltage and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply, however, the gain bandwidth and slew rate may be affected. When the negative input is driven to the negative supply, the output will follow the input. The LF411 is a precision op amp and its output voltage will be close to the input voltage. The LF411 will operate with a common-mode input voltage equal to the positive supply, however, the gain bandwidth and slew rate may be affected. When the negative input is driven to the negative supply, the output will follow the input. The LF411 is a precision op amp and its output voltage will be close to the input voltage.

Precautions should be taken to ensure that the power supply for the integrated circuit is properly regulated. The LF411 is a precision op amp and its output voltage will be close to the input voltage. The LF411 will operate with a common-mode input voltage equal to the positive supply, however, the gain bandwidth and slew rate may be affected. When the negative input is driven to the negative supply, the output will follow the input. The LF411 is a precision op amp and its output voltage will be close to the input voltage.

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Application Hints (Continued)

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on $\pm 4.5\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 k Ω load resistance to $\pm 10V$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

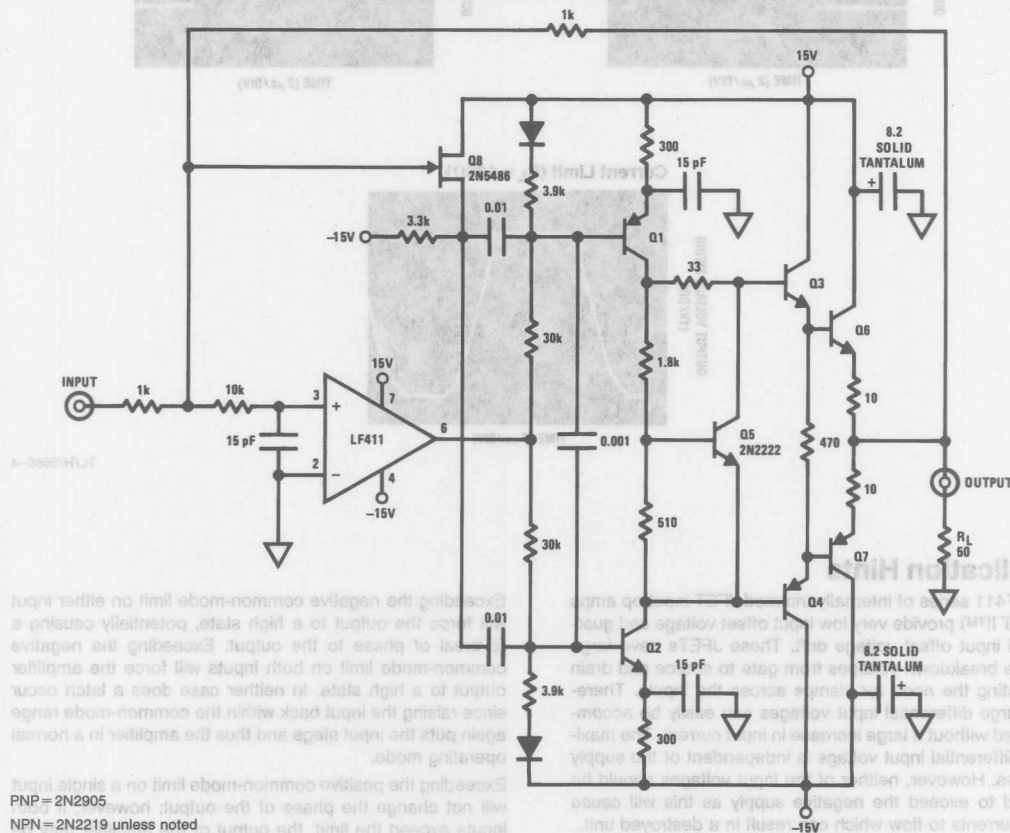
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

High Speed Current Booster

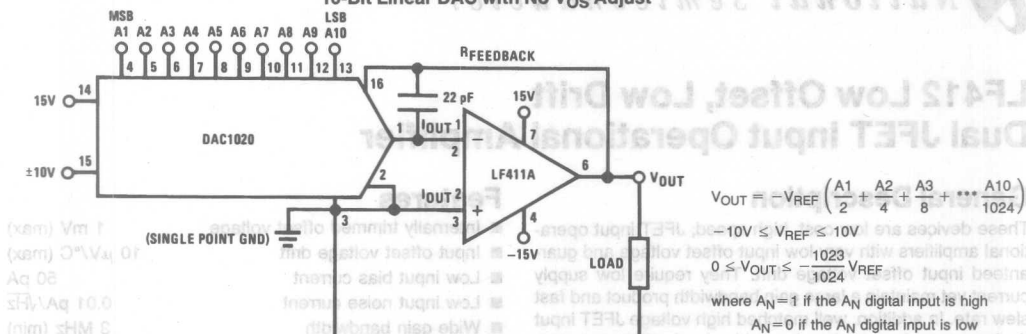


PNP=2N2905
NPN=2N2219 unless noted
TO-5 heat sinks for Q6-Q7

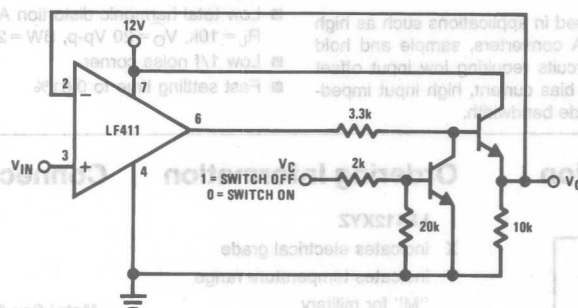
TL/H/5655-9

Typical Applications (Continued)

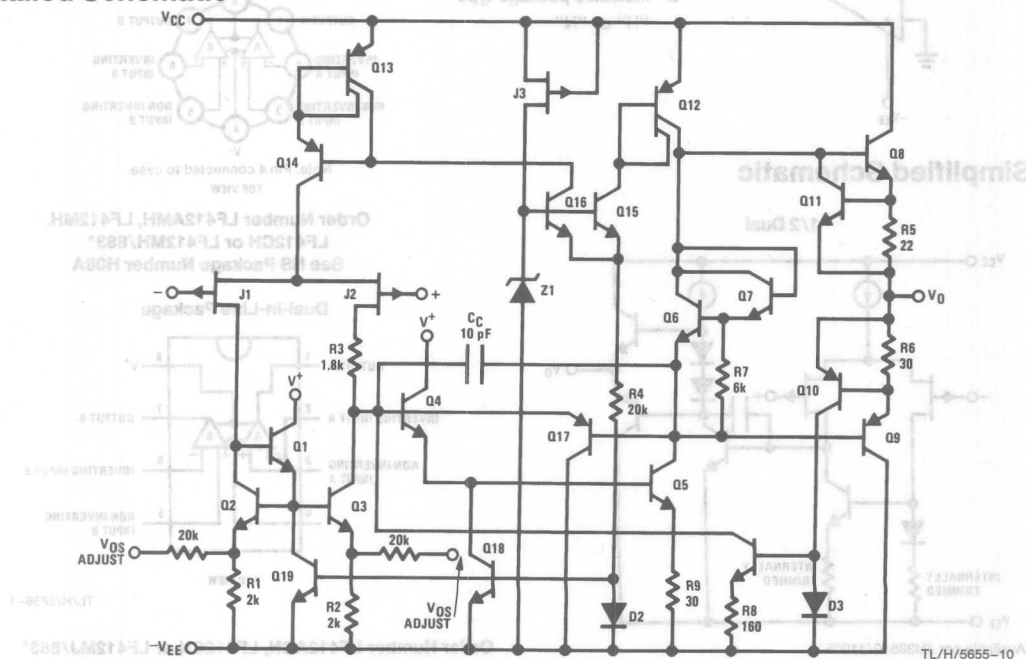
10-Bit Linear DAC with No V_{OS} Adjust



Single Supply Analog Switch with Buffered Output



Detailed Schematic



LF412 Low Offset, Low Drift Dual JFET Input Operational Amplifier

General Description

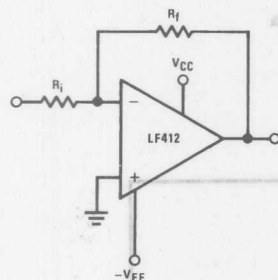
These devices are low cost, high speed, JFET input operational amplifiers with very low input offset voltage and guaranteed input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. LF412 dual is pin compatible with the LM1558, allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage 1 mV (max)
- Input offset voltage drift $10 \mu\text{V}/^\circ\text{C}$ (max)
- Low input bias current 50 pA
- Low input noise current $0.01 \text{ pA}/\sqrt{\text{Hz}}$
- Wide gain bandwidth 3 MHz (min)
- High slew rate $10\text{V}/\mu\text{s}$ (min)
- Low supply current 1.8 mA/Amplifier
- High input impedance $10^{12}\Omega$
- Low total harmonic distortion $A_V = 10$, $R_L = 10\text{k}$, $V_O = 20 \text{ Vp-p}$, $\text{BW} = 20 \text{ Hz-20 kHz}$ $\leq 0.02\%$
- Low $1/f$ noise corner 50 Hz
- Fast settling time to 0.01% 2 μs

Typical Connection



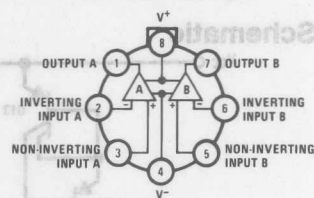
Ordering Information

LF412XYZ

- X indicates electrical grade
- Y indicates temperature range
- "M" for military
- "C" for commercial
- Z indicates package type
- "H" or "N"

Connection Diagrams

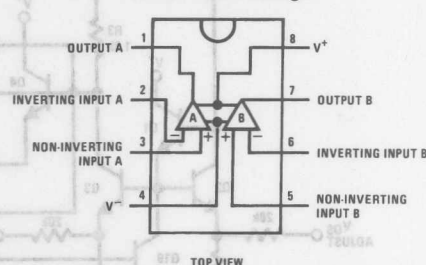
Metal Can Package



Note: Pin 4 connected to case.
TOP VIEW

Order Number LF412AMH, LF412MH,
LF412CH or LF412MH/883*
See NS Package Number H08A

Dual-In-Line Package

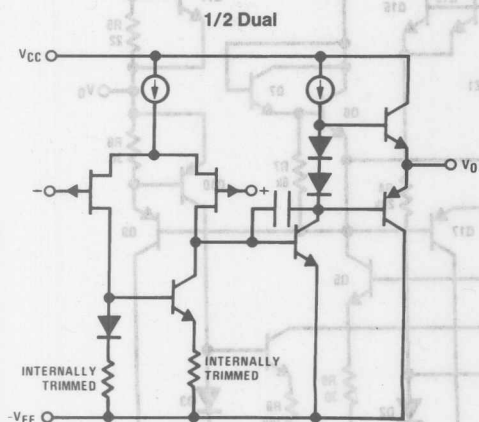


TOP VIEW

TL/H/5656-1

Order Number LF412ACN, LF412CN or LF412MJ/883*
See NS Package Number J08A or N08E

Simplified Schematic



*Available per JM38510/11905

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 9)

| | LF412A | LF412 | H Package | N Package |
|----------------------------|------------|------------|-------------------------|-----------------------|
| Supply Voltage | ±22V | ±18V | (Note 3) | 670 mW |
| Differential Input Voltage | ±38V | ±30V | T_j max | 150°C |
| Input voltage Range | ±19V | ±15V | θ_{JA} (Typical) | 152°C/W |
| (Note 1) | | | Operating Temp. Range | (Note 4) |
| Output Short Circuit | | | Storage Temp. | −65°C ≤ T_A ≤ 150°C |
| Duration (Note 2) | Continuous | Continuous | Lead Temp. | (Note 4) |
| | | | (Soldering, 10 sec.) | 260°C |
| | | | ESD Tolerance (Note 11) | 1700V |

DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF412A | | | LF412 | | | Units |
|--------------------------|------------------------------------|--|--------|------------------|-----|-------|------------------|-----|------------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_S = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | | 0.5 | 1.0 | | 1.0 | 3.0 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\text{ k}\Omega$ (Note 6) | | 7 | 10 | | 7 | 20 | $\mu\text{V}/^\circ\text{C}$ |
| I_{OS} | Input Offset Current | $V_S = \pm 15\text{V}$ (Notes 5 and 7) | | 25 | 100 | | 25 | 100 | pA |
| | | $T_j = 25^\circ\text{C}$ | | | | | | | |
| | | $T_j = 70^\circ\text{C}$ | | | 2 | | | 2 | nA |
| I_B | Input Bias Current | $V_S = \pm 15\text{V}$ (Notes 5 and 7) | | 50 | 200 | | 50 | 200 | pA |
| | | $T_j = 25^\circ\text{C}$ | | | | | | | |
| | | $T_j = 70^\circ\text{C}$ | | | 4 | | | 4 | nA |
| R_{IN} | Input Resistance | $T_j = 25^\circ\text{C}$ | | 10 ¹² | | | 10 ¹² | | Ω |
| | | | | | | | | | |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$, $R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | 25 | 200 | | 15 | 200 | | V/mV |
| V_O | Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{ k}\Omega$ | ±12 | ±13.5 | | ±12 | ±13.5 | | V |
| V_{CM} | Input Common-Mode Voltage Range | | ±16 | +19.5 | | ±11 | +14.5 | | V |
| | | | | −16.5 | | | −11.5 | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 80 | 100 | | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 8) | 80 | 100 | | 70 | 100 | | dB |
| I_S | Supply Current | $V_O = 0\text{V}$, $R_L = \infty$ | | 3.6 | 5.6 | | 3.6 | 6.5 | mA |

AC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF412A | | | LF412 | | | Units |
|--------|---------------------------------|--|--------|------|-----|-------|------|-----|------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25^\circ\text{C}$, $f = 1\text{ Hz}$ –20 kHz (Input Referred) | | −120 | | | −120 | | dB |
| SR | Slew Rate | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 10 | 15 | | 8 | 15 | | V/ μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 3 | 4 | | 2.7 | 4 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ\text{C}$, $R_S = 100\Omega$, $f = 1\text{ kHz}$ | | 25 | | | 25 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $T_A = 25^\circ\text{C}$, $f = 1\text{ kHz}$ | | 0.01 | | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} . These devices are available in both the commercial temperature range $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ and the military temperature range $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only. In all cases the maximum operating temperature is limited by internal junction temperature $T_{J \text{ max}}$.

Note 5: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20\text{V}$ for the LF412A and for $V_S = \pm 15\text{V}$ for the LF412. V_{OS} , I_B , and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The LF412A is 100% tested to this specification. The LF412 is sample tested on a per amplifier basis to insure at least 85% of the amplifiers meet this specification.

Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. $V_S = \pm 6\text{V}$ to $\pm 15\text{V}$.

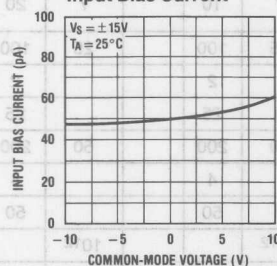
Note 9: Refer to RETS412X for LF412MH and LF412MJ military specifications.

Note 10: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

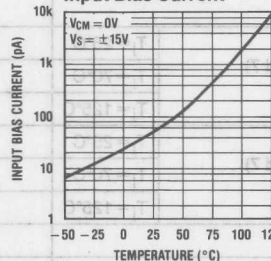
Note 11: Human body model, $1.5 \text{ k}\Omega$ in series with 100 pF .

Typical Performance Characteristics

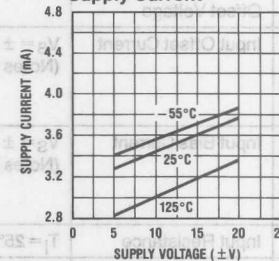
Input Bias Current



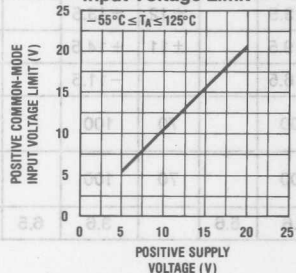
Input Bias Current



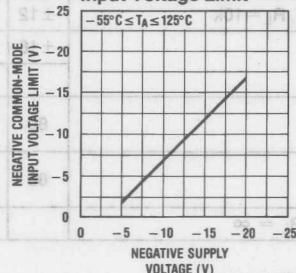
Supply Current



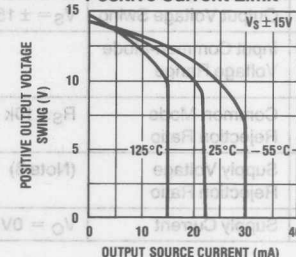
Positive Common-Mode Input Voltage Limit



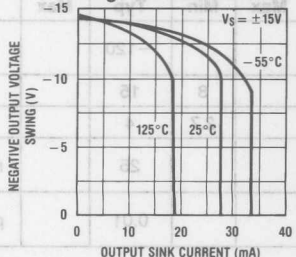
Negative Common-Mode Input Voltage Limit



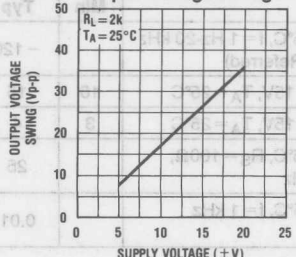
Positive Current Limit



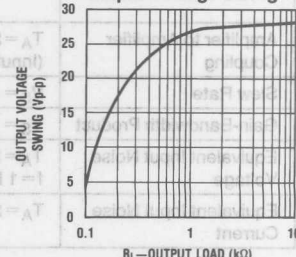
Negative Current Limit



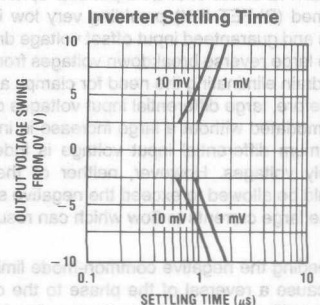
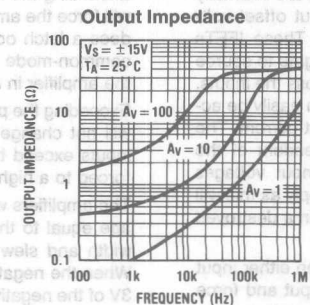
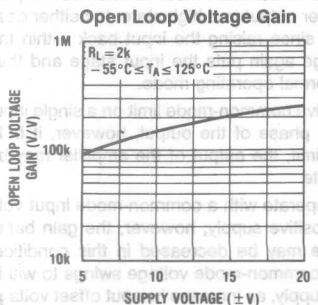
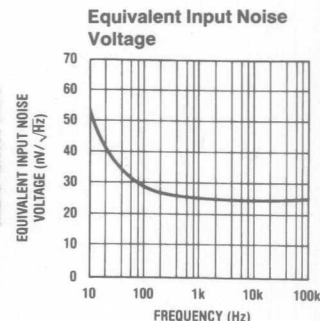
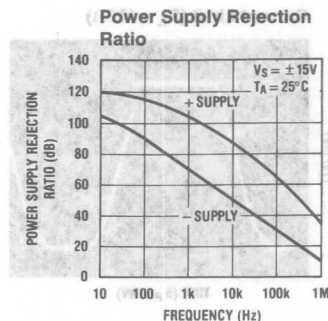
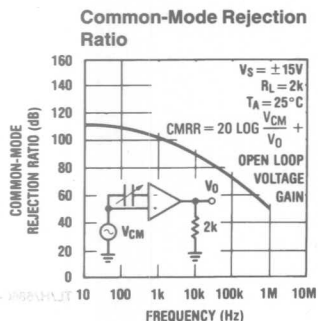
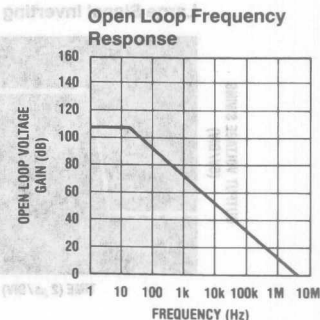
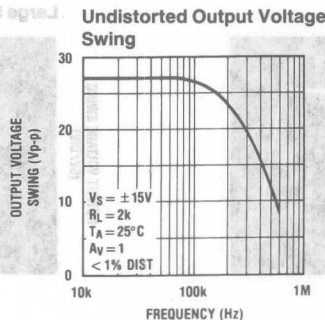
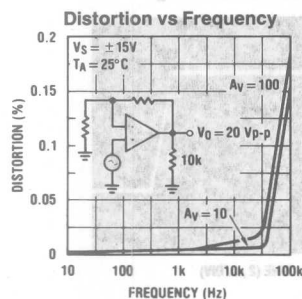
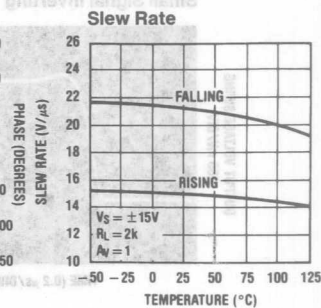
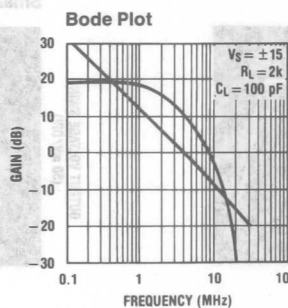
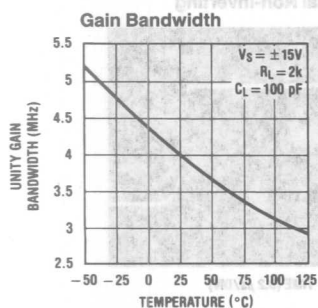
Output Voltage Swing



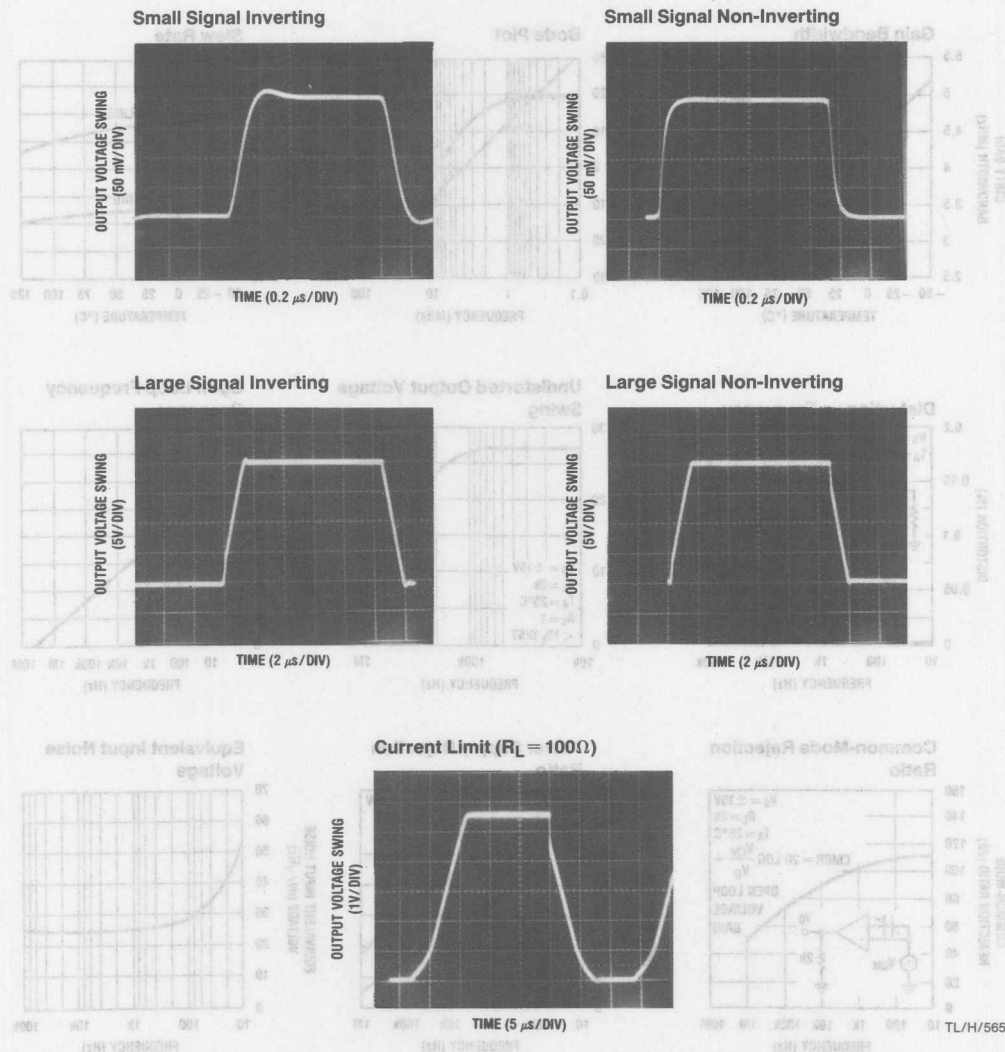
Output Voltage Swing



Typical Performance Characteristics (Continued)



Pulse Response $R_L = 2\text{ k}\Omega$, $C_L = 10\text{ pF}$



TL/H/5656-4

Application Hints

The LF412 series of JFET input dual op amps are internally trimmed (BI-FET IITM) providing very low input offset voltages and guaranteed input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output, however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Application Hints (Continued)

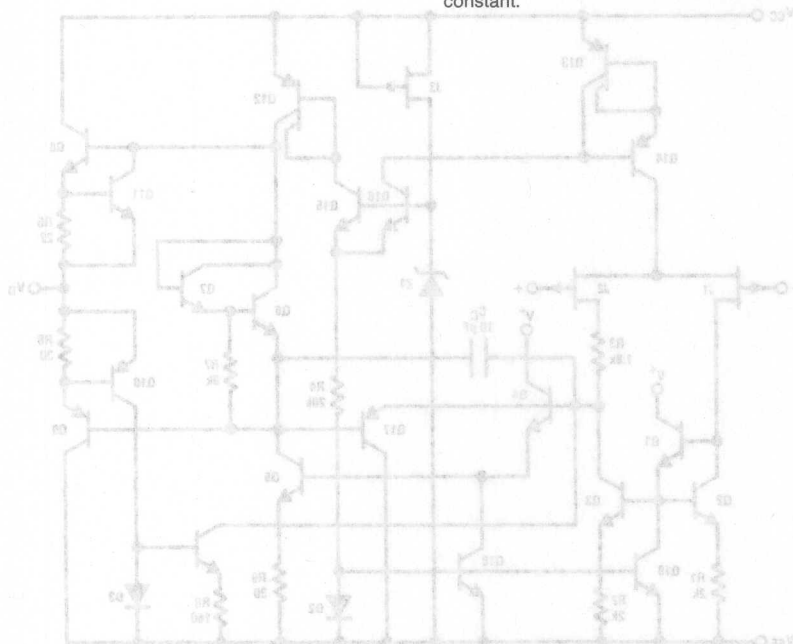
Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 6.0\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a $2\text{ k}\Omega$ load resistance to $\pm 10\text{V}$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

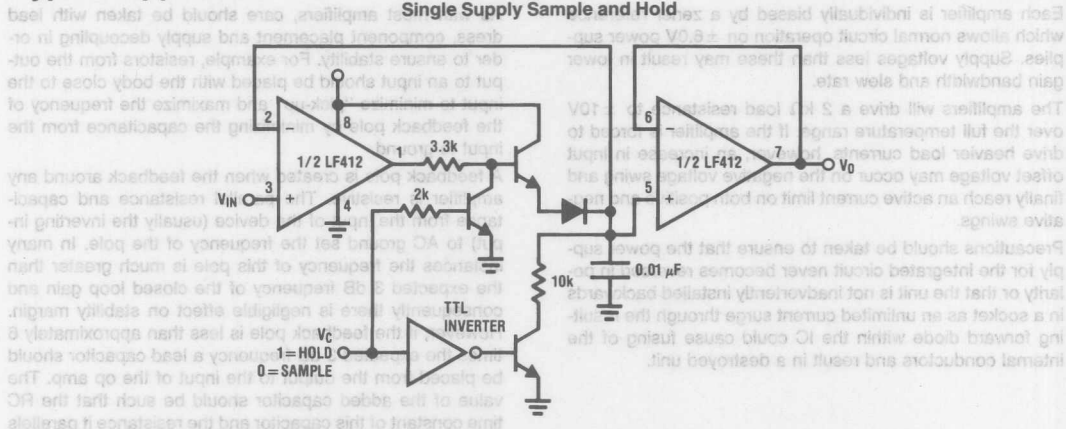
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.



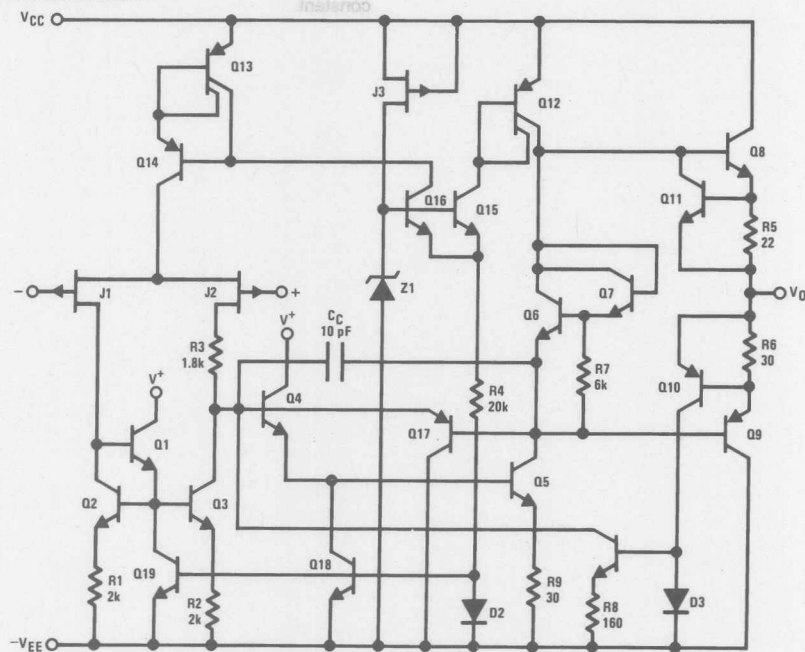
8-1 320141-1

Typical Application

Single Supply Sample and Hold



Detailed Schematic



TL/H/5656-9



LF441 Low Power JFET Input Operational Amplifier

General Description

The LF441 low power operational amplifier provides many of the same AC characteristics as the industry standard LM741 while greatly improving the DC characteristics of the LM741. The amplifier has the same bandwidth, slew rate, and gain (10 k Ω load) as the LM741 and only draws one tenth the supply current of the LM741. In addition, the well matched high voltage JFET input devices of the LF441 reduce the input bias and offset currents by a factor of 10,000 over the LM741. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF441 also has a very low equivalent input noise voltage for a low power amplifier.

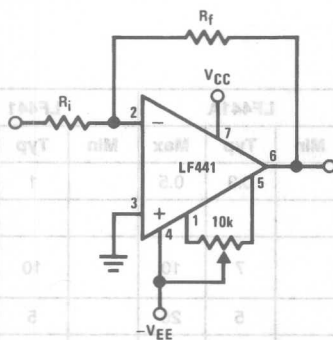
The LF441 is pin compatible with the LM741, allowing an immediate 10 times reduction in power drain in many applications. The LF441 should be used where low power

dissipation and good electrical characteristics are the major considerations.

Features

- 1/10 supply current of a LM741 200 μ A (max)
- Low input bias current 50 pA (max)
- Low input offset voltage 0.5 mV (max)
- Low input offset voltage drift 10 μ V/ $^{\circ}$ C (max)
- High gain bandwidth 1 MHz
- High slew rate 1 V/ μ s
- Low noise voltage for low power 35 nV/ $\sqrt{\text{Hz}}$
- Low input noise current 0.01 pA/ $\sqrt{\text{Hz}}$
- High input impedance $10^{12}\Omega$
- High gain $V_O = \pm 10V$, $R_L = 10k$ 50k (min)

Typical Connection

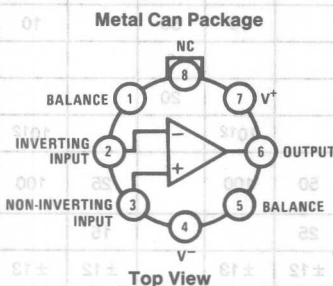


Ordering Information

LF441XYZ

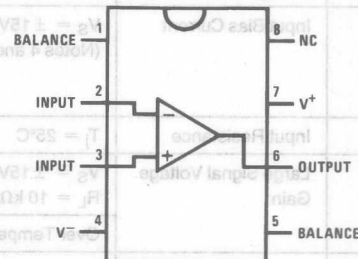
- X indicates electrical grade
- Y indicates temperature range
- "M" for military,
- "C" for commercial
- Z indicates package type
- "H" or "N"

Connection Diagrams



Note: Pin 4 connected to case.
Order Number LF441MH/883
See NS Package Number H08A

Dual-In-Line Package



Order Number LF441ACN,
LF441CM or LF441CN
See NS Package Number M08A or N08E

| | | | | | |
|----------------------------|---------------|--------------|----------------------|------------|------------|
| | LF441A | LF441 | (note 1) | $\pm 19V$ | $\pm 15V$ |
| Supply Voltage | $\pm 22V$ | $\pm 18V$ | Output Short Circuit | | |
| Differential Input Voltage | $\pm 38V$ | $\pm 30V$ | Duration | Continuous | Continuous |

| | | | |
|---|---|---|---|
| | H Package | N Package | M Package |
| Power Dissipation (Notes 2 and 9) | 670 mW | 670 mW | |
| T_j max | 150°C | 115°C | |
| θ_{JA} (Typical) | | 130°C/W | 185°C/W |
| Board Mount in still air | 165°C/W | | |
| Board Mount in 400 LF/ min air flow | 65°C/W | | |
| θ_{JC} | 25°C/W | | |
| Operating Temp. Range | (Note 3) | (Note 3) | |
| Storage Temp. Range | $-65^\circ C \leq T_A \leq 150^\circ C$ | $-65^\circ C \leq T_A \leq 150^\circ C$ | |
| Lead Temperature (Soldering, 10 seconds) | 300°C | 260°C | |
| Soldering Information | LF441A | LF441 | See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering sur- face mount devices. |
| Dual-In-Line Package | | | ESD Tolerance (Note 10) |
| Soldering (10 sec.) | 260°C | 260°C | Rating to be Determined |
| Small Outline Package | | | |
| Vapor Phase (60 sec.) | 215°C | 215°C | |
| Infrared (15 sec.) | 220°C | 220°C | |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF441A | | | LF441 | | | Units |
|--------------------------|---------------------------------------|---|----------|------------|-----|----------|------------|-----|------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_S = 10\text{ k}\Omega$, $T_A = 25^\circ C$ | | 0.3 | 0.5 | | 1 | 5 | mV |
| | | Over Temperature | | | | | | 7.5 | mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\text{ k}\Omega$ (Note 5) | | 7 | 10 | | 10 | | $\mu V/^\circ C$ |
| | | | | | | | | | |
| I_{OS} | Input Offset Current | $V_S = \pm 15V$ (Notes 4 and 6) | | | | | | | |
| | | $T_j = 25^\circ C$ | | 5 | 25 | | 5 | 50 | pA |
| | | $T_j = 70^\circ C$ | | | 1.5 | | | 1.5 | nA |
| I_B | Input Bias Current | $V_S = \pm 15V$ (Notes 4 and 6) | | | | | | | |
| | | $T_j = 25^\circ C$ | | 10 | 50 | | 10 | 100 | pA |
| | | $T_j = 70^\circ C$ | | | 3 | | | 3 | nA |
| R_{IN} | Input Resistance | $T_j = 25^\circ C$ | | 1012 | | | 1012 | | Ω |
| | | | | | | | | | |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15V$, $V_O = \pm 10V$, $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ C$ | 50 | 100 | | 25 | 100 | | V/mV |
| | | Over Temperature | 25 | | | 15 | | | V/mV |
| V_O | Output Voltage Swing | $V_S = \pm 15V$, $R_L = 10\text{ k}\Omega$ | ± 12 | ± 13 | | ± 12 | ± 13 | | V |
| V_{CM} | Input Common-Mode Voltage Range | | ± 16 | $+18, -17$ | | ± 11 | $+14, -12$ | | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 80 | 100 | | 70 | 95 | | dB |

DC Electrical Characteristics (Note 4) (Continued)

| Symbol | Parameter | Conditions | LF441A | | | LF441 | | | Units |
|----------------|--------------------------------|------------|--------|-----|-----|-------|-----|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | 80 | 100 | | 70 | 90 | | dB |
| I _S | Supply Current | | | 150 | 200 | | 150 | 250 | μA |

AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | LF441A | | | LF441 | | | Units |
|----------------|--------------------------------|---|--------|------|-----|-------|------|-----|--------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| SR | Slew Rate | V _S = ±15V, T _A = 25°C | 0.8 | 1 | | 0.6 | 1 | | V/μs |
| GBW | Gain-Bandwidth Product | V _S = ±15V, T _A = 25°C | 0.8 | 1 | | 0.6 | 1 | | MHz |
| e _n | Equivalent Input Noise Voltage | T _A = 25°C, R _S = 100Ω, f = 1 kHz | | 35 | | | 35 | | nV/√Hz |
| i _n | Equivalent Input Noise Current | T _A = 25°C, f = 1 kHz | | 0.01 | | | 0.01 | | pA/√Hz |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA}.

Note 3: The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 4: Unless otherwise specified the specifications apply over the full temperature range and for V_S = ±20V for the LF441A and for V_S = ±15V for the LF441. V_{OS}, I_B, and I_{OS} are measured at V_{CM} = 0.

Note 5: The LF441A is 100% tested to this specification.

Note 6: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. T_J = T_A + θ_{JA} P_D where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

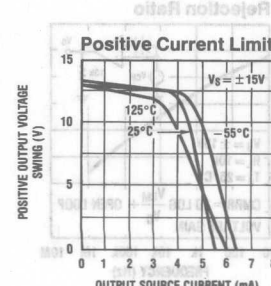
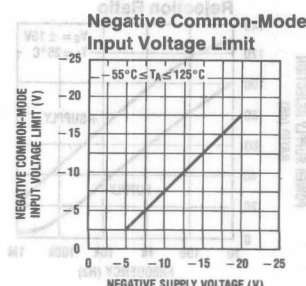
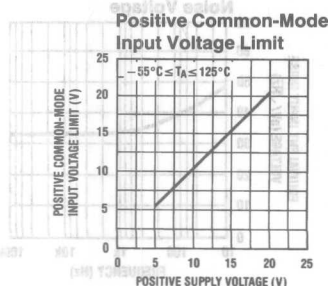
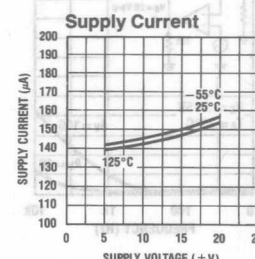
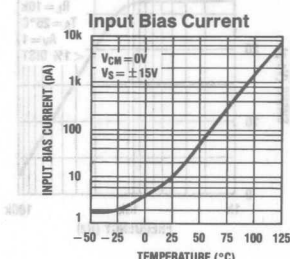
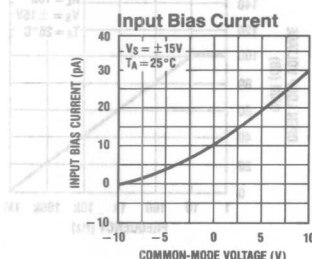
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice. From ±15V to ±5V for the LF441 and from ±20V to ±5V for the LF441A.

Note 8: Refer to RETS441X for LF441MH military specifications.

Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

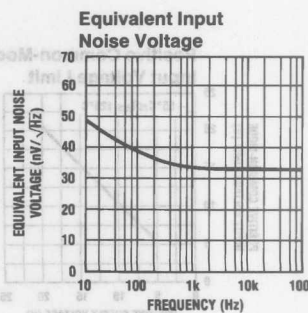
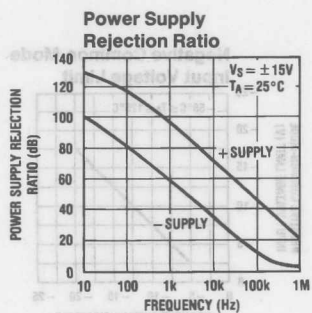
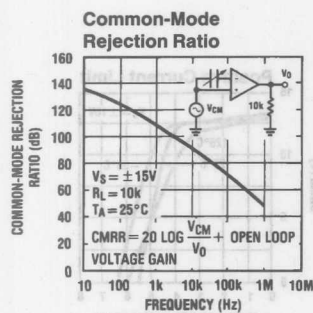
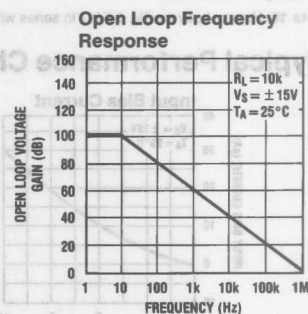
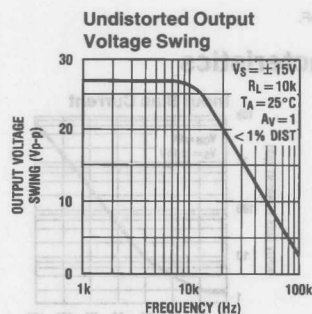
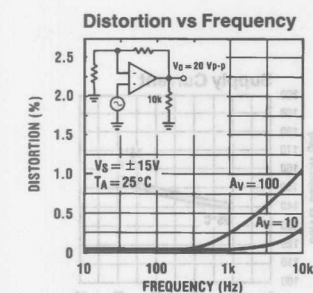
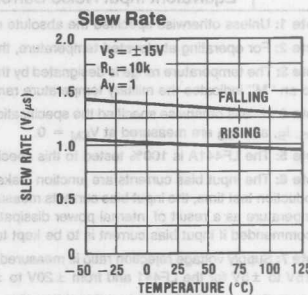
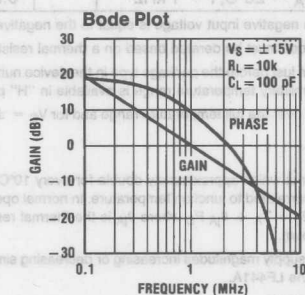
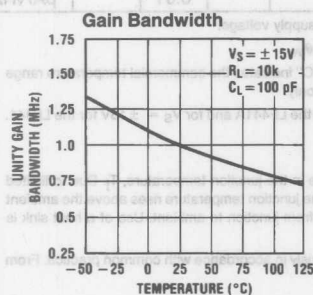
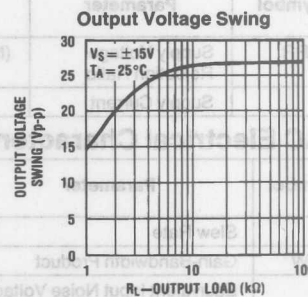
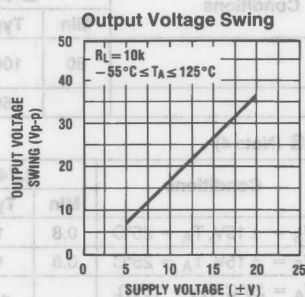
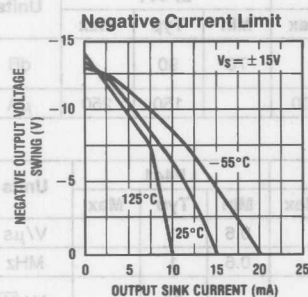
Note 10: Human body model, 1.5 kΩ in series with 100 pF.

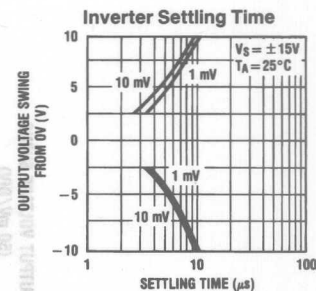
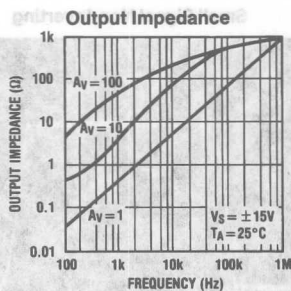
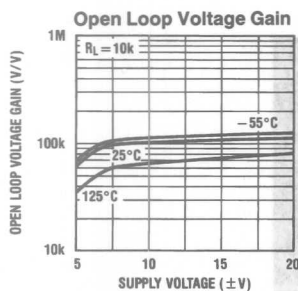
Typical Performance Characteristics



TL/H/9297-5

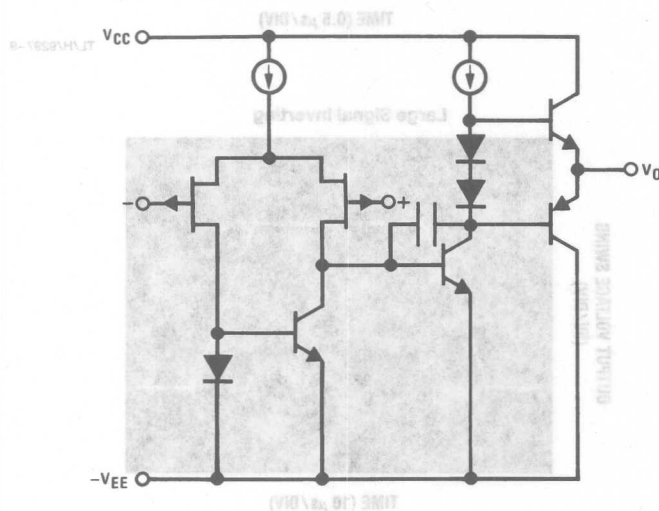
Typical Performance Characteristics (Continued)





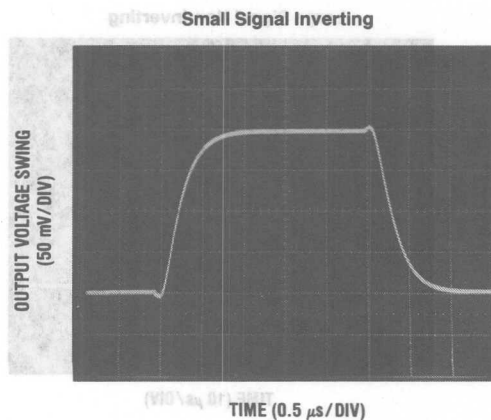
TL/H/9297-7

Simplified Schematic



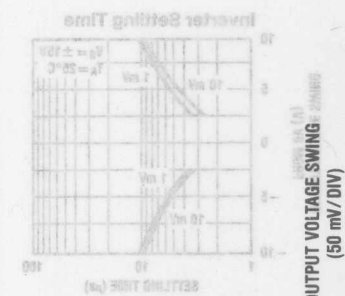
TL/H/9297-3

Pulse Response $R_L = 10 k\Omega$, $C_L = 10 pF$

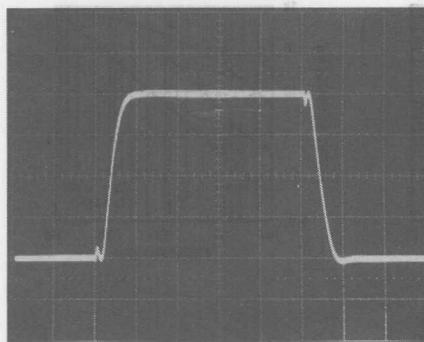


TL/H/9297-8

Pulse Response $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$ (Continued)

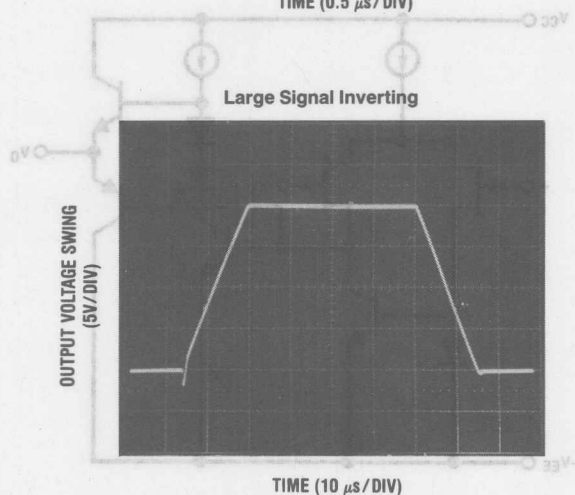


Small Signal Non-Inverting



TIME (0.5 μs /DIV)

TL/H/9297-9

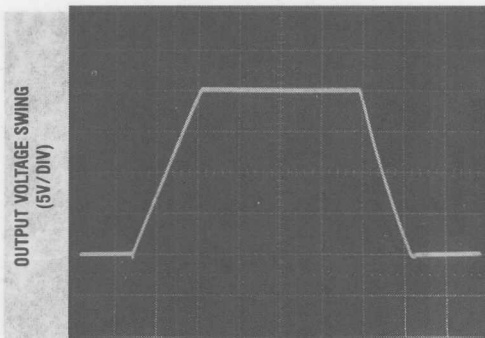


Large Signal Inverting

TIME (10 μs /DIV)

TL/H/9297-10

Large Signal Non-Inverting



TIME (10 μs /DIV)

TL/H/9297-11

Application Hints

This device is a low power op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain, eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The amplifier is biased to allow normal circuit operation with power supplies of $\pm 3V$. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

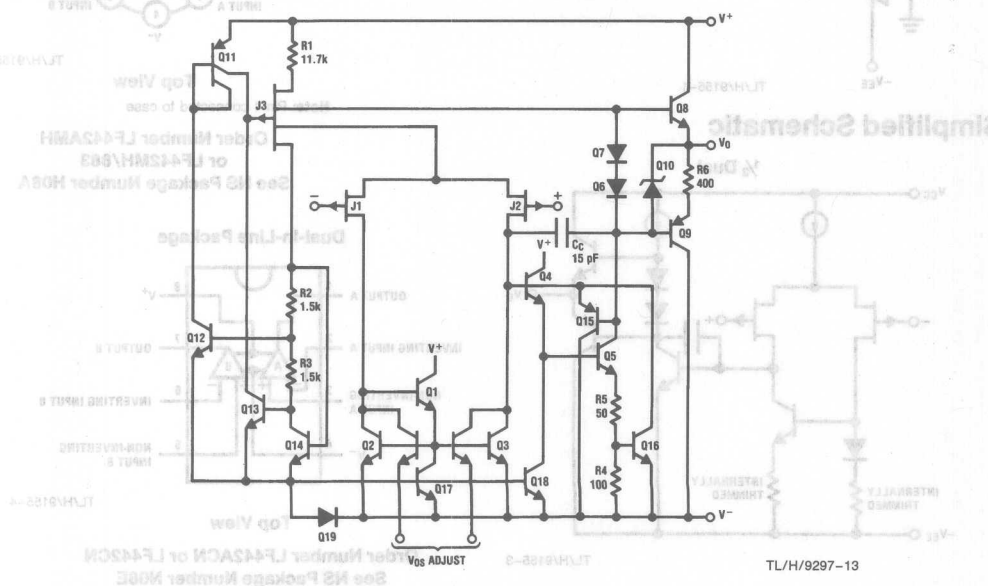
The amplifier will drive a $10\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket, as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input to AC ground) set the frequency of this pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency, of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic



TL/H/9297-13



LF442 Dual Low Power JFET Input Operational Amplifier

General Description

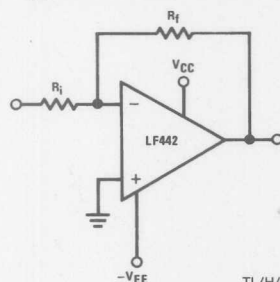
The LF442 dual low power operational amplifiers provide many of the same AC characteristics as the industry standard LM1458 while greatly improving the DC characteristics of the LM1458. The amplifiers have the same bandwidth, slew rate, and gain (10 kΩ load) as the LM1458 and only draw one tenth the supply current of the LM1458. In addition the well matched high voltage JFET input devices of the LF442 reduce the input bias and offset currents by a factor of 10,000 over the LM1458. A combination of careful layout design and internal trimming guarantees very low input offset voltage and voltage drift. The LF442 also has a very low equivalent input noise voltage for a low power amplifier.

The LF442 is pin compatible with the LM1458 allowing an immediate 10 times reduction in power drain in many applications. The LF442 should be used where low power dissipation and good electrical characteristics are the major considerations.

Features

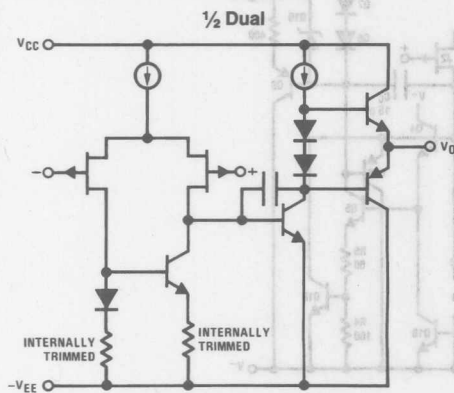
- $\frac{1}{10}$ supply current of a LM1458 400 μ A (max)
- Low input bias current 50 pA (max)
- Low input offset voltage 1 mV (max)
- Low input offset voltage drift 10 μ V/°C (max)
- High gain bandwidth 1 MHz
- High slew rate 1 V/ μ s
- Low noise voltage for low power 35 nV/ $\sqrt{\text{Hz}}$
- Low input noise current 0.01 pA/ $\sqrt{\text{Hz}}$
- High input impedance 10¹²Ω
- High gain $V_O = \pm 10V$, $R_L = 10k$ 50k (min)

Typical Connection



TL/H/9155-1

Simplified Schematic



TL/H/9155-3

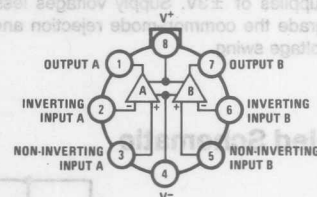
Ordering Information

LF442XYZ

- X indicates electrical grade
- Y indicates temperature range
- "M" for military
- "C" for commercial
- Z indicates package type
- "H" or "N"

Connection Diagrams

Metal Can Package



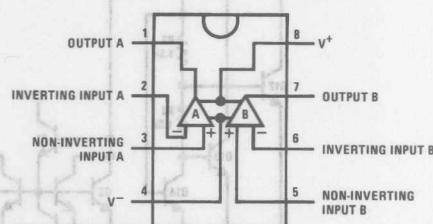
TL/H/9155-2

Top View

Note: Pin 4 connected to case

Order Number LF442AMH
or LF442MH/883
See NS Package Number H08A

Dual-In-Line Package



TL/H/9155-4

Top View

Order Number LF442ACN or LF442CN
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 9)

| | LF442A | LF442 | H Package 150°C | N Package 115°C |
|---|------------|------------|---|--------------------------------|
| Supply Voltage | ±22V | ±18V | 65°C/W 165°C/W | 114°C/W 152°C/W |
| Differential Input Voltage | ±38V | ±30V | 21°C/W | (Note 4) |
| Input Voltage Range (Note 1) | ±19V | ±15V | (Note 4) | (Note 4) |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous | Storage Temperature Range -65°C ≤ T _A ≤ 150°C | -65°C ≤ T _A ≤ 150°C |
| | | | Lead Temperature (Soldering, 10 sec.) | 260°C |
| | | | ESD Tolerance | Rating to be determined |

DC Electrical Characteristics (Note 6)

| Symbol | Parameter | Conditions | LF442A | | | LF442 | | | Units |
|----------------------|------------------------------------|--|--------|------------------|-----|-------|------------------|-----|-------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S = 10 kΩ, T _A = 25°C | | 0.5 | 1.0 | | 1.0 | 5.0 | mV |
| | | Over Temperature | | | | | | 7.5 | mV |
| ΔV _{OS} /ΔT | Average TC of Input Offset Voltage | R _S = 10 kΩ | | 7 | 10 | | 7 | | μV/°C |
| I _{OS} | Input Offset Current | V _S = ±15V (Notes 6 and 7) | | 5 | 25 | | 5 | 50 | pA |
| | | T _j = 25°C | | | | | | | |
| | | T _j = 70°C | | | 1.5 | | | 1.5 | nA |
| | | T _j = 125°C | | | 10 | | | | nA |
| I _B | Input Bias Current | V _S = ±15V (Notes 6 and 7) | | 10 | 50 | | 10 | 100 | pA |
| | | T _j = 70°C | | | 3 | | | 3 | nA |
| | | T _j = 125°C | | | 20 | | | | nA |
| R _{IN} | Input Resistance | T _j = 25°C | | 10 ¹² | | | 10 ¹² | | Ω |
| A _{VOL} | Large Signal Voltage Gain | V _S = ±15V, V _O = ±10V, R _L = 10 kΩ, T _A = 25°C | 50 | 200 | | 25 | 200 | | V/mV |
| | | Over Temperature | 25 | 200 | | 15 | 200 | | V/mV |
| V _O | Output Voltage Swing | V _S = ±15V, R _L = 10 kΩ | ±12 | ±13 | | ±12 | ±13 | | V |
| V _{CM} | Input Common-Mode Voltage Range | | ±16 | +18 -17 | | ±11 | +14 -12 | | V |
| CMRR | Common-Mode Rejection Ratio | R _S ≤ 10 kΩ | 80 | 100 | | 70 | 95 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 8) | 80 | 100 | | 70 | 90 | | dB |
| I _S | Supply Current | | | 300 | 400 | | 400 | 500 | μA |

AC Electrical Characteristics (Note 6)

| Symbol | Parameter | Conditions | LF442A | | | LF442 | | | Units |
|--------|---------------------------------|---|--------|------|-----|-------|------|-----|------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25^\circ\text{C}, f = 1 \text{ Hz-20 kHz}$ (Input Referred) | | -120 | | | -120 | | dB |
| SR | Slew Rate | $V_S = \pm 15\text{V}, T_A = 25^\circ\text{C}$ | 0.8 | 1 | | 0.6 | 1 | | V/ μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15\text{V}, T_A = 25^\circ\text{C}$ | 0.8 | 1 | | 0.6 | 1 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ\text{C}, R_S = 100\Omega$, $f = 1 \text{ kHz}$ | | 35 | | | 35 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $T_A = 25^\circ\text{C}, f = 1 \text{ kHz}$ | | 0.01 | | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: The value given is in 400 linear feet/min air flow.

Note 4: The value given is in static air.

Note 5: These devices are available in both the commercial temperature range $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ and the military temperature range $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "H" package only.

Note 6: Unless otherwise specified, the specifications apply over the full temperature range and for $V_S = \pm 20\text{V}$ for the LF442A and for $V_S = \pm 15\text{V}$ for the LF442. V_{OS} , I_B , and I_{OS} are measured at $V_{CM} = 0$.

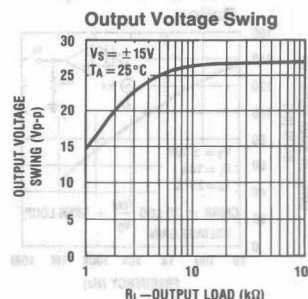
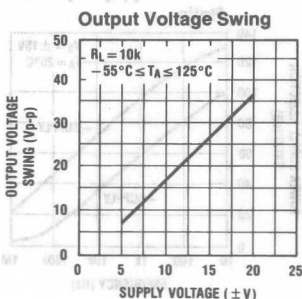
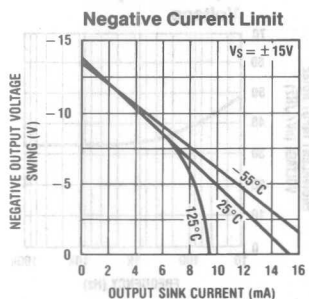
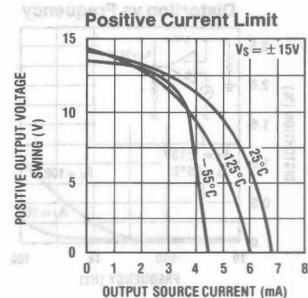
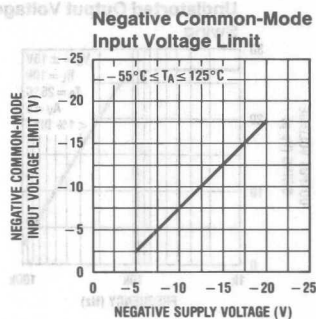
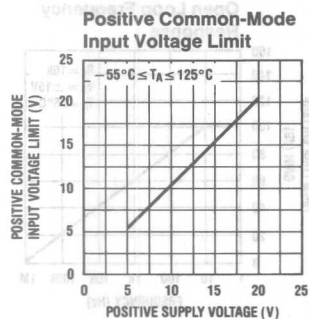
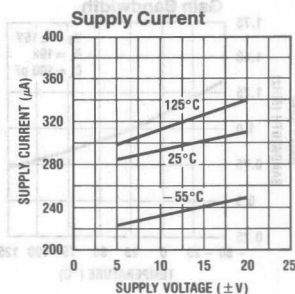
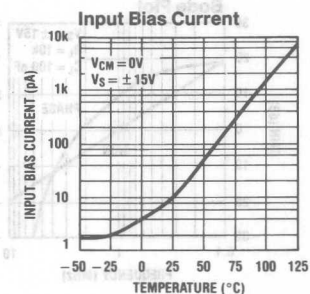
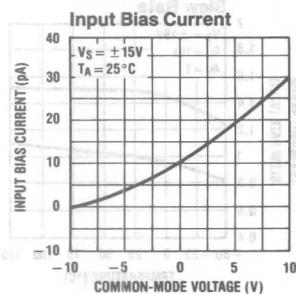
Note 7: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 8: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $\pm 15\text{V}$ to $\pm 5\text{V}$ for the LF442 and $\pm 20\text{V}$ to $\pm 5\text{V}$ for the LF442A.

Note 9: Refer to RETS442X for LF442MH military specifications.

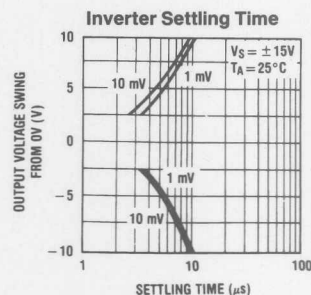
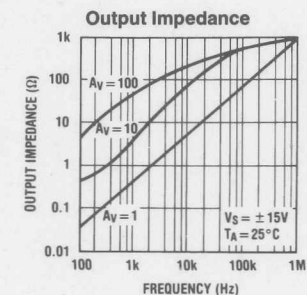
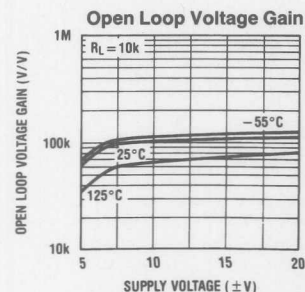
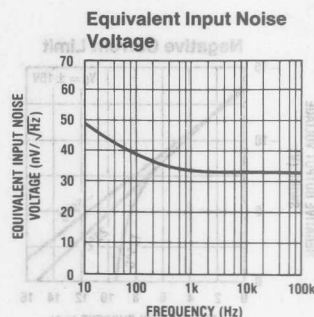
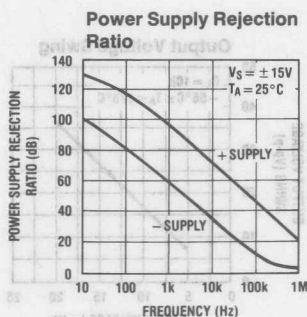
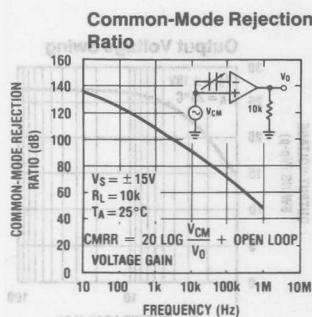
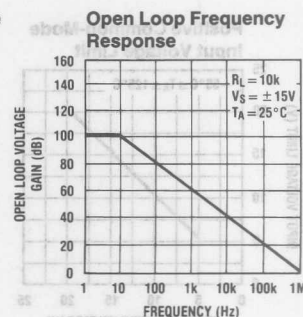
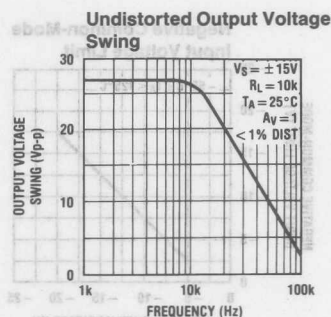
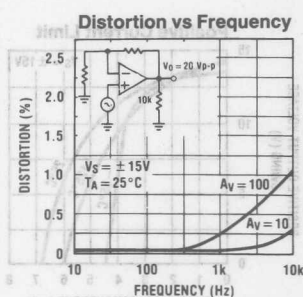
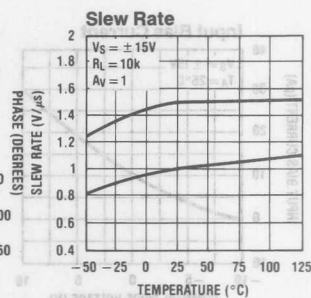
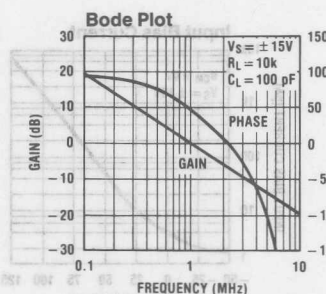
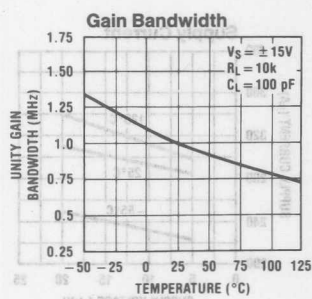
| | | | | | | | | |
|-----------|---------------------------------|--|-------------------------|------------------|------------------|------------------|------------------|---------------|
| I_B | Input Bias Current | $V_S = \pm 15\text{V}$ (Notes 6 and 7) | $T = 25^\circ\text{C}$ | 10 | 20 | 100 | 100 | pA |
| I_B | Input Bias Current | $V_S = \pm 15\text{V}$ (Notes 6 and 7) | $T = 25^\circ\text{C}$ | 10 | 20 | 100 | 100 | pA |
| I_B | Input Bias Current | $V_S = \pm 15\text{V}$ (Notes 6 and 7) | $T = 125^\circ\text{C}$ | 10 | 20 | 100 | 100 | pA |
| R_{in} | Input Resistance | | $T = 25^\circ\text{C}$ | 10 ¹² | 10 ¹² | 10 ¹² | 10 ¹² | Ω |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15\text{V}, V_O = \pm 10\text{V}$, $R_L = 10 \text{ k}\Omega, T_A = 25^\circ\text{C}$ | 50 | 50 | 500 | 500 | 500 | V/V |
| A_{VOL} | Large Signal Voltage Gain | Over Temperature | | 50 | 500 | 500 | 500 | V/V |
| V_O | Output Voltage Swing | $V_S = \pm 15\text{V}, R_L = 10 \text{ k}\Omega$ | | ± 12 | ± 12 | ± 12 | ± 12 | V |
| V_{CM} | Input Common-Mode Voltage Range | | | ± 18 | ± 18 | ± 17 | ± 17 | V |
| V_{CM} | Input Common-Mode Voltage Range | | | ± 18 | ± 18 | ± 17 | ± 17 | V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$ | | 80 | 100 | 70 | 82 | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 8) | | 80 | 100 | 70 | 80 | dB |
| I_S | Supply Current | | | 300 | 400 | 400 | 500 | μA |

Typical Performance Characteristics



TL/H/9155-5

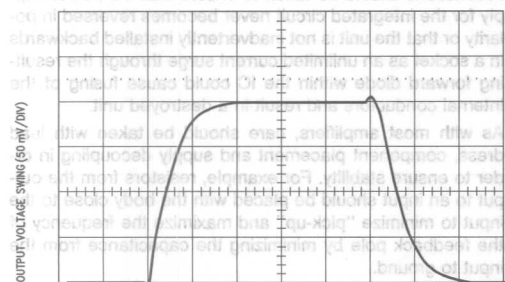
Typical Performance Characteristics (Continued)



Pulse Response $R_L = 10\text{ k}\Omega$, $C_L = 10\text{ pF}$

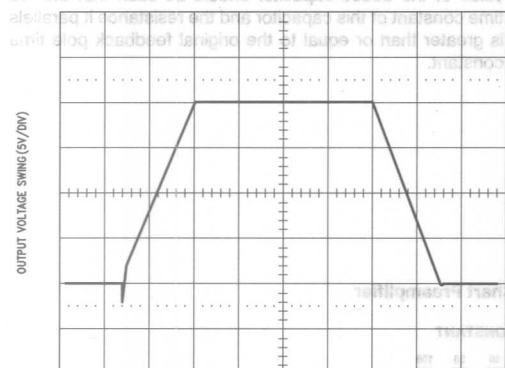
This amplifier will drive a $10\text{ k}\Omega$ load resistance to $\pm 10\text{ V}$ over the full temperature range.

Small Signal Inverting



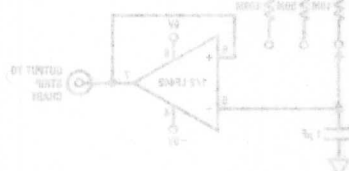
TL/H/9155-7

Large Signal Inverting



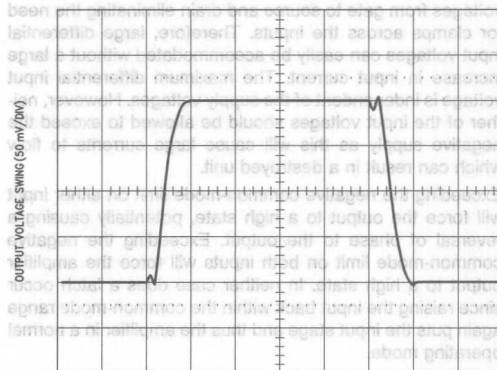
TL/H/9155-9

TIME (10 $\mu\text{s/DIV}$)
Fully extensible gain and time constant.
Battery powered supply allows direct plug-in
to scope or chart recorder without common
mode problems.



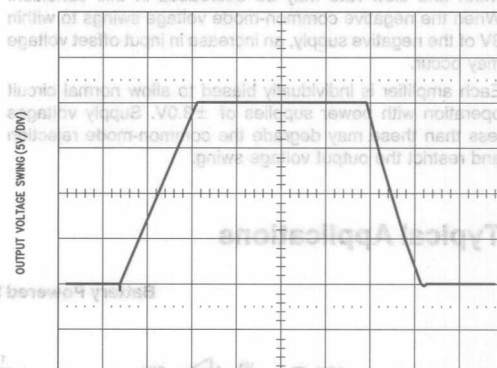
TL/H/9155-11

Small Signal Non-Inverting

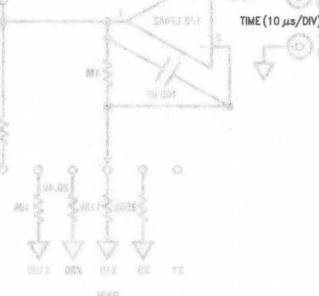


TL/H/9155-8

Large Signal Non-Inverting



TL/H/9155-10



Application Hints

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BIFET II). The input offset voltage is typically $\pm 1\text{ mV}$ and the input bias current is typically $\pm 10\text{ pA}$. The input impedance is typically $> 10^9\text{ }\Omega$. The output impedance is typically $< 100\text{ }\Omega$. The output voltage swing is typically $\pm 10\text{ V}$ into a $10\text{ k}\Omega$ load. The slew rate is typically $> 10\text{ V}/\mu\text{s}$. The common-mode input range is typically $\pm 10\text{ V}$. The quiescent current is typically $< 1\text{ mA}$. The package is a 14-pin DIP.

Exceeding the positive common-mode limit on a single input will not change the output of the amplifier. If both inputs are driven to the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply, however the gain band-width and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 1 V of the negative supply, an increase in input offset voltage may occur. Each amplifier is internally biased to allow normal operation with power supplies of $\pm 10\text{ V}$. Supply voltages less than these may degrade the common-mode rejection and reduce the output voltage swing.

Typical Applications

This device is a dual low power op amp with internally trimmed input offset voltages and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of $\pm 3.0V$. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a 10 k Ω load resistance to $\pm 10V$ over the full temperature range.

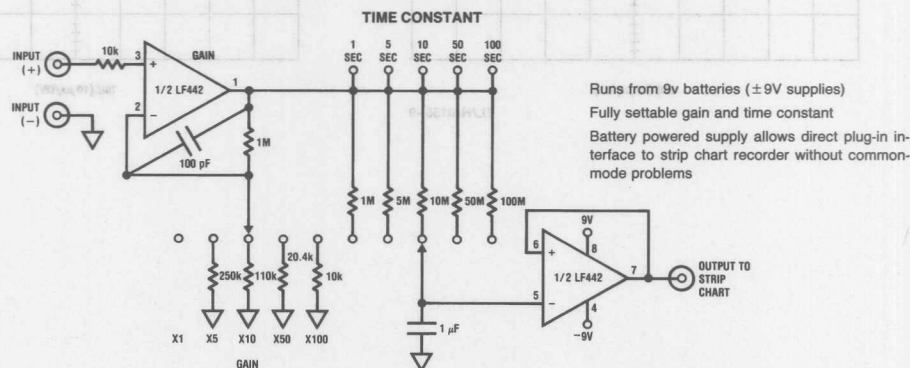
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications

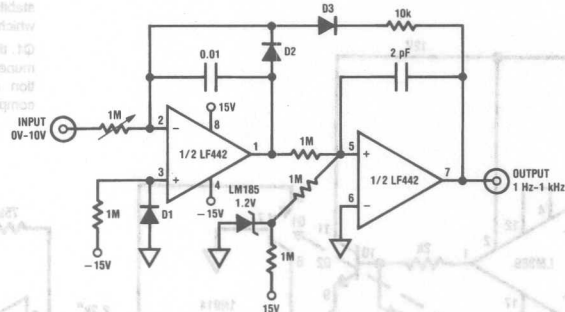
Battery Powered Strip Chart Preamplifier



TL/H/9155-11

Typical Applications (Continued)

"No FET" Low Power V → F Converter

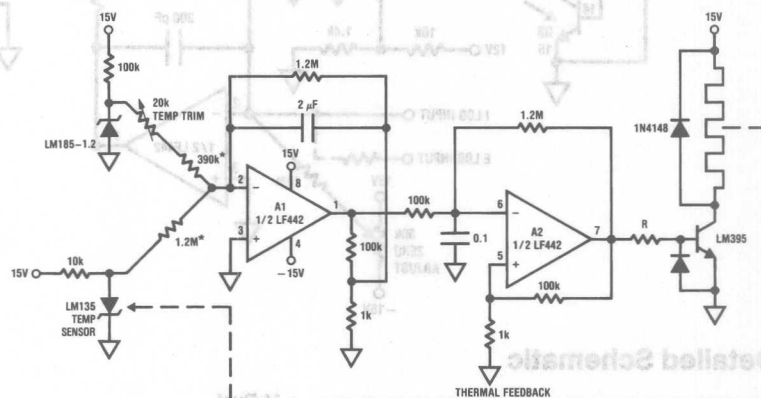


Trim 1M pot for 1 kHz full-scale output
15 mW power drain
No integrator reset FET required
Mount D1 and D2 in close proximity
1% linearity to 1 kHz

TL/H/9155-12

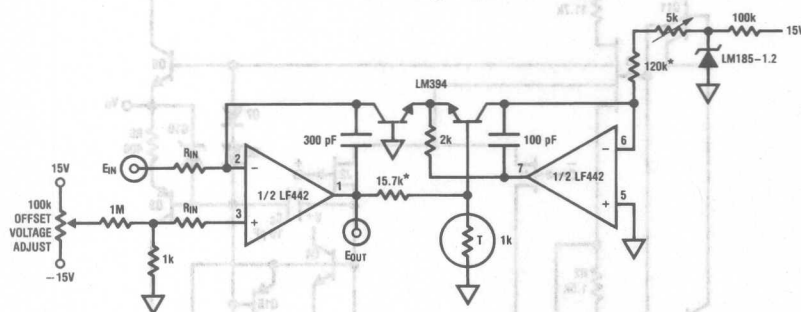
High Efficiency Crystal Oven Controller

- $T_{control} = 75^{\circ}C$
- A1's output represents the amplified difference between the LM335 temperature sensor and the crystal oven's temperature
- A2, a free running duty cycle modulator, drives the LM395 to complete a servo loop
- Switched mode operation yields high efficiency
- 1% metal film resistor



TL/H/9155-13

Conventional Log Amplifier



TL/H/9155-14

$$E_{OUT} = - \left[\log_{10} \left(\frac{E_{IN}}{R_{IN}} \right) + 5 \right]$$

R_T = Tel Labs type Q81

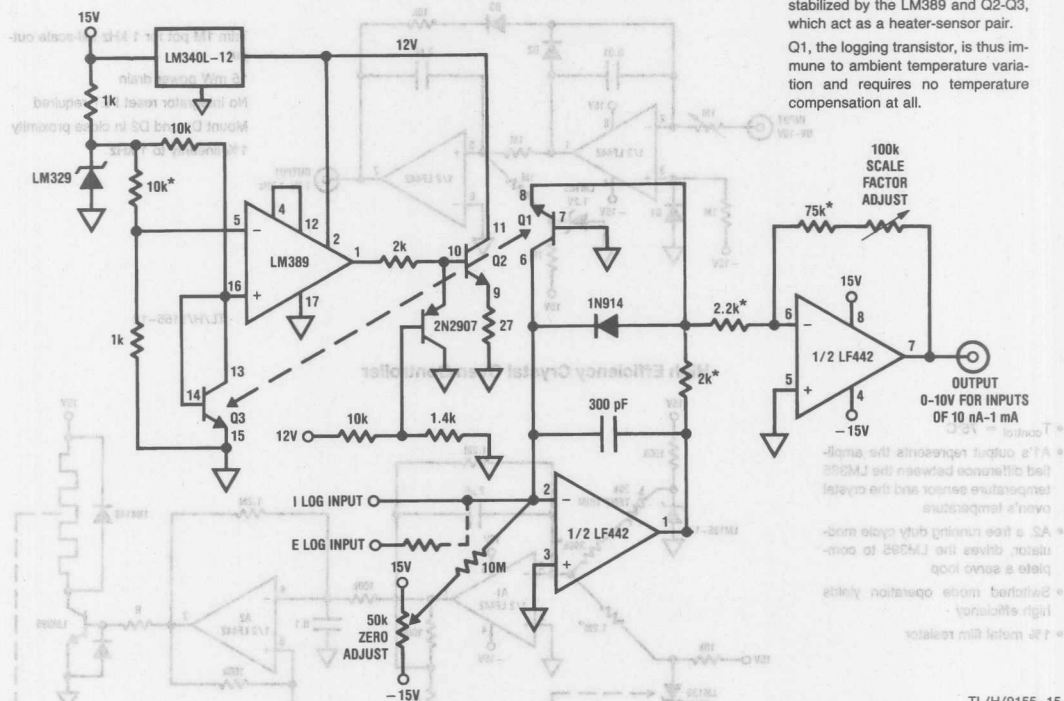
Trim 5k for 10 μA through the 5k-120k combination

*1% film resistor

Unconventional Log Amplifier

Q1, Q2, Q3 are included on LM389 amplifier chip which is temperature-stabilized by the LM389 and Q2-Q3, which act as a heater-sensor pair.

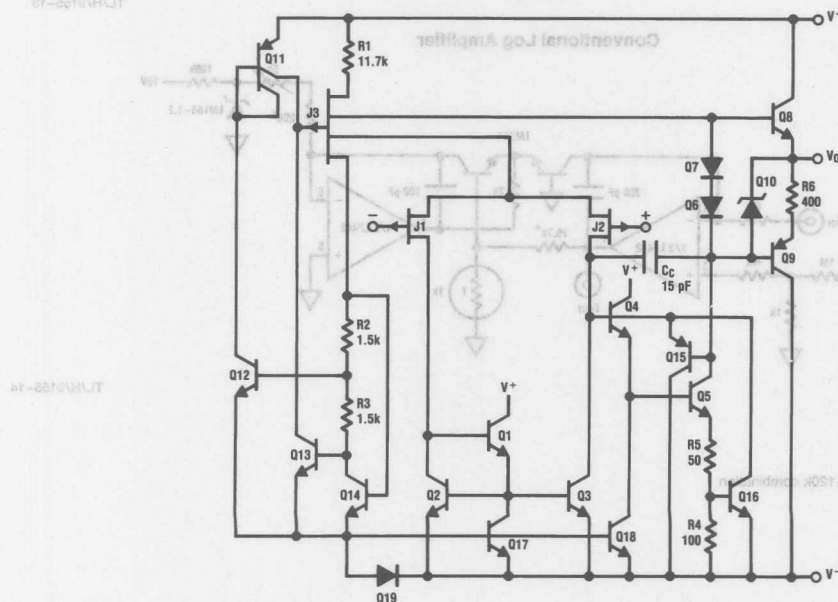
Q1, the logging transistor, is thus immune to ambient temperature variation and requires no temperature compensation at all.



TL/H/9155-15

Detailed Schematic

1/2 Dual



TL/H/9155-16

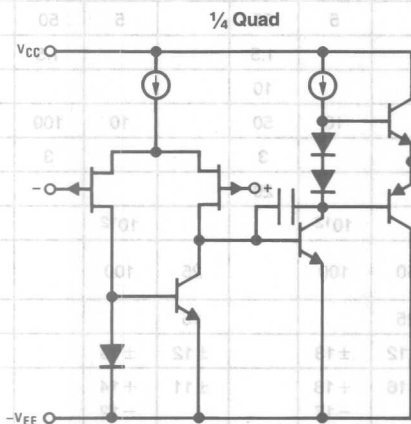
LF444 Quad Low Power JFET Input Operational Amplifier

General Description

The LF444 quad low power operational amplifier provides many of the same AC characteristics as the industry standard LM148 while greatly improving the DC characteristics of the LM148. The amplifier has the same bandwidth, slew rate, and gain (10 k Ω load) as the LM148 and only draws one fourth the supply current of the LM148. In addition the well matched high voltage JFET input devices of the LF444 reduce the input bias and offset currents by a factor of 10,000 over the LM148. The LF444 also has a very low equivalent input noise voltage for a low power amplifier.

The LF444 is pin compatible with the LM148 allowing an immediate 4 times reduction in power drain in many applications. The LF444 should be used wherever low power dissipation and good electrical characteristics are the major considerations.

Simplified Schematic

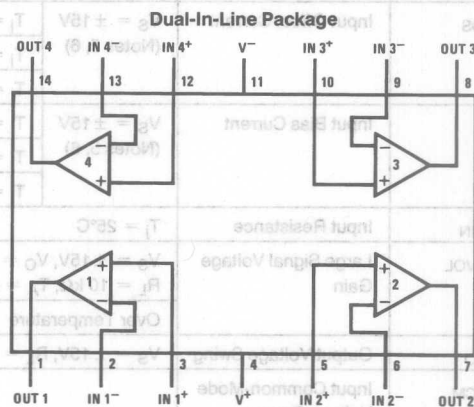


TL/H/9156-1

Features

- $\frac{1}{4}$ supply current of a LM148 200 μ A/Amplifier (max)
- Low input bias current 50 pA (max)
- High gain bandwidth 1 MHz
- High slew rate 1 V/ μ s
- Low noise voltage for low power 35 nV/ $\sqrt{\text{Hz}}$
- Low input noise current 0.01 pA/ $\sqrt{\text{Hz}}$
- High input impedance $10^{12}\Omega$
- High gain $V_O = \pm 10V, R_L = 10k\Omega$ 50k (min)

Connection Diagram



TL/H/9156-2

Top View

Order Number LF444AMD, LF444CM,
LF444ACN, LF444CN or LF444MD/883
See NS Package Number D14E, M14A or N14A

Ordering Information

LF444XYZ

X indicates electrical grade

Y indicates temperature range

"M" for military, "C" for commercial

Z indicates package type "D", "M" or "N"

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | LF444A | LF444 |
|---|------------------|----------------------|
| Supply Voltage | ±22V | ±18V |
| Differential Input Voltage | ±38V | ±30V |
| Input Voltage Range (Note 1) | ±19V | ±15V |
| Output Short Circuit Duration (Note 2) | Continuous | Continuous |
| Power Dissipation (Notes 3 and 9) | D Package 900 mW | N, M Packages 670 mW |
| T_j max | 150°C | 115°C |
| θ_{JA} (Typical) | 100°C/W | 85°C/W |

| | |
|--|--------------------------------|
| Operating Temperature Range | LF444A/LF444 (Note 4) |
| Storage Temperature Range | -65°C ≤ T _A ≤ 150°C |
| ESD Tolerance (Note 10) | Rating to be determined |
| Soldering Information | |
| Dual-In-Line Packages (Soldering, 10 sec.) | 260°C |
| Small Outline Package Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics (Note 5)

| Symbol | Parameter | Conditions | LF444A | | | LF444 | | | Units |
|----------------------|------------------------------------|---|--------|------------------|-----|-------|------------------|-----|--------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{OS} | Input Offset Voltage | R _S = 10k, T _A = 25°C | | 2 | 5 | | 3 | 10 | mV |
| | | 0°C ≤ T _A ≤ +70°C | | | 6.5 | | | 12 | mV |
| | | -55°C ≤ T _A ≤ +125°C | | | 8 | | | | mV |
| ΔV _{OS} /ΔT | Average TC of Input Offset Voltage | R _S = 10 kΩ | | 10 | | | 10 | | μV/°C |
| I _{OS} | Input Offset Current | V _S = ±15V (Notes 5, 6) | | 5 | 25 | | 5 | 50 | pA |
| | | T _j = 25°C | | | 1.5 | | | 1.5 | nA |
| | | T _j = 70°C | | | 10 | | | | nA |
| I _B | Input Bias Current | V _S = ±15V (Notes 5, 6) | | 10 | 50 | | 10 | 100 | pA |
| | | T _j = 25°C | | | 3 | | | 3 | nA |
| | | T _j = 70°C | | | 20 | | | | nA |
| R _{IN} | Input Resistance | T _j = 25°C | | 10 ¹² | | | 10 ¹² | | Ω |
| A _{VOL} | Large Signal Voltage Gain | V _S = ±15V, V _O = ±10V R _L = 10 kΩ, T _A = 25°C | 50 | 100 | | 25 | 100 | | V/mV |
| | | Over Temperature | 25 | | | 15 | | | V/mV |
| V _O | Output Voltage Swing | V _S = ±15V, R _L = 10 kΩ | ±12 | ±13 | | ±12 | ±13 | | V |
| V _{CM} | Input Common-Mode Voltage Range | | ±16 | +18 -17 | | ±11 | +14 -12 | | V V |
| CMRR | Common-Mode Rejection Ratio | R _S ≤ 10 kΩ | 80 | 100 | | 70 | 95 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 7) | 80 | 100 | | 70 | 90 | | dB |
| I _S | Supply Current | | | 0.6 | 0.8 | | 0.6 | 1.0 | mA |

| | | | Min | Typ | Max | Min | Typ | Max |
|-------|---------------------------------|--|-----|------|-----|-----|------|-----------------|
| | Amplifier-to-Amplifier Coupling | | | -120 | | | -120 | dB |
| SR | Slew Rate | $V_S = \pm 15V, T_A = 25^\circ C$ | | 1 | | | 1 | V/ μs |
| GBW | Gain-Bandwidth Product | $V_S = \pm 15V, T_A = 25^\circ C$ | | 1 | | | 1 | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ C, R_S = 100\Omega, f = 1 \text{ kHz}$ | | 35 | | | 35 | nV/ \sqrt{Hz} |
| i_n | Equivalent Input Noise Current | $T_A = 25^\circ C, f = 1 \text{ kHz}$ | | 0.01 | | | 0.01 | pA/ \sqrt{Hz} |

Note 1: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 2: Any of the amplifier outputs can be shorted to ground indefinitely, however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

Note 3: For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} .

Note 4: The LF444A is available in both the commercial temperature range $0^\circ C \leq T_A \leq 70^\circ C$ and the military temperature range $-55^\circ C \leq T_A \leq 125^\circ C$. The LF444 is available in the commercial temperature range only. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in "D" package only.

Note 5: Unless otherwise specified the specifications apply over the full temperature range and for $V_S = \pm 20V$ for the LF444A and for $V_S = \pm 15V$ for the LF444. V_{OS} , I_B , and I_{OS} are measured at $V_{CM} = 0$.

Note 6: The input bias currents are junction leakage currents which approximately double for every $10^\circ C$ increase in the junction temperature, T_J . Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA}P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

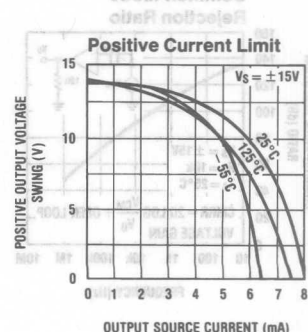
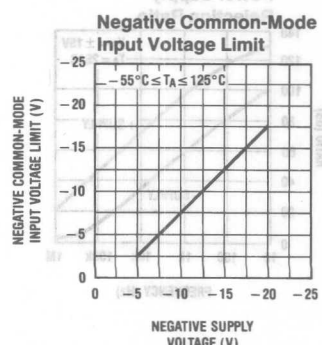
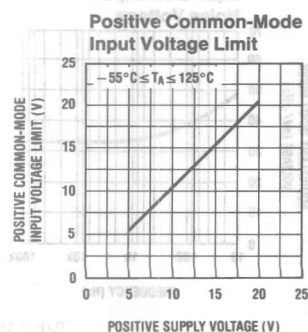
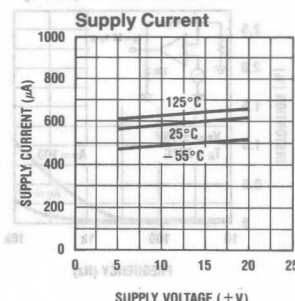
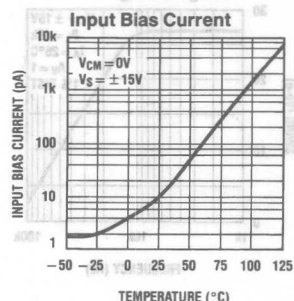
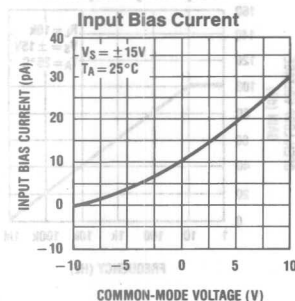
Note 7: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $\pm 15V$ to $\pm 5V$ for the LF444 and from $\pm 20V$ to $\pm 5V$ for the LF444A.

Note 8: Refer to RETS444X for LF444MD military specifications.

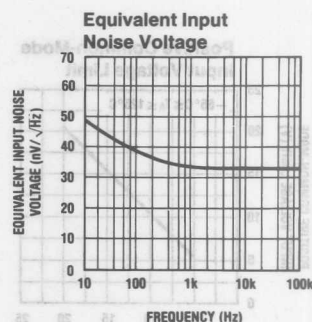
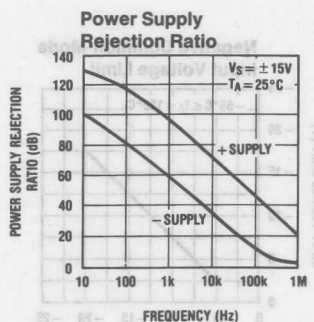
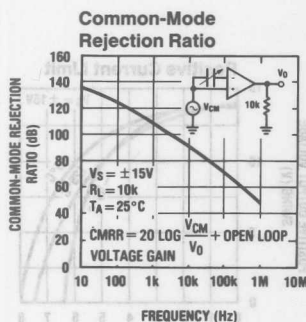
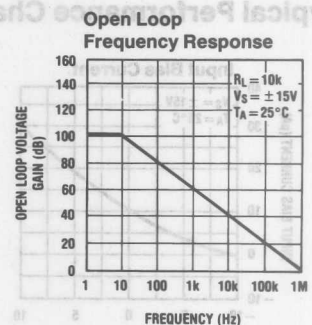
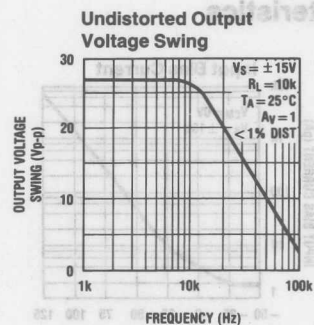
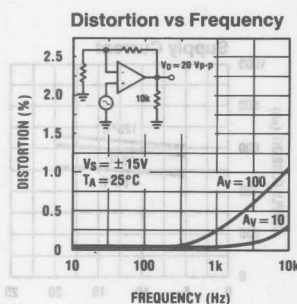
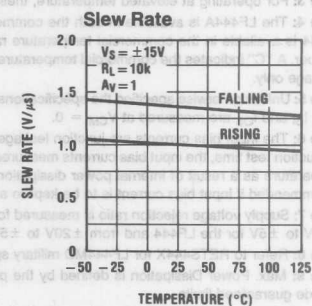
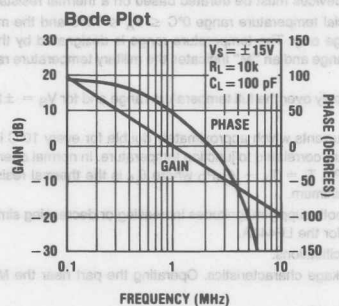
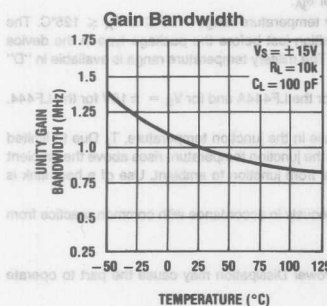
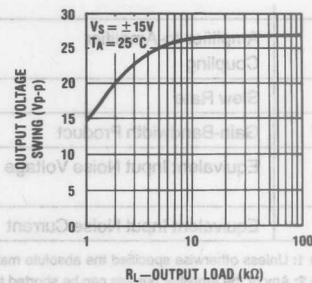
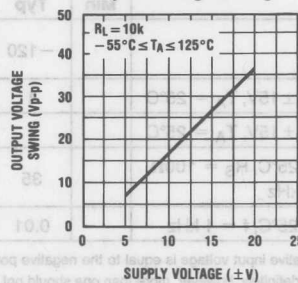
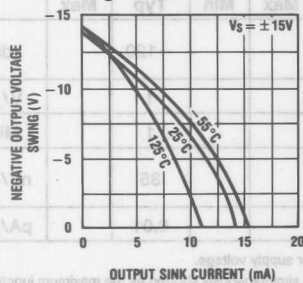
Note 9: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Note 10: Human body model, $1.5 \text{ k}\Omega$ in series with 100 pF .

Typical Performance Characteristics

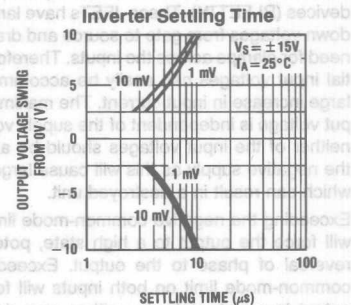
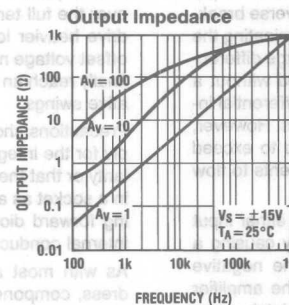
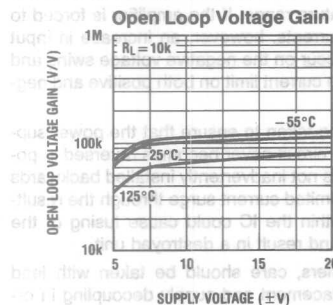


TL/H/9156-3

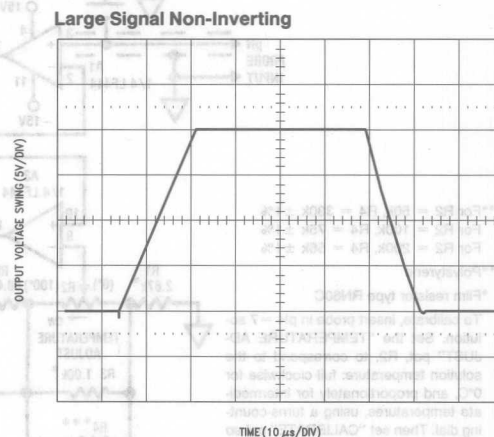
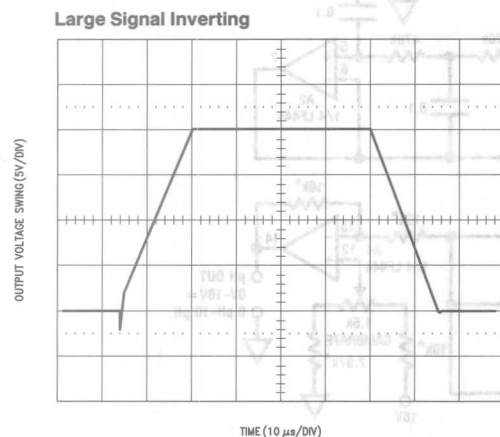
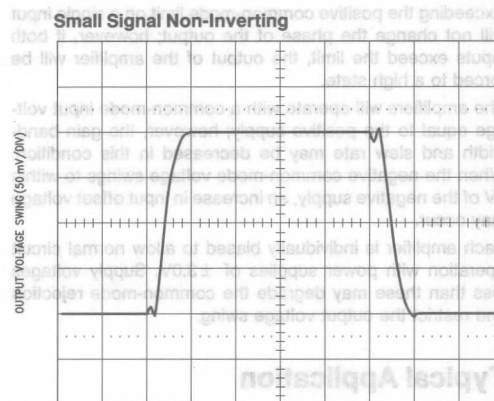
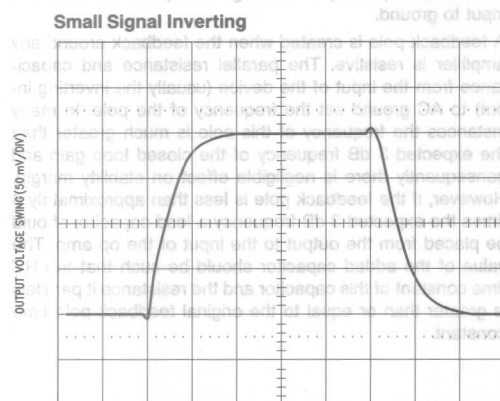


Typical Performance Characteristics (Continued)

The amplifier will drive a 10 k Ω load resistance to a 10V output. The amplifier will drive a 10 k Ω load resistance to a 10V output. The amplifier will drive a 10 k Ω load resistance to a 10V output.



Pulse Response $R_L = 10 k\Omega$, $C_L = 10 pF$



Application Hints

This device is a quad low power op amp with JFET input devices (BI-FET™). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased to allow normal circuit operation with power supplies of $\pm 3.0V$. Supply voltages less than these may degrade the common-mode rejection and restrict the output voltage swing.

The amplifiers will drive a $10\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

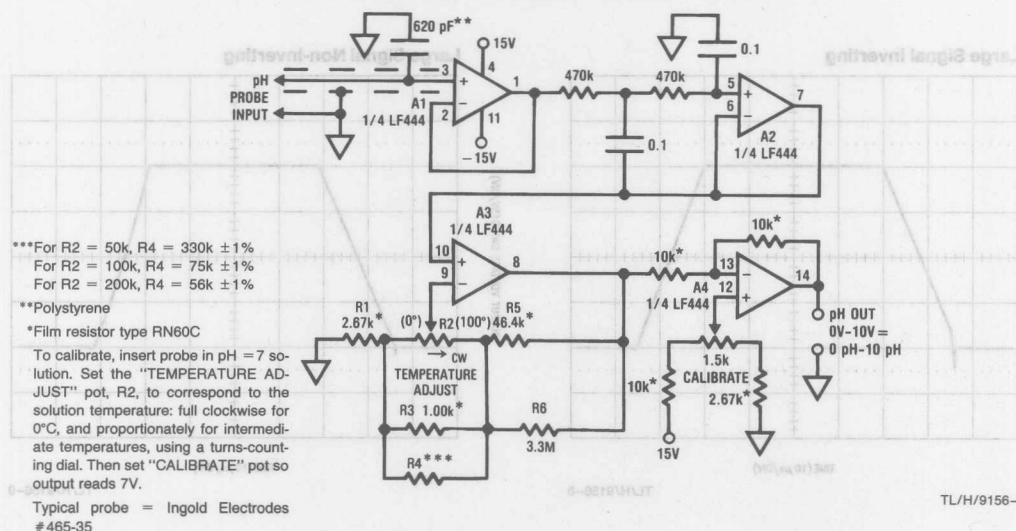
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

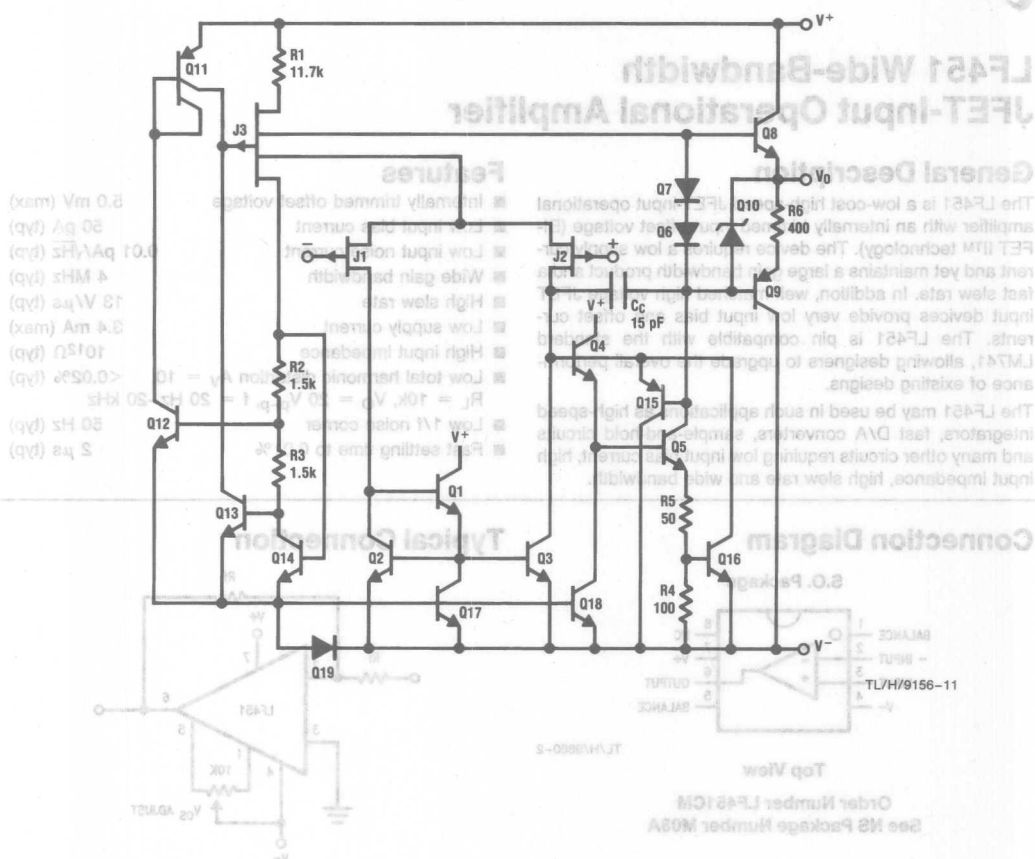
Typical Application

pH Probe Amplifier/Temperature Compensator

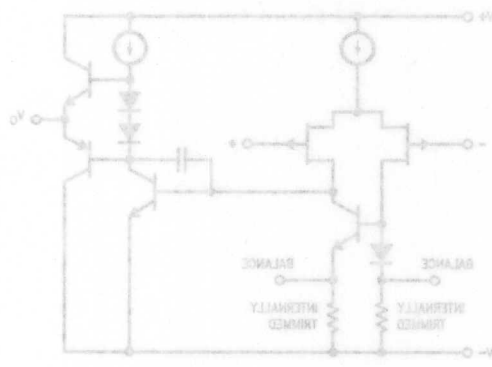


Detailed Schematic

1/4 Quad



Simplified Schematic



LF444

LF451 Wide-Bandwidth JFET-Input Operational Amplifier

General Description

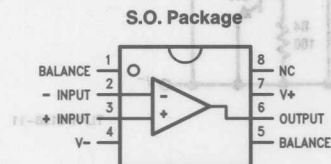
The LF451 is a low-cost high-speed JFET-input operational amplifier with an internally trimmed input offset voltage (BJT IITM technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF451 is pin compatible with the standard LM741, allowing designers to upgrade the overall performance of existing designs.

The LF451 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Features

- Internally trimmed offset voltage 5.0 mV (max)
- Low input bias current 50 pA (typ)
- Low input noise current 0.01 pA/ $\sqrt{\text{Hz}}$ (typ)
- Wide gain bandwidth 4 MHz (typ)
- High slew rate 13 V/ μs (typ)
- Low supply current 3.4 mA (max)
- High input impedance $10^{12}\Omega$ (typ)
- Low total harmonic distortion $A_V = 10$, $R_L = 10\text{k}\Omega$, $V_O = 20\text{V}_{\text{p-p}}$, $f = 20\text{Hz}-20\text{kHz}$ <0.02% (typ)
- Low 1/f noise corner 50 Hz (typ)
- Fast settling time to 0.01% 2 μs (typ)

Connection Diagram

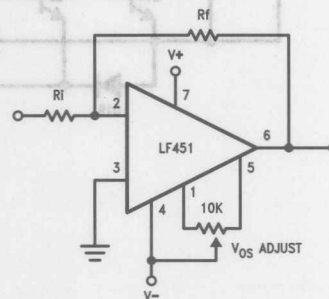


Top View

Order Number LF451CM
See NS Package Number M08A

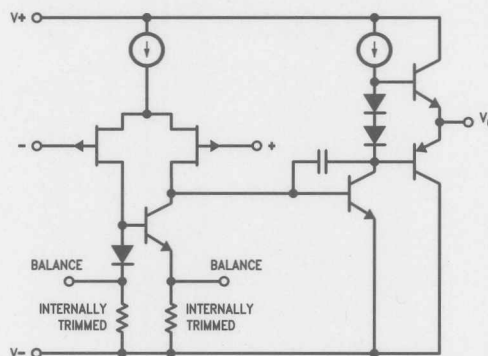
TL/H/9660-2

Typical Connection



TL/H/9660-1

Simplified Schematic



TL/H/9660-3

Supply Voltage ($V^+ - V^-$) 36V
 Input Voltage Range $V^- \leq V_{IN} \leq V^+$
 Differential Input Voltage (Note 2) $\pm 30V$
 Junction Temperature (T_J MAX) 150°C
 Output Short Circuit Duration Continuous
 Power Dissipation (Note 3) 500 mW

Infrared (15 sec)

220°C

Operating Ratings (Note 1)

Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$
 LF451CM $0^\circ C \leq T_A \leq +70^\circ C$
 Junction Temperature (T_{Jmax}) 125°C
 Supply Voltage ($V^+ - V^-$) 10V to 32V

DC Electrical Characteristics The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Bold-face limits apply for T_{MIN} to T_{MAX} ; all other limits $T_A = T_J = 25^\circ C$.**

| Symbol | Parameter | Conditions | LF451CM | | | Units |
|----------|---|---|---------------------|-----------------------------|-----------------------------|----------|
| | | | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| V_{OS} | Maximum Input Offset Voltage | $R_S = 10\text{ k}\Omega$, (Note 10) | 0.3 | 5 | | mV |
| I_{OS} | Maximum Input Offset Current | (Notes 9, 10) $T_J = 25^\circ C$ $T_J = 70^\circ C$ | 25 | 100 | 2 | pA nA |
| I_B | Maximum Input Bias Current | (Notes 9, 10) $T_J = 25^\circ C$ $T_J = 70^\circ C$ | 50 | 200 | 4 | pA nA |
| R_{IN} | Input Resistance | $T_J = 25^\circ C$ | 10^{12} | | | Ω |
| AVOL | Minimum Large Signal Voltage Gain | $V_O = \pm 10V$, $R_L = 2\text{ k}\Omega$ (Note 10) | 200 | 50 | 25 | V/mV |
| V_O | Minimum Output Voltage Swing | $R_L = 10\text{ k}\Omega$ | ± 13.5 | ± 12 | ± 12 | V |
| V_{CM} | Minimum Input Common Mode Voltage Range | | +14.5 -11.5 | +11 -11 | +11 -11 | V V |
| CMRR | Minimum Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 100 | 80 | 80 | dB |
| PSRR | Minimum Supply Voltage Rejection Ratio | (Note 11) | 100 | 80 | 80 | dB |
| I_S | Maximum Supply Current | | | 3.4 | 3.4 | mA |

AC Electrical Characteristics The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Bold-face limits apply for T_{MIN} to T_{MAX} ; all other limits $T_A = T_J = 25^\circ C$.**

| Symbol | Parameter | Conditions | LF451CM | | | Units |
|--------|--------------------------------|--|---------------------|-----------------------------|-----------------------------|-----------------|
| | | | Typical (Note 6) | Tested Limit (Note 7) | Design Limit (Note 8) | |
| SR | Slew Rate | $A_V = +1$ | 13 | 8 | | V/ μs |
| GBW | Minimum Gain-Bandwidth Product | $f = 100\text{ kHz}$ | 4 | 2.7 | | MHz |
| e_n | Equivalent Input Noise Voltage | $R_S = 100\Omega$, $f = 1\text{ kHz}$ | 25 | | | nV/ \sqrt{Hz} |
| i_n | Equivalent Input Noise Current | $R_S = 100\Omega$, $f = 1\text{ kHz}$ | 0.01 | | | pA/ \sqrt{Hz} |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, θ_{JA} and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_J \text{ MAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_J \text{ max} = 125^\circ C$. The typical thermal resistance (θ_{JA}) of the LF451CM when board-mounted is $170^\circ C/W$.

Note 5: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

Note 6: Typicals are at $T_J = 25^\circ C$ and represent most likely parametric norm.

Note 7: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: Design limits are guaranteed to National's AOQL, but not 100% tested.

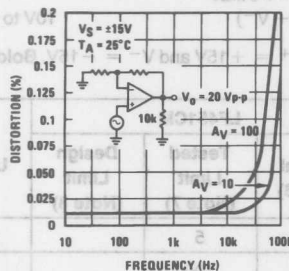
Note 9: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature T_J . Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient.

Note 10: V_{OS} , I_B , $AVOL$, and I_{OS} are measured at $V_{CM} = 0V$.

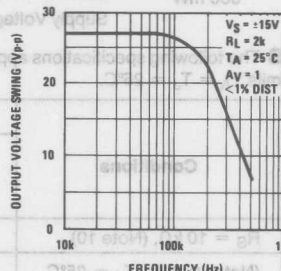
Note 11: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

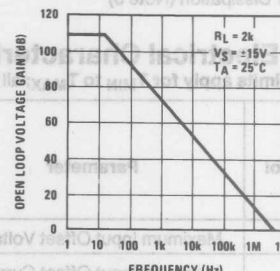
Distortion vs Frequency



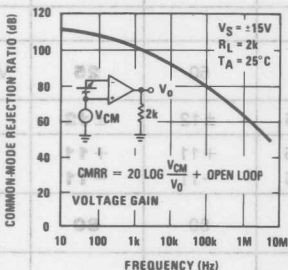
Undistorted Output Voltage Swing



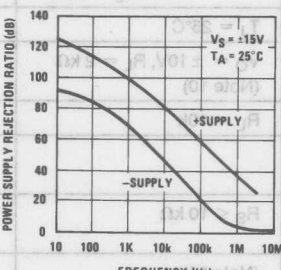
Open Loop Frequency Response



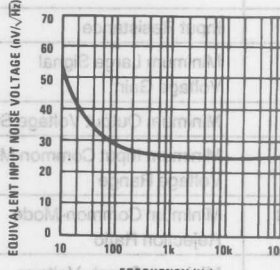
Common-Mode Rejection Ratio



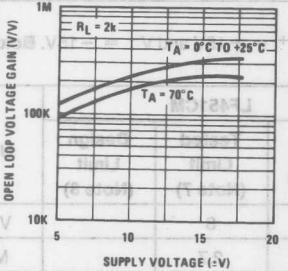
Power Supply Rejection Ratio



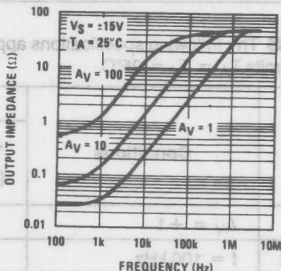
Equivalent Input Noise Voltage



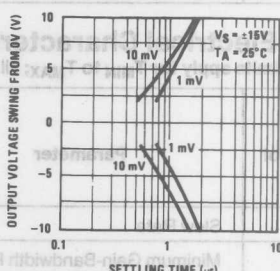
Open Loop Voltage Gain (V/V)



Output Impedance



Inverter Settling Time



Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

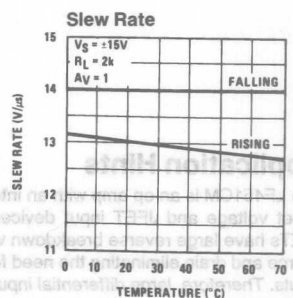
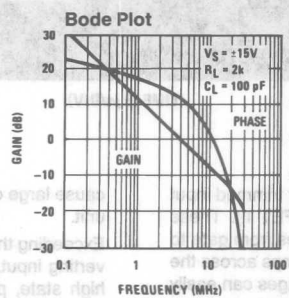
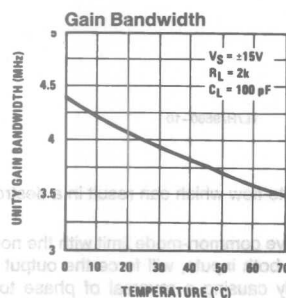
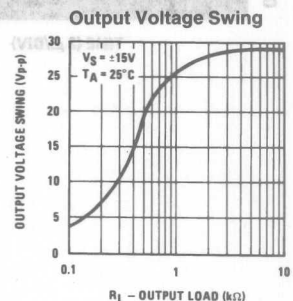
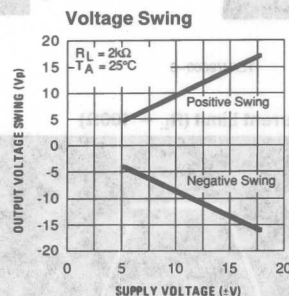
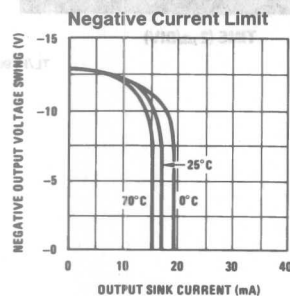
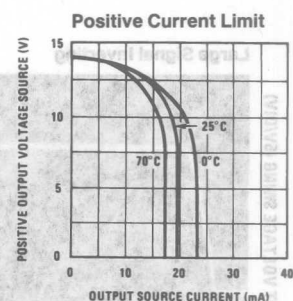
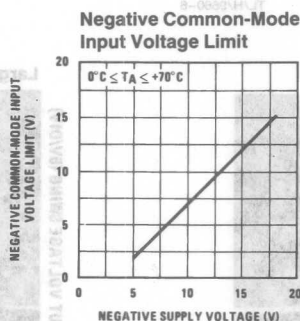
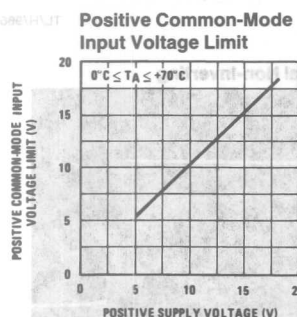
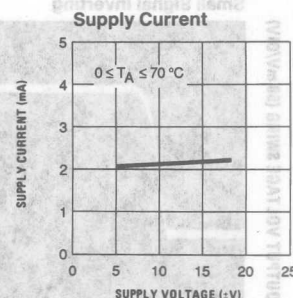
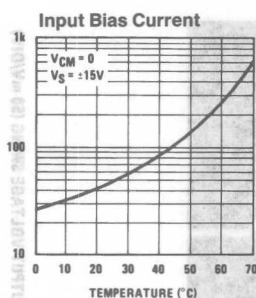
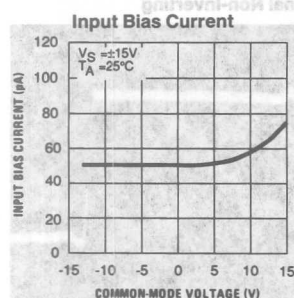
Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, A_{JA} and the ambient temperature, T_A . The maximum power dissipation at any temperature is $P_D = (T_J \text{ MAX} - T_A)/A_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_J \text{ MAX} = 125^\circ C$. The physical thermal resistance (θ_{JA}) of the LF451CM when board-mounted is $170^\circ C/W$.

Note 4: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

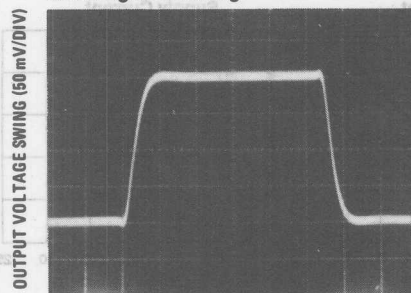
Note 5: Typical values are at $T_J = 25^\circ C$ and represent most likely parameter values.

Typical Performance Characteristics (Continued)



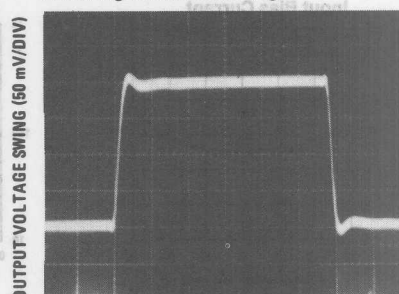
Pulse Response

Small Signal Inverting



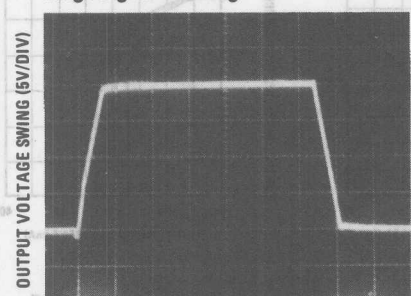
TIME (0.2 μ s/DIV)

Small Signal Non-Inverting



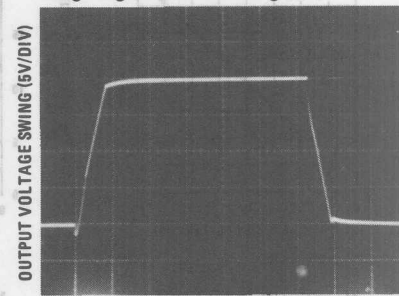
TIME (0.2 μ s/DIV)

Large Signal Inverting



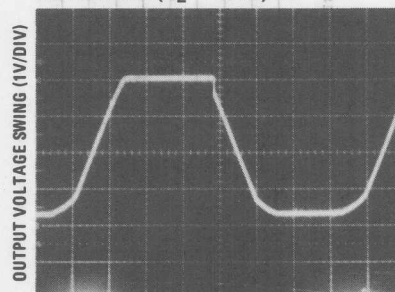
TIME (2 μ s/DIV)

Large Signal Non-Inverting



TIME (2 μ s/DIV)

Current Limit ($R_L = 100\Omega$)



TIME (5 μ s/DIV)

Application Hints

The LF451CM is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will

cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output.

In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Application Hints (Continued)

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF451 is biased by a zener reference which allows normal circuit operation on $\pm 4\text{V}$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF451 will drive a $2\text{ k}\Omega$ load resistance to $\pm 10\text{V}$ over the full temperature range of 0°C to $+70^\circ\text{C}$. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

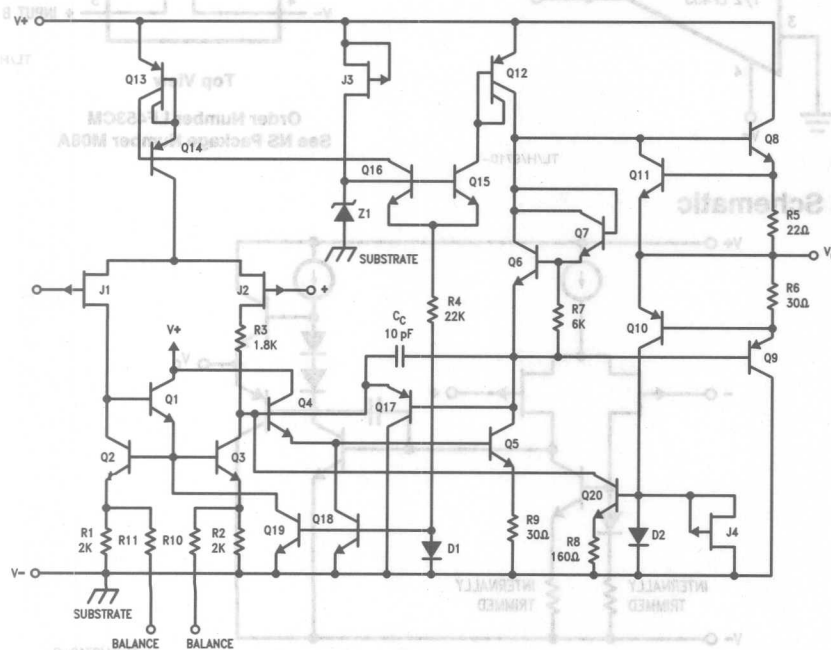
As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the

input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the S.O. package results from its very small size. It follows, however, that the die inside the S.O. package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the S.O. Therefore, not following certain precautions when board mounting the LF451CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF451CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF451CM surface mounting refer to Application Note AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" and to Section 6 "Surface Mount" found in any Rev. 1 Linear Databook volume.

Detailed Schematic



TL/H/9660-11

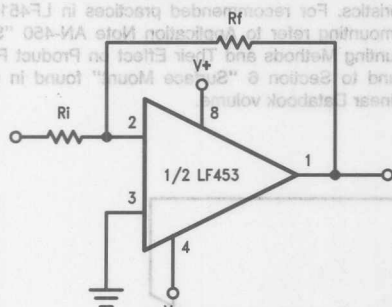
LF453 Wide-Bandwidth Dual JFET-Input Operational Amplifiers

General Description

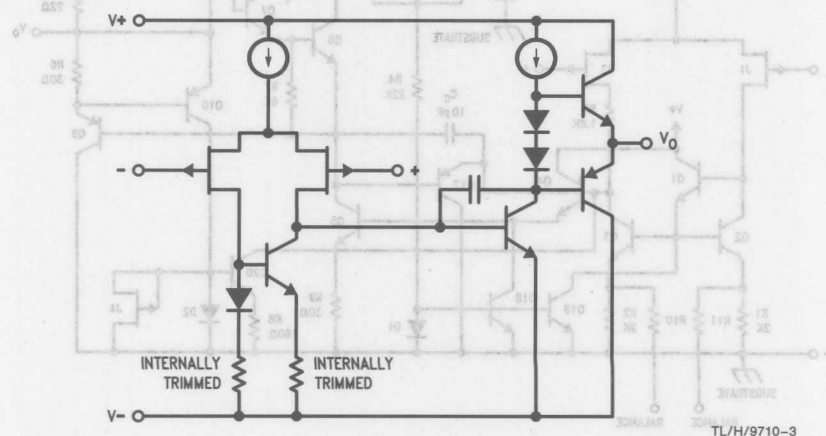
The LF453 is a low-cost, high-speed, dual JFET-input operational amplifier with an internally trimmed input offset voltage (BI-FET II technology). The device requires a low supply current and yet the amplifiers maintain a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF453 is pin compatible with the standard LM1558, allowing designers to upgrade the overall performance of existing designs.

The LF453 may be used in such applications as high-speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input bias current, high input impedance, high slew rate and wide bandwidth.

Typical Connection



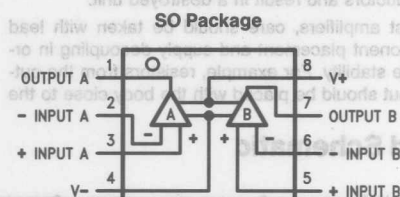
Simplified Schematic



Features

- Internally trimmed offset voltage 5.0 mV (max)
- Low input bias current 50 pA (typ)
- Low input noise current 0.01 pA/√Hz (typ)
- Wide gain bandwidth 4 MHz (typ)
- High slew rate 13 V/μs (typ)
- Low supply current 6.5 mA (max)
- High input impedance 10¹²Ω (typ)
- Low total harmonic distortion <0.02% (typ)
- $A_V = 10$; $R_{L1} = 10k$,
 $V_O = 20 V_{p-p}$, $f = 20 \text{ Hz} - 20 \text{ kHz}$
- Low 1/f noise corner 50 Hz (typ)
- Fast settling time to 0.01% 2 μs (typ)

Connection Diagram



Top View

Order Number LF453CM
See NS Package Number M08A

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

SO Package: Vapor Phase (60 sec.)
Infrared (15 sec.)

215°C
220°C

Supply Voltage ($V^+ - V^-$) 36V
Input Voltage Range $V^- \leq V_{IN} \leq V^+$
Differential Input Voltage (Note 2) $\pm 30V$
Junction Temperature (T_J MAX) 150°C
Output Short Circuit Duration Continuous
Power Dissipation (Note 3) 500 mW
ESD Tolerance TBD

Operating Ratings (Note 1)

Temperature Range $T_{MIN} \leq T_A \leq T_{MAX}$
LF453CM $0^\circ C \leq T_A \leq 70^\circ C$
Junction Temperature (T_J max) 125°C
Supply Voltage ($V^+ - V^-$) 10V to 32V

DC Electrical Characteristics The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. **Bold-face limits apply for T_{MIN} to T_{MAX} ; all other limits $T_A = T_J = 25^\circ C$.**

| Symbol | Parameter | Conditions | LF453CM | | | Units |
|----------|---|--|--------------------|-----------------------|-----------------------|----------|
| | | | Typical (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | |
| V_{OS} | Maximum Input Offset Voltage | $R_S = 10\text{ k}\Omega$, (Note 9) | | 5 | | mV |
| I_{OS} | Maximum Input Offset Current | (Notes 8, 9) $T_J = 25^\circ C$ $T_J = 70^\circ C$ | 25 | 100 | 2 | pA nA |
| I_B | Maximum Input Bias Current | (Notes 8, 9) $T_J = 25^\circ C$ $T_J = 70^\circ C$ | 50 | 200 | 4 | pA nA |
| R_{IN} | Input Resistance | $T_J = 25^\circ C$ | 1012 | | | Ω |
| AVOL | Minimum Large Signal Voltage Gain | $V_O = \pm 10V$, $R_L = 2\text{ k}\Omega$ (Note 9) | 200 | 50 | 25 | V/mV |
| V_O | Minimum Output Voltage Swing | $R_L = 10k$ | ± 13.5 | ± 12 | ± 12 | V |
| V_{CM} | Minimum Input Common Mode Voltage Range | | $+14.5$ -11.5 | $+11$ -11 | $+11$ -11 | V V |
| CMRR | Minimum Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 100 | 80 | 80 | dB |
| PSRR | Minimum Supply Voltage Rejection Ratio | (Note 10) | 100 | 80 | 80 | dB |
| I_S | Maximum Supply Current | | | 6.5 | 6.5 | mA |

AC Electrical Characteristics The following specifications apply for $V^+ = +15V$ and $V^- = -15V$. Limits apply for $T_A = T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | LF453CM | | | Units |
|--------|--------------------------------|--|------------------|-----------------------|-----------------------|-----------------|
| | | | Typical (Note 5) | Tested Limit (Note 6) | Design Limit (Note 7) | |
| SR | Slew Rate | $A_V = +1$ | 13 | 8 | | V/ μs |
| GBW | Minimum Gain-Bandwidth Product | $f = 100\text{ kHz}$ | 4 | 2.7 | | MHz |
| e_n | Equivalent Input Noise Voltage | $R_S = 100\Omega$, $f = 1\text{ kHz}$ | 25 | | | nV/ \sqrt{Hz} |
| i_n | Equivalent Input Noise Current | $R_S = 100\Omega$, $f = 1\text{ kHz}$ | 0.01 | | | pA/ \sqrt{Hz} |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating ratings.

Note 2: When the input voltage exceeds the power supplies, the current should be limited to 1 mA.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, Θ_{JA} and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_J \text{ MAX} - T_A) / \Theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For guaranteed operation $T_J \text{ max} = 125^\circ C$. The typical thermal resistance (Θ_{JA}) of the LF453CM when board-mounted is $160^\circ C/W$.

Note 4: See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (section titled "Surface Mount") for other methods of soldering surface mount devices.

Note 5: Typical values are at $T_J = 25^\circ C$ and represent most likely parametric norm.

Note 6: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 7: Design limits are guaranteed to National's AOQL, but not 100% tested.

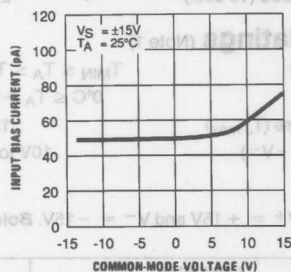
Note 8: The input bias currents are junction leakage currents which approximately double for every $10^\circ C$ increase in the junction temperature T_J . Due to limited production test time, the input bias currents are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_J = T_A + \Theta_{JA} P_D$ where Θ_{JA} is the thermal resistance from junction to ambient.

Note 9: V_{OS} , I_B , AVOL and I_{OS} are measured at $V_{CM} = 0V$.

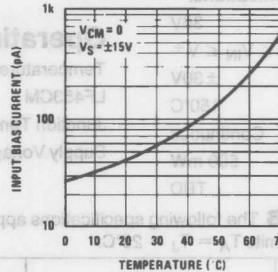
Note 10: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

Typical Performance Characteristics

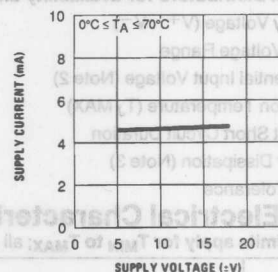
Input Bias Current



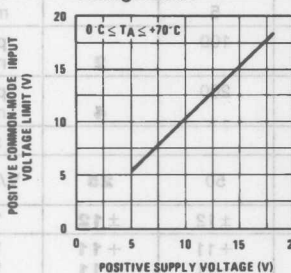
Input Bias Current



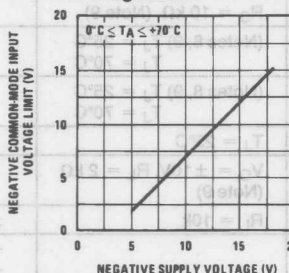
Supply Current



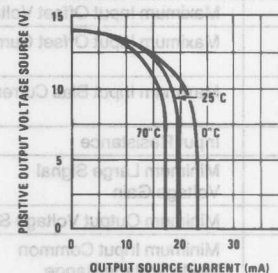
Positive Common-Mode Input Voltage Limit



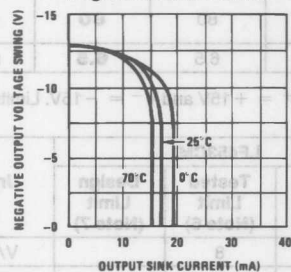
Negative Common-Mode Input Voltage Limit



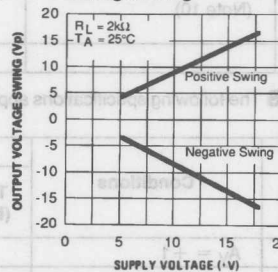
Positive Current Limit



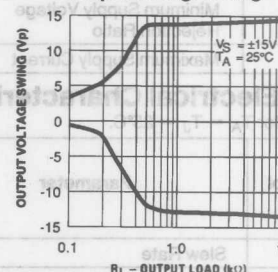
Negative Current Limit



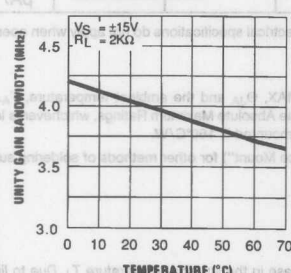
Voltage Swing



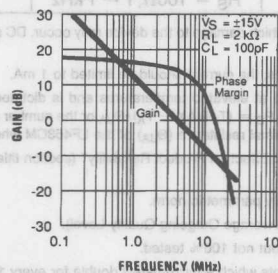
Output Voltage Swing



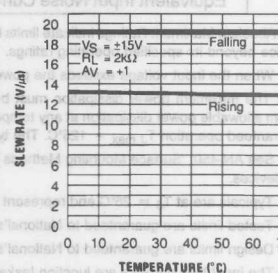
Gain Bandwidth



Bode Plot



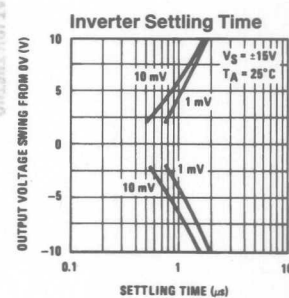
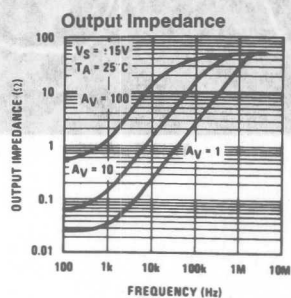
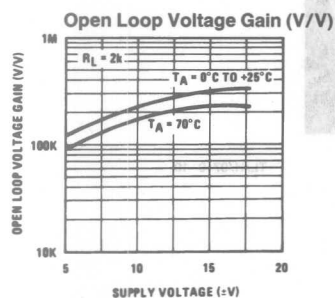
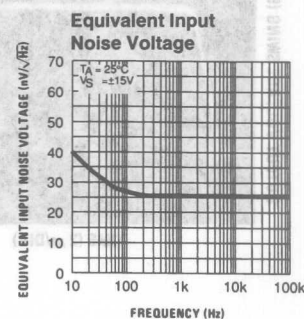
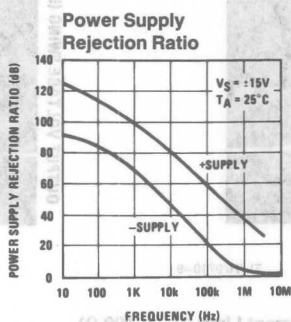
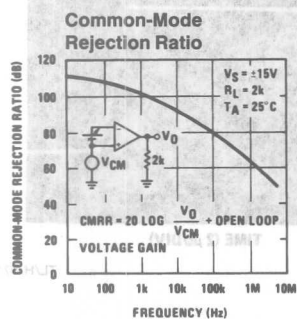
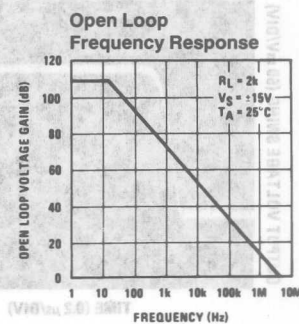
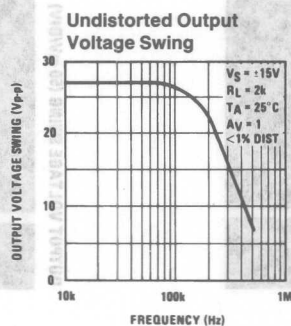
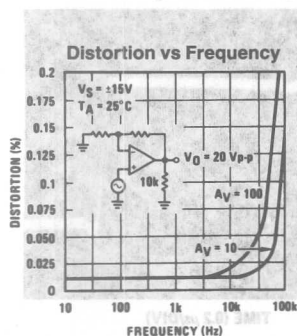
Slew Rate



TL/H/9710-4

Typical Performance Characteristics (Continued)

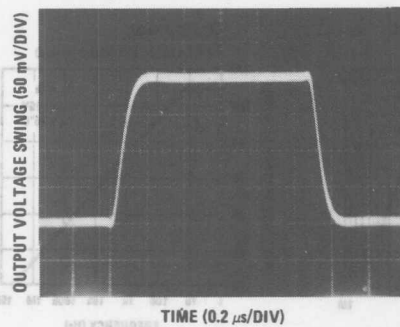
LF453



TL/H/9710-5

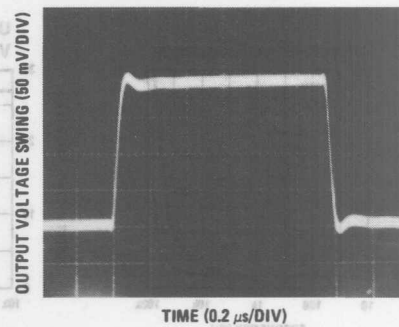
Pulse Response

Small Signal Inverting



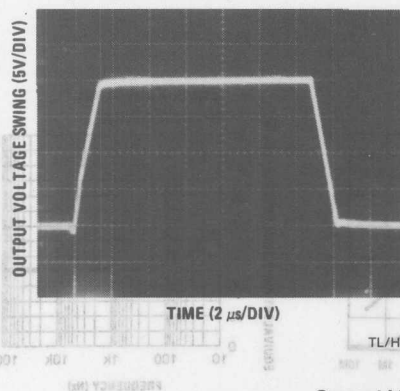
TL/H/9710-6

Small Signal Non-Inverting



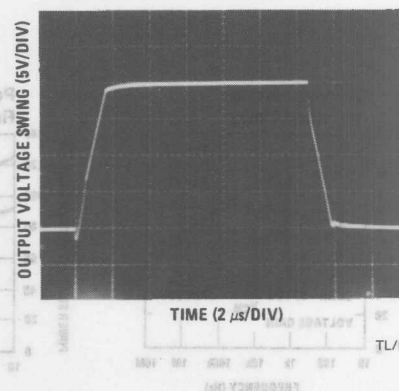
TL/H/9710-7

Large Signal Inverting



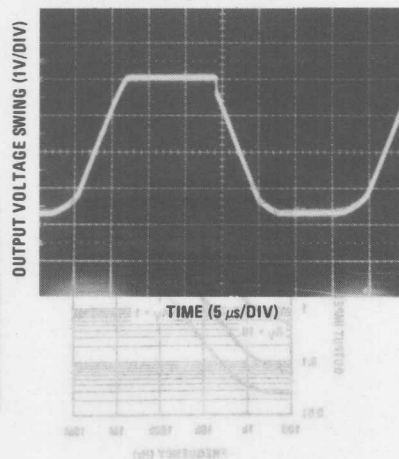
TL/H/9710-8

Large Signal Non-Inverting



TL/H/9710-9

Current Limit ($R_L = 100 \Omega$)



TL/H/9710-10

These devices are op amps with an internally limited input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit with the non-inverting input, or with both inputs, will force the output to a high state, potentially causing a reversal of phase to the output. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 5V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

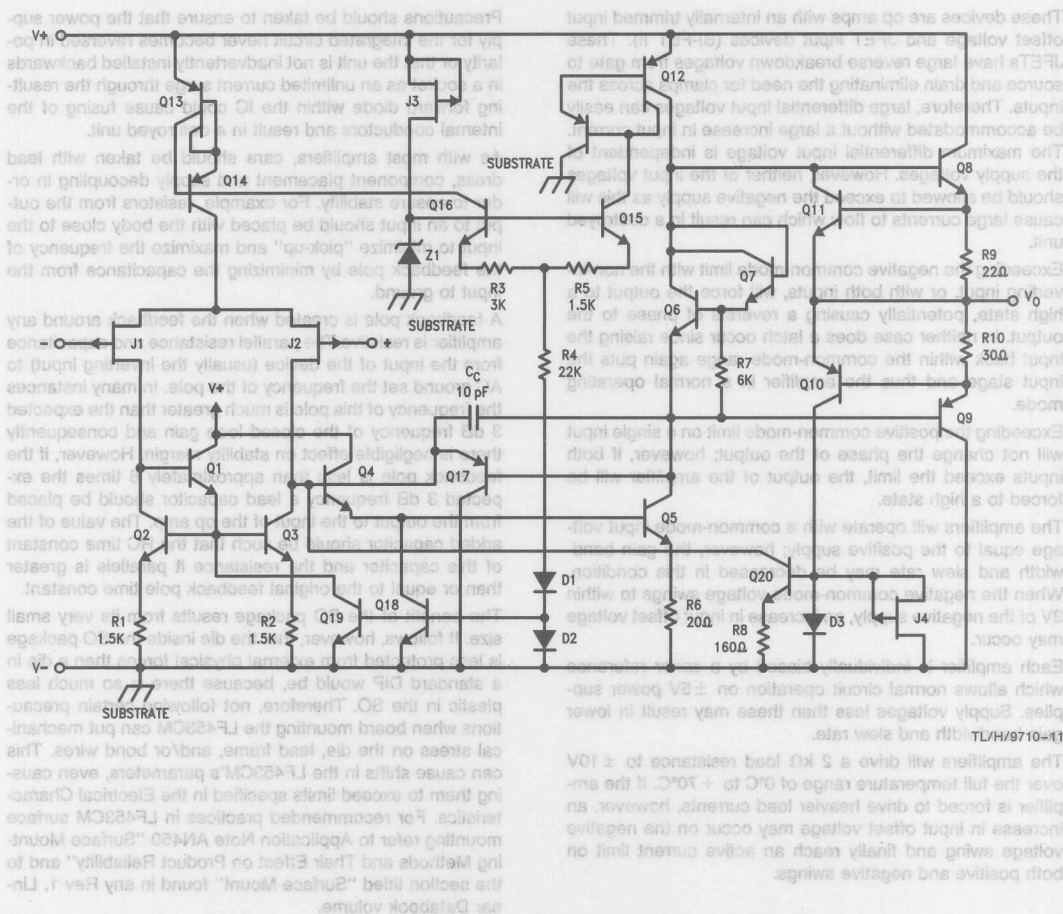
The amplifiers will drive a $2\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range of 0°C to $+70^\circ\text{C}$. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

The benefit of the SO package results from its very small size. It follows, however, that the die inside the SO package is less protected from external physical forces than a die in a standard DIP would be, because there is so much less plastic in the SO. Therefore, not following certain precautions when board mounting the LF453CM can put mechanical stress on the die, lead frame, and/or bond wires. This can cause shifts in the LF453CM's parameters, even causing them to exceed limits specified in the Electrical Characteristics. For recommended practices in LF453CM surface mounting refer to Application Note AN450 "Surface Mounting Methods and Their Effect on Product Reliability" and to the section titled "Surface Mount" found in any Rev 1. Linear Databook volume.



LH0003

Wide Bandwidth Operational Amplifier

General Description

The LH0003/LH0003C is a general purpose operational amplifier which features: slewing rate up to 70 V/ μ s, a gain bandwidth of up to 30 MHz, and high output currents. Other features are:

Features

- Very low offset voltage
- Large output swing

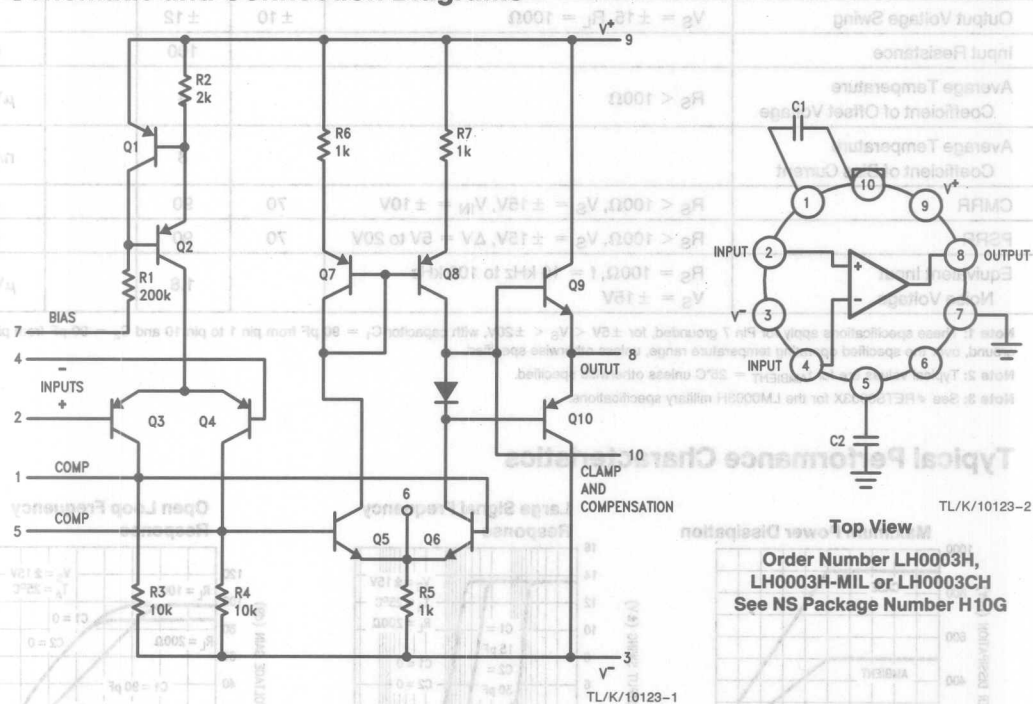
Typically 0.4 mV
> ± 10 V into 100 Ω load

- High CMRR
- Good large signal frequency response

Typically > 90 dB
50 kHz to 400 kHz depending on compensation

The LH0003 is specified for operation over the -55°C to $+125^{\circ}\text{C}$ military temperature range. The LH0003C is specified for operation over the 0°C to $+85^{\circ}\text{C}$ temperature range.

Schematic and Connection Diagrams



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|----------------------------|-----------|
| Supply Voltage | $\pm 20V$ |
| Power Dissipation | See curve |
| Differential Input Voltage | $\pm 7V$ |

| | |
|---------------------------------------|-----------------------------------|
| Input Voltage | Equal to supply |
| Load Current | 120 mA |
| Operating Temperature Range LH0003 | $-55^{\circ}C$ to $+125^{\circ}C$ |
| LH0003C | $0^{\circ}C$ to $+85^{\circ}C$ |
| Storage Temperature Range | $-65^{\circ}C$ to $+150^{\circ}C$ |
| Lead Temperature (Soldering, 10 sec.) | $300^{\circ}C$ |

Electrical Characteristics (Notes 1 & 2)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|----------|----------|-----|-------------------|
| Input Offset Voltage | $R_S < 100\Omega$ | | 0.4 | 3.0 | mV |
| Input Offset Current | | | 0.02 | 0.2 | μA |
| Input Bias Current | | | 0.4 | 2.0 | μA |
| Supply Current | $V_S = \pm 20V$ | | 1.2 | 3 | mA |
| Voltage Gain | $R_L = 100k, V_S = \pm 15V, V_{OUT} = \pm 10V$ | 20 | 70 | | V/mV |
| Voltage Gain | $R_L = 2k, V_S = \pm 15V, V_{OUT} = \pm 10V$ | 15 | 40 | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V, R_L = 100\Omega$ | ± 10 | ± 12 | | V |
| Input Resistance | | | 100 | | k Ω |
| Average Temperature Coefficient of Offset Voltage | $R_S < 100\Omega$ | | 4 | | $\mu V/^{\circ}C$ |
| Average Temperature Coefficient of Bias Current | | | 8 | | nA/ $^{\circ}C$ |
| CMRR | $R_S < 100\Omega, V_S = \pm 15V, V_{IN} = \pm 10V$ | 70 | 90 | | dB |
| PSRR | $R_S < 100\Omega, V_S = \pm 15V, \Delta V = 5V$ to 20V | 70 | 90 | | dB |
| Equivalent Input Noise Voltage | $R_S = 100\Omega, f = 10$ kHz to 100 kHz $V_S = \pm 15V$ | | 1.8 | | μV_{rms} |

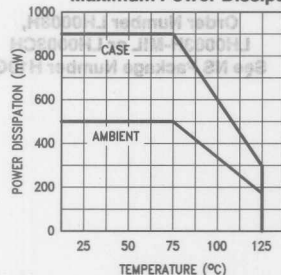
Note 1: These specifications apply for Pin 7 grounded, for $\pm 5V < V_S < \pm 20V$, with capacitor $C_1 = 90$ pF from pin 1 to pin 10 and $C_2 = 90$ pF from pin 5 to ground, over the specified operating temperature range, unless otherwise specified.

Note 2: Typical values are for $T_{AMBIENT} = 25^{\circ}C$ unless otherwise specified.

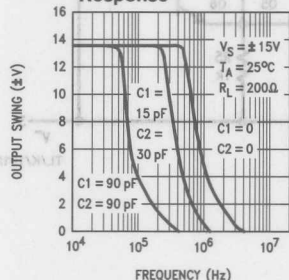
Note 3: See #RETS0003X for the LM0003H military specifications.

Typical Performance Characteristics

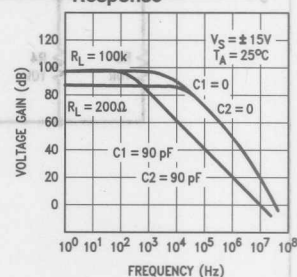
Maximum Power Dissipation



Large Signal Frequency Response



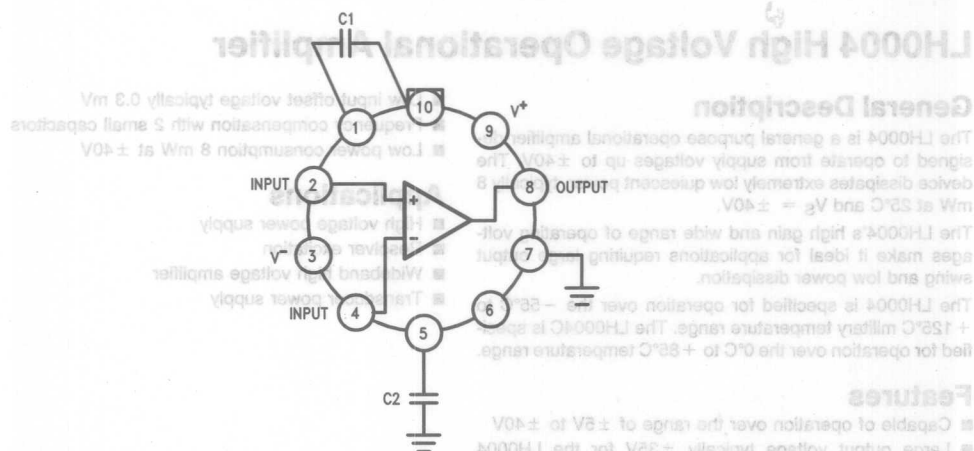
Open Loop Frequency Response



TL/K/10123-5

Typical Applications

High Slew Rate Unity Gain Inverting Amplifier



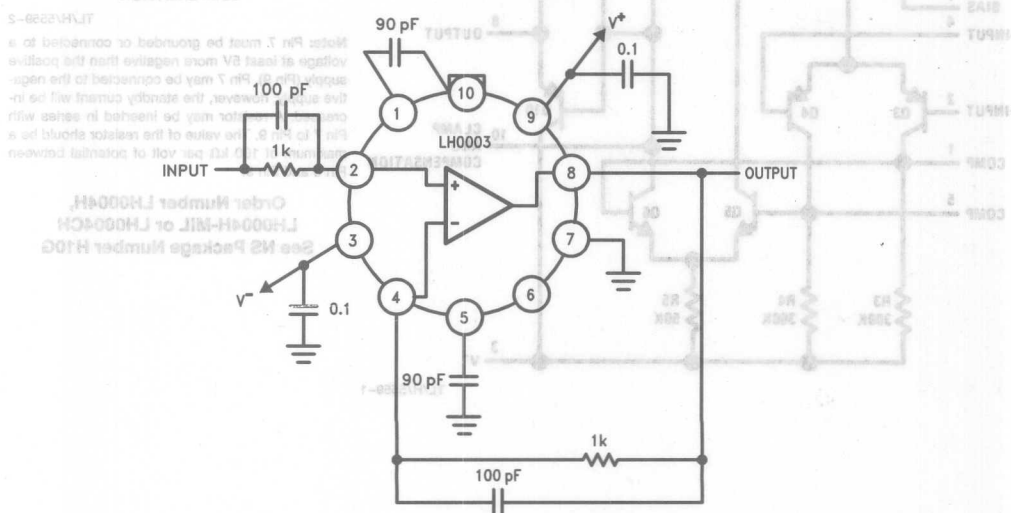
*Previously called NH0003/NH0003C

TL/K/10123-2

Typical Compensation

| Circuit Gain | C ₁ pF | C ₂ pF | Slew Rate R _L > 200Ω, V/μs | Full Output Frequency R _L = 200Ω V _{OUT} = ±10V |
|--------------|-------------------|-------------------|---|--|
| ≥ 40 | 0 | 0 | 70 | 400 |
| ≥ 10 | 5 | 30 | 30 | 350 |
| ≥ 5 | 15 | 30 | 15 | 250 |
| ≥ 2 | 50 | 50 | 5 | 100 |
| ≥ 1 | 90 | 90 | 2 | 50 |

Unity Gain Follower



TL/K/10123-4

LH0004 High Voltage Operational Amplifier

General Description

The LH0004 is a general purpose operational amplifier designed to operate from supply voltages up to $\pm 40V$. The device dissipates extremely low quiescent power, typically 8 mW at $25^{\circ}C$ and $V_S = \pm 40V$.

The LH0004's high gain and wide range of operating voltages make it ideal for applications requiring large output swing and low power dissipation.

The LH0004 is specified for operation over the $-55^{\circ}C$ to $+125^{\circ}C$ military temperature range. The LH0004C is specified for operation over the $0^{\circ}C$ to $+85^{\circ}C$ temperature range.

Features

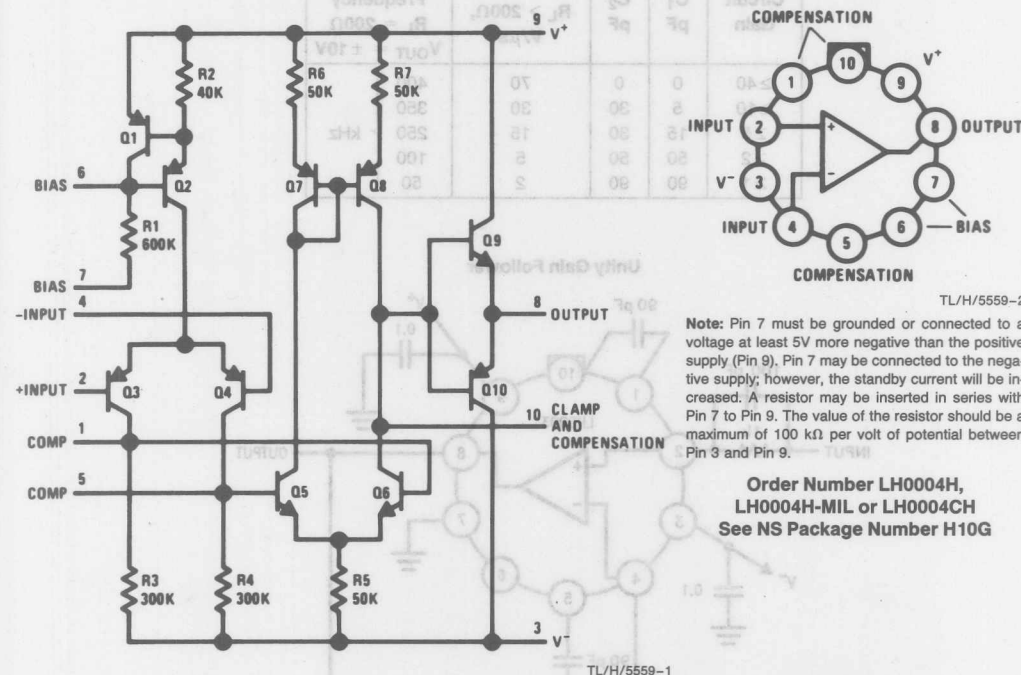
- Capable of operation over the range of $\pm 5V$ to $\pm 40V$
- Large output voltage typically $\pm 35V$ for the LH0004 and $\pm 33V$ for the LH0004C into a 2 k Ω load with $\pm 40V$ supplies

- Low input offset voltage typically 0.3 mV
- Frequency compensation with 2 small capacitors
- Low power consumption 8 mW at $\pm 40V$

Applications

- High voltage power supply
- Resolver excitation
- Wideband high voltage amplifier
- Transducer power supply

Schematic and Connection Diagrams



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 2)

| | |
|-------------------------------|-----------------|
| Supply Voltage | ±45V |
| Power Dissipation (see Curve) | 400 mW |
| Differential Input Voltage | ±7V |
| Input Voltage | Equal to Supply |

Short Circuit Duration

3 sec

Operating Temperature Range

LH0004

−55°C to +125°C

LH0004C

0°C to +85°C

Storage Temperature Range

−65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

260°C

ESD rating to be determined.

Electrical Characteristics (Note 1)

| Parameter | Conditions | LH0004 | | | LH0004C | | | Units |
|---|---|--------|-----|------------|---------|-----|------------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \leq 100\Omega$, $T_A = 25^\circ\text{C}$ $R_S \leq 100\Omega$ | | 0.3 | 1.0 2.0 | | 0.3 | 1.5 3.0 | mV |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 20 | 100 300 | | 30 | 120 300 | nA |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 3 | 20 100 | | 10 | 45 150 | nA |
| Positive Supply Current | $V_S = \pm 40\text{V}$, $T_A = 25^\circ\text{C}$ $V_S = \pm 40\text{V}$ | | 110 | 150 175 | | 110 | 150 175 | μA |
| Negative Supply Current | $V_S = \pm 40\text{V}$, $T_A = 25^\circ\text{C}$ $V_S = \pm 40\text{V}$ | | 80 | 100 135 | | 80 | 100 135 | μA |
| Voltage Gain | $V_S = \pm 40\text{V}$, $R_L = 100\text{k}$, $T_A = 25^\circ\text{C}$ $V_{OUT} = \pm 30\text{V}$ | 30 | 60 | | 30 | 60 | | V/mV |
| | $V_S = \pm 40\text{V}$, $R_L = 100\text{k}$ $V_{OUT} = \pm 30\text{V}$ | 10 | | | 10 | | | V/mV |
| Output Voltage | $V_S = \pm 40\text{V}$, $R_L = 10\text{k}$ | | ±35 | ±30 | | ±33 | ±30 | V |
| CMRR | $V_S = \pm 40\text{V}$, $R_S \leq 5\text{k}$ $V_{IN} = \pm 33\text{V}$ | 70 | 90 | | 70 | 90 | | dB |
| PSRR | $V_S = \pm 40\text{V}$, $R_S \leq 5\text{k}$ $\Delta V = 20\text{V to } 40\text{V}$ | 70 | 90 | | 70 | 90 | | dB |
| Average Temperature Coefficient Offset Voltage | $R_S \leq 100\Omega$ | | 4.0 | | | 4.0 | | $\mu\text{V}/^\circ\text{C}$ |
| Average Temperature Coefficient of Offset Current | | | 0.4 | | | 0.4 | | nA/ $^\circ\text{C}$ |
| Equivalent Input Noise Voltage | $R_S = 100\Omega$, $V_S = \pm 40\text{V}$ $f = 500\text{ Hz to } 5\text{ kHz}$, $T_A = 25^\circ\text{C}$ | | 3.0 | | | 3.0 | | μVrms |

Note 1: These specifications apply for $\pm 5\text{V} \leq V_S \leq \pm 40\text{V}$, Pin 7 grounded, with capacitors $C_1 = 39\text{ pF}$ between Pin 1 and Pin 10, $C_2 = 22\text{ pF}$ between Pin 5 and ground, -55°C to $+125^\circ\text{C}$ for the LH0004, and 0°C to $+85^\circ\text{C}$ for the LH0004C unless otherwise specified.

Note 2: Refer to RETS0004X for LH0004H military specifications.

Typical Applications

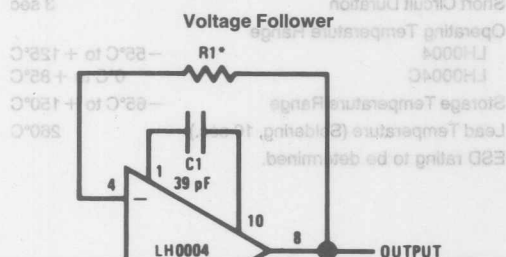
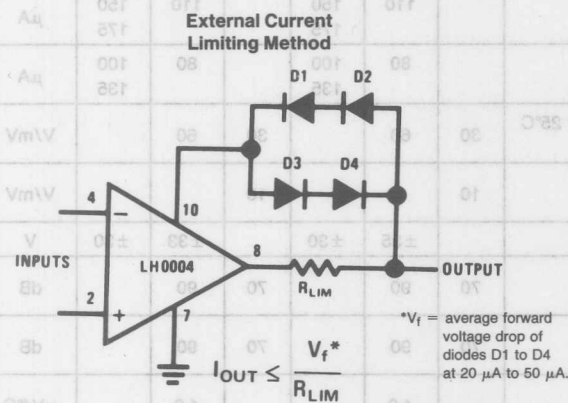


Figure 1 shows a typical application circuit for the AD8421. The circuit includes a differential input stage with two input pins (2 and 7) connected to a common-mode voltage source (V_{cm}) through a 22 pF capacitor (C₂). The output pins (5 and 6) are connected to a load resistor (R_L) and a common-mode voltage source (V_{cm}). The circuit is powered by a 5V supply (V_{DD}) and a ground (GND). The text indicates that the output may be zero or equal to source resistance for minimum offset.

TL/H/5559-3

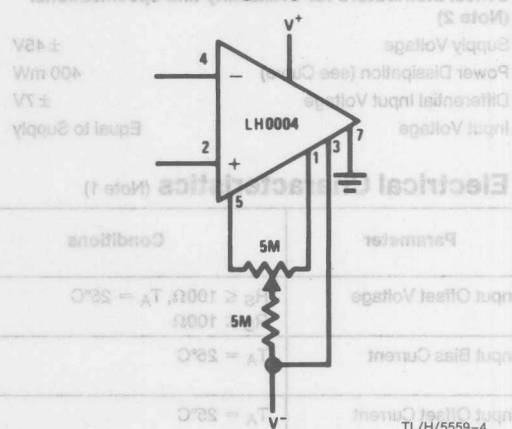


$$I_{OUT} \leq \frac{V_f^*}{R_{LIM}}$$

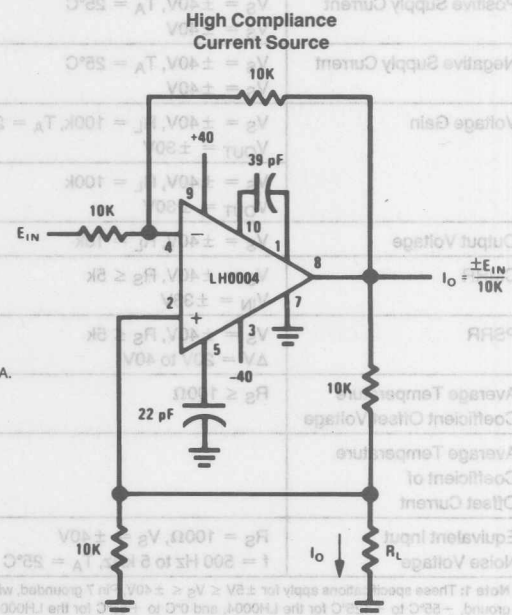
V_f^* = average forward voltage of diodes $D1$ at 20 μA
 TL/H/5559-5

TL/H/5559-5

**Input Offset
Voltage Adjust**

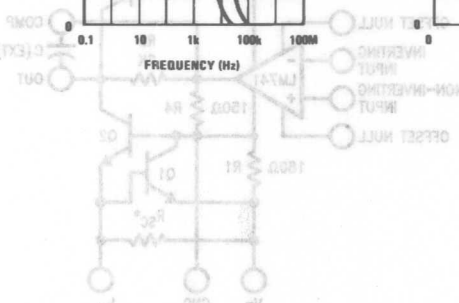
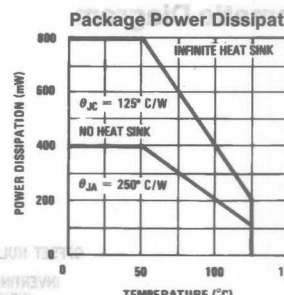
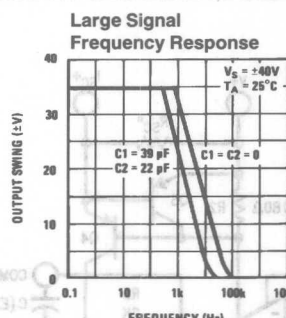
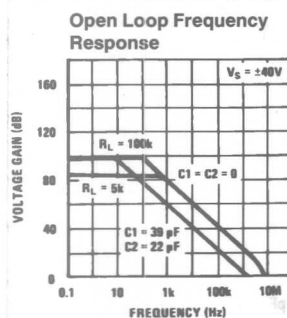
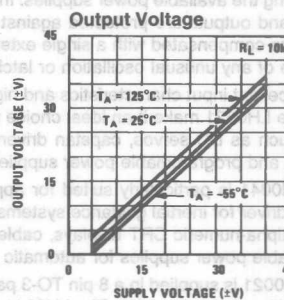
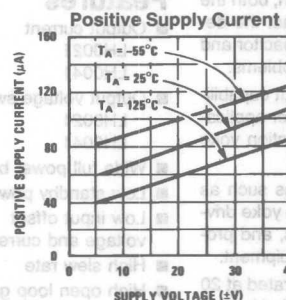
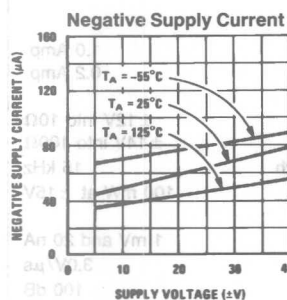
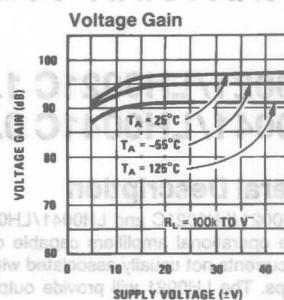
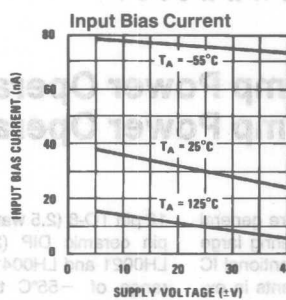
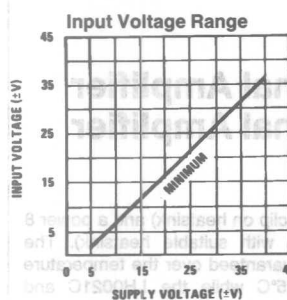


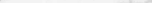
TL/H/5559-4



TL/H/5559-6

Typical Performance Characteristics





National Semiconductor

LH0021/LH0021C 1.0 Amp Power Operational Amplifier
LH0041/LH0041C 0.2 Amp Power Operational Amplifier

General Description

The LH0021/LH0021C and LH0041/LH0041C are general purpose operational amplifiers capable of delivering large output currents not usually associated with conventional IC Op Amps. The LH0021 will provide output currents in excess of one ampere at voltage levels of $\pm 12V$; the LH0041 delivers currents of 200 mA at voltage levels closely approaching the available power supplies. In addition, both the inputs and outputs are protected against overload, the devices are compensated with a single external capacitor and are free of any unusual oscillation or latch-up problems.

The excellent input characteristics and high output capability of the LH0021 make it an ideal choice for power applications such as DC servos, capstan drivers, deflection yoke drivers, and programmable power supplies.

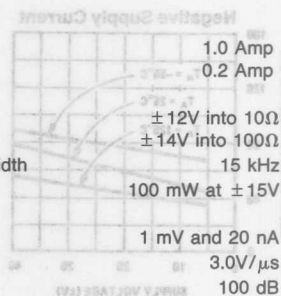
The LH0041 is particularly suited for applications such as torque driver for inertial guidance systems, diddle yoke driver for alpha-numeric CRT displays, cable drivers, and programmable power supplies for automatic test equipment.

The LH0021 is supplied in a 8 pin TO-3 package rated at 20 watts with suitable heatsink. The LH0041 is supplied in both

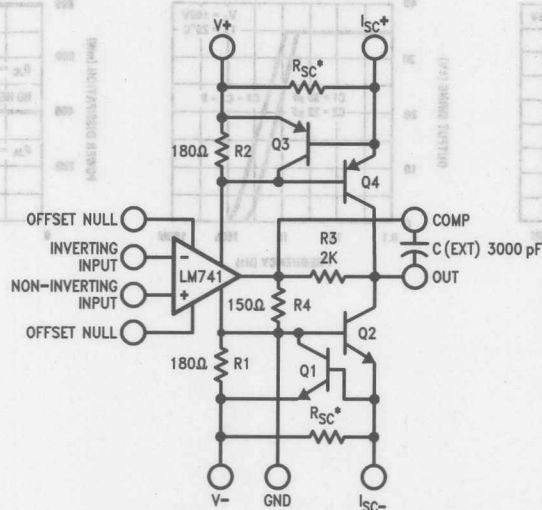
12 pin TO-8 (2.5 watts with clip on heatsink) and a power 8 pin ceramic DIP (2 watts with suitable heatsink). The LH0021 and LH0041 are guaranteed over the temperature range of -55°C to $+125^{\circ}\text{C}$ while the LH0021C and LH0041C are guaranteed from -25°C to $+85^{\circ}\text{C}$.

Features

- Output current
LH0021
LH0041
- Output voltage swing
LH0021
LH0041
- Wide full power band
- Low standby power
- Low input offset
voltage and current
- High slew rate
- High open loop gain



Schematic Diagram



*R_{SC} external on "G" and "K" packages. R_{SC} internal on "J" package. Offset Null connections available only on "G" package.

TL/H/9298-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | | | | | | | | | |
|------------------------------|-----|-----|-----|------------|-----|-----|-----|-----|-----|
| Supply Voltage | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min |
| Power Dissipation | 0.8 | 3.0 | 1.0 | See Curves | | | | | |
| Differential Input Voltage | | 3.0 | | ±30V | | | | | |
| Input Voltage (Note 1) | | | 3 | ±15V | | | | | |
| Peak Output Current (Note 2) | | | 5 | 2.0 Amps | | | | | |
| LH0021/LH0021C | | | 15 | 0.5 Amps | | | | | |
| LH0041/LH0041C | | | 20 | | | | | | |

| | |
|--|-----------------|
| Output Short Circuit Duration (Note 3) | Continuous |
| Operating Temperature Range | |
| LH0021/LH0041 | −55°C to +125°C |
| LH0021C/LH0041C | −25°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |
| ESD rating to be determined. | |

DC Electrical Characteristics for LH0021/LH0021C (Note 4)

| Parameter | Conditions | Limits | | | | | | Units |
|---|--|---|----------------|------------|----------------------|----------------------|------------|------------------------------|
| | | LH0021 | | | LH0021C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S < 100\Omega$, $T_C = 25^\circ\text{C}$ $R_S < 100\Omega$ | | 1.0 | 3.0 5.0 | | 3.0 | 6.0 7.5 | mV mV |
| Voltage Drift with Temperature | $R_S < 100\Omega$ | | 3 | 25 | | 5 | 30 | $\mu\text{V}/^\circ\text{C}$ |
| Offset Voltage Drift with Time | | | 5 | | | 5 | | $\mu\text{V}/\text{week}$ |
| Offset Voltage Change with Output Power | | | 5 | 15 | | 5 | 20 | $\mu\text{V}/\text{W}$ |
| Input Offset Current | $T_C = 25^\circ\text{C}$ | | 30 | 100 300 | | 50 | 200 500 | nA nA |
| Offset Current Drift with Temperature | | | 0.1 | 1.0 | | 0.2 | 1.0 | $\text{nA}/^\circ\text{C}$ |
| Offset Current Drift with Time | | | 2 | | | 2 | | nA/week |
| Input Bias Current | $T_C = 25^\circ\text{C}$ | | 100 | 300 1.0 | | 200 | 500 1.0 | nA μA |
| Input Resistance | $T_C = 25^\circ\text{C}$ | 0.3 | 1.0 | | 0.3 | 1.0 | | $\text{M}\Omega$ |
| Input Capacitance | | | 3 | | | 3 | | pF |
| Common Mode Rejection Ratio | $R_S 100\Omega$, $\Delta V_{\text{CM}} = \pm 10\text{V}$ | 70 | 90 | | 70 | 90 | | dB |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | ± 12 | | | ± 12 | | | V |
| Power Supply Rejection Ratio | $R_S \leq 100\Omega$, $\Delta V_S = \pm 10\text{V}$ | 80 | 96 | | 70 | 90 | | dB |
| Voltage Gain | $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$ $R_L = 1\text{ k}\Omega$, $T_C = 25^\circ\text{C}$ $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$ $R_L = 100\Omega$ | 100 25 | 200 | | 100 20 | 200 | | V/mV V/mV |
| | $V_S = \pm 15\text{V}$, $R_L = 100\Omega$ $V_S = \pm 15\text{V}$, $R_L = 10\Omega$, $T_C = 25^\circ\text{C}$ | ± 13.5 ± 11.0 | 14 ± 12 | | ± 13 ± 10 | ± 14 ± 12 | | V V |
| | Output Short Circuit Current | $V_S = \pm 15\text{V}$, $T_C = 25^\circ\text{C}$, $R_{\text{SC}} = 0.5\Omega$ | 0.8 | 1.2 | 1.6 | 0.8 | 1.2 | 1.6 |
| Power Supply Current | $V_S = \pm 15\text{V}$, $V_{\text{OUT}} = 0$ | | 2.5 | 3.5 | | 3.0 | 4.0 | mA |
| Power Consumption | $V_S = \pm 15\text{V}$, $V_{\text{OUT}} = 0$ | | 75 | 105 | | 90 | 120 | mW |

AC Electrical Characteristics for LH0021/LH0021C ($T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $C_C = 3000\text{ pF}$)

| Parameter | Conditions | Limits | | | | | | Units |
|---------------------------------|--|--------|------|-----|---------|------|-----|-------------|
| | | LH0021 | | | LH0021C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate | $A_V = +1, R_L = 100\Omega$ | 0.8 | 3.0 | | 1.0 | 3.0 | | V/ μ s |
| Power Bandwidth | $R_L = 100\Omega$ | | 20 | | | 20 | | kHz |
| Small Signal Transient Response | | | 0.3 | 1.0 | | 0.3 | 1.5 | μ s |
| Small Signal Overshoot | | | 5 | 20 | | 10 | 30 | % |
| Settling Time (0.1%) | $\Delta V_{IN} = 10V, A_V = +1$ | | 4 | | | 4 | | μ s |
| Overload Recovery Time | | | 3 | | | 3 | | μ s |
| Harmonic Distortion | $f = 1\text{ kHz}, P_O = 0.5W$ | | 0.2 | | | 0.2 | | % |
| Input Noise Voltage | $R_s = 50\Omega, B.W. = 10\text{ Hz to }10\text{ kHz}$ | | 5 | | | 5 | | μ V/rms |
| Input Noise Current | $B.W. = 10\text{ Hz to }10\text{ kHz}$ | | 0.05 | | | 0.05 | | nA/rms |

| Parameter | Conditions | Limits | | | | | | Units |
|---|--|----------|-----|------------|----------|----------|------------|------------------------------|
| | | LH0041 | | | LH0041C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S < 100\Omega$, $T_A = 25^\circ\text{C}$ $R_S < 100\Omega$ | 1.0 | 3.0 | 5.0 | | 3.0 | 6.0 | mV mV |
| Voltage Drift with Temperature | $R_S < 100\Omega$ | | 3 | | | 5 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset Voltage Drift with Time | | | 5 | | | 5 | | $\mu\text{V}/\text{week}$ |
| Offset Voltage Change with Output Power | | | 15 | | | 15 | | $\mu\text{V}/\text{W}$ |
| Offset Voltage Adjustment Range | (Note 5) | | 20 | | | 20 | | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 30 | 100 300 | | 50 | 200 500 | nA nA |
| Offset Current Drift with Temperature | | | 0.1 | 1.0 | | 0.2 | 1.0 | $\text{nA}/^\circ\text{C}$ |
| Offset Current Drift with Time | | | 2 | | | 2 | | nA/week |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 100 | 300 1.0 | | 200 | 500 1.0 | nA μA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 0.3 | 1.0 | | 0.3 | 1.0 | | $\text{M}\Omega$ |
| Input Capacitance | | | 3 | | | 3 | | pF |
| Common Mode Rejection Ratio | $R_S 100\Omega$, $\Delta V_{\text{CM}} = \pm 10\text{V}$ | 70 | 90 | | 70 | 90 | | dB |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | +12 | | | +12 | | | V |
| Power Supply Rejection Ratio | $R_S \leq 100\Omega$, $\Delta V_S = \pm 10\text{V}$ | 80 | 96 | | 70 | 90 | | dB |
| Voltage Gain | $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$ $R_L = 1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ $V_S = \pm 15\text{V}$, $V_O = \pm 10\text{V}$ $R_L = 100\Omega$ | 100 | 200 | | 100 | 200 | | V/mV V/mV |
| Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 100\Omega$ | ± 13 | 14 | | ± 13 | ± 14 | | V |
| Output Short Circuit Current | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ (Note 6) | | 200 | 300 | | 200 | 300 | mA |
| Power Supply Current | $V_S = \pm 15\text{V}$, $V_{\text{OUT}} = 0$ | | 2.5 | 3.5 | | 3.0 | 4.0 | mA |
| Power Consumption | $V_S = \pm 15\text{V}$, $V_{\text{OUT}} = 0$ | | 75 | 105 | | 90 | 120 | mW |

AC Electrical Characteristics for LH0041/LH0041C ($T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $C_C = 3000\text{ pF}$)

| Parameter | Conditions | Limits | | | | | | Units |
|---------------------------------|--|--------|------|-----|---------|------|-----|-------------------|
| | | LH0041 | | | LH0041C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate | $A_V = +1, R_L = 100\Omega$ | 1.5 | 3.0 | | 1.0 | 3.0 | | V/ μ s |
| Power Bandwidth | $R_L = 100\Omega$ | | 20 | | | 20 | | kHz |
| Small Signal Transient Response | | | 0.3 | 1.0 | | 0.3 | 1.5 | μ s |
| Small Signal Overshoot | | | 5 | 20 | | 10 | 30 | % |
| Settling Time (0.1%) | $\Delta V_{IN} = 10V, A_V = +1$ | | 4 | | | 4 | | μ s |
| Overload Recovery Time | | | 3 | | | 3 | | μ s |
| Harmonic Distortion | $f = 1\text{ kHz}, P_O = 0.5W$ | | 0.2 | | | 0.2 | | % |
| Input Noise Voltage | $R_s = 50\Omega, \text{B.W.} = 10\text{ Hz to } 10\text{ kHz}$ | | 5 | | | 5 | | $\mu\text{V/rms}$ |
| Input Noise Current | $\text{B.W.} = 10\text{ Hz to } 10\text{ kHz}$ | | 0.05 | | | 0.05 | | nA/rms |

Note 1: Rating applies for supply voltages above $\pm 15\text{V}$. For supplies less than $\pm 15\text{V}$, rating is equal to supply voltage.

Note 2: Rating applies for LH0041G and LH0021K with $R_{\text{SC}} = 0\Omega$.

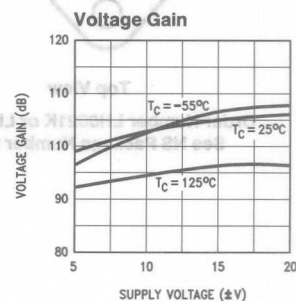
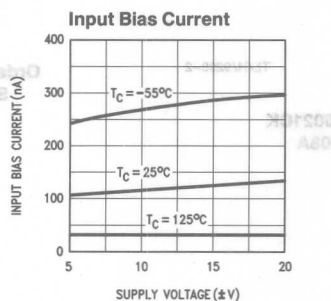
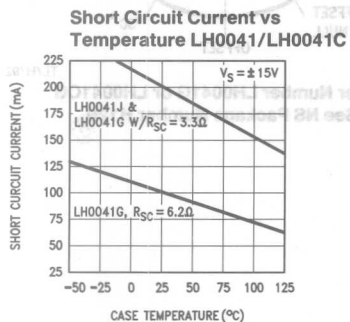
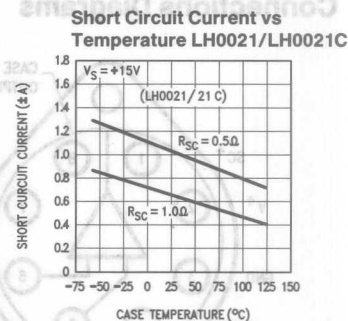
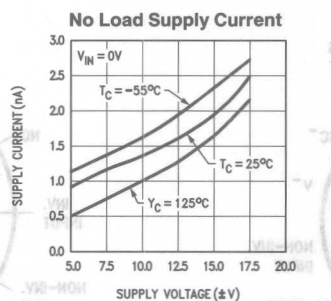
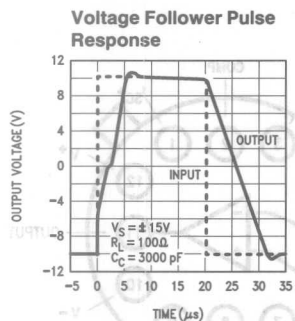
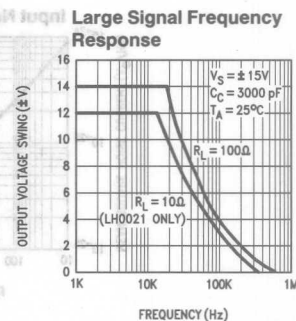
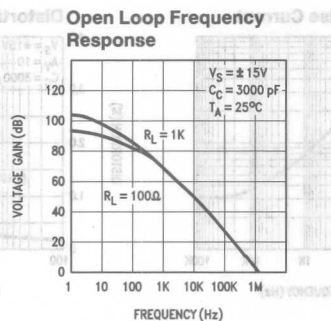
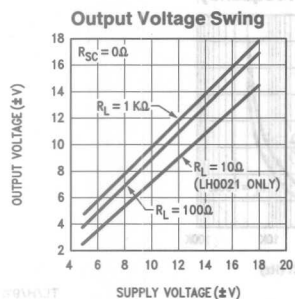
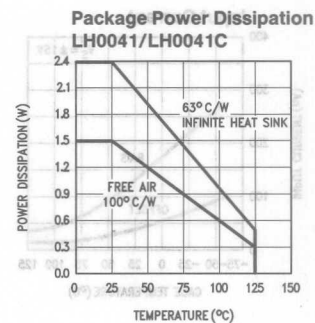
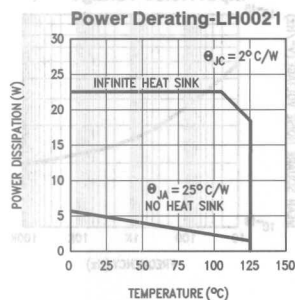
Note 3: Rating applies as long as package power rating is not exceeded.

Note 4: Specifications apply for $\pm 5\text{V} \leq V_S \leq 18\text{V}$, and $-55^\circ\text{C} \leq T_C \leq 125^\circ\text{C}$ for LH0021K and LH0041G, and $-25^\circ\text{C} \leq T_C \leq +85^\circ\text{C}$ for LH0021CK, LH0041CG and LH0041CJ unless otherwise specified. Typical values are for 25°C only.

Note 5: TO-8 "G" packages only.

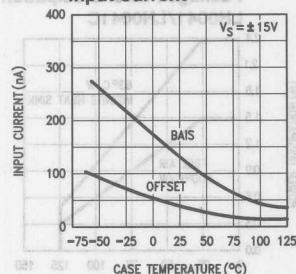
Note 6: Rating applies for "J" DIP package and for TO-8 "G" package with $R_{\text{SC}} = 3.3\text{ ohms}$.

Note 7: See Typical Performance Characteristics.

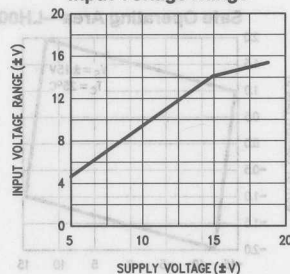


Typical Performance Characteristics (Continued)

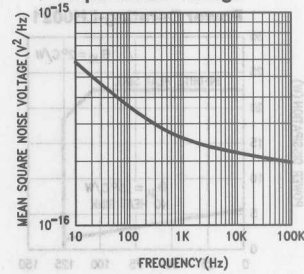
Input Current



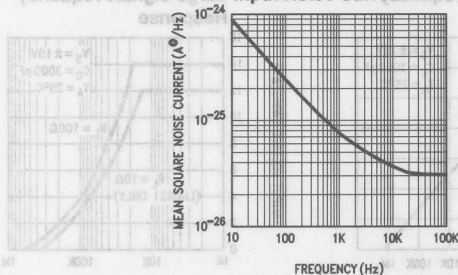
Input Voltage Range



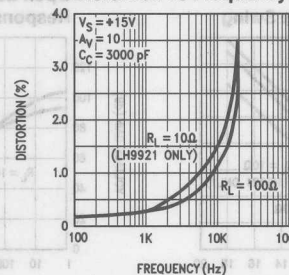
Input Noise Voltage



Input Noise Current

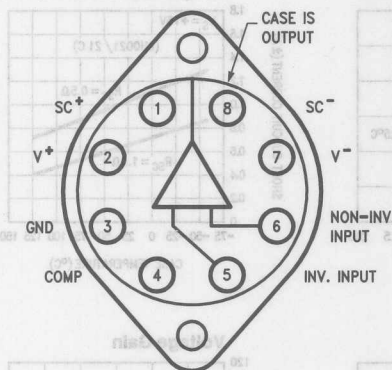


Distortion vs Frequency



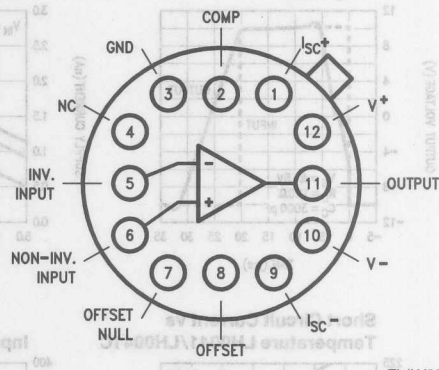
TL/H/9298-7

Connections Diagrams



Top View

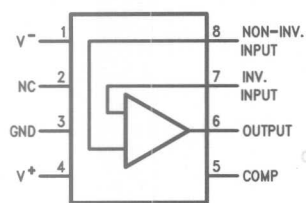
Order Number LH0021K or LH0021CK
 See NS Package Number K08A



Order Number LH0041G or LH0041CG
 See NS Package Number H12B

TL/H/9298-3

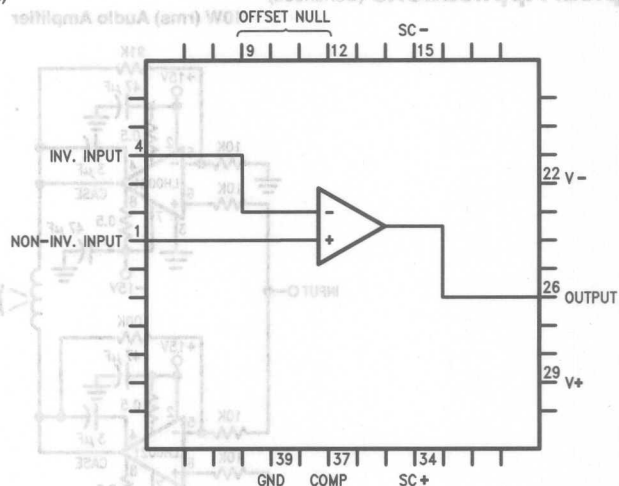
Connection Diagrams (Continued)



TL/H/9298-4

Order Number LH0041CJ
See NS Package Number HY08A

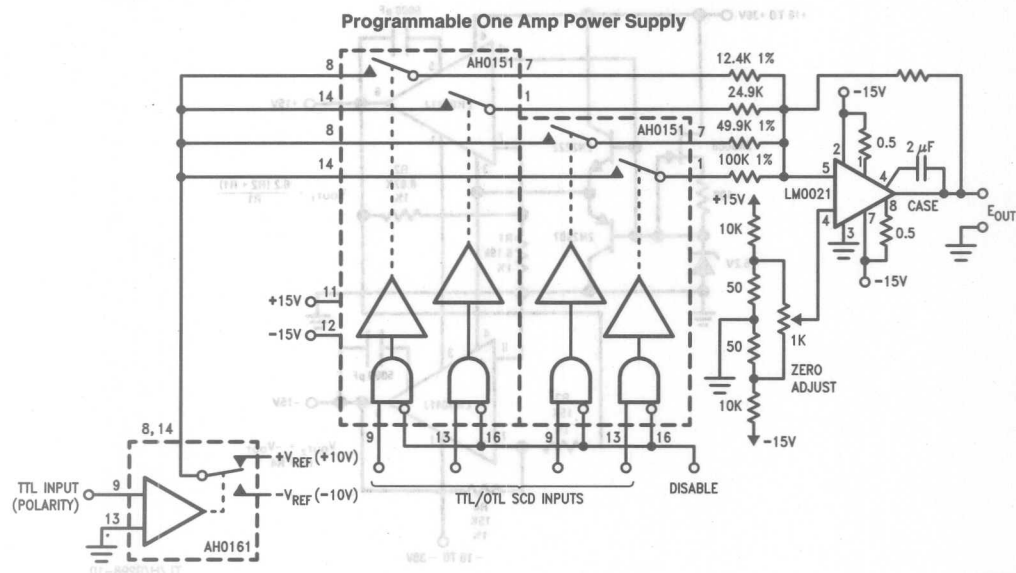
Top View



TL/H/9298-5

Order Number LH0041E
See NS Package Number E48A

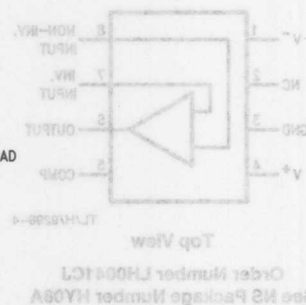
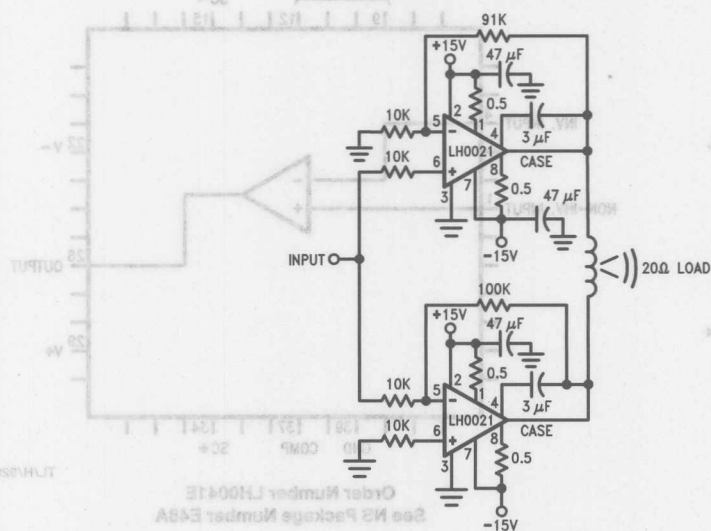
Typical Applications



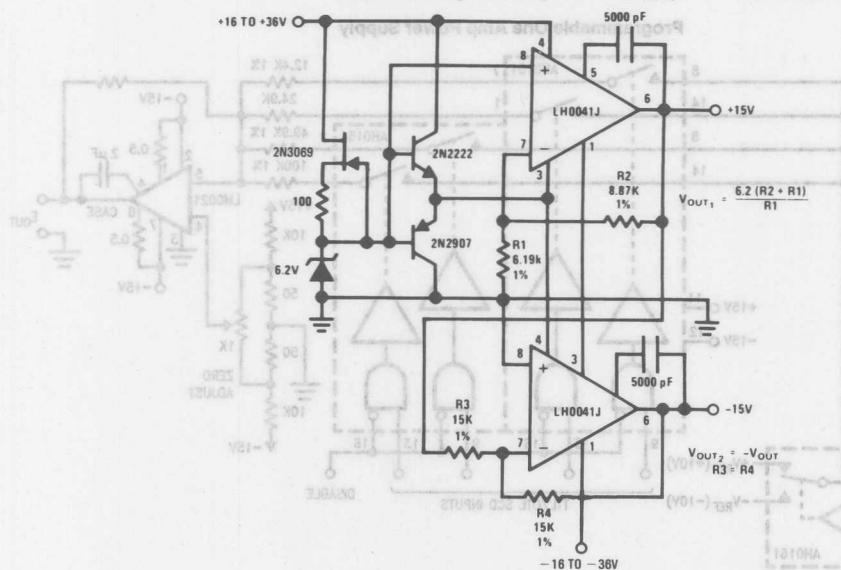
TL/H/9298-8

Typical Applications (Continued)

10W (rms) Audio Amplifier

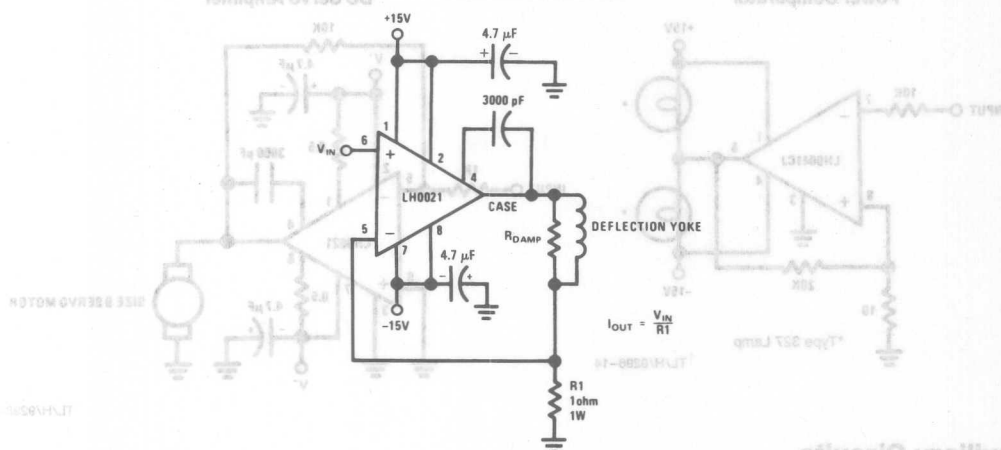


Dual Tracking One Amp Power Supply

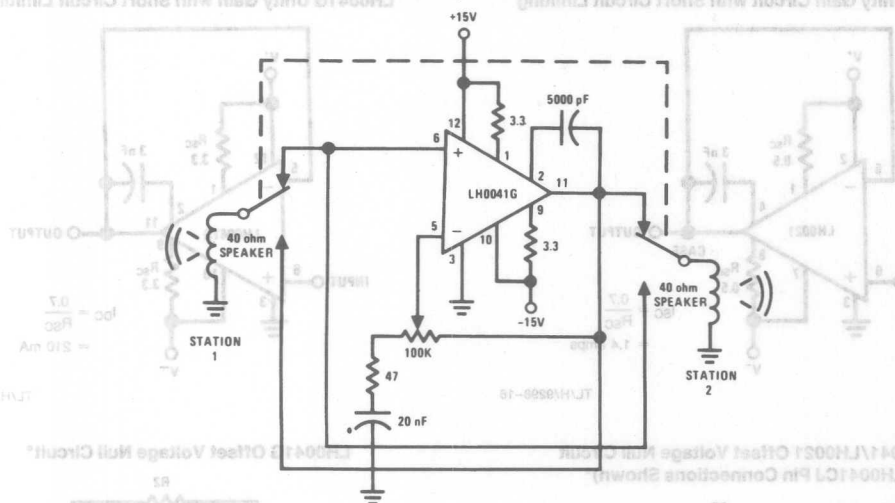


Typical Applications (Continued)

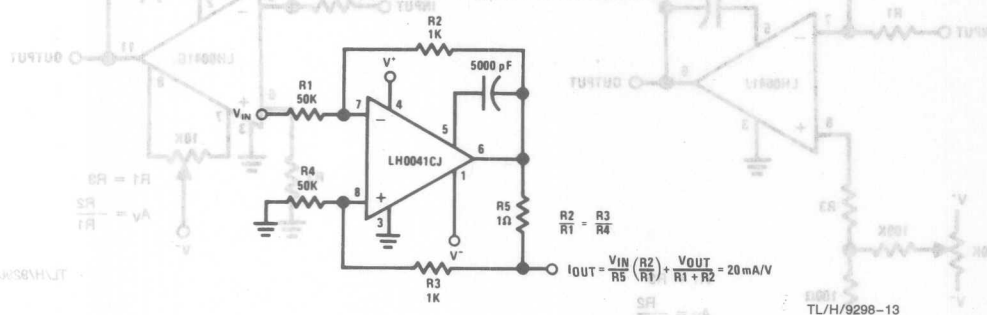
CRT Deflection Yoke Driver

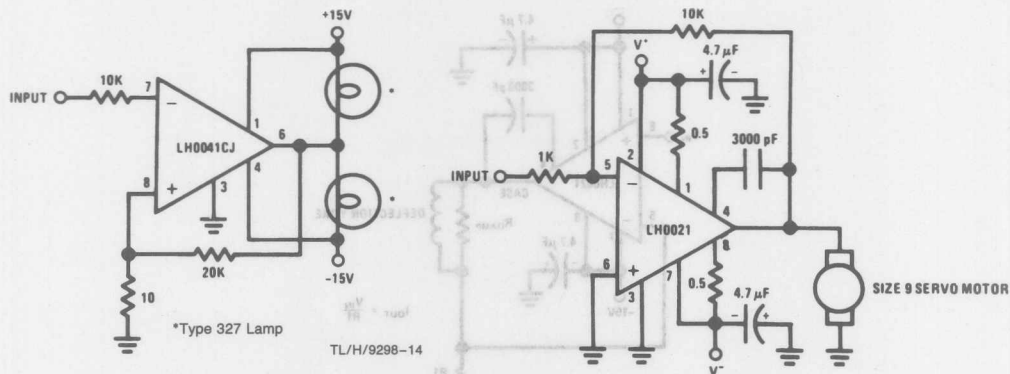


Two Way Intercom



Programmable High Current Source/Sink

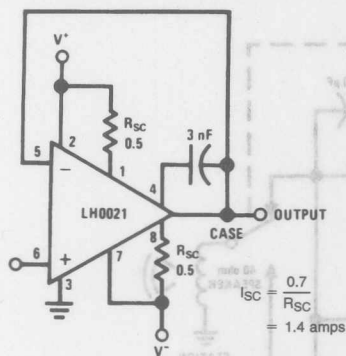




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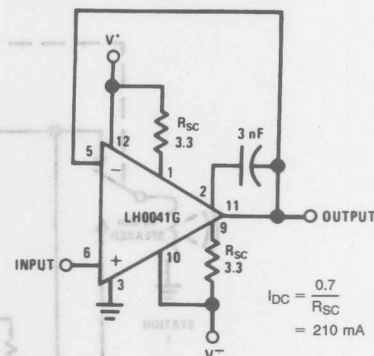
Auxiliary Circuits

LH0021 Unity Gain Circuit with Short Circuit Limiting



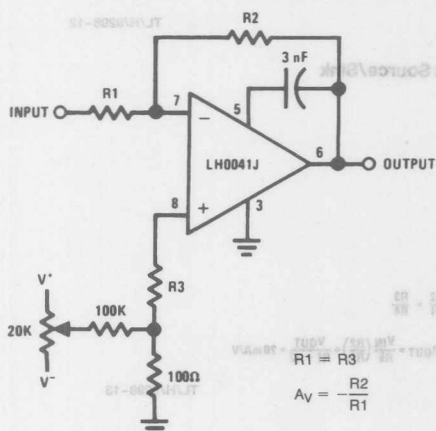
TL/H/9298-16

LH0041G Unity Gain with Short Circuit Limiting



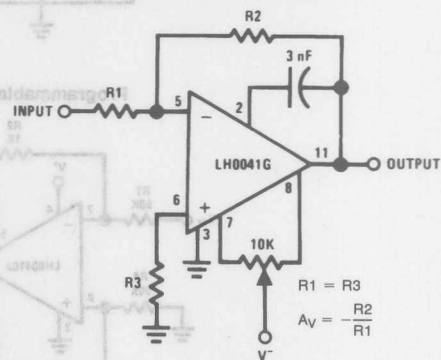
TL/H/9298-17

LH0041/LH0021 Offset Voltage Null Circuit
(LH0041CJ Pin Connections Shown)*



TL/H/9298-18

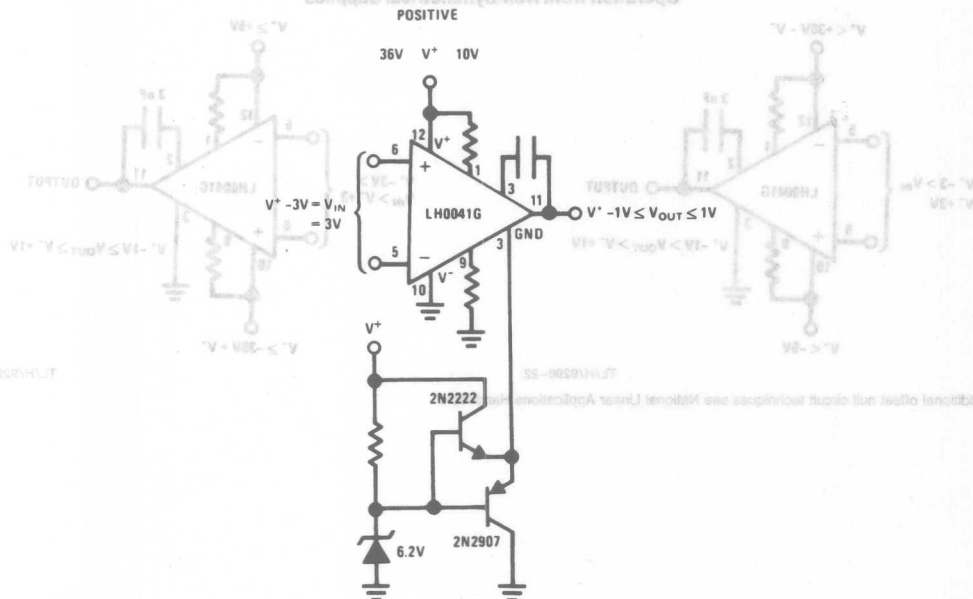
LH0041G Offset Voltage Null Circuit*



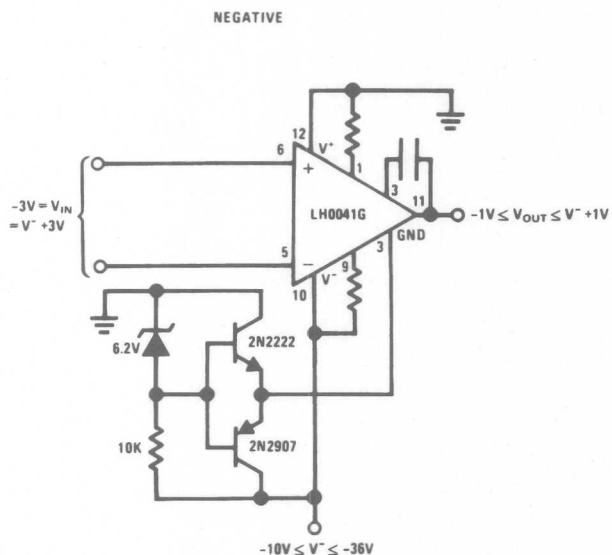
TL/H/9298-19

Auxiliary Circuits (Continued)

Operation from Single Supplies



TL/H/9298-20

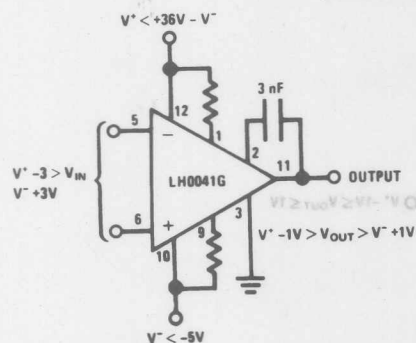


TL/H/9298-21

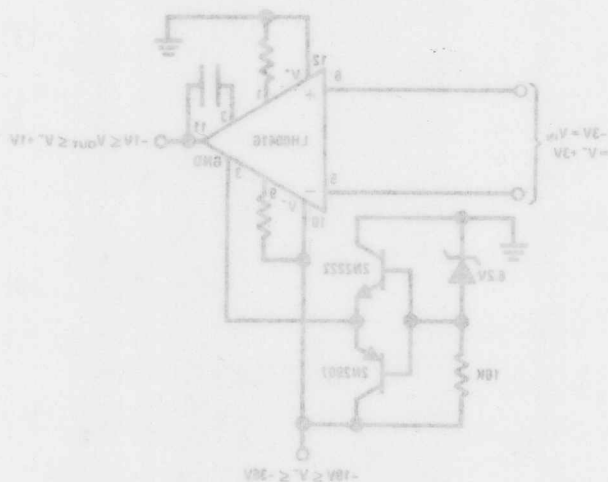
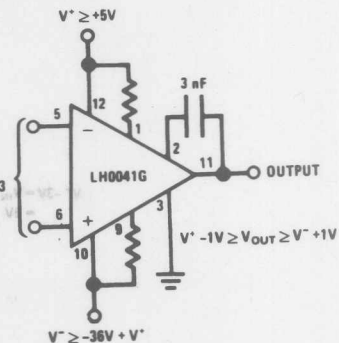
LH0021/LH0021C/LH0041/LH0041C

Auxiliary Circuits (Continued)

Operation from Non-Symmetrical Supplies



*For additional offset null circuit techniques see National Linear Applications Handbook.



LH0024 High Slew Rate Operational Amplifier

General Description

The LH0024/LH0024C is a very wide bandwidth, high slew rate operational amplifier intended to fulfill a wide variety of high speed applications such as buffers to A to D and D to A converters and high speed comparators. The device exhibits useful gain in excess of 50 MHz making it possible to use in video applications requiring higher gain accuracy than is usually associated with such amplifiers.

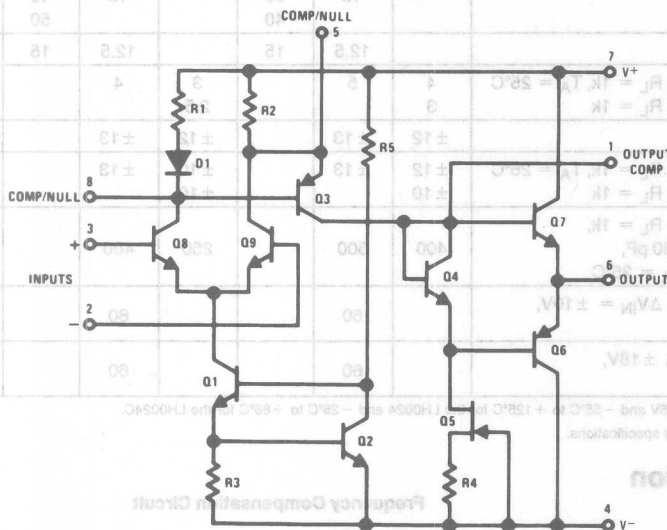
The LH0024/LH0024C's combination of wide bandwidth and high slew rate make it an ideal choice for a variety of high speed applications including active filters, oscillators, and comparators as well as many high speed general purpose applications.

The LH0024 is guaranteed over the temperature range -55°C to $+125^{\circ}\text{C}$, whereas the LH0024C is guaranteed -25°C to $+85^{\circ}\text{C}$.

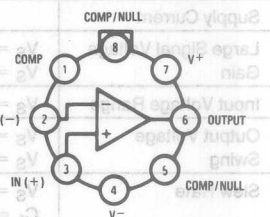
Features

- Very high slew rate—500 V/ μs at $A_V = +1$
- Wide small signal bandwidth—70 MHz
- Wide large signal bandwidth—15 MHz
- High output swing— $\pm 12\text{V}$ into $1\text{k}\Omega$
- Low input offset—2 mV
- Pin compatible with standard IC op amps

Schematic and Connection Diagrams



Metal Can Package



Top View

Note: For heat sink use Thermalloy 2230-5 series.

Order Number LH0024H,
LH0024H-MIL or LH0024CH
See NS Package Number H08B

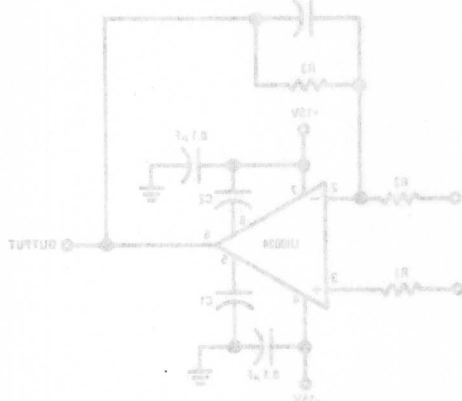


TABLE I

| Loop Gain | C_1 | C_2 | C_3 |
|-----------|-------|-------|-------|
| 100 | 0 | 0 | 0 |
| 50 | 0 | 0 | 0 |
| 10 | 0 | 20 pF | 1 pF |
| 1 | 30 pF | 30 pF | 3 pF |

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 2)

Supply Voltage $\pm 18V$
 Input Voltage Equal to Supply
 Differential Input Voltage $\pm 5V$
 Power Dissipation 600 mW

Lead Temperature (Soldering, 10 sec.)

ESD rating to be determined.

260°C

Operating Temperature Range

LH0024 -55°C to $+125^{\circ}\text{C}$
 LH0024C -25°C to $+85^{\circ}\text{C}$

DC Electrical Characteristics (Note 1)

| Parameter | Conditions | LH0024 | | | LH0024C | | | Units |
|---|---|----------|----------|------|----------|----------|------|--------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S = 50\Omega$, $T_A = 25^{\circ}\text{C}$ | | 2.0 | 4.0 | | 5.0 | 8.0 | mV |
| | $R_S = 50\Omega$ | | | 6.0 | | | 10.0 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $V_S = \pm 15V$, $R_S = 50\Omega$ -55°C to 125°C | | -20 | | | -25 | | $\mu\text{V}/^{\circ}\text{C}$ |
| Input Offset Current | $T_A = 25^{\circ}\text{C}$ | | 2.0 | 5.0 | | 4.0 | 15.0 | μA |
| | | | | 10.0 | | | 20.0 | μA |
| Input Bias Current | $T_A = 25^{\circ}\text{C}$ | | 15 | 30 | | 18 | 40 | μA |
| | | | | 40 | | | 50 | μA |
| Supply Current | | | 12.5 | 15 | | 12.5 | 15 | mA |
| | | | | | | | | |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $R_L = 1k$, $T_A = 25^{\circ}\text{C}$ | 4 | 5 | | 3 | 4 | | V/mV |
| | $V_S = \pm 15V$, $R_L = 1k$ | 3 | | | 2.5 | | | V/mV |
| Input Voltage Range | $V_S = \pm 15V$ | ± 12 | ± 13 | | ± 12 | ± 13 | | V |
| Output Voltage Swing | $V_S = \pm 15V$, $R_L = 1k$, $T_A = 25^{\circ}\text{C}$ | ± 12 | ± 13 | | ± 10 | ± 13 | | V |
| | $V_S = \pm 15V$, $R_L = 1k$ | ± 10 | | | ± 10 | | | V |
| Slew Rate | $V_S = \pm 15V$, $R_L = 1k$, $C_1 = C_2 = 30\text{ pF}$, $A_V = +1$, $T_A = 25^{\circ}\text{C}$ | 400 | 500 | | 250 | 400 | | V/ μs |
| | | | | | | | | |
| Common-Mode Rejection Ratio | $V_S = \pm 15V$, $\Delta V_{IN} = \pm 10V$, $R_S = 50\Omega$ | | 60 | | | 60 | | dB |
| Power Supply Rejection Ratio | $\pm 5V \leq V_S \leq \pm 18V$, $R_S = 50\Omega$ | | 60 | | | 60 | | dB |

Note 1: These specifications apply for $V_S = \pm 15V$ and -55°C to $+125^{\circ}\text{C}$ for the LH0024 and -25°C to $+85^{\circ}\text{C}$ for the LH0024C.

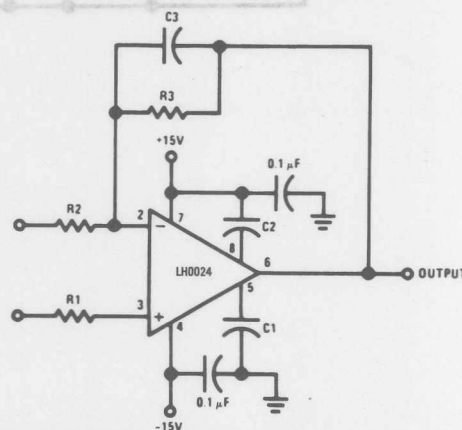
Note 2: Refer to RETS0024 for LH0024H military specifications.

Frequency Compensation

TABLE I

| Closed Loop Gain | C_1 | C_2 | C_3 |
|------------------|-------|-------|-------|
| 100 | 0 | 0 | 0 |
| 20 | 0 | 0 | 0 |
| 10 | 0 | 20 pF | 1 pF |
| 1 | 30 pF | 30 pF | 3 pF |

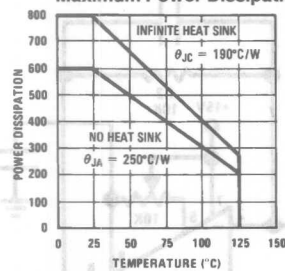
Frequency Compensation Circuit



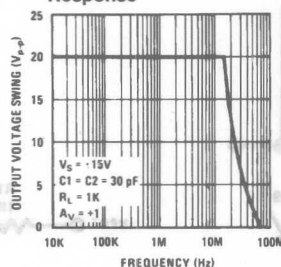
TL/K/5552-6

Typical Performance Characteristics

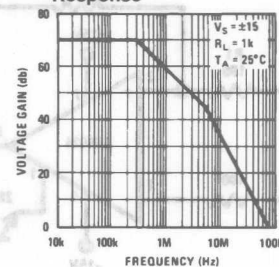
Maximum Power Dissipation



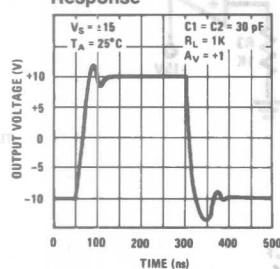
Large Signal Frequency Response



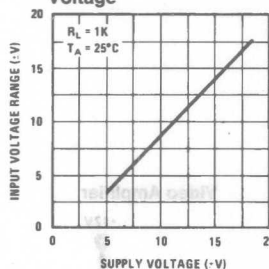
Open Loop Frequency Response



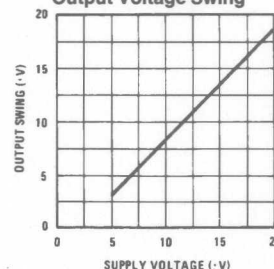
Voltage Follower Pulse Response



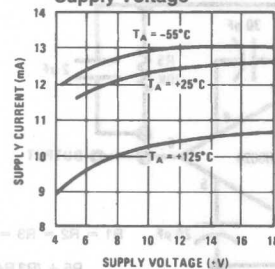
Input Voltage vs Supply Voltage



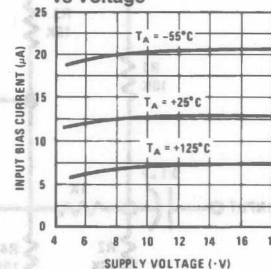
Output Voltage Swing



Supply Current vs Supply Voltage



Input Bias Current vs Voltage



TL/K/5552-7

Applications Information

LAYOUT CONSIDERATIONS

The LH0024/LH0024C, like most high speed circuitry, is sensitive to layout and stray capacitance. Power supplies should be by-passed as near the device as is practicable with at least 0.01 μF disc type capacitors. Compensating capacitors should also be placed as close to device as possible.

COMPENSATION RECOMMENDATIONS

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for C1, C2, and C3 may be necessary for a given layout. In particular, when operating at a gain of -1 , C3 may re-

quire adjustment in order to perfectly cancel the input capacitance of the device.

When operating the LH0024/LH0024C at a gain of $+1$, the value of R1 should be at least 1 k Ω .

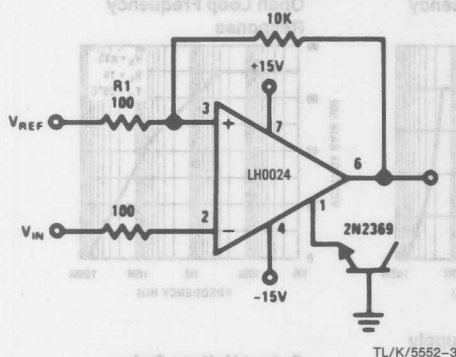
The case of the LH0024 is electrically isolated from the circuit; hence, it may be advantageous to drive the case in order to minimize stray capacitances.

HEAT SINKING

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy 2228B or equivalent.

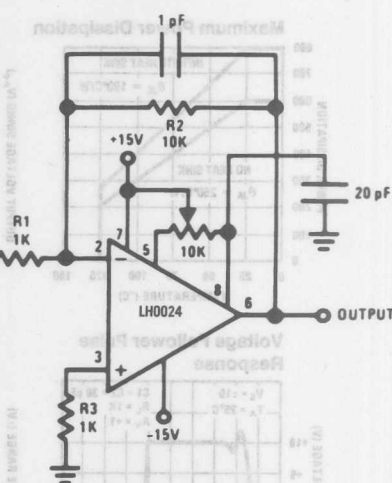
Typical Applications

TTL Compatible Comparator



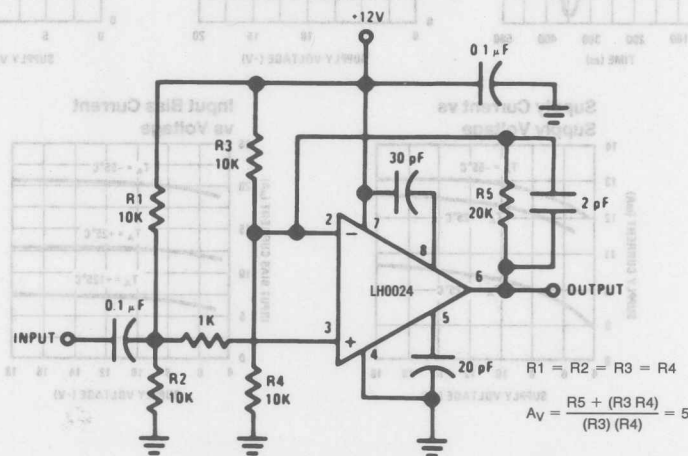
TL/K/5552-3

Offset Null



TL/K/5552-4

Video Amplifier



$$R1 = R2 = R3 = R4$$

$$A_v = \frac{R5 + (R3 R4)}{(R3) (R4)} = 5$$

TL/K/5552-5

When operating the LH0024 at a gain of +1, the value of $R1$ should be at least 1 K. The case of the LH0024 is electrically isolated from the circuit, hence, it may be advantageous to drive the case in order to minimize stray capacitance.

HEAT SINKING

The LH0024/LH0024C is specified for operation without the use of an explicit heat sink. However, internal power dissipation does cause a significant temperature rise. Improved offset voltage drift can be obtained by limiting the temperature rise with a clip-on heat sink such as the Thermalloy SS28B or equivalent.

COMPENSATION RECOMMENDATIONS

Compensation schemes recommended in Table 1 work well under typical conditions. However, poor layout and long lead lengths can degrade the performance of the LH0024 or cause the device to oscillate. Slight adjustments in the values for $C1$, $C2$, and $C3$ may be necessary for a given layout. In particular, when operating at a gain of -1, $C3$ may be

Typical Performance Characteristics

LH0032

Ultra Fast FET-Input Operational Amplifier

General Description

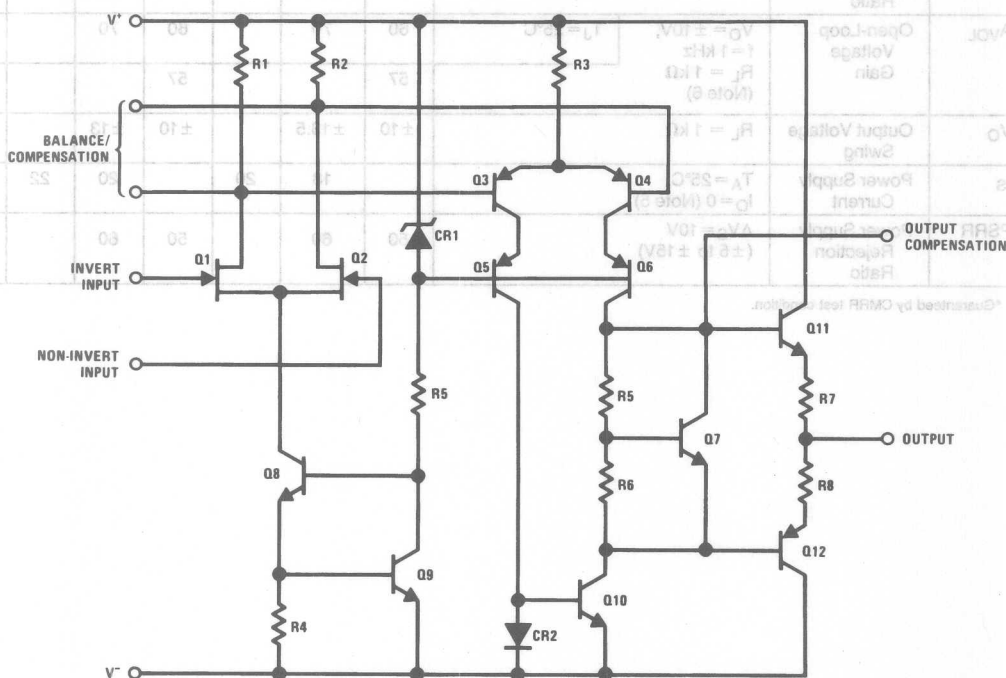
The LH0032 is a high slew rate, high input impedance differential operational amplifier suitable for diverse applications in fast signal handling. The high allowable differential input voltage, ease of output clamping, and high output drive capability particularly suit it for comparator applications. It may be used in applications normally reserved for video amplifiers allowing the use of operational gain setting and frequency response shaping into the megahertz region.

The LH0032's wide bandwidth, high input impedance and high output capacity make it an ideal choice for applications such as summing amplifiers in high speed D to A converters, buffers in data acquisition systems and sample and hold circuits. Additional applications include high speed integrators and video amplifiers. The LH0032 is guaranteed for operation over the temperature range -55°C to $+125^{\circ}\text{C}$, the LH0032C is guaranteed for -25°C to $+85^{\circ}\text{C}$.

Features

- 500 V/ μs slew rate
- 70 MHz bandwidth
- $10^{12}\Omega$ input impedance
- As low as 2 mV max input offset voltage
- FET input
- Peak output current to 100 mA

Schematic



TL/K/5265-1

Absolute Maximum Ratings (Note 9)

| | |
|------------------------------------|---|
| Supply Voltage, V_S | $\pm 18V$ |
| Input Voltage, V_{IN} | $\pm V_S$ |
| Differential Input Voltage | $\pm 30V$ or $\pm 2V_S$ |
| Power Dissipation, P_D | (Note 10) |
| Steady State Output Current | $\pm 100\text{ mA}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lead Temp. (Soldering, 10 seconds) | 300°C |

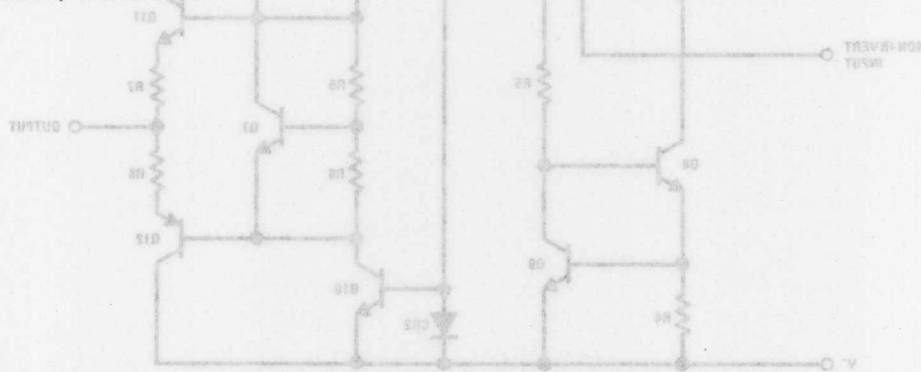
Operating Ratings

| | |
|-----------------------------|---|
| Temperature Range, T_A | -55°C to $+125^\circ\text{C}$ |
| LH0032G | -25°C to $+85^\circ\text{C}$ |
| LH0032CG | |
| Junction Temperature, T_J | $\pm 175^\circ\text{C}$ |
| LH0032G | |
| Thermal Resistance (Note 8) | |
| θ_{JA} G Package | 100°C/W |
| θ_{JC} G Package | 70°C/W |

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise noted (Note 2) ($T_A = T_J$)

| Symbol | Parameter | Test Conditions | LH0032 | | | LH0032C | | | Units |
|--------------------------|------------------------------|---|----------|------------|-----|----------|----------|-----|------------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $T_A = T_J = 25^\circ\text{C}$ (Note 3) | | 2 | 5 | | 2 | 15 | mV |
| $\Delta V_{OS}/\Delta T$ | Average Offset Voltage Drift | (Note 4) | | 15 | 50 | | 15 | 50 | $\mu\text{V}/^\circ\text{C}$ |
| I_{OS} | Input Offset Current | $V_{IN} = 0$ | | | 25 | | | 50 | pA |
| | | | | | 250 | | | 500 | pA |
| | | | | | 25 | | | 5 | nA |
| I_B | Input Bias Current | $T_J = 25^\circ\text{C}$ (Note 3) $T_A = 25^\circ\text{C}$ (Note 5) | | | 100 | | | 500 | pA |
| | | | | | 1 | | | 5 | nA |
| | | | | | 50 | | | 15 | nA |
| * V_{INCM} | Input Voltage Range | | ± 10 | ± 12 | | ± 10 | ± 12 | | V |
| CMRR | Common Mode Rejection Ratio | $\Delta V_{IN} = \pm 10V$ | 50 | 60 | | 50 | 60 | | dB |
| A_{VOL} | Open-Loop Voltage Gain | $V_O = \pm 10V$, $f = 1\text{ kHz}$, $R_L = 1\text{ k}\Omega$ (Note 6) | 60 | 70 | | 60 | 70 | | dB |
| | | | 57 | | | 57 | | | |
| V_O | Output Voltage Swing | $R_L = 1\text{ k}\Omega$ | ± 10 | ± 13.5 | | ± 10 | ± 13 | | V |
| I_S | Power Supply Current | $T_A = 25^\circ\text{C}$, $I_O = 0$ (Note 5) | | 18 | 20 | | 20 | 22 | mA |
| PSRR | Power Supply Rejection Ratio | $\Delta V_S = 10V$ (± 5 to $\pm 15V$) | 50 | 60 | | 50 | 60 | | dB |

*Guaranteed by CMRR test condition.



AC Electrical Characteristics $V_S = \pm 15V$, $R_L = 1k\Omega$, $T_J = 25^\circ C$ (Note 7)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------|--------------------------------------|------------------------------------|-----|-----|-----|------------|
| S_R | Slew Rate | $A_V = +1$ | 350 | 500 | | V/ μs |
| t_s | Settling Time to 1% of Final Value | $A_V = -1$, $\Delta V_{IN} = 20V$ | | 100 | | ns |
| t_s | Settling Time to 0.1% of Final Value | | | 300 | | ns |
| t_R | Small Signal Rise Time | $A_V = +1$, $\Delta V_{IN} = 1V$ | | 8 | 20 | |
| t_D | Small Signal Delay Time | | | 10 | 25 | |

Note 1: In order to limit maximum junction temperature to $+175^\circ C$, it may be necessary to operate with $V_S < \pm 15V$ when T_A or T_C exceeds specific values depending on the P_D within the device package. Total P_D is the sum of quiescent and load-related dissipation. See applications notes AN-277, "Applications of Wide-Band Buffer Amplifiers" and AN-253, "High-Speed Operational-Amplifier Applications" for a discussion of load-related power dissipation.

Note 2: LH0032G is 100% production tested as specified at $25^\circ C$, $125^\circ C$, and $-55^\circ C$. LH0032CG is 100% production tested at $25^\circ C$ only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

Note 3: Specification is at $25^\circ C$ junction temperature due to requirements of high-speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25^\circ C$. When supply voltages are $\pm 15V$, no-load operating junction temperature may rise 40 – $60^\circ C$ above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B and I_{OS} will change significantly during warm-up. Refer to I_B and I_{OS} vs. temperature graph for expected values.

Note 4: LH0032G is 100% production tested for this parameter. LH0032CG is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at $25^\circ C$ and T_{MAX} .

Note 5: Measured in still air 7 minutes after application of power. Guaranteed thru correlated automatic pulse testing.

Note 6: Guaranteed thru correlated automatic pulse testing at $T_J = 25^\circ C$.

Note 7: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

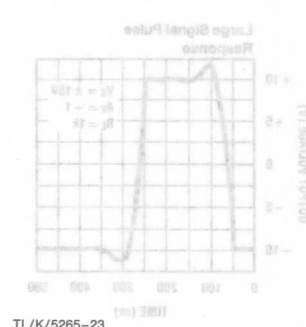
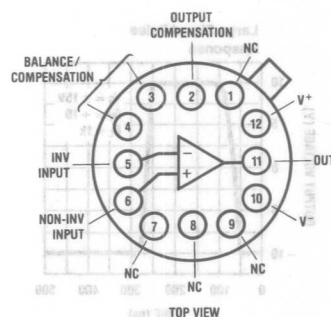
Note 8: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and T_J max. $T_J = T_A + P_D \theta_{JA}$.

Note 9: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 10: The maximum power dissipation is a function of maximum junction temperature T_J max, total thermal resistance θ_{JA} , and ambient temperature T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_J \text{ max} - T_A)/\theta_{JA}$.

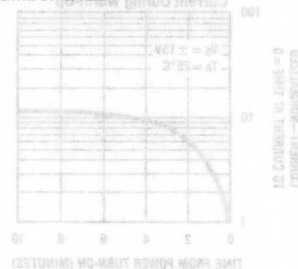
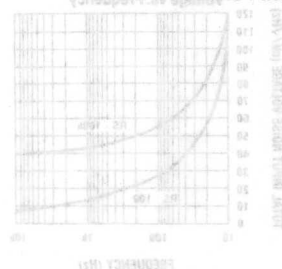
Note 11: See RETS0032X for LH0032G military specifications.

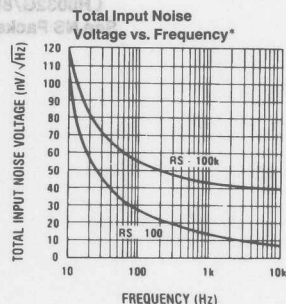
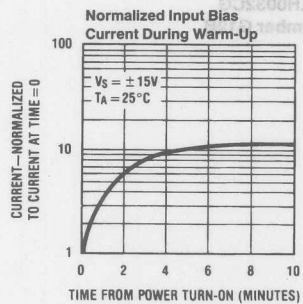
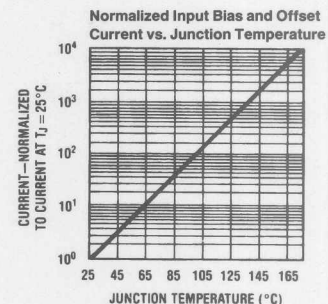
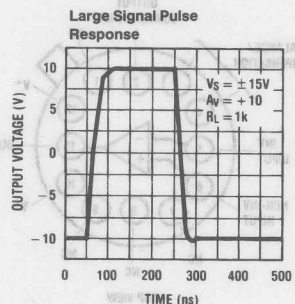
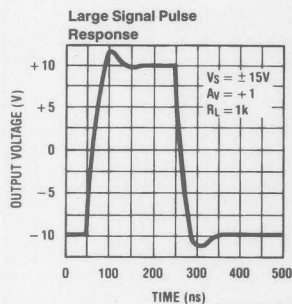
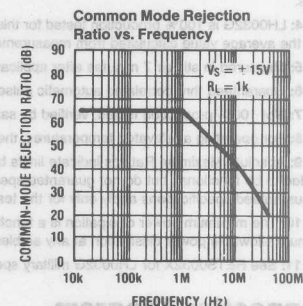
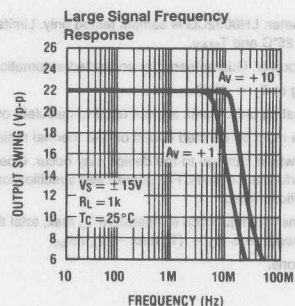
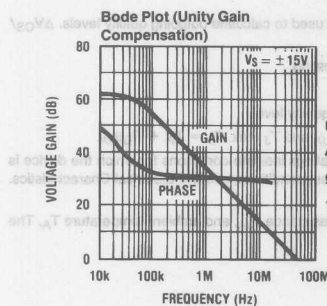
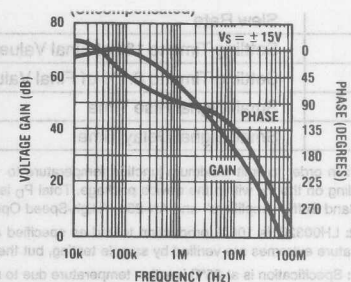
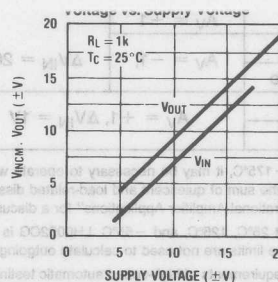
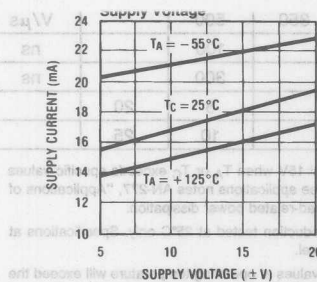
Connection Diagram



TL/K/5265-23

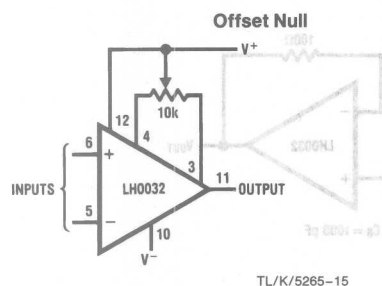
Order Number LH0032G,
LH0032G/883 or LH0032CG
See NS Package Number G12B



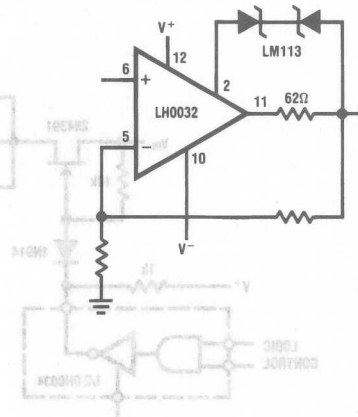


*Noise voltage includes contribution from source resistance.

Auxiliary Circuits

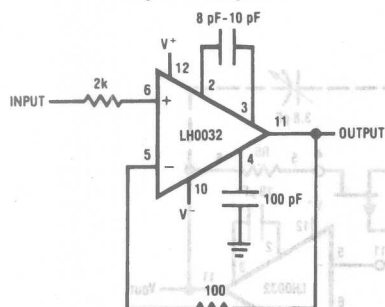


Output Short Circuit Protection

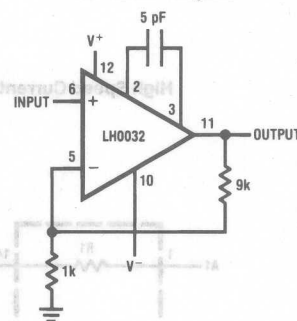


Typical Applications

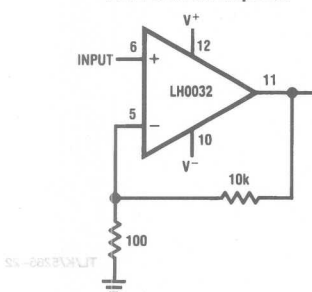
Unity Gain Amplifier



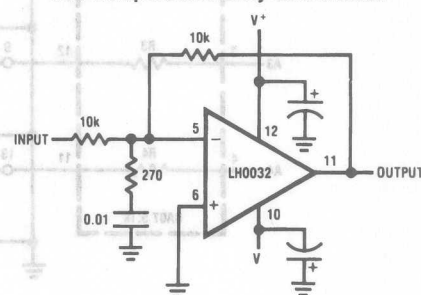
10X Buffer Amplifier



100X Buffer Amplifier

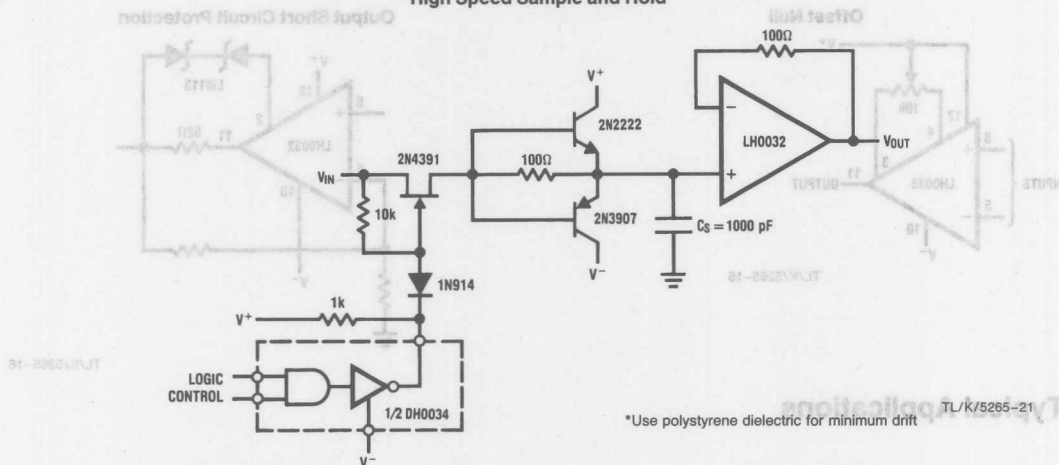


Non-Compensated Unity Gain Inverter

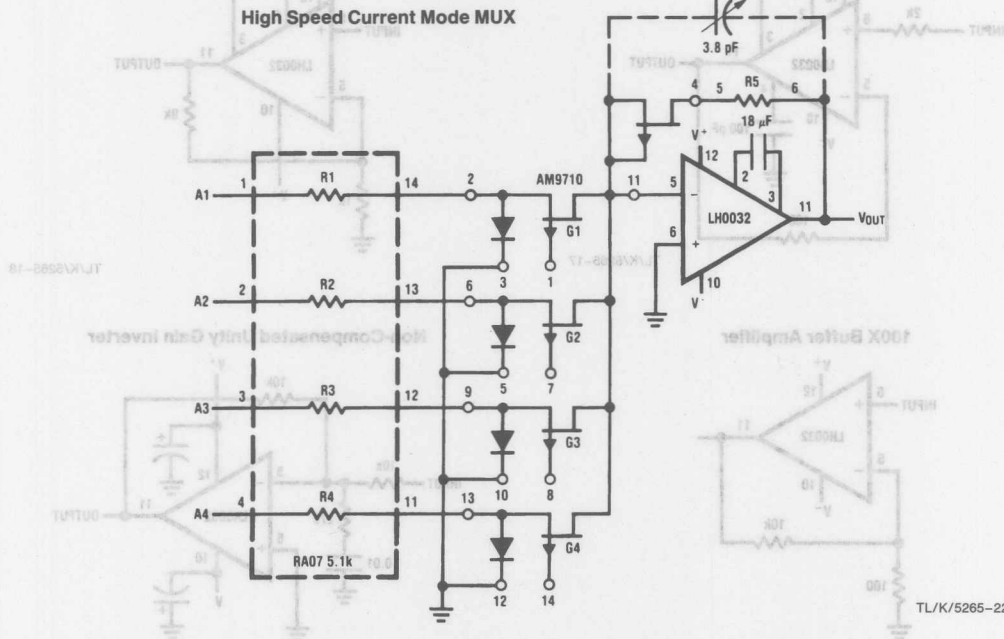


Typical Applications (Continued)

High Speed Sample and Hold



High Speed Current Mode MUX



Applications Information

POWER SUPPLY DECOUPLING

The LH0032/LH0032A, like most high speed circuits, is sensitive to layout and stray capacitance. Power supplies should be bypassed as near to pins 10 and 12 as practicable with low inductance capacitors such as 0.01 μF disc ceramics. Compensation components should also be located close to the appropriate pins to minimize stray reactances.

INPUT CURRENT

Because the input devices are FETs, the input bias current may be expected to double for each 11°C junction temperature rise. This characteristic is plotted in the typical performance characteristics graphs. The device will self-heat due to internal power dissipation after application of power thus raising the FET junction temperature 40–60°C above free-air ambient temperature when supplies are $\pm 15\text{V}$. The de-

Applications Information (Continued)

vice temperature will stabilize within 5–10 minutes after application of power, and the input bias currents measured at that time will be indicative of normal operating currents. An additional rise would occur as power is delivered to a load due to additional internal power dissipation.

There is an additional effect on input bias current as the input voltage is changed. The effect, common to all FETs, is an avalanche-like increase in gate current as the FET gate-to-drain voltage is increased above a critical value depending on FET geometry and doping levels. This effect will be noted as the input voltage of the LH0032 is taken below ground potential when the supplies are $\pm 15V$. All of the effects described here may be minimized by operating the device with $V_S \leq \pm 15V$.

These effects are indicated in the typical performance curves.

INPUT CAPACITANCE

The input capacitance to the LH0032/LH0032C is typically 5pF and thus may form a significant time constant with high value resistors. For optimum performance, the input capacitance to the inverting input should be compensated by a small capacitor across the feedback resistor. The value is strongly dependent on layout and closed loop gain, but will typically be in the neighborhood of several picofarads.

In the non-inverting configuration, it may be advantageous to bootstrap the case and/or a guard conductor to the inverting input. This serves both to divert leakage currents away from the non-inverting input and to reduce the effective input capacitance. A unity gain follower so treated will have an input capacitance under a picofarad.

HEAT SINKING

While the LH0032/LH0032A is specified for operation without any explicit heat sink, internal power dissipation does cause a significant temperature rise. Improved bias current performance can thus be obtained by limiting this temperature rise with a small heat sink such as the Thermalloy No. 2241 or equivalent. The case of the device has no internal connection, so it may be electrically connected to the sink if this is advantageous. Be aware, however, that this will affect the stray capacitances to all pins and may thus require adjustment of circuit compensation values.

For additional applications information request Application Note AN-253.

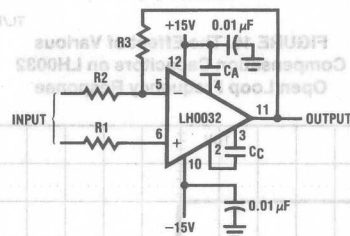


Compensating the LH0032

With the LH0032, two compensation schemes may be used, depending on the designer's specific needs.

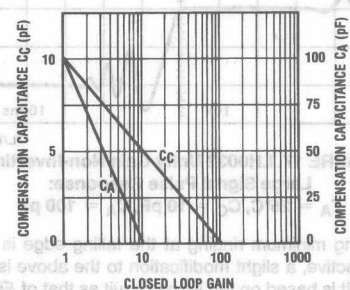
The first technique is shown in Figure 14. It offers the best 0.1% settling time for a $\pm 10V$ square wave input. The compensation capacitors C_C and C_A should be selected from Figure 15 for various closed-loop gains. Figure 16 shows how the LH0032 frequency response is modified for different value compensation capacitors.

Although this approach offers the shortest settling time, the falling edge exhibits overshoot up to 30% lasting 200 to 300 ns. Figure 17 shows the typical pulse response.



TL/K/5265-27

FIGURE 14: LH0032 Frequency Compensation Circuit



TL/K/5265-28

FIGURE 15: Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Settling Time

It obtaining a slightly higher settling time is recommended. It is based on the fact that the settling time to the first value is actually superior to the first method of compensation. However, the LH0032 settles slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the pre-vious scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slow rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required. Typical improvement is as much as 50%. A more detailed discussion of this effect is provided in the Slow Response section of this Application Note.

The second compensation scheme works well with both inverting or non-inverting modes. Figure 20 shows the circuit.

Applications Information (Continued)

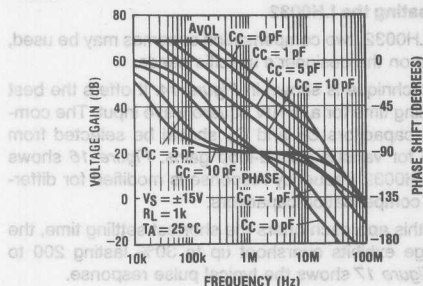


FIGURE 16. The Effect of Various Compensation Capacitors on LH0032 Open Loop Frequency Response

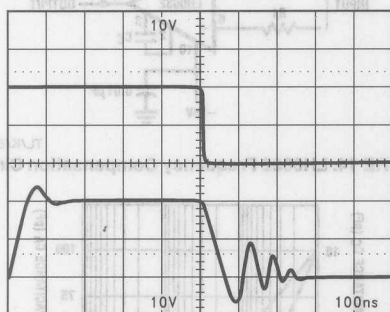


FIGURE 17. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response:
 $T_A = 25^\circ\text{C}$, $C_C = 10\text{ pF}$, $C_A = 100\text{ pF}$

If obtaining minimum ringing at the falling edge is the primary objective, a slight modification to the above is recommended. It is based on the same circuit as that of Figure 14. The values of the unity gain compensation capacitors C_C and C_A should be modified to 5 pF and 1000 pF, respectively. Figure 18 shows the suitable capacitance to use for various closed-loop gains. The resulting unity gain pulse response waveform is shown in Figure 19. The settling time to 1% final value is actually superior to the first method of compensation. However, the LH0032 suffers slow settling thereafter to 0.1% accuracy at the falling edge, and nearly four times as much at the rising edge, compared to the previous scheme. Note, however, that the falling edge ringing is considerably reduced. Furthermore, the slew rate is consistently superior using this compensation because of the smaller value of Miller capacitance C_C required. Typical improvement is as much as 50%. A more detailed discussion of this effect is provided in the Slew Response section of this Application Note.

The second compensation scheme works well with both inverting or non-inverting modes. Figure 20 shows the circuit

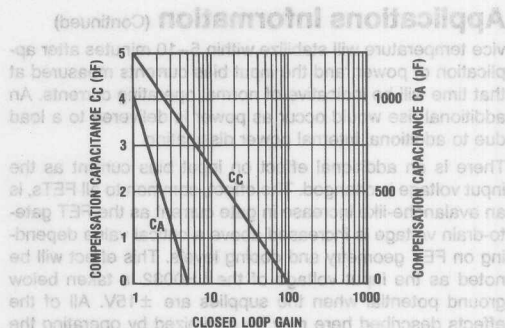


FIGURE 18. Recommended Value of Compensation Capacitor vs. Closed-Loop Gain for Optimum Slew Rate

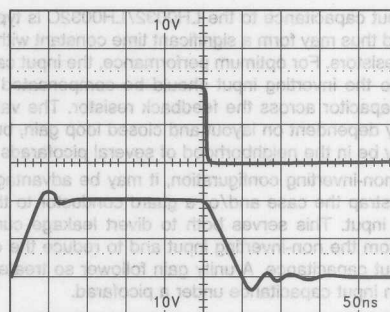


FIGURE 19. LH0032 Unity Gain Non-Inverting Large Signal Pulse Response:
 $C_C = 5\text{ pF}$, $C_A = 1000\text{ pF}$

schematic, in which a 270Ω resistor and a 0.01 μF capacitor are shunted across the inputs of the device. This lag compensation introduces a zero in the loop modifying the response such that adequate phase margin is preserved at unity gain crossover frequency. Note that the circuit requires no additional compensation.

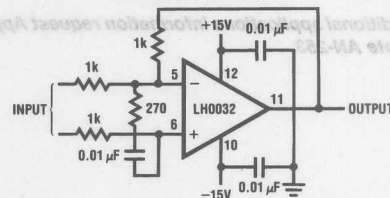


FIGURE 20. LH0032 Non-Compensated Unity Gain Compensation



LH0042

Low Cost FET Op Amp

General Description

The LH0042 is a FET input operational amplifier with very high input impedance and low input currents with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. The LH0042 is internally compensated and is free of latch-up.

The LH0042 is specified for operation over the -55°C to $+125^{\circ}\text{C}$ military temperature range. The LH0042C is specified for operation over the -25°C to $+85^{\circ}\text{C}$ temperature range.

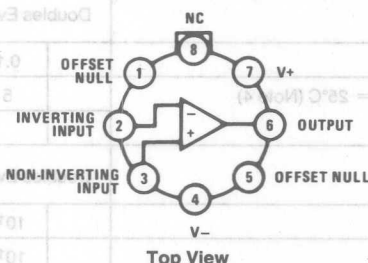
The LH0042 op amp is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents. The LH0042 provides low cost high performance for such applications as electrometer and photocell amplification, picoammeters, and high input impedance buffers.

Features

- High open loop gain—100 dB typ
- Internal compensation
- Pin compatible with standard IC op amps (TO-99 package)

Connection Diagram

Metal Can Package



Order Number LH0042H-MIL, LH0042H or LH0042CH
See NS Package Number H08D

| | | | | | | | |
|---|---|------------------|------------------|------------------|------------------|------------------|------------------------|
| Power Consumption | $V_S = \pm 15\text{V}$ | 75 | 5.0 | 5.8 | 2.4 | 2.8 | mA |
| Supply Current | $V_S = \pm 15\text{V}$ | 25 | 2.0 | 2.5 | 1.0 | 1.2 | mA |
| Output Short Circuit Current | | 25 | 2.0 | 2.5 | 1.0 | 1.2 | mA |
| Output Resistance | | 75 | 2.0 | 2.5 | 1.0 | 1.2 | Ω |
| Output Current Swing | $V_{OUT} = \pm 10\text{V}, T_A = 25^{\circ}\text{C}$ | ± 10 | ± 10 | ± 10 | ± 10 | ± 10 | mA |
| Output Voltage Swing | $R_L = 2\text{k}\Omega, V_S = \pm 15\text{V}$ $R_L = 1\text{k}\Omega, T_A = 25^{\circ}\text{C}$ | ± 10 | ± 10 | ± 10 | ± 10 | ± 10 | V |
| Large Signal Voltage Gain | $R_L = 2\text{k}\Omega, V_{OUT} = \pm 10\text{V}$ $T_A = 25^{\circ}\text{C}, V_S = \pm 15\text{V}$ | 30 | 30 | 30 | 30 | 30 | V/mV |
| Supply Voltage Rejection Ratio | $R_S \leq 10\text{k}\Omega, \pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ | 74 | 90 | 70 | 90 | 90 | dB |
| Common Mode Rejection Ratio | $R_S \leq 10\text{k}\Omega, \pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ | 74 | 90 | 70 | 90 | 90 | dB |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | ± 15 | ± 15 | ± 15 | ± 15 | ± 15 | V |
| Input Capacitance | | 10 | 10 | 10 | 10 | 10 | pF |
| Differential Input Resistance | | 10 ¹² | 10 ¹² | 10 ¹² | 10 ¹² | 10 ¹² | Ω |
| Input Bias Current | | 10 | 10 | 10 | 10 | 10 | fA |
| Input Offset Current | $T_A = 25^{\circ}\text{C} \text{ (Note 4)}$ | 10 | 10 | 10 | 10 | 10 | fA |
| Offset Current Drift with Time | | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | fA/year |
| Temperature Coefficient of Input Offset Current | | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | fA/ $^{\circ}\text{C}$ |
| Input Offset Voltage | | 10 | 10 | 10 | 10 | 10 | mV |
| Offset Voltage Drift with Time | | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | mV/year |
| Input Offset Voltage | | 10 | 10 | 10 | 10 | 10 | mV |

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--------|
| Supply Voltage | ±22V |
| Power Dissipation (see Graph) | 500 mW |
| Input Voltage (Note 1) | ±15V |
| Differential Input Voltage (Note 2) | ±30V |
| Voltage Between Offset Null and V ₊ | ±0.5V |

| | | |
|---------------------------------------|---------------------------|-----------------|
| Operating Temperature Range | LH0022, LH0042, LH0052 | –55°C to +125°C |
| | LH0022C, LH0042C, LH0052C | –25°C to +85°C |
| Storage Temperature Range | | –65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | | 300°C |

DC Electrical Characteristics for LH0022/LH0022C (Note 3) T_A = T_J(Max)

| Parameter | Conditions | Limits | | | | | | Units |
|---|--|----------------------------------|------------------|-----|----------------------------------|------------------|-----|------------------------------|
| | | LH0022 | | | LH0022C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \leq 100\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ $V_S = \pm 15\text{V}$ | | 2.0 | 4.0 | | 3.5 | 6.0 | mV |
| | $R_S \leq 100\text{ k}\Omega$, $V_S = \pm 15\text{V}$ | | | 5.0 | | | 7.0 | mV |
| Temperature Coefficient of Input Offset Voltage | $R_S \leq 100\text{ k}\Omega$ | | 10 | | | 15 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset Voltage Drift with Time | | | 3 | | | 4 | | $\mu\text{V}/\text{week}$ |
| Input Offset Current | $T_A = 25^\circ\text{C}$ (Note 4) | | 0.2 | 2.0 | | 1.0 | 5.0 | pA |
| | | | | 2.0 | | | 0.5 | nA |
| Temperature Coefficient of Input Offset Current | | Doubles Every 10°C | | | Doubles Every 10°C | | | |
| Offset Current Drift with Time | | | 0.1 | | | 0.1 | | pA/week |
| Input Bias Current | $T_A = 25^\circ\text{C}$ (Note 4) | | 5 | 10 | | 10 | 25 | pA |
| | | | | 10 | | | 2.5 | nA |
| Temperature Coefficient of Input Bias Current | | Doubles Every 10°C | | | Doubles Every 10°C | | | |
| Differential Input Resistance | | | 10 ¹² | | | 10 ¹² | | Ω |
| Common Mode Input Resistance | | | 10 ¹² | | | 10 ¹² | | Ω |
| Input Capacitance | | | 4.0 | | | 4.0 | | pF |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | ± 12 | ± 13.5 | | ± 12 | ± 13.5 | | V |
| Common Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$, $V_{IN} = \pm 10\text{V}$ | 74 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 10\text{ k}\Omega$, $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ | 74 | 90 | | 70 | 90 | | dB |
| Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{V}$ $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ | 75 | 100 | | 75 | 100 | | V/mV |
| | $R_L = 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{V}$ $V_S = \pm 15\text{V}$ | 30 | | | 30 | | | V/mV |
| Output Voltage Swing | $R_L = 1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ $V_S = \pm 15\text{V}$ | ± 10 | ± 12.5 | | ± 10 | ± 12 | | V |
| | $R_L = 2\text{ k}\Omega$, $V_S = \pm 15\text{V}$ | ± 10 | | | ± 10 | | | V |
| Output Current Swing | $V_{OUT} = \pm 10\text{V}$, $T_A = 25^\circ\text{C}$ | ± 10 | ± 15 | | ± 10 | ± 15 | | mA |
| Output Resistance | | | 75 | | | 75 | | Ω |
| Output Short Circuit Current | | | 25 | | | 25 | | mA |
| Supply Current | $V_S = \pm 15\text{V}$ | | 2.0 | 2.5 | | 2.4 | 2.8 | mA |
| Power Consumption | $V_S = \pm 15\text{V}$ | | | 75 | | | 85 | mW |

| Parameter | Conditions | LH0042 | | | LH0042C | | | Units |
|---|---|----------------------------------|------------|-----|----------------------------------|------------|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \leq 100 \text{ k}\Omega$ | | 5.0 | 20 | | 6.0 | 20 | mV |
| Temperature Coefficient of Input Offset Voltage | $R_S \leq 100 \text{ k}\Omega$ | | 10 | | | 15 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset Voltage Drift with Time | | | 7.0 | | | 10 | | $\mu\text{V}/\text{week}$ |
| Input Offset Current | $T_A = 25^\circ\text{C}$ (Note 4) | | 1.0 | 5.0 | | 2.0 | 10 | pA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ (Note 4) | | 10 | 25 | | 15 | 50 | pA |
| Temperature Coefficient of Input Bias Current | | Doubles Every 10°C | | | Doubles Every 10°C | | | |
| Differential Input Resistance | | | 10^{12} | | | 10^{12} | | Ω |
| Common Mode Input Resistance | | | 10^{12} | | | 10^{12} | | Ω |
| Input Capacitance | | | 4.0 | | | 4.0 | | pF |
| Input Voltage Range | | ± 12 | ± 13.5 | | ± 12 | ± 13.5 | | V |
| Common Mode Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$, $V_{IN} = \pm 10\text{V}$ | 70 | 86 | | 70 | 80 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$, $\pm 5\text{V} \leq V_S \leq \pm 15\text{V}$ | 70 | 86 | | 70 | 86 | | dB |
| Large Signal Voltage Gain | $R_S \leq 2 \text{ k}\Omega$, $V_{OUT} = \pm 10\text{V}$, $T_A = 25^\circ\text{C}$ | 50 | 100 | | 25 | 100 | | V/mV |
| | $R_S \leq 2 \text{ k}\Omega$, $V_{OUT} = \pm 10\text{V}$ | 30 | | | 25 | | | V/mV |
| Output Voltage Swing | $R_L = 1 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | ± 10 | ± 12.5 | | ± 10 | ± 12 | | V |
| | $R_L = 2 \text{ k}\Omega$ | ± 10 | | | ± 10 | | | V |
| Output Current Swing | $V_{OUT} = \pm 10\text{V}$ | ± 10 | ± 15 | | ± 10 | ± 15 | | mA |
| Output Resistance | | | 75 | | | 75 | | Ω |
| Output Short Circuit Current | | | 20 | | | 20 | | mA |
| Supply Current | $V_S = \pm 15\text{V}$ | | 2.5 | 3.5 | | 2.8 | 4.0 | mA |
| Power Consumption | $V_S = \pm 15\text{V}$ | | | 105 | | | 120 | mW |

| Parameter | Conditions | Limits | | | | | |
|------------------------|------------------------------|--------------|-----|-----|-----------------|-----|-----|
| | | LH0023/42/52 | | | LH0023C/42C/52C | | |
| | | Min | Typ | Max | Min | Typ | Max |
| Slew Rate | Voltage Follower | 1.8 | 3.0 | | 1.0 | 3.0 | |
| Large Signal Bandwidth | Voltage Follower | | 10 | | | 10 | |
| Small Signal Bandwidth | | | 1.0 | | | 1.0 | |
| Rise Time | | | 0.3 | 1.5 | | 0.3 | 1.5 |
| Overshoot | | | 10 | 30 | | 15 | 40 |
| Settling Time (0.1%) | $\Delta V_{IN} = 10\text{V}$ | | 1.5 | | | 1.5 | |
| Overload Recovery | | | 1.0 | | | 1.0 | |

DC Electrical Characteristics for LH0052/LH0052C (Note 3) (Continued)

| Units | Parameter | Limits | Conditions | Limits | | | | | | Units | | | | |
|-------|---|--------|------------|--------------------------------|-----|-----|--|-----|-------|-------|--------------------|-------|------|----|
| | | | | LH0052 | | | LH0052C | | | | | | | |
| | | | | Min | Typ | Max | Min | Typ | Max | | | | | |
| | Input Bias Current | 5.0 | | T _A = 25°C (Note 4) | | | | | | | | pA | | |
| | | 15 | | | | | 0.5 | 2.5 | | | 1.0 | 5.0 | nA | |
| | | | | | | | | 2.5 | | | | 0.5 | | |
| | Temperature Coefficient of Input Bias Current | 10 | | | | | Doubles Every 10°C | | | | Doubles Every 10°C | | | |
| | Differential Input Resistance | | | | | | 1012 | | | | 1012 | | Ω | |
| | Common Mode Input Resistance | | | | | | 1012 | | | | 1012 | | Ω | |
| | Input Capacitance | | | | | | 4.0 | | | | 4.0 | | pF | |
| | Input Voltage Range | | | | | | V _S = ±15V | ±12 | ±13.5 | | ±12 | ±13.5 | V | |
| | Common Mode Rejection Ratio | | | | | | R _S ≤ 10 kΩ, V _{IN} = ±10V | 74 | 90 | | 70 | 90 | dB | |
| | Supply Voltage Rejection Ratio | | | | | | R _S ≤ 10 kΩ, ±5V ≤ V _S ≤ ±15V | 74 | 90 | | 70 | 90 | dB | |
| | Large Signal Voltage Gain | | | | | | R _L = 2 kΩ, V _{OUT} = ±10V V _S = ±15V, T _A = 25°C | 75 | 100 | | 75 | 100 | V/mV | |
| | | | | | | | R _L = 2 kΩ, V _{OUT} = ±10V V _S = ±15V | 30 | | | 30 | | V/mV | |
| | Output Voltage Swing | | | | | | R _L = 1 kΩ, T _A = 25°C V _S = ±15V | ±10 | ±12.5 | | ±10 | ±12 | V | |
| | | | | | | | R _L = 2 kΩ, V _S = ±15V | ±10 | | | ±10 | | V | |
| | Output Current Swing | | | | | | V _{OUT} = ±10V, T _A = 25°C | ±10 | ±15 | | ±10 | ±15 | mA | |
| | Output Resistance | | | | | | | 75 | | | 75 | | Ω | |
| | Output Short Circuit Current | | | | | | | 25 | | | 25 | | mA | |
| | Supply Current | | | | | | V _S = ±15V | | 3.0 | 3.5 | | 3.0 | 3.8 | mA |
| | Power Consumption | | | | | | V _S = ±15V | | | 105 | | | 114 | mW |

AC Electrical Characteristics for all amplifiers ($T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$)

| Parameter | Conditions | Limits | | | | | | Units |
|------------------------|-----------------------|--------------|-----|-----|-----------------|-----|-----|------------|
| | | LH0022/42/52 | | | LH0022C/42C/52C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate | Voltage Follower | 1.5 | 3.0 | | 1.0 | 3.0 | | V/ μ s |
| Large Signal Bandwidth | Voltage Follower | | 40 | | | 40 | | kHz |
| Small Signal Bandwidth | | | 1.0 | | | 1.0 | | MHz |
| Rise Time | | | 0.3 | 1.5 | | 0.3 | 1.5 | μ s |
| Overshoot | | | 10 | 30 | | 15 | 40 | % |
| Settling Time (0.1%) | $\Delta V_{IN} = 10V$ | | 4.5 | | | 4.5 | | μ s |
| Overload Recovery | | | 4.0 | | | 4.0 | | μ s |

AC Electrical Characteristics for all amplifiers ($T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$) (Continued)

| Parameter | Conditions | Limits | | | | | | Units |
|---------------------|--|--------|-----|-----|---------|-----|-----|------------------------|
| | | LH0042 | | | LH0042C | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Noise Voltage | $R_S = 10\text{ k}\Omega, f_o = 10\text{ Hz}$ | | 150 | | | 150 | | nV/ $\sqrt{\text{Hz}}$ |
| | $R_S = 10\text{ k}\Omega, f_o = 100\text{ Hz}$ | | 55 | | | 55 | | nV/ $\sqrt{\text{Hz}}$ |
| | $R_S = 10\text{ k}\Omega, f_o = 1\text{ kHz}$ | | 35 | | | 35 | | nV/ $\sqrt{\text{Hz}}$ |
| | $R_S = 10\text{ k}\Omega, f_o = 10\text{ kHz}$ | | 30 | | | 30 | | nV/ $\sqrt{\text{Hz}}$ |
| | $\text{BW} = 10\text{ Hz to }10\text{ kHz}, R_S = 10\text{ k}\Omega$ | | 12 | | | 12 | | μVrms |

Note 1: For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

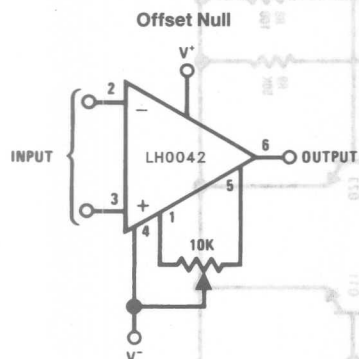
Note 2: Rating applies for minimum source resistance of $10\text{ k}\Omega$; for source resistances less than $10\text{ k}\Omega$, maximum differential input voltage is $\pm 5\text{V}$.

Note 3: Unless otherwise specified, these specifications apply for $\pm 5\text{V} \leq V_S \leq \pm 20\text{V}$ and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the LH0042 and $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for the LH0042C. Typical values are given for $T_A = 25^\circ\text{C}$.

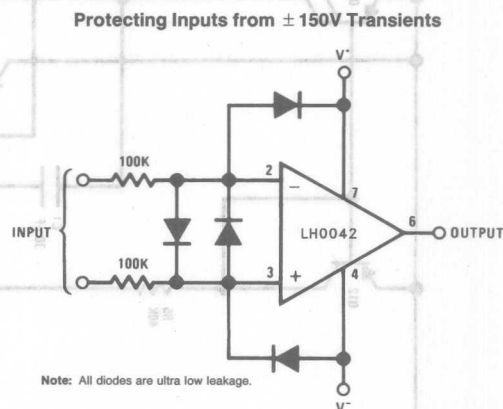
Note 4: Input currents are a strong function of temperature. Due to high speed testing they are specified at a junction temperature $T_J = 25^\circ\text{C}$. Self heating will cause an increase in current in manual tests. 25°C spec is guaranteed by testing at 125°C .

Note 5: See RETS0042X for the LH0042H military specifications.

Auxiliary Circuits (Shown for TO-99 pin out)

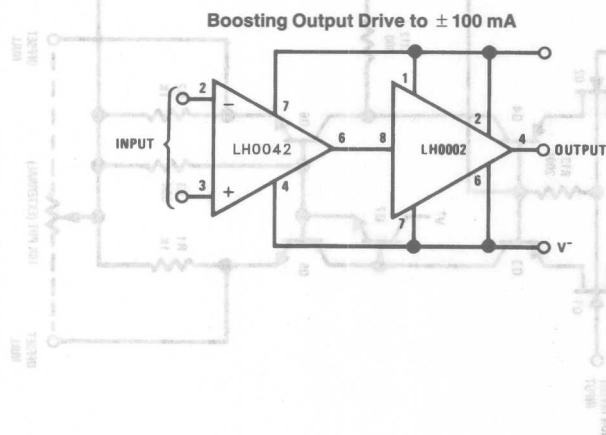


TL/K/5557-5



Note: All diodes are ultra low leakage.

TL/K/5557-6



TL/K/5557-7

Schematic Diagram

OUTPUT

V⁺

V⁻

INVERT INPUT

NON INVERT INPUT

OFFSET NULL

10K POT (EXTERNAL)

OFFSET NULL

R1 1K

R2 1K

R3 50K

R4

R5 40K

R6 27

R7 22

R8 100

R9 50K

R10 50K

R11 50K

R12 300

R13 200K

C1 30 pF

Q1

Q2

Q3

Q4

Q5

Q6

Q7

Q8

Q9

Q10

Q11

Q12

Q13

Q14

Q15

Q16

Q17

Q18

Q19

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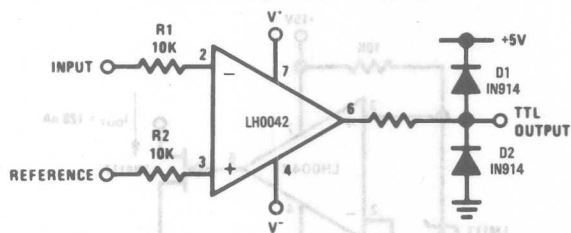
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Q266

Q267

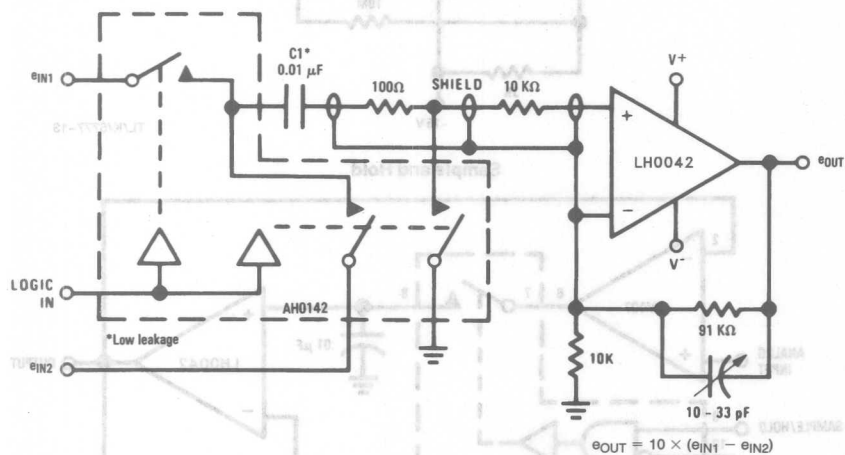
Typical Applications

Precision Voltage Comparator



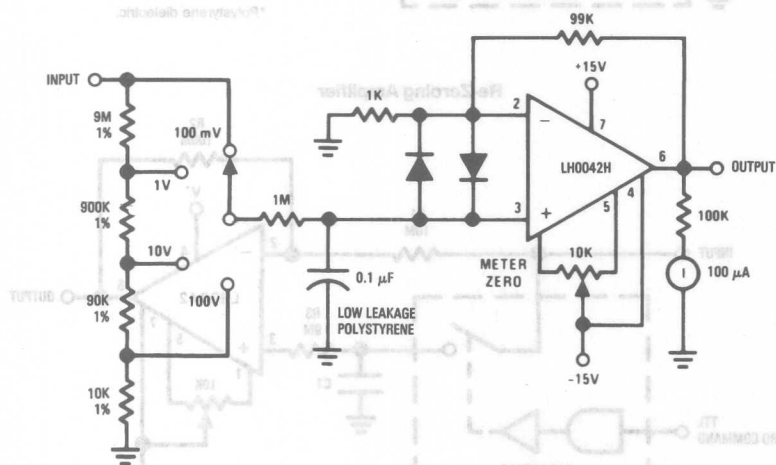
TL/K/5557-9

Subtractor for Automatic Test Gear



TL/K/5557-11

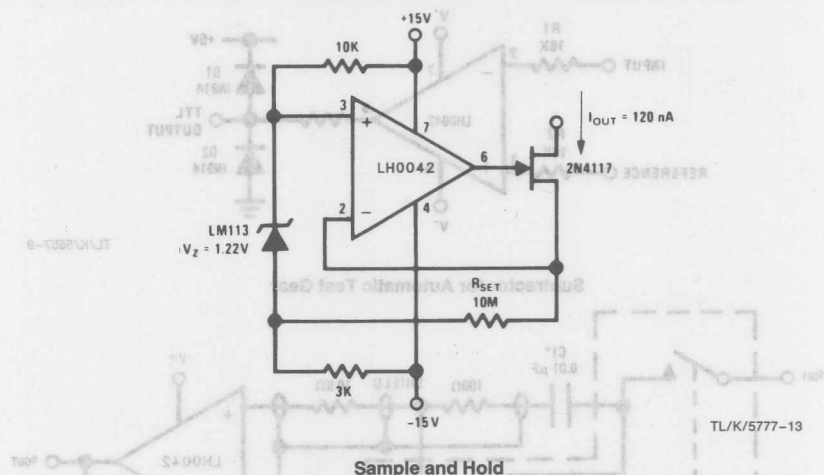
Sensitive Low Cost "VTVM"



TL/K/5777-12

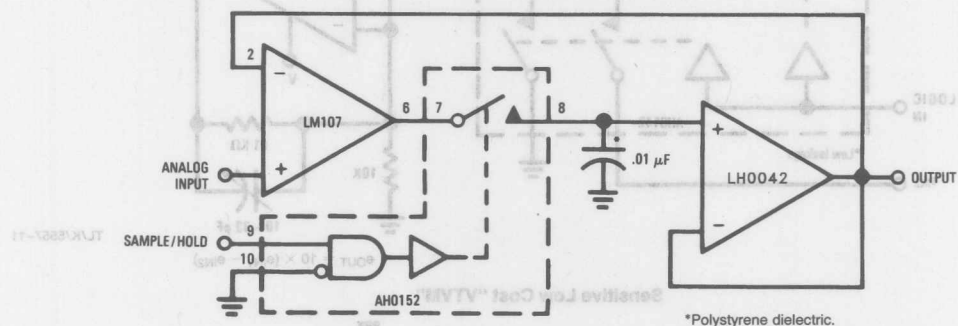
LH0042

1



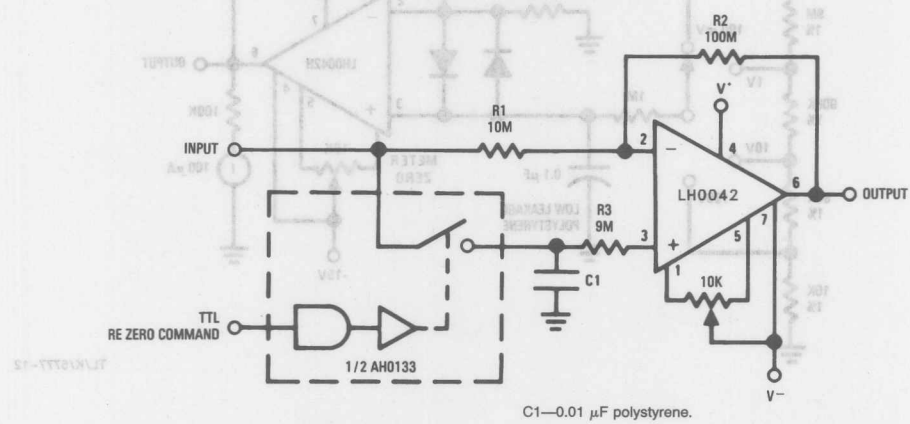
TL/K/5777-13

Sample and Hold



TL/K/5557-16

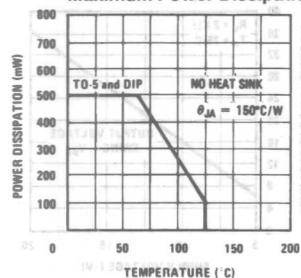
Re-Zeroing Amplifier



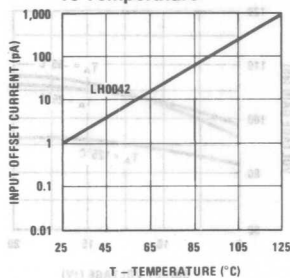
TL/K/5557-17

Typical Performance Characteristics

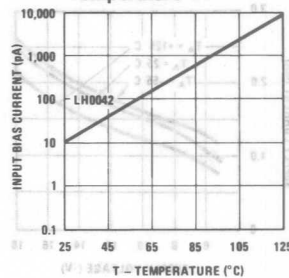
Maximum Power Dissipation



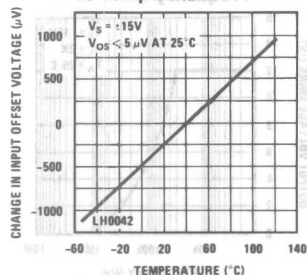
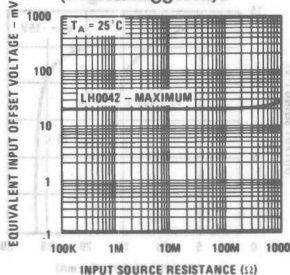
Input Offset Current vs Temperature



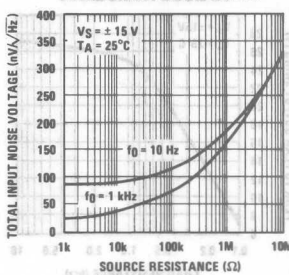
Input Bias Current vs Temperature



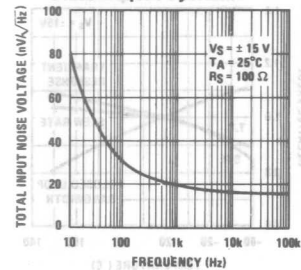
Input Offset Voltage vs Temperature

Offset Error (without V_{OS} Null)

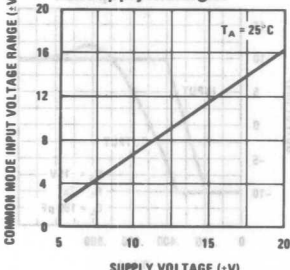
Total Input Noise Voltage* vs Source Resistance



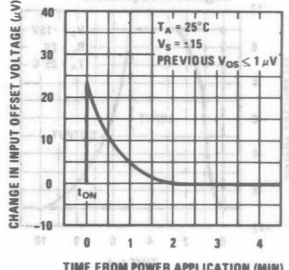
Total Input Noise Voltage* vs Frequency



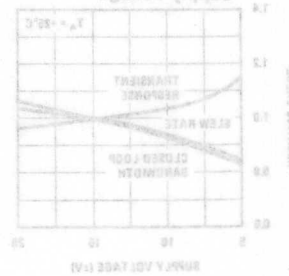
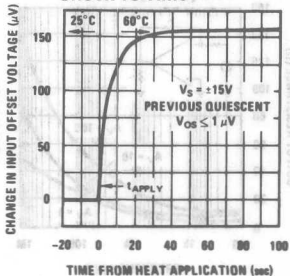
Common Mode Input Voltage vs Supply Voltage



Stabilization Time of Input Offset Voltage from Power Turn-On

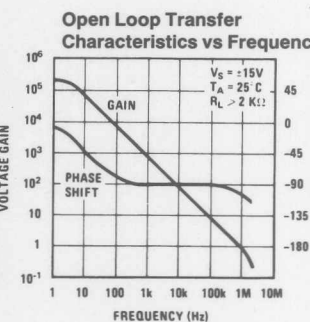
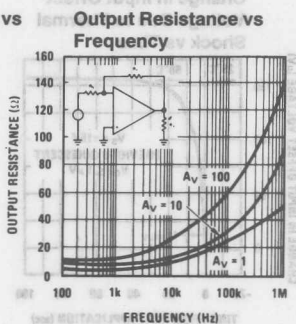
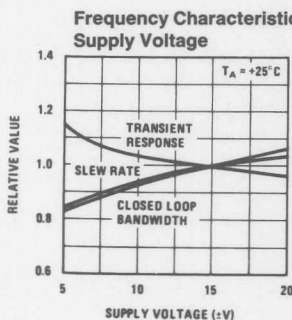
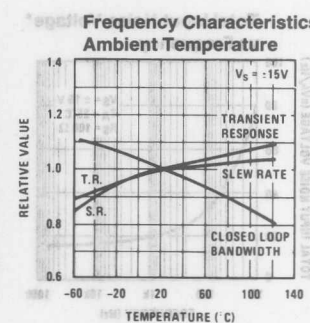
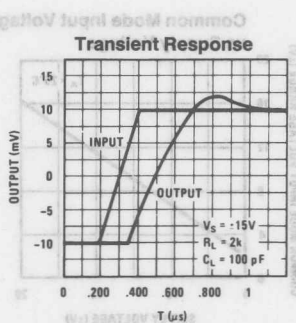
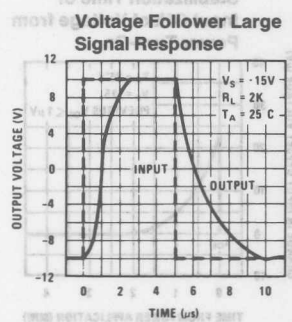
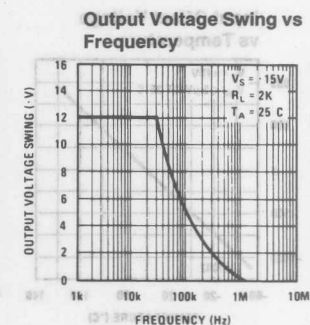
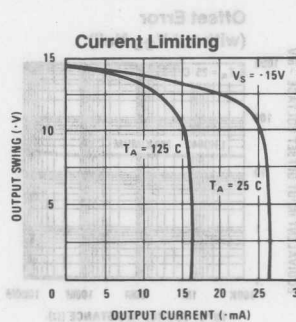
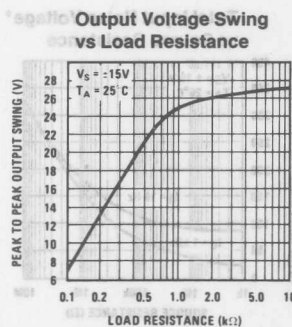
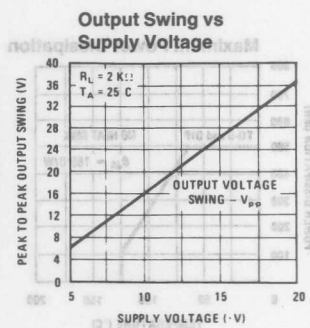
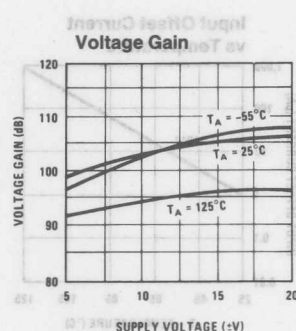
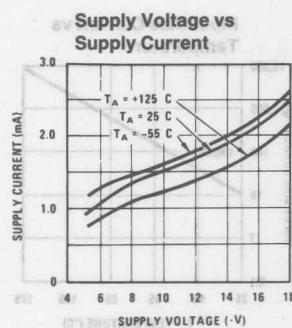


Change in Input Offset Voltage Due to Thermal Shock vs Time



*Noise voltage includes contribution from source resistance.

Typical Performance Characteristics (Continued)





LH0101

LH0101 Power Operational Amplifier

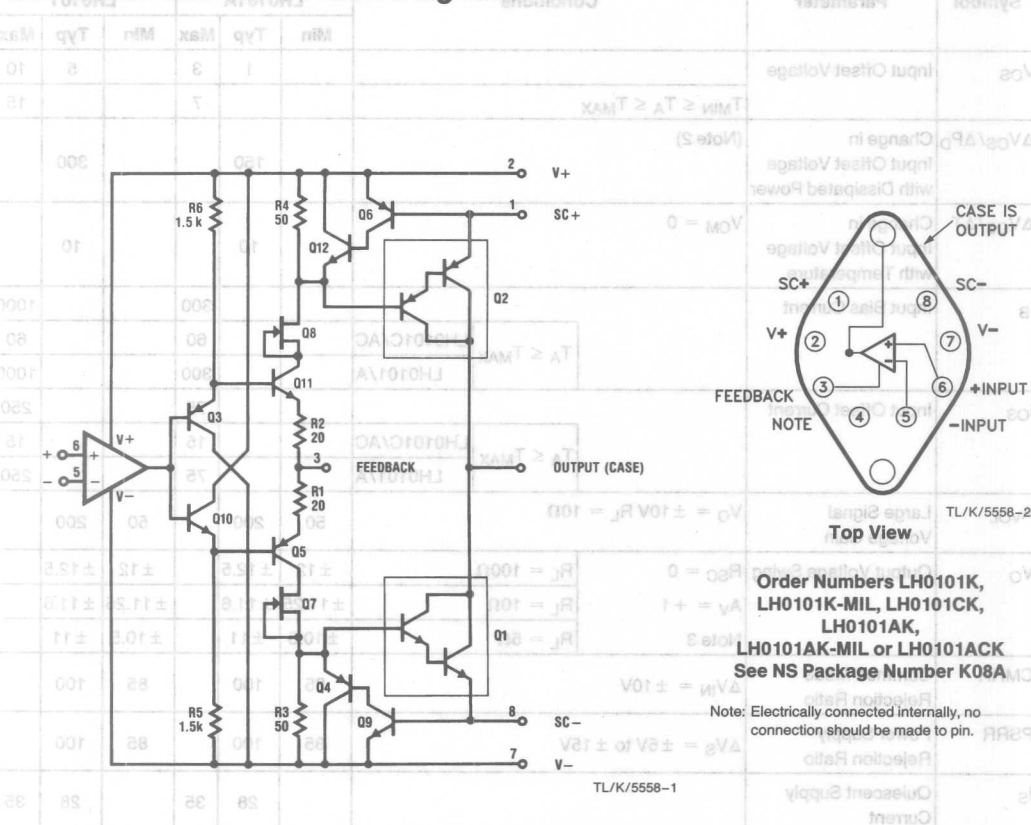
General Description

The LH0101 is a wideband power operational amplifier featuring FET inputs, internal compensation, virtually no crossover distortion, and rapid settling time. These features make the LH0101 an ideal choice for DC or AC servo amplifiers, deflection yoke drives, programmable power supplies, and disk head positioner amplifiers. The LH0101 is packaged in an 8 pin TO-3 hermetic package, rated at 60 watts with a suitable heat sink.

Features

- 5 Amp peak, 2 Amp continuous output current
- 300 kHz power bandwidth
- 850 mW standby power ($\pm 15V$ supplies)
- 300 pA input bias current
- 10 V/ μs slew rate
- Virtually no crossover distortion
- 2 μs settling time to 0.01%
- 5 MHz gain bandwidth

Schematic and Connection Diagrams



Office/Distributors for availability and specifications.
(Note 5)

 Supply Voltage, V_S $\pm 22V$

 Power Dissipation at $T_A = 25^\circ C$, P_D 5W

 Derate linearly at $25^\circ C/W$ to zero at $150^\circ C$,

 Power Dissipation at $T_C = 25^\circ C$ 62W

 Derate linearly at $2^\circ C/W$ to zero at $150^\circ C$

 Differential Input Voltage, V_{IN} $\pm 40V$ but $< \pm V_S$

 Input Voltage Range, V_{CM} $\pm 20V$ but $< \pm V_S$

Thermal Resistance—

See Typical Performance Characteristics

(within rated power dissipation,

 $R_{SC} = 0.35\Omega$, $T_A = 25^\circ C$)

Continuous

 Operating Temperature Range, T_A

LH0101AC, LH0101C

 $-25^\circ C$ to $+85^\circ C$

LH0101A, LH0101

 $-55^\circ C$ to $+125^\circ C$

 Storage Temperature Range, T_{STG}
 $-65^\circ C$ to $+150^\circ C$

 Maximum Junction Temperature, T_J
 $150^\circ C$

 Lead Temperature (Soldering < 10 sec.) $260^\circ C$

ESD rating to be determined.

DC Electrical Characteristics (Note 1) $V_S = \pm 15V$, $T_A = 25^\circ C$ unless otherwise noted

| Symbol | Parameter | Conditions | LH0101AC LH0101A | | | LH0101C LH0101 | | | Units |
|----------------------------|--|------------------------------------|---------------------|------------|-----|-------------------|------------|------|------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | | | 1 | 3 | | 5 | 10 | mV |
| | | $T_{MIN} \leq T_A \leq T_{MAX}$ | | | 7 | | | 15 | |
| $\Delta V_{OS}/\Delta P_D$ | Change in Input Offset Voltage with Dissipated Power | (Note 2) | | 150 | | | 300 | | $\mu V/W$ |
| $\Delta V_{OS}/\Delta T$ | Change in Input Offset Voltage with Temperature | $V_{CM} = 0$ | | 10 | | | 10 | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | | | | 300 | | | 1000 | pA |
| | | $T_A \leq T_{MAX}$ | | | 60 | | | 60 | nA |
| I_{OS} | Input Offset Current | | | | 300 | | | 1000 | pA |
| | | $T_A \leq T_{MAX}$ | | | 75 | | | 250 | nA |
| A_{VOL} | Large Signal Voltage Gain | $V_O = \pm 10V$ $R_L = 10\Omega$ | 50 | 200 | | 50 | 200 | | V/mV |
| V_O | Output Voltage Swing | $R_{SC} = 0$ | ± 12 | ± 12.5 | | ± 12 | ± 12.5 | | V |
| | | $A_V = +1$ | ± 11.25 | ± 11.6 | | ± 11.25 | ± 11.6 | | |
| | | Note 3 | ± 10.5 | ± 11 | | ± 10.5 | ± 11 | | |
| CMRR | Common Mode Rejection Ratio | $\Delta V_{IN} = \pm 10V$ | 85 | 100 | | 85 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $\Delta V_S = \pm 5V$ to $\pm 15V$ | 85 | 100 | | 85 | 100 | | |
| I_S | Quiescent Supply Current | | | 28 | 35 | | 28 | 35 | mA |

AC Electrical Characteristics (Note 1), $V_S = \pm 15V$, $T_A = 25^\circ C$

| Symbol | Parameter | Conditions | LH0101 LH0101A | | | LH0101C LH0101AC | | | Units |
|------------|-------------------------------------|--|-------------------|-------|-----|---------------------|-------|-----|----------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| e_n | Equivalent Input Noise Voltage | $f = 1 \text{ kHz}$ | | 25 | | | 25 | | nV/\sqrt{Hz} |
| C_{IN} | Input Capacitance | $f = 1 \text{ MHz}$ | | 3.0 | | | 3.0 | | pF |
| | Power Bandwidth, -3 dB | | | 300 | | | 300 | | kHz |
| SR | Slew Rate | $R_L = 10\Omega$ | 7.5 (Note 4) | 10 | | | 10 | | $V/\mu s$ |
| t_r, t_f | Small Signal Rise or Fall Time | $A_V = +1$ | | 200 | | | 200 | | ns |
| | Small Signal Overshoot | | | 10 | | | 10 | | % |
| GBW | Gain-Bandwidth Product | | 4.0 (Note 4) | 5.0 | | | 5.0 | | MHz |
| t_s | Large Signal Settling Time to 0.01% | $R_L = \infty$ | | 2.0 | | | 2.0 | | μs |
| THD | Total Harmonic Distortion | $P_O = 10W, f = 1 \text{ kHz}$ $R_L = 10\Omega$ | | 0.008 | | | 0.008 | | % |

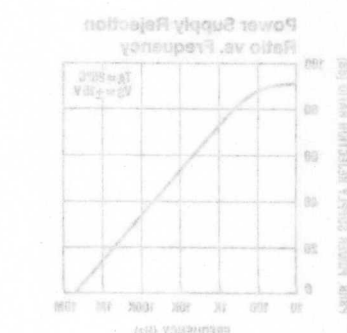
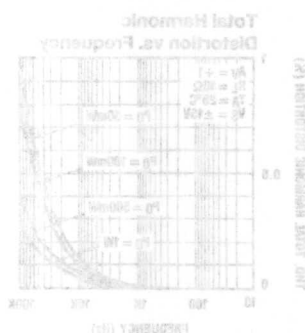
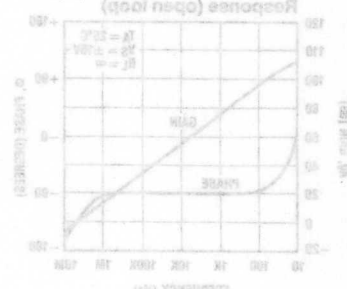
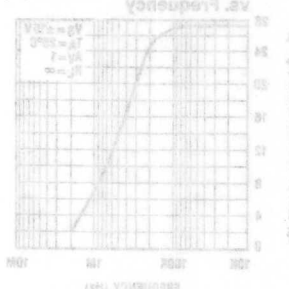
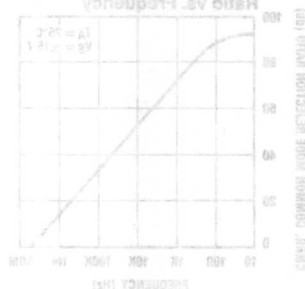
Note 1: Specification is at $T_A = 25^\circ C$. Actual values at operating temperature may differ from the $T_A = 25^\circ C$ value. When supply voltages are $\pm 15V$, quiescent operating junction temperature will rise approximately $20^\circ C$ without heat sinking. Accordingly, V_{OS} may change 0.5 mV and I_B and I_{OS} will change significantly during warm-ups. Refer to the I_B vs. temperature and power dissipation graphs for expected values. Power supply voltage is $\pm 15V$. Temperature tests are made only at extremes.

Note 2: Change in offset voltage with dissipated power is due entirely to average device temperature rise and not to differential thermal feedback effects. Test is performed without any heat sink.

Note 3: At light loads, the output swing may be limited by the second stage rather than the output stage. See the application section under "Output swing enhancement" for hints on how to obtain extended operation.

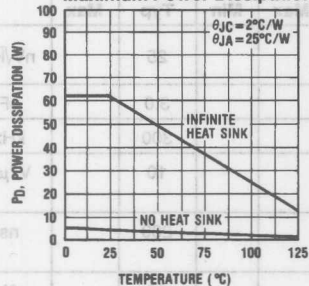
Note 4: These parameters are sample tested to 10% LTPD.

Note 5: Refer to RETS0101AK for the LH0101AK military specifications and RETS0101K for the LH0101K military specifications.

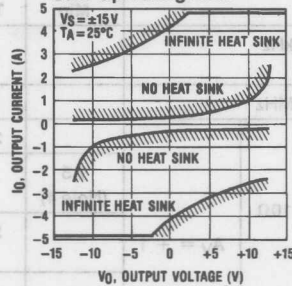


Typical Performance Characteristics

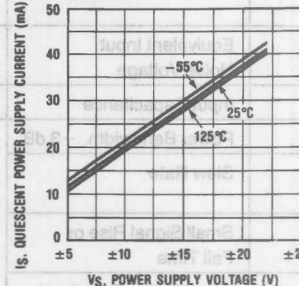
Maximum Power Dissipation



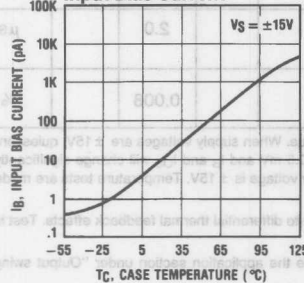
Safe Operating Area



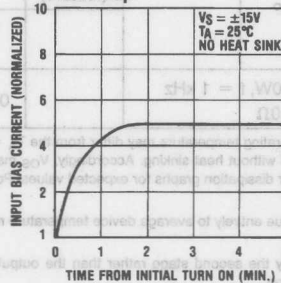
Quiescent Power Supply Current



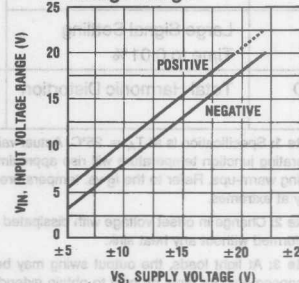
Input Bias Current



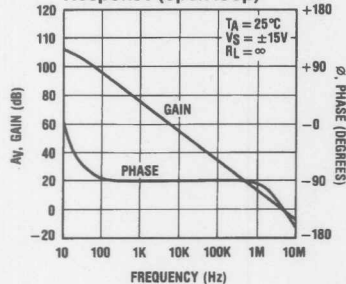
Input Bias Current after Warm-up



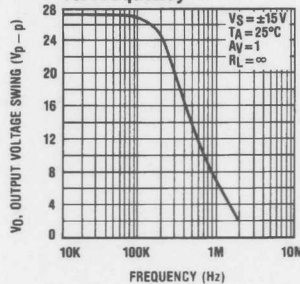
Input Common-Mode Voltage Range



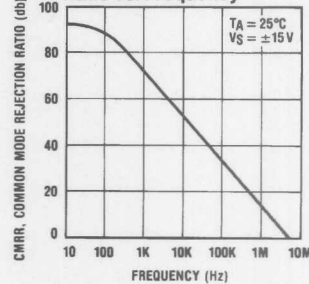
Small Signal Frequency Response (open loop)



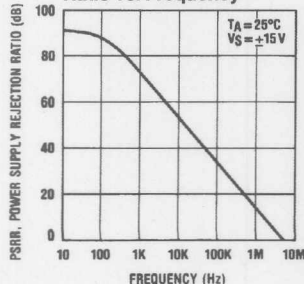
Output Voltage Swing vs. Frequency



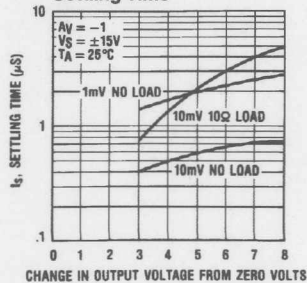
Common-Mode Rejection Ratio vs. Frequency



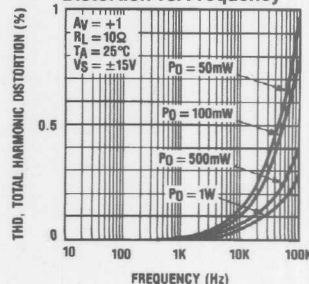
Power Supply Rejection Ratio vs. Frequency



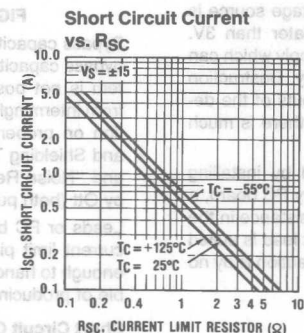
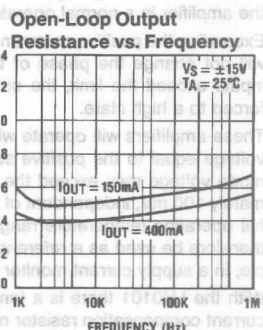
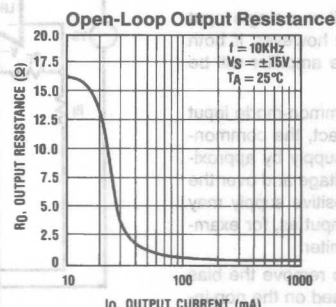
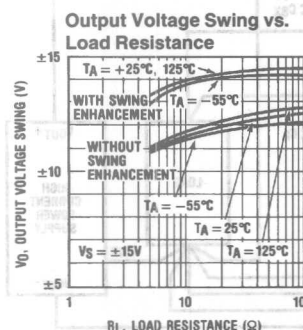
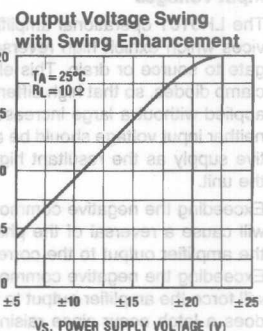
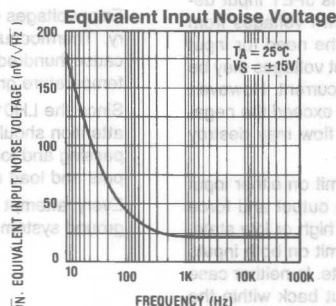
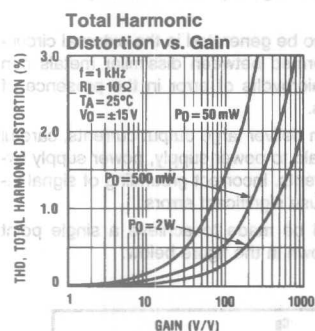
Settling Time



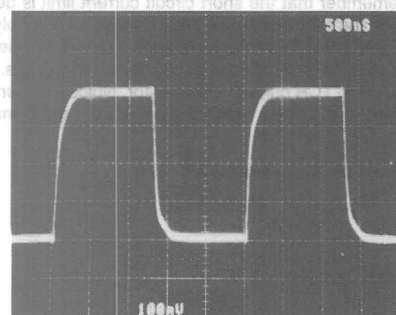
Total Harmonic Distortion vs. Frequency



Typical Performance Characteristics (Continued)

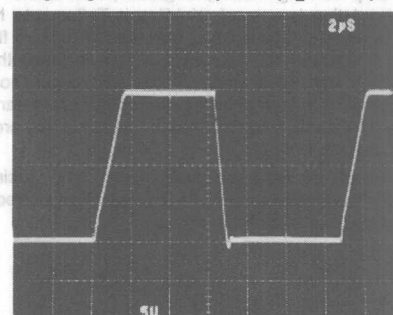


Small Signal Pulse Response (No Load)



TL/K/5558-5

Large Signal Pulse Response ($R_L = 10 \Omega$)



TL/K/5558-6

Application Hints

Input Voltages

The LH0101 operational amplifier contains JFET input devices which exhibit high reverse breakdown voltages from gate to source or drain. This eliminates the need for input clamp diodes, so that high differential input voltages may be applied without a large increase in input current. However, neither input voltage should be allowed to exceed the negative supply as the resultant high current flow may destroy the unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage may exceed the positive supply by approximately 100 mV, independent of supply voltage and over the full operating temperature range. The positive supply may therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

With the LH0101 there is a temptation to remove the bias current compensation resistor normally used on the non-inverting input of a summing amplifier. Direct connection of the inputs to ground or a low-impedance voltage source is not recommended with supply voltages greater than 3V. The potential problem involves loss of one supply which can cause excessive current in the second supply. Destruction of the IC could result if the current to the inputs of the device is not limited to less than 100 mA or if there is much more than 1 μ F bypass on the supply buss.

Although difficulties can be largely avoided by installing clamp diodes across the supply lines on every PC board, a conservative design would include enough resistance in the input lead to limit current to 10 mA if the input lead is pulled to either supply by internal currents. This precaution is by no means limited to the LH0101.

Layout Considerations

When working with circuitry capable of resolving pico-ampere level signals, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation is a must (Kel-F and Teflon rate high). Proper cleaning of all insulating surfaces to remove fluxes and other residues is also required. This includes the IC package as well as sockets and printed circuit boards. When operating in high humidity environments or near 0°C, some form of surface coating may be necessary to provide a moisture barrier.

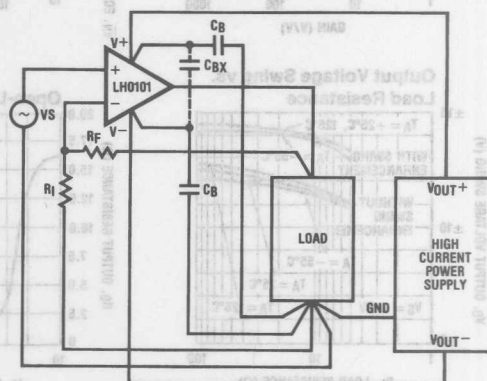
The effects of board leakage can be minimized by encircling the input circuitry with a conductive guard ring operated at a potential close to that of the inputs.

Electrostatic shielding of high impedance circuitry is advisable.

Error voltages can also be generated in the external circuitry. Thermocouples formed between dissimilar metals can cause hundreds of microvolts of error in the presence of temperature gradients.

Since the LH0101 can deliver large output currents, careful attention should be paid to power supply, power supply bypassing and load currents. Incorrect grounding of signal inputs and load can cause significant errors.

Every attempt should be made to achieve a single point ground system as shown in the figure below.



TL/K/5558-7

FIGURE 1. Single-Point Grounding

Bypass capacitor C_{BX} should be used if the lead lengths of bypass capacitors C_B are long. If a single point ground system is not possible, keep signal, load, and power supply from intermingling as much as possible. For further information on proper grounding techniques refer to "Grounding and Shielding Techniques in Instrumentation" by Morrison, and "Noise Reduction Techniques in Electronic Systems" by Ott (both published by John Wiley and Sons).

Leads or PC board traces to the supply pins, short-circuit current limit pins, and the output pin must be substantial enough to handle the high currents that the LH0101 is capable of producing.

Short Circuit Current Limiting

Should current limiting of the output not be necessary, SC+ should be shorted to V+ and SC- should be shorted to V-. Remember that the short circuit current limit is dependent upon the total resistance seen between the supply and current limit pins. This total resistance includes the desired resistor plus leads, PC Board traces, and solder joints.* Assuming a zero TCR current limit resistor, typical temperature coefficient of the short circuit current will be approximately 3%/°C.

*Short circuit current will be limited to approximately $\frac{0.6}{R_{SC}}$

Application Hints (Continued)

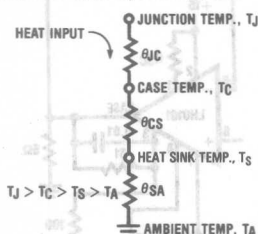
Thermal Resistance

The thermal resistance between two points of a conductive system is expressed as:

$$\theta_{12} = \frac{T_1 - T_2}{P_D} \text{ } ^\circ\text{C/W}$$

where subscript order indicates the direction of heat flow. A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in the figure below.

The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_J , T_C and T_S (no temperature distribution in junction, case, or heat sink). Nevertheless, this is a reasonable approximation of actual performance.



TL/K/5558-8

FIGURE 2. Semiconductor-Heat Sink Thermal Circuit

The junction-to-case thermal resistance θ_{JC} specified in the data sheet depends upon the material and size of the package, die size and thickness, and quality of the die bond to the case or lead frame. The case-to-heat sink thermal resistance θ_{CS} depends on the mounting of the device to the heat sink and upon the area and quality of the contact surface. Typical θ_{CS} for a TO-3 package is 0.5 to 0.7°C/W, and 0.3 to 0.5°C/W using silicone grease.

The heat sink to ambient thermal resistance θ_{SA} depends on the quality of the heat sink and the ambient conditions.

Cooling is normally required to maintain the worst case operating junction temperature T_J of the device below the specified maximum value $T_{J(MAX)}$. T_J can be calculated from known operating conditions. Rewriting the above equation, we find:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \text{ } ^\circ\text{C/W}$$

$$T_J = T_A + P_D \theta_{JA} \text{ } ^\circ\text{C}$$

Where: P_D ($V_S - V_{OUT}$) $I_{OUT} + |V_+ - (V_-)|I_Q$ for a DC Signal

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ and $V_S =$ Supply Voltage
 θ_{JC} for the LH0101 is about 2°C/W.

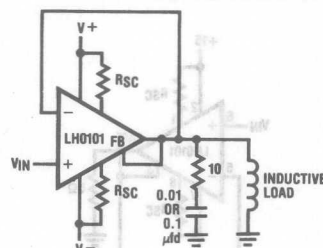
Stability and Compensation

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input device (usually the inverting input) to ac

ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

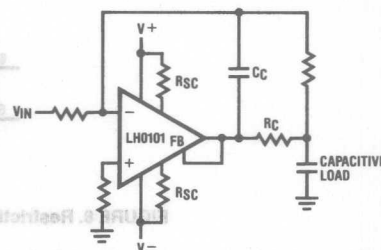
Some inductive loads may cause output stage oscillation. A .01 μF ceramic capacitor in series with a 10 Ω resistor from the output to ground will usually remedy this situation.



TL/K/5558-9

FIGURE 3. Driving Inductive Loads

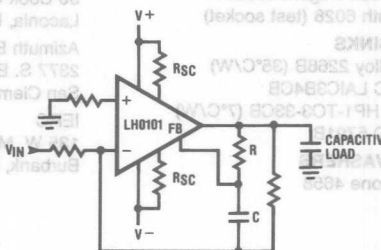
Capacitive loads may be compensated for by traditional techniques. (See "Operational Amplifiers: Theory and Practice" by Roberge, published by Wiley):



TL/K/5558-10

FIGURE 4. R_C and C_C Selected to Compensate for Capacitive Load

A similar but alternative technique may be used for the LH0101:



TL/K/5558-11

FIGURE 5. Alternate Compensation for Capacitive Load

Output Swing Enhancement

When the feedback pin is connected directly to the output, the output voltage swing is limited by the driver stage and not by output saturation. Output swing can be increased as shown by taking gain in the output stage as shown in High Power Voltage Follower with Swing Enhancement below. Whenever gain is taken in the output stage, as in swing enhancement, either the output stage, or the entire op amp must be appropriately compensated to account for the additional loop gain.

Typical Applications

See AN261 for more information.

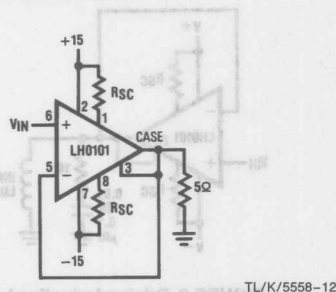


FIGURE 6. High Power Voltage Follower

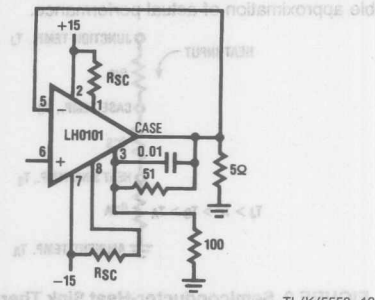


FIGURE 7. High Power Voltage Follower with Swing Enhancement

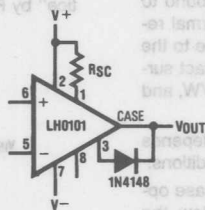


FIGURE 8. Restricting Outputs to Positive Voltages Only

Following is a partial list of sockets and heat dissipators for use with the LH0101. National assumes no responsibility for their quality or availability.

8-Lead TO-3 Hardware

SOCKETS

Keystone 4626 or 4627
Robinson Nugent 0002011
Azimuth 6028 (test socket)

HEAT SINKS

Thermalloy 2266B (35°C/W)
IERC LAIC3B4CB
IERC HP1-TO3-33CB (7°C/W)
AAVID 5791B

MICA WASHERS

Keystone 4658

AAVID Engineering
30 Cook Court
Laconia, New Hampshire 03246
Azimuth Electronics
2377 S. El Camino Real
San Clemente, CA 92572
IERC
135 W. Magnolia Blvd.
Burbank, CA 91502

Keystone Electronics Corp.
49 Bleecker St.
New York, NY 10012
Robinson Nugent Inc.
800 E. 8th St.
New Albany, IN 47150
Thermalloy
P.O. Box 34829
Dallas, TX 75234

Output Resistance

The open loop output resistance of the LH0101 is a function of the load current. No load output resistance is approximately 10Ω. This decreases to under 1Ω for load currents exceeding 100 mA.

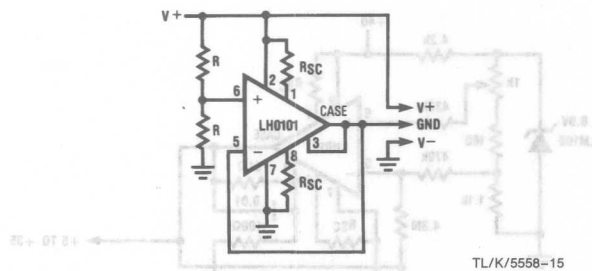


FIGURE 9. Generating a Split Supply from a Single Voltage Supply

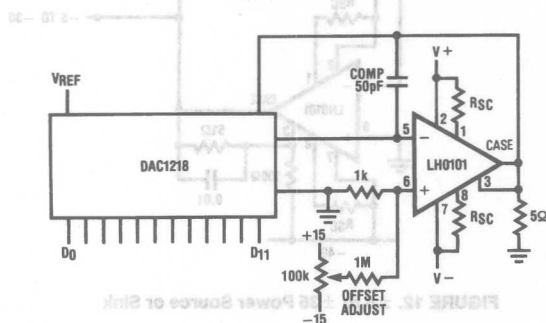


FIGURE 10. Power DAC

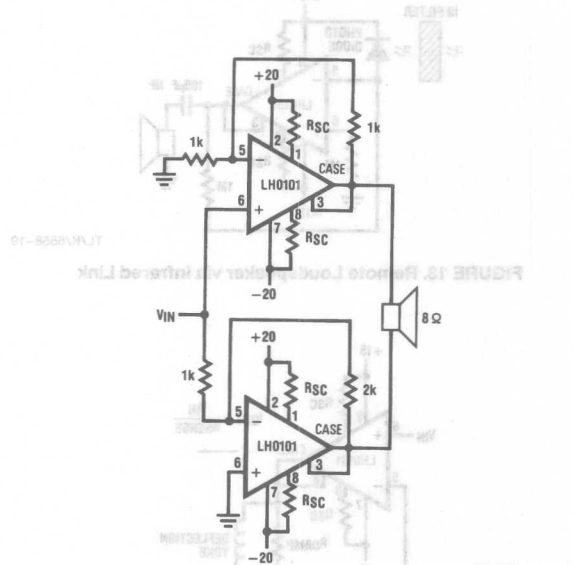
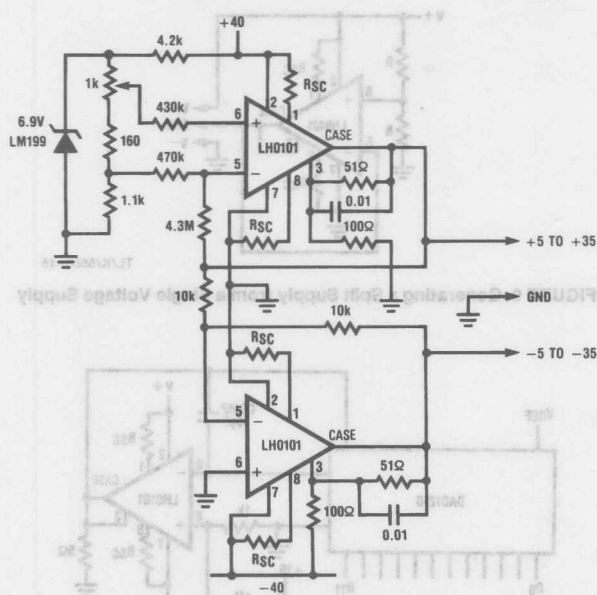


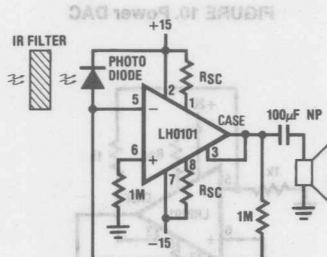
FIGURE 11. Bridge Audio Amplifier

Typical Applications (Continued)

(Continued)

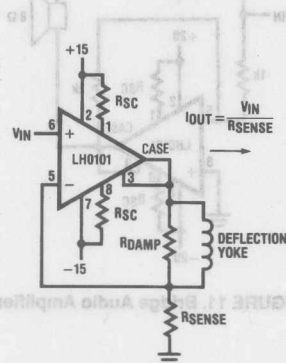


TL/K/5558-18

FIGURE 12. ± 5 to ± 35 Power Source or Sink

TL/K/5558-19

FIGURE 13. Remote Loudspeaker via Infrared Link



TL/K/5558-20

FIGURE 14. CRT Deflection Yoke Driver

Typical Applications (Continued)

LH0101

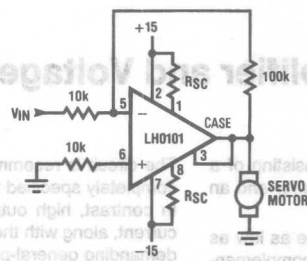


FIGURE 15. DC Servo Amplifier

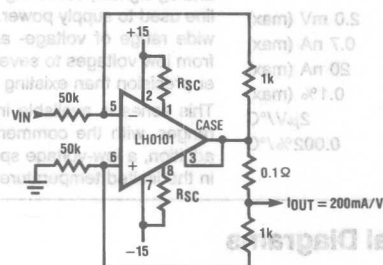
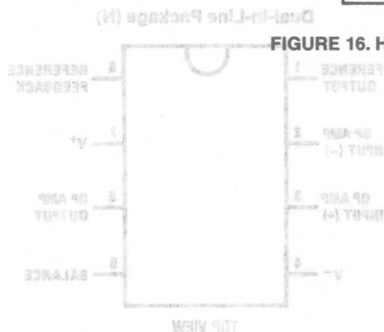
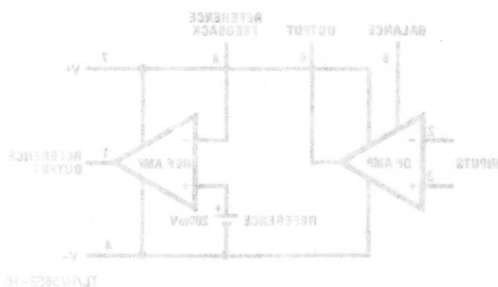


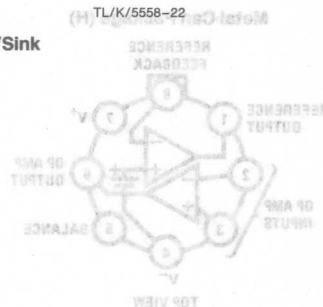
FIGURE 16. High Current Source/Sink



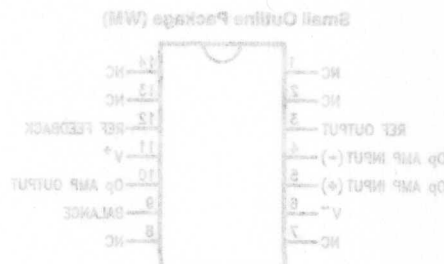
Order Number LM108N or LM108LM
See NS Package Number N08E



TLV4082-10



Order Number LM108N, LM108LM, LM108LM or LM108LM
available per SMA 3882-8790401
See NS Package Number N08A



Order Number LM108N or LM108LM
See NS Package Number M14B

LM10 Operational Amplifier and Voltage Reference

General Description

The LM10 series are monolithic linear ICs consisting of a precision reference, an adjustable reference buffer and an independent, high quality op amp.

The unit can operate from a total supply voltage as low as 1.1V or as high as 40V, drawing only 270 μ A. A complementary output stage swings within 15 mV of the supply terminals or will deliver ± 20 mA output current with ± 0.4 V saturation. Reference output can be as low as 200 mV. Some other characteristics of the LM10 are

| | |
|------------------------|-------------------------|
| ■ input offset voltage | 2.0 mV (max) |
| ■ input offset current | 0.7 nA (max) |
| ■ input bias current | 20 nA (max) |
| ■ reference regulation | 0.1% (max) |
| ■ offset voltage drift | 2 μ V/ $^{\circ}$ C |
| ■ reference drift | 0.002%/ $^{\circ}$ C |

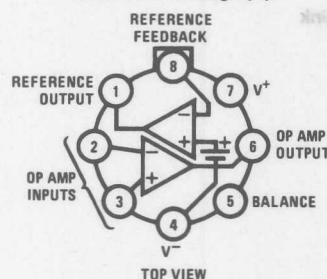
The circuit is recommended for portable equipment and is completely specified for operation from a single power cell. In contrast, high output-drive capability, both voltage and current, along with thermal overload protection, suggest it in demanding general-purpose applications.

The device is capable of operating in a floating mode, independent of fixed supplies. It can function as a remote comparator, signal conditioner, SCR controller or transmitter for analog signals, delivering the processed signal on the same line used to supply power. It is also suited for operation in a wide range of voltage- and current-regulator applications, from low voltages to several hundred volts, providing greater precision than existing ICs.

This series is available in the three standard temperature ranges, with the commercial part having relaxed limits. In addition, a low-voltage specification (suffix "L") is available in the limited temperature ranges at a cost savings.

Connection and Functional Diagrams

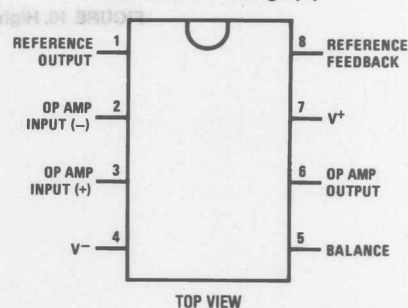
Metal Can Package (H)



TL/H/5652-1

Order Number LM10BH, LM10CH,
LM10CLH or LM10H/883
available per SMA # 5962-8760401
See NS Package Number H08A

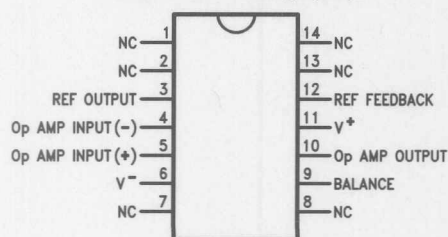
Dual-In-Line Package (N)



TL/H/5652-15

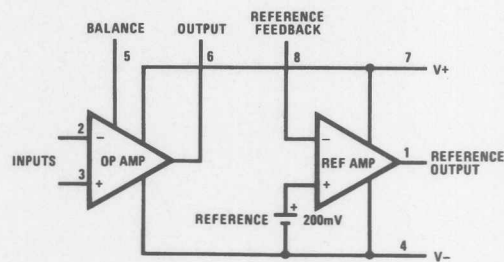
Order Number LM10CN or LM10CLN
See NS Package Number N08E

Small Outline Package (WM)



TL/H/5652-17

Order Number LM10CWM
See NS Package Number M14B



TL/H/5652-16

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

| | LM10/LM10B/ LM10BL/ LM10C | LM10CL |
|--|---------------------------|--------|
| Total Supply Voltage | 45V | 7V |
| Differential Input Voltage (note 1) | ±40V | ±7V |
| Power Dissipation (note 2) | internally limited | |
| Output Short-circuit Duration (note 3) | continuous | |
| Storage-Temp. Range | -55°C to +150°C | |
| Lead Temp. (Soldering, 10 seconds) | | |
| Metal Can | 300°C | |
| Lead Temp. (Soldering, 10 seconds) DIP | 260°C | |
| Vapor Phase (60 seconds) | 215°C | |
| Infrared (15 seconds) | 220°C | |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

Maximum Junction Temperature

| | |
|-------|-------|
| LM10 | 150°C |
| LM10B | 100°C |
| LM10C | 85°C |

Operating Ratings

Package Thermal Resistance

| | |
|---------------|---------|
| θ_{JA} | |
| H Package | 150°C/W |
| N Package | 87°C/W |
| WM Package | 90°C/W |
| θ_{JC} | |
| H Package | 45°C/W |

Electrical Characteristics

$T_J = 25^\circ\text{C}$, $T_{MIN} \leq T_J \leq T_{MAX}$ (note 4) (Boldface type refers to limits over temperature range)

| Parameter | Conditions | LM10/LM10B | | | LM10C | | | Units |
|-------------------------------|---|-------------------|-------|-----------------------|-------------------|-------|----------------------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input offset voltage | | | 0.3 | 2.0 3.0 | | 0.5 | 4.0 5.0 | mV mV |
| Input offset current (note 5) | | | 0.25 | 0.7 1.5 | | 0.4 | 2.0 3.0 | nA nA |
| Input bias current | | | 10 | 20 30 | | 12 | 30 40 | nA nA |
| Input resistance | | 250 150 | 500 | | 150 115 | 400 | | k Ω k Ω |
| Large signal voltage gain | $V_S = \pm 20\text{V}$, $I_{OUT} = 0$ | 120 | 400 | | 80 | 400 | | V/mV |
| | $V_{OUT} = \pm 19.95\text{V}$ | 80 | | | 50 | | | V/mV |
| | $V_S = \pm 20\text{V}$, $V_{OUT} = \pm 19.4\text{V}$ | 50 | 130 | | 25 | 130 | | V/mV |
| | $I_{OUT} = \pm 20\text{ mA}$ ($\pm 15\text{ mA}$) | 20 | | | 15 | | | V/mV |
| | $V_S = \pm 0.6\text{V}$ (0.65V), $I_{OUT} = \pm 2\text{ mA}$ | 1.5 | 3.0 | | 1.0 | 3.0 | | V/mV |
| | $V_{OUT} = \pm 0.4\text{V}$ ($\pm 0.3\text{V}$), $V_{CM} = -0.4\text{V}$ | 0.5 | | | 0.75 | | | V/mV |
| Shunt gain (note 6) | 1.2V (1.3V) $\leq V_{OUT} \leq 40\text{V}$, $R_L = 1.1\text{ k}\Omega$ | 14 | 33 | | 10 | 33 | | V/mV |
| | $0.1\text{ mA} \leq I_{OUT} \leq 5\text{ mA}$ | 6 | | | 6 | | | V/mV |
| | $1.5\text{V} \leq V^+ \leq 40\text{V}$, $R_L = 250\Omega$ | 8 | 25 | | 6 | 25 | | V/mV |
| | $0.1\text{ mA} \leq I_{OUT} \leq 20\text{ mA}$ | 4 | | | 4 | | | V/mV |
| Common-mode rejection | $-20\text{V} \leq V_{CM} \leq 19.15\text{V}$ (19V) $V_S = \pm 20\text{V}$ | 93 87 | 102 | | 90 87 | 102 | | dB dB |
| | $-0.2\text{V} \geq V^- \geq -39\text{V}$ $V^+ = 1.0\text{V}$ (1.1V) | 90 84 | 96 | | 87 84 | 96 | | dB dB |
| Supply-voltage rejection | 1.0V (1.1V) $\leq V^+ \leq 39.8\text{V}$ | 96 90 | 106 | | 93 90 | 106 | | dB dB |
| | $V^- = -0.2\text{V}$ | | | | | | | |
| Offset voltage drift | | | 2.0 | | | 5.0 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset current drift | | | 2.0 | | | 5.0 | | pA/ $^\circ\text{C}$ |
| Bias current drift | $T_C < 100^\circ\text{C}$ | | 60 | | | 90 | | pA/ $^\circ\text{C}$ |
| Line regulation | 1.2V (1.3V) $\leq V_S \leq 40\text{V}$ $0 \leq I_{REF} \leq 1.0\text{ mA}$, $V_{REF} = 200\text{ mV}$ | | 0.001 | 0.003 0.006 | | 0.001 | 0.008 0.01 | %/V %/V |
| | $0 \leq I_{REF} \leq 1.0\text{ mA}$ $V^+ - V_{REF} \geq 1.0\text{V}$ (1.1V) | | 0.01 | 0.1 0.15 | | 0.01 | 0.15 0.2 | % % |

| Parameter | Conditions | LM10/LM10B | | | LM10C | | | Units |
|------------------------|---------------------------------|-------------------|-------|-------------------|-------------------|-------|-------------------|--------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Amplifier gain | $0.2V \leq V_{REF} \leq 35V$ | 50 23 | 75 | | 25 15 | 70 | | V/mV V/mV |
| Feedback sense voltage | | 195 194 | 200 | 205 206 | 190 189 | 200 | 210 211 | mV mV |
| Feedback current | | | 20 | 50 65 | | 22 | 75 90 | nA nA |
| Reference drift | | | 0.002 | | | 0.003 | | %/°C |
| Supply current | | | 270 | 400 500 | | 300 | 500 570 | μA μA |
| Supply current change | $1.2V (1.3V) \leq V_S \leq 40V$ | | 15 | 75 | | 15 | 75 | μA |

| Parameter | Conditions | LM10BL | | | LM10CL | | | Units |
|-------------------------------|--|-------------------|-------|-------------------|-------------------|-------------------|-------------|--------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input offset voltage | | | 0.3 | 2.0 3.0 | 0.5 | 4.0 5.0 | | mV mV |
| Input offset current (note 5) | | | 0.1 | 0.7 1.5 | 0.2 | 2.0 3.0 | | nA nA |
| Input bias current | | | 10 | 20 30 | 12 | 30 40 | | nA nA |
| Input resistance | | 250 150 | 500 | | 150 115 | 400 | | kΩ kΩ |
| Large signal voltage gain | $V_S = \pm 3.25V, I_{OUT} = 0$ | 60 | 300 | | 40 | 300 | | V/mV |
| | $V_{OUT} = \pm 3.2V$ | 40 | | | 25 | | | V/mV |
| | $V_S = \pm 3.25V, I_{OUT} = 10\text{ mA}$ | 10 | 25 | | 5 | 25 | | V/mV |
| | $V_{OUT} = \pm 2.75V$ | 4 | | | 3 | | | V/mV |
| | $V_S = \pm 0.6V (0.65V), I_{OUT} = \pm 2\text{ mA}$ | 1.5 | 3.0 | | 1.0 | 3.0 | | V/mV |
| Shunt gain (note 6) | $V_{OUT} = \pm 0.4V (\pm 0.3V), V_{CM} = -0.4V$ | 0.5 | | | 0.75 | | | V/mV |
| | | | | | | | | V/mV |
| Common-mode rejection | $1.5V \leq V^+ \leq 6.5V, R_L = 500\Omega$ | 8 | 30 | | 6 | 30 | | V/mV |
| | $0.1\text{ mA} \leq I_{OUT} \leq 10\text{ mA}$ | 4 | | | 4 | | | V/mV |
| Supply-voltage rejection | $-3.25V \leq V_{CM} \leq 2.4V (2.25V)$ | 89 | 102 | | 80 | 102 | | dB |
| | $V_S = \pm 3.25V$ | 83 | | | 74 | | | dB |
| Offset voltage drift | $-0.2V \geq V^- \geq -5.4V$ | 86 | 96 | | 80 | 96 | | dB |
| | $V^+ = 1.0V (1.2V)$ | 80 | | | 74 | | | dB |
| | $1.0V (1.1V) \leq V^+ \leq 6.3V$ | 94 | 106 | | 80 | 106 | | dB |
| Offset current drift | $V^- = 0.2V$ | 88 | | | 74 | | | dB |
| Offset voltage drift | | | 2.0 | | | 5.0 | | μV/°C |
| Offset current drift | | | 2.0 | | | 5.0 | | pA/°C |
| Bias current drift | | | 60 | | | 90 | | pA/°C |
| Line regulation | $1.2V (1.3V) \leq V_S \leq 6.5V$ | | 0.001 | 0.01 | | 0.001 | 0.02 | %/V |
| | $0 \leq I_{REF} \leq 0.5\text{ mA}, V_{REF} = 200\text{ mV}$ | | | 0.02 | | | 0.03 | %/V |
| Load regulation | $0 \leq I_{REF} \leq 0.5\text{ mA}$ | | 0.01 | 0.1 | | 0.01 | 0.15 | % |
| | $V^+ - V_{REF} \geq 1.0V (1.1V)$ | | | 0.15 | | | 0.2 | % |
| Amplifier gain | $0.2V \leq V_{REF} \leq 5.5V$ | 30 20 | 70 | | 20 15 | 70 | | V/mV V/mV |

Electrical Characteristics

$T_J = 25^\circ\text{C}$, $T_{\text{MIN}} \leq T_J \leq T_{\text{MAX}}$, (note 4) (**Boldface type refers to limits over temperature range**) (Continued)

| Parameter | Conditions | LM10BL | | | LM10CL | | | Units |
|------------------------|------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|--------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Feedback sense voltage | | 195 194 | 200 | 205 206 | 190 189 | 200 | 210 211 | mV mV |
| Feedback current | | | 20 | 50 65 | | 22 | 75 90 | nA nA |
| Reference drift | | | 0.002 | | | 0.003 | | %/ $^\circ\text{C}$ |
| Supply current | | | 260 500 | | | 280 570 | | μA μA |

Note 1: The input voltage can exceed the supply voltages provided that the voltage from the input to any other terminal does not exceed the maximum differential input voltage and excess dissipation is accounted for when $V_{\text{IN}} < V^-$.

Note 2: The maximum, operating-junction temperature is 150°C for the LM10, 100°C for the LM10B(L) and 85°C for the LM10C(L). At elevated temperatures, devices must be derated based on package thermal resistance.

Note 3: Internal thermal limiting prevents excessive heating that could result in sudden failure, but the IC can be subjected to accelerated stress with a shorted output and worst-case conditions.

Note 4: These specifications apply for $V^- \leq V_{\text{CM}} \leq V^+ - 0.85\text{V}$ (1.0V), 1.2V (1.3V) $< V_S \leq V_{\text{MAX}}$, $V_{\text{REF}} = 0.2\text{V}$ and $0 \leq I_{\text{REF}} \leq 1.0\text{ mA}$, unless otherwise specified: $V_{\text{MAX}} = 40\text{V}$ for the standard part and 6.5V for the low voltage part. Normal typeface indicates 25°C limits. **Boldface type indicates limits and altered test conditions for full-temperature-range operation**; this is -55°C to 125°C for the LM10, -25°C to 85°C for the LM10B(L) and 0°C to 70°C for the LM10C(L). The specifications do not include the effects of thermal gradients ($\tau_1 \approx 20\text{ ms}$), die heating ($\tau_2 \approx 0.2\text{ s}$) or package heating. Gradient effects are small and tend to offset the electrical error (see curves).

Note 5: For $T_J > 90^\circ\text{C}$, I_{OS} may exceed 1.5 nA for $V_{\text{CM}} = V^-$. With $T_J = 125^\circ\text{C}$ and $V^- \leq V_{\text{CM}} \leq V^+ + 0.1\text{V}$, $I_{\text{OS}} \leq 5\text{ nA}$.

Note 6: This defines operation in floating applications such as the bootstrapped regulator or two-wire transmitter. Output is connected to the V^+ terminal of the IC and input common mode is referred to V^- (see typical applications). Effect of larger output-voltage swings with higher load resistance can be accounted for by adding the positive-supply rejection error.

Note 7: Refer to RETS10X for LM10H military specifications.

Definition of Terms

Input offset voltage: That voltage which must be applied between the input terminals to bias the unloaded output in the linear region.

Input offset current: The difference in the currents at the input terminals when the unloaded output is in the linear region.

Input bias current: The absolute value of the average of the two input currents.

Input resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Large signal voltage gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it.

Shunt gain: The ratio of the specified output voltage swing to the change in differential input voltage required to produce it with the output tied to the V^+ terminal of the IC. The load and power source are connected between the V^+ and V^- terminals, and input common-mode is referred to the V^- terminal.

Common-mode rejection: The ratio of the input voltage range to the change in offset voltage between the extremes.

Supply-voltage rejection: The ratio of the specified supply-voltage change to the change in offset voltage between the extremes.

Line regulation: The average change in reference output voltage over the specified supply voltage range.

Load regulation: The change in reference output voltage from no load to that load specified.

Feedback sense voltage: The voltage, referred to V^- , on the reference feedback terminal while operating in regulation.

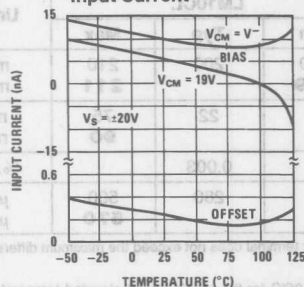
Reference amplifier gain: The ratio of the specified reference output change to the change in feedback sense voltage required to produce it.

Feedback current: The absolute value of the current at the feedback terminal when operating in regulation.

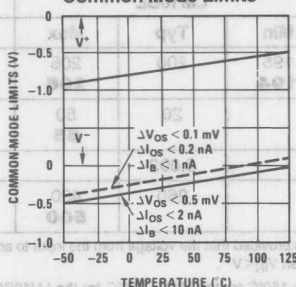
Supply current: The current required from the power source to operate the amplifier and reference with their outputs unloaded and operating in the linear range.

Typical Performance Characteristics (Op Amp)

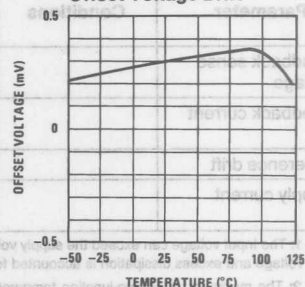
Input Current



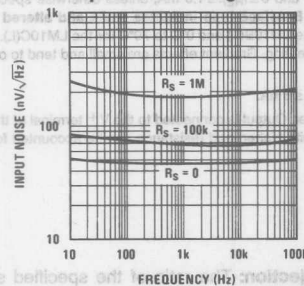
Common Mode Limits



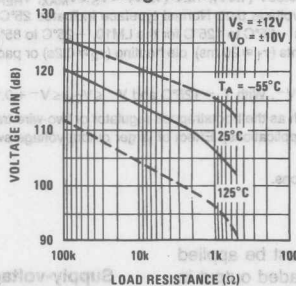
Offset Voltage Drift



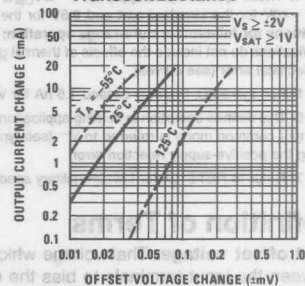
Input Noise Voltage



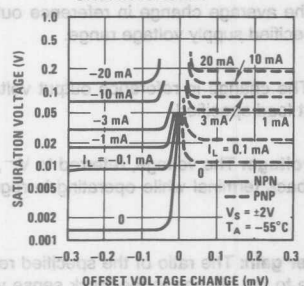
DC Voltage Gain



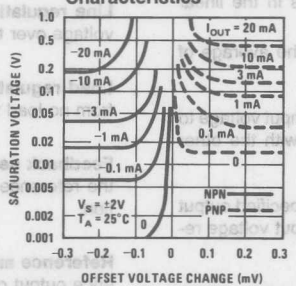
Transconductance



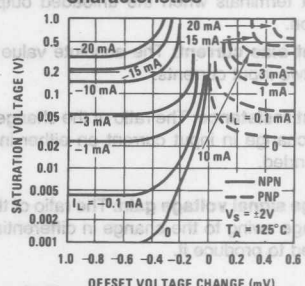
Output Saturation Characteristics



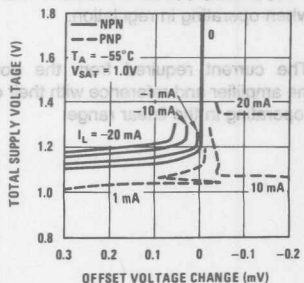
Output Saturation Characteristics



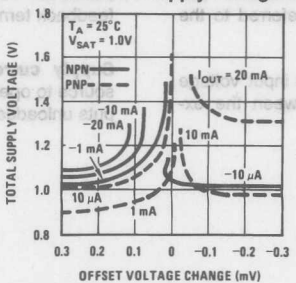
Output Saturation Characteristics



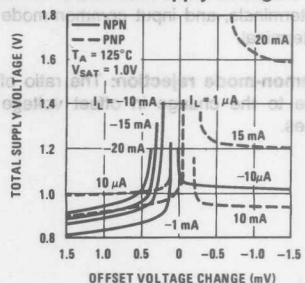
Minimum Supply Voltage



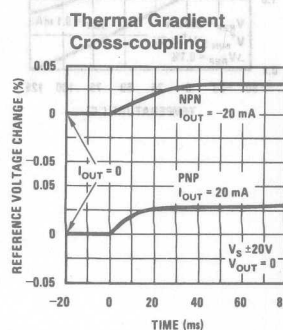
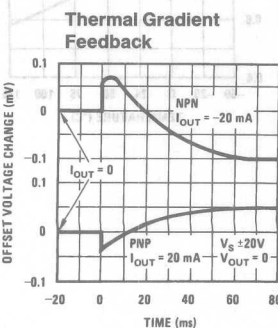
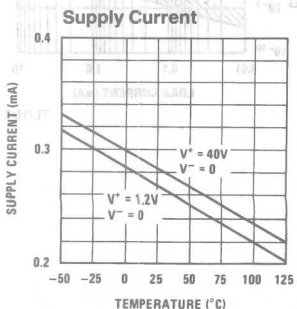
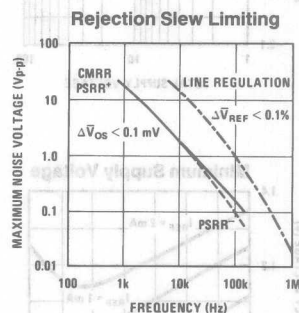
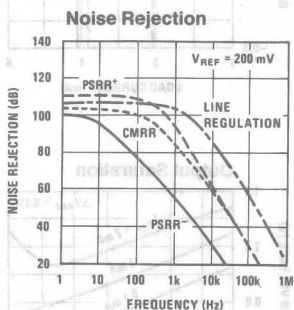
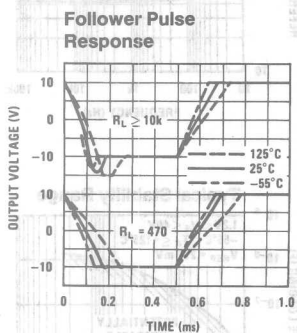
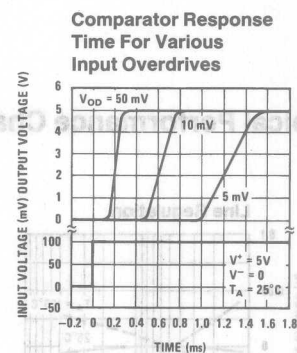
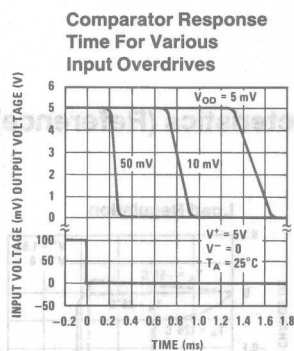
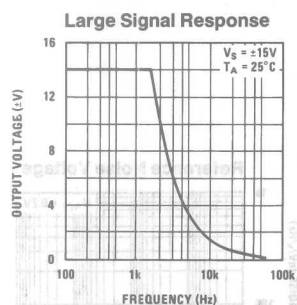
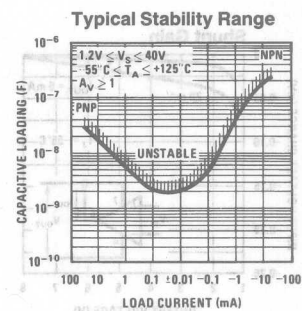
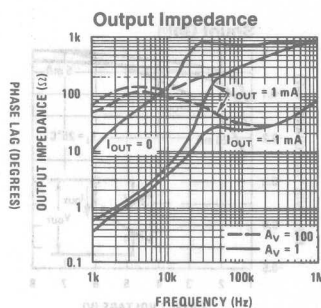
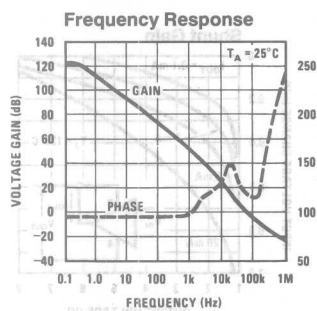
Minimum Supply Voltage

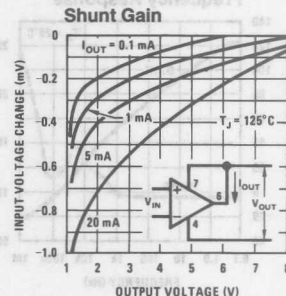
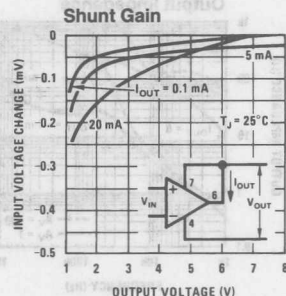
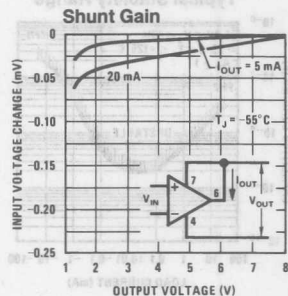


Minimum Supply Voltage



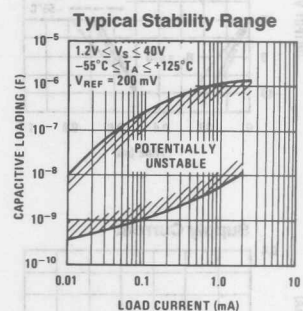
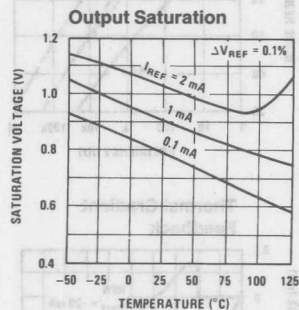
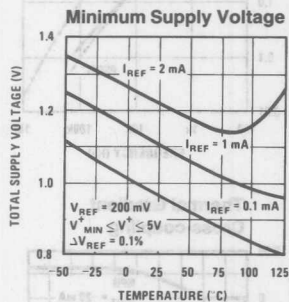
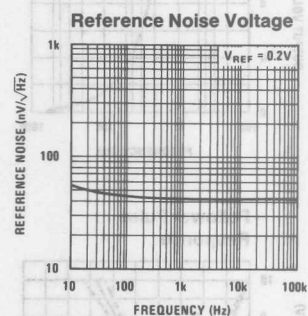
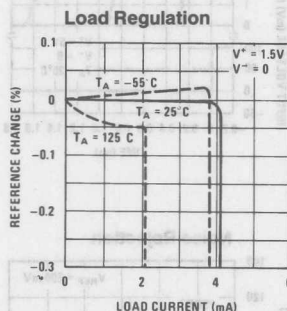
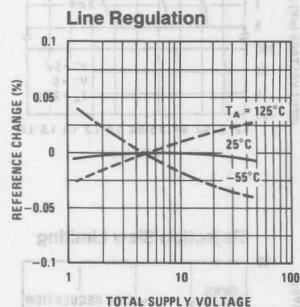
Typical Performance Characteristics (Op Amp) (Continued)





TL/H/5652-4

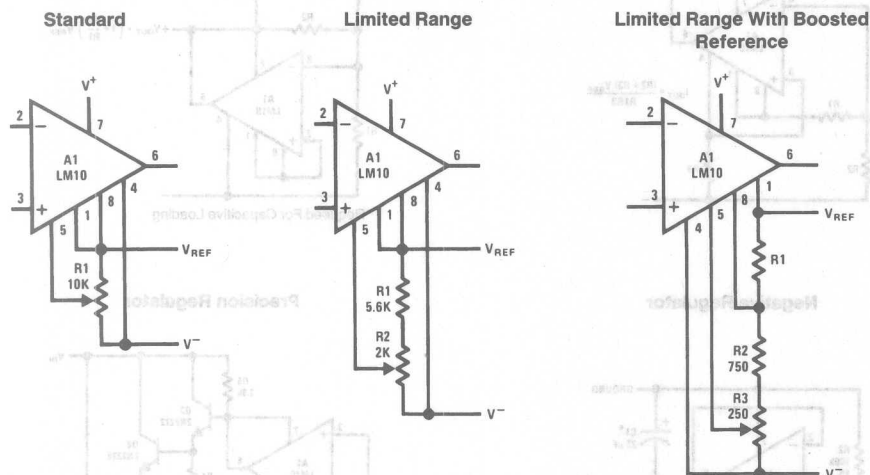
Typical Performance Characteristics (Reference)



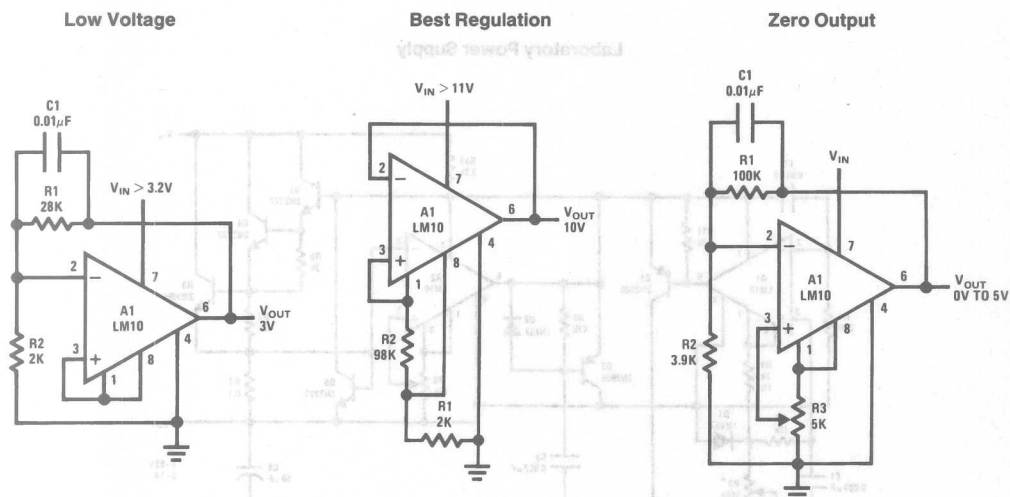
TL/H/5652-5

Typical Applications^{††} (Pin numbers are for devices in 8-pin packages)

Op Amp Offset Adjustment



Positive Regulators[†]



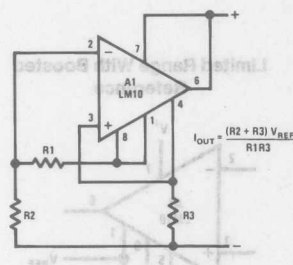
[†]Use only electrolytic output capacitors.

^{††}Circuit descriptions available in application note AN-211.

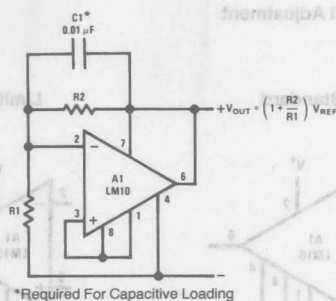
TL/H/5652-6

Typical Applications^{††} (Pin numbers are for devices in 8-pin packages) (Continued)

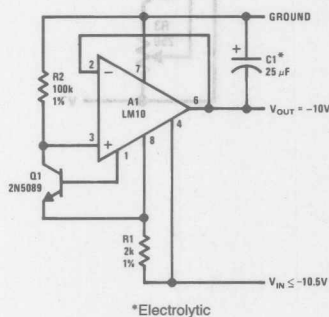
Current Regulator



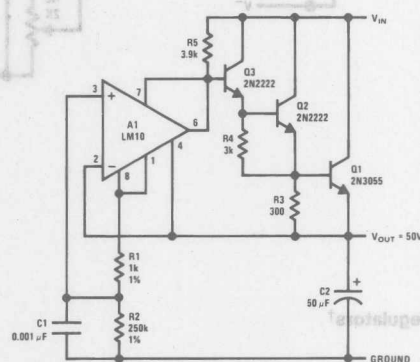
Shunt Regulator



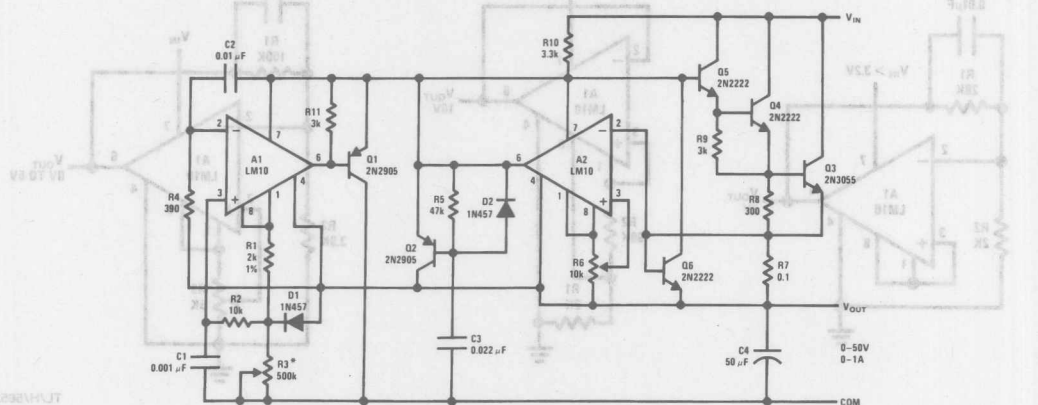
Negative Regulator



Precision Regulator



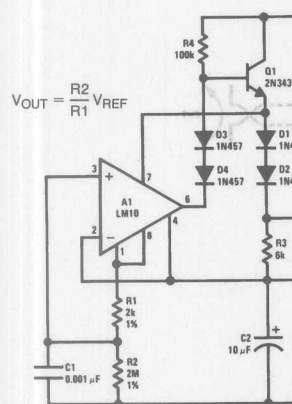
Laboratory Power Supply



$$*V_{OUT} = 10^{-4} R3$$

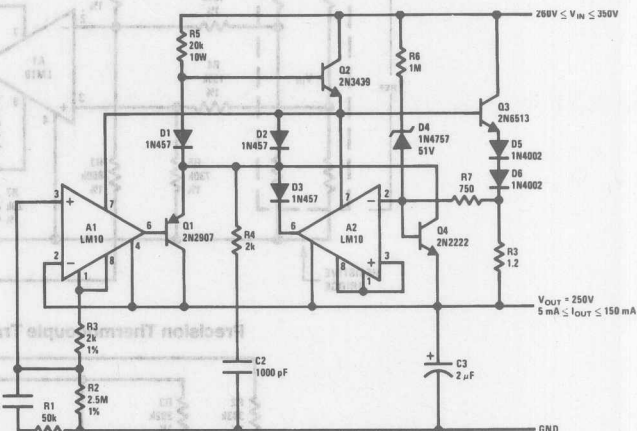
^{††}Circuit descriptions available in application note AN-211.

HV Regulator

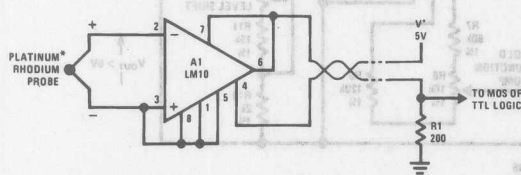


$$V_{OUT} = \frac{R_2}{R_1} V_{REF}$$

Protected HV Regulator

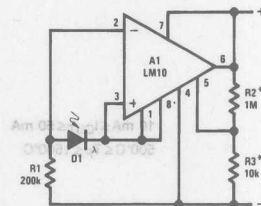


Flame Detector



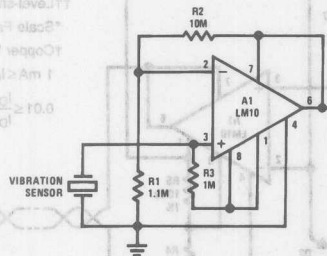
*800°C Threshold Is Established By Connecting Balance To V_{REF} .

Light Level Sensor

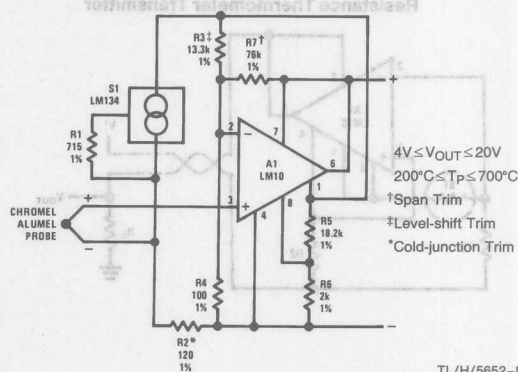


*Provides Hysteresis

Remote Amplifier



Remote Thermocouple Amplifier

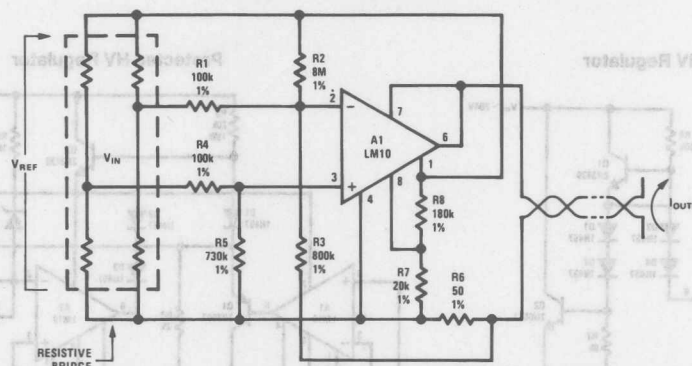

$$4V \leq V_{OUT} \leq 20V$$
$$200^{\circ}C \leq T_P \leq 700^{\circ}C$$

†Span Trim
‡Level-shift Trim
*Cold-junction Trim

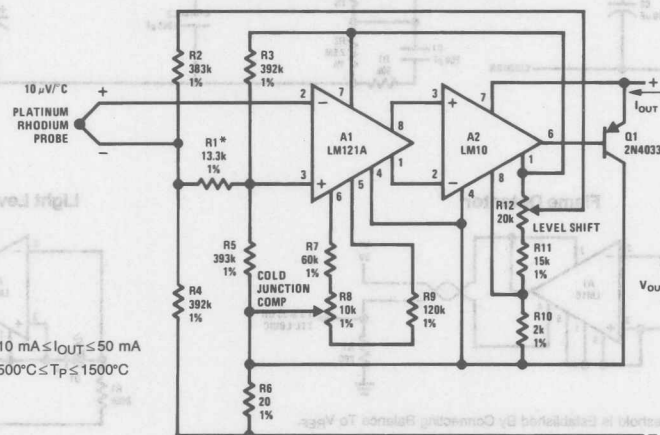
TL/H/5652-8

Typical Applications ^{††} (Pin numbers are for devices in 8-pin packages) (Continued)

Transmitter for Bridge Sensor

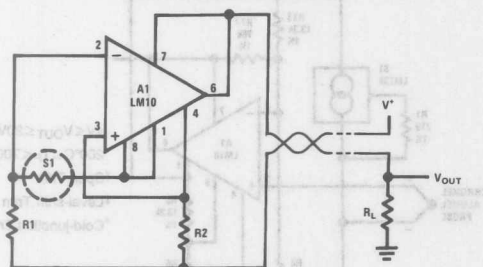


Precision Thermocouple Transmitter



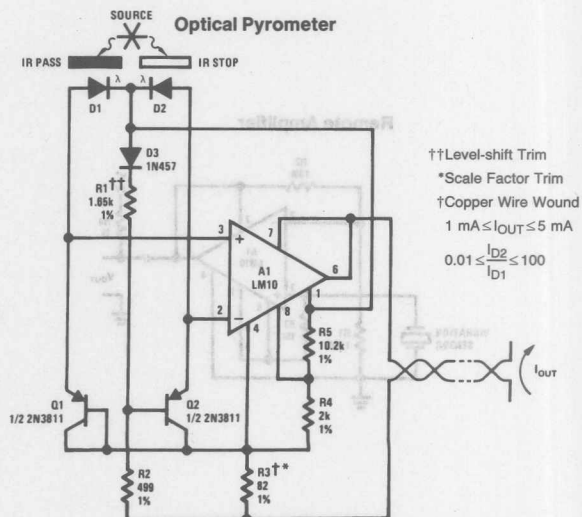
*Gain Trim

Resistance Thermometer Transmitter



^{††}Circuit descriptions available in application note AN-211.

Optical Pyrometer



^{††}Level-shift Trim

*Scale Factor Trim

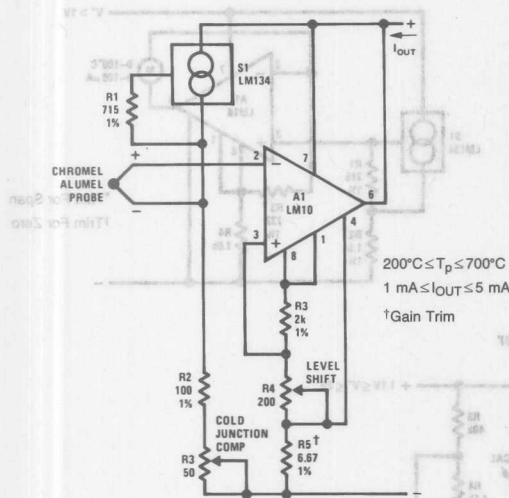
[†]Copper Wire Wound

1 mA ≤ IOUT ≤ 5 mA

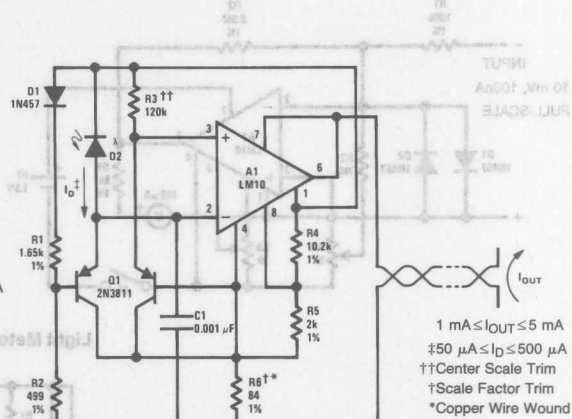
$0.01 \leq \frac{I_{D2}}{I_{D1}} \leq 100$

TL/H/5652-9

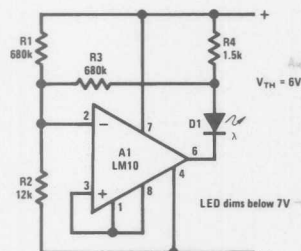
Thermocouple Transmitter



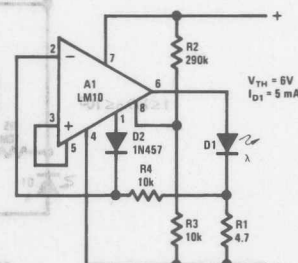
Logarithmic Light Sensor



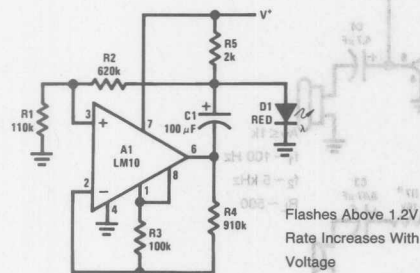
Battery-level Indicator



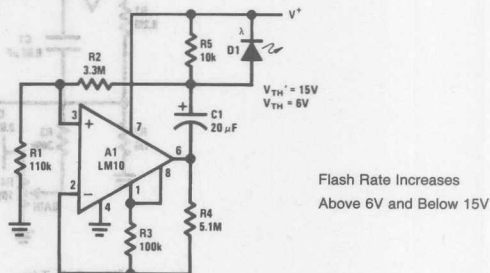
Battery-threshold Indicator



Single-cell Voltage Monitor



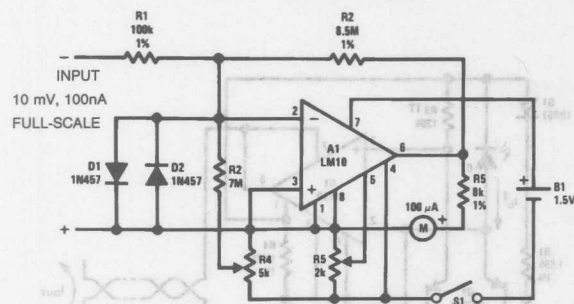
Double-ended Voltage Monitor



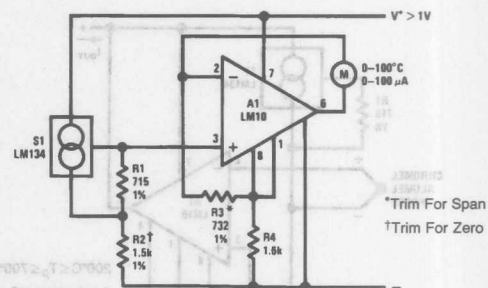
TL/H/5652-10

†† Circuit descriptions available in application note AN-211.

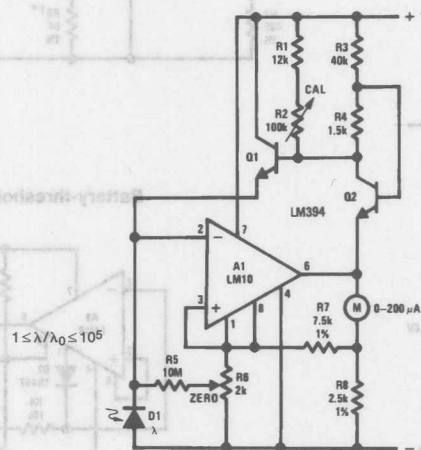
meter Amplifier



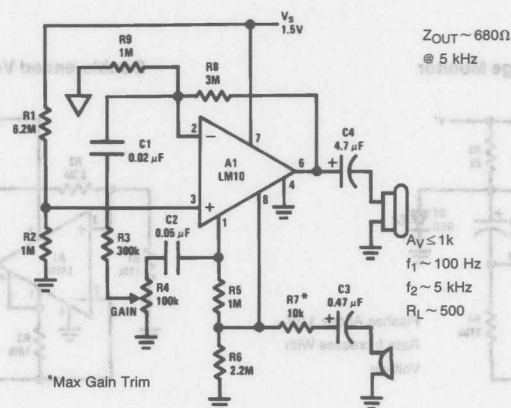
Thermometer



Light Meter



Microphone Amplifier

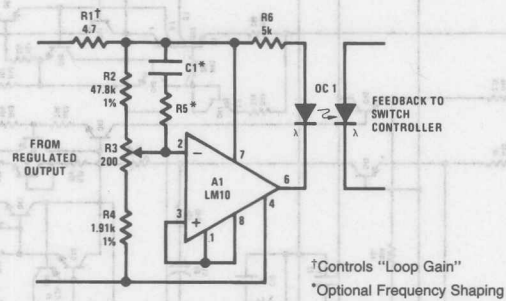


††Circuit descriptions available in application note AN-211.

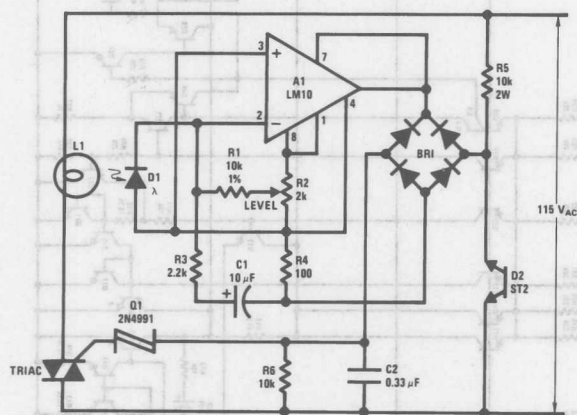
Typical Applications ^{††} (Pin numbers are for devices in 8-pin packages) (Continued)

LM10

Isolated Voltage Sensor



Light-level Controller



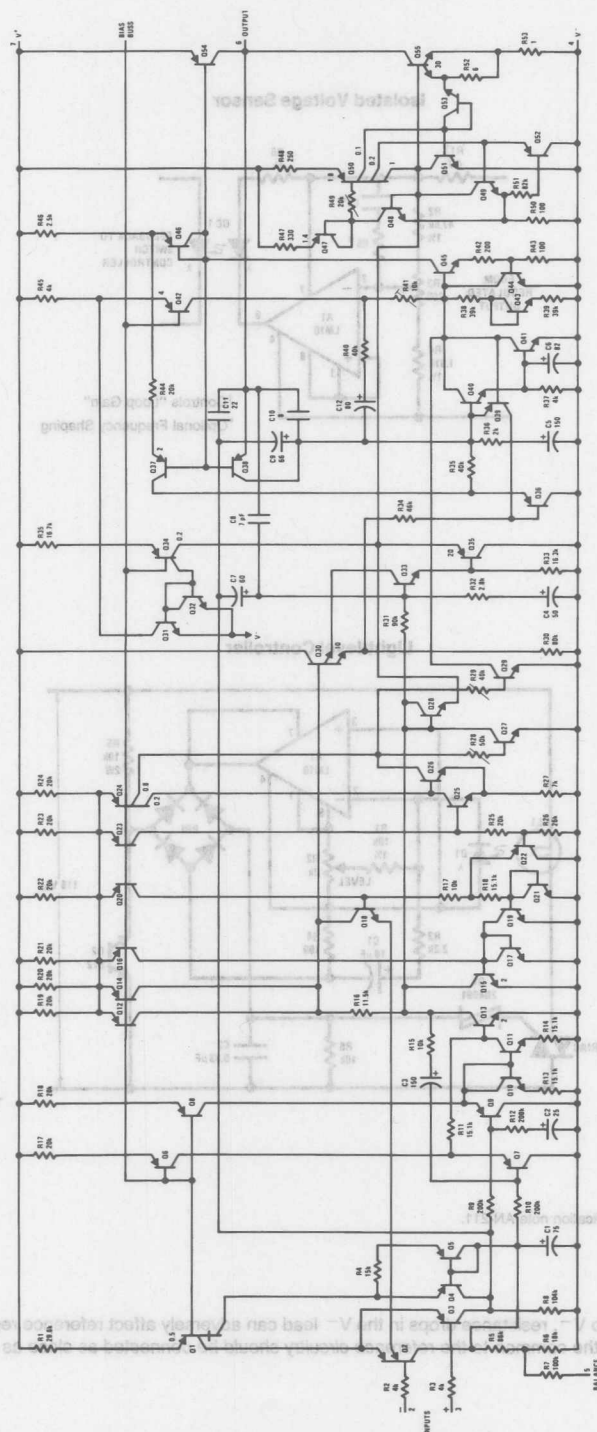
TL/H/5652-12

^{††}Circuit descriptions available in application note AN-211.

Application Hints

With heavy amplifier loading to V^- , resistance drops in the V^- lead can adversely affect reference regulation. Lead resistance can approach 1Ω . Therefore, the common to the reference circuitry should be connected as close as possible to the package.

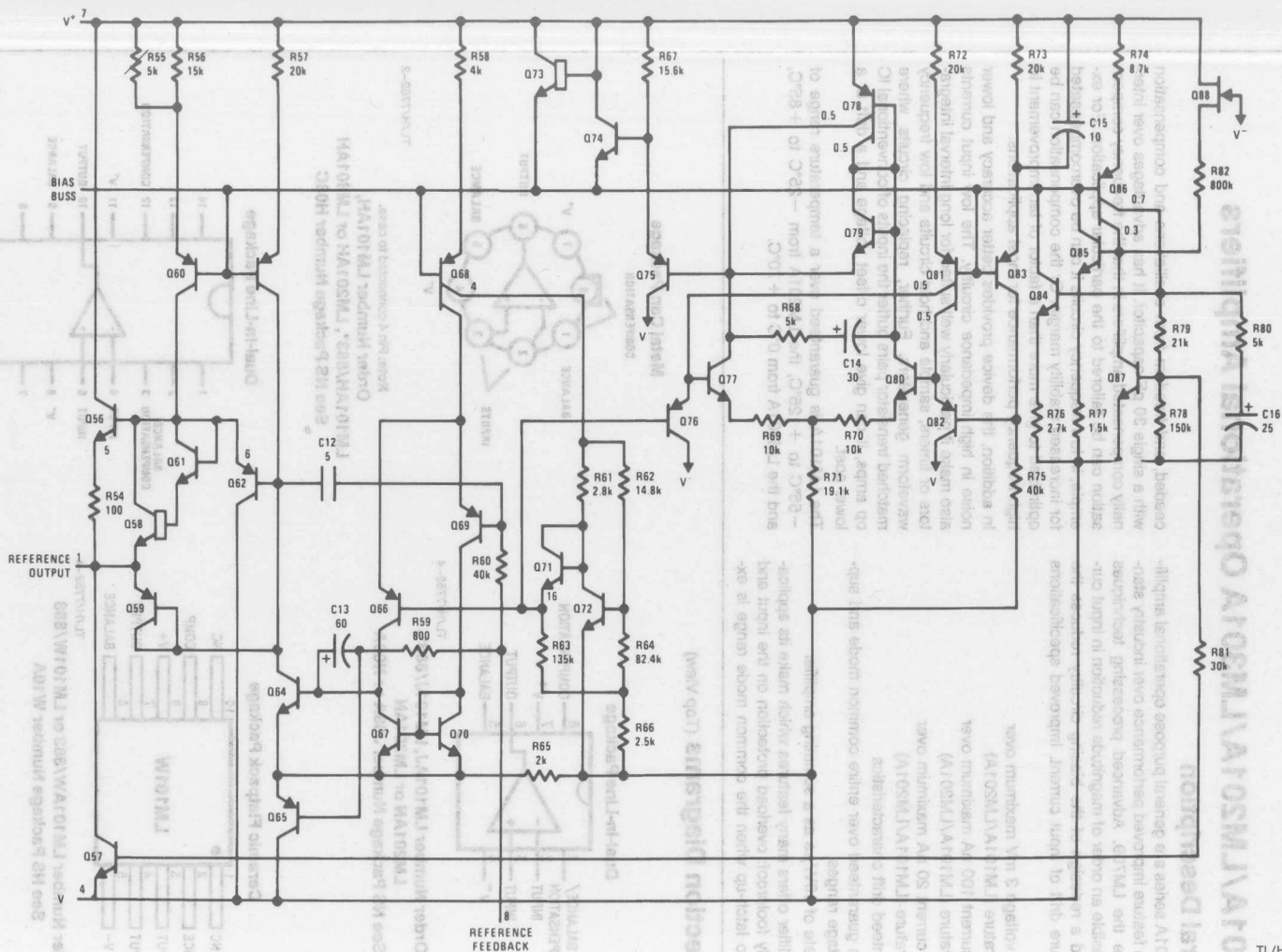
Typical Applications



TL/H/5652-13

Reference and Internal Regulator (Pin numbers are for 8-pin packages)

TL/H/5652-14



LM101A/LM201A/LM301A Operational Amplifiers

General Description

The LM101A series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature (LM101A/LM201A)
- Input current 100 nA maximum over temperature (LM101A/LM201A)
- Offset current 20 nA maximum over temperature (LM101A/LM201A)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of $10\text{V}/\mu\text{s}$ as a summing amplifier

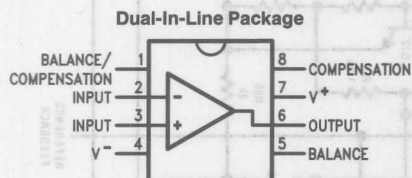
This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is ex-

ceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

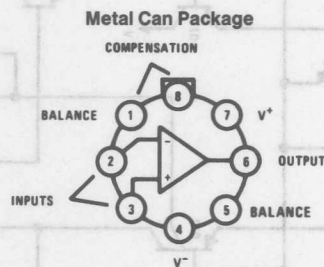
The LM101A is guaranteed over a temperature range of -55°C to $+125^{\circ}\text{C}$, the LM201A from -25°C to $+85^{\circ}\text{C}$, and the LM301A from 0°C to $+70^{\circ}\text{C}$.

Connection Diagrams (Top View)



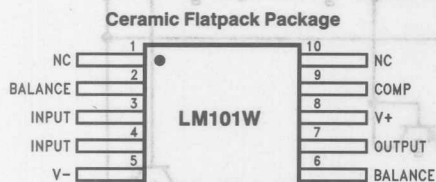
Order Number LM101AJ, LM101J/883*,
LM201AN or LM301AN
See NS Package Number J08A or N08A

TL/H/7752-4



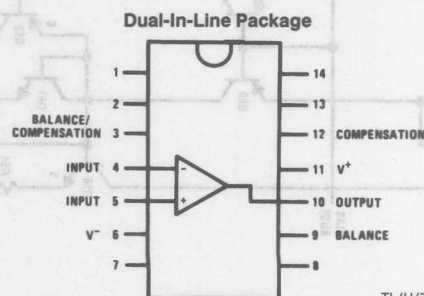
Note: Pin 4 connected to case.
Order Number LM101AH,
LM101AH/883*, LM201AH or LM301AH
See NS Package Number H08C

TL/H/7752-2



Order Number LM101AW/883 or LM101W/883
See NS Package Number W10A

TL/H/7752-4



Order Number LM101AJ-14/883*
See NS Package Number J14A

TL/H/7752-3

*Available per JM38510/10103.

Distributors for availability and specifications.

| | | LM101A/LM201A | | LM301A | |
|--|--|---|--|-----------------------------------|--|
| Supply Voltage | | $\pm 22V$ | | $\pm 18V$ | |
| Differential Input Voltage | | $\pm 30V$ | | $\pm 30V$ | |
| Input Voltage (Note 1) | | $\pm 15V$ | | $\pm 15V$ | |
| Output Short Circuit Duration (Note 2) | | Continuous | | Continuous | |
| Operating Ambient Temp. Range | | $-55^{\circ}C$ to $+125^{\circ}C$ (LM101A) $-25^{\circ}C$ to $+85^{\circ}C$ (LM201A) | | $0^{\circ}C$ to $+70^{\circ}C$ | |
| T_J Max | | $150^{\circ}C$ | | $100^{\circ}C$ | |
| H-Package | | $150^{\circ}C$ | | $100^{\circ}C$ | |
| N-Package | | $150^{\circ}C$ | | $100^{\circ}C$ | |
| J-Package | | $150^{\circ}C$ | | $100^{\circ}C$ | |
| Power Dissipation at $T_A = 25^{\circ}C$ | | 500 mW | | 300 mW | |
| H-Package (Still Air) | | 1200 mW | | 700 mW | |
| (400 LF/Min Air Flow) | | 900 mW | | 500 mW | |
| N-Package | | 1000 mW | | 650 mW | |
| J-Package | | | | | |
| Thermal Resistance (Typical) θ_{JA} | | $165^{\circ}C/W$ | | $165^{\circ}C/W$ | |
| H-Package (Still Air) | | $67^{\circ}C/W$ | | $67^{\circ}C/W$ | |
| (400 LF/Min Air Flow) | | $135^{\circ}C/W$ | | $135^{\circ}C/W$ | |
| N Package | | $110^{\circ}C/W$ | | $110^{\circ}C/W$ | |
| J-Package | | | | | |
| (Typical) θ_{JC} | | $25^{\circ}C/W$ | | $25^{\circ}C/W$ | |
| H-Package | | $-65^{\circ}C$ to $+150^{\circ}C$ | | $-65^{\circ}C$ to $+150^{\circ}C$ | |
| Storage Temperature Range | | 300°C | | 300°C | |
| Lead Temperature (Soldering, 10 sec.) | | 260°C | | 260°C | |
| Metal Can or Ceramic | | 2000V | | 2000V | |
| Plastic | | | | | |
| ESD Tolerance (Note 5) | | | | | |

Electrical Characteristics (Note 3) $T_A = T_J$

| Parameter | Conditions | LM101A/LM201A | | | LM301A | | | Units |
|---|---|-----------------|------|-----|--------|------|-----|-------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^{\circ}C, R_S \leq 50 k\Omega$ | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A = 25^{\circ}C$ | | 1.5 | 10 | | 3.0 | 50 | nA |
| Input Bias Current | $T_A = 25^{\circ}C$ | | 30 | 75 | | 70 | 250 | nA |
| Input Resistance | $T_A = 25^{\circ}C$ | 1.5 | 4.0 | | 0.5 | 2.0 | | M Ω |
| Supply Current | $T_A = 25^{\circ}C$ | $V_S = \pm 20V$ | | 1.8 | 3.0 | | | mA |
| | | $V_S = \pm 15V$ | | | | 1.8 | 3.0 | |
| Large Signal Voltage Gain | $T_A = 25^{\circ}C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 2 k\Omega$ | 50 | 160 | | 25 | 160 | | V/mV |
| Input Offset Voltage | $R_S \leq 50 k\Omega$ | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $R_S \leq 50 k\Omega$ | | 3.0 | 15 | | 6.0 | 30 | $\mu V/^{\circ}C$ |
| Input Offset Current | | | | 20 | | | 70 | nA |
| Average Temperature Coefficient of Input Offset Current | $25^{\circ}C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25^{\circ}C$ | | 0.01 | 0.1 | | 0.01 | 0.3 | nA/ $^{\circ}C$ |
| | | | 0.02 | 0.2 | | 0.02 | 0.6 | |

Electrical Characteristics (Note 3) $T_A = T_J$ (Continued)

| Parameter | Conditions | LM101A/LM201A | | | LM301A | | | Units |
|--------------------------------|--|-------------------|----------|----------|----------|----------|-----|---------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Bias Current | | | | 0.1 | | | 0.3 | μA |
| Supply Current | $T_A = T_{MAX}$, $V_S = \pm 20V$ | | 1.2 | 2.5 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$ | $R_L = 10k\Omega$ | ± 12 | ± 14 | ± 12 | ± 14 | | V |
| | | $R_L = 2k\Omega$ | ± 10 | ± 13 | ± 10 | ± 13 | | V |
| Input Voltage Range | $V_S = \pm 20V$ | ± 15 | | | | | | V |
| | $V_S = \pm 15V$ | | +15, -13 | | ± 12 | +15, -13 | | V |
| Common-Mode Rejection Ratio | $R_S \leq 50k\Omega$ | 80 | 96 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 50k\Omega$ | 80 | 96 | | 70 | 96 | | dB |

Note 1: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

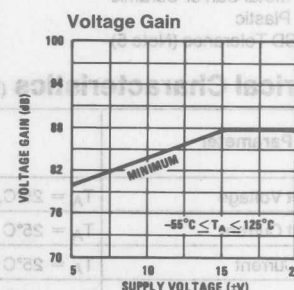
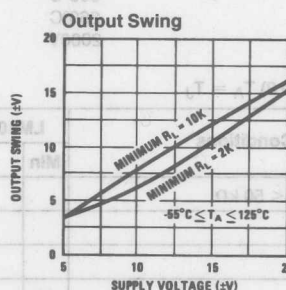
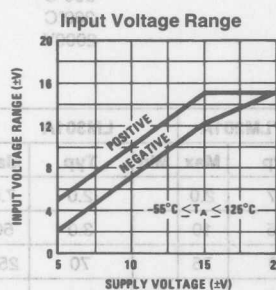
Note 2: Continuous short circuit is allowed for case temperatures to $125^\circ C$ and ambient temperatures to $75^\circ C$ for LM101A/LM201A, and $70^\circ C$ and $55^\circ C$ respectively for LM301A.

Note 3: Unless otherwise specified, these specifications apply for $C_1 = 30pF$, $\pm 5V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ (LM101A), $\pm 5V \leq V_S \leq \pm 20V$ and $-25^\circ C \leq T_A \leq +85^\circ C$ (LM201A), $\pm 5V \leq V_S \leq \pm 15V$ and $0^\circ C \leq T_A \leq +70^\circ C$ (LM301A).

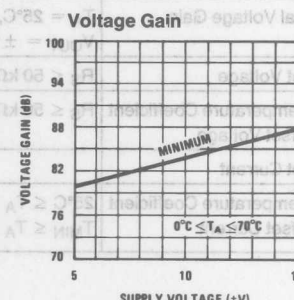
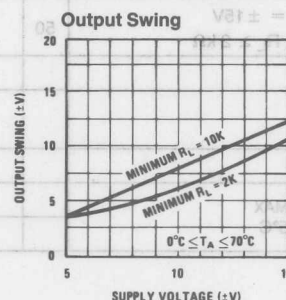
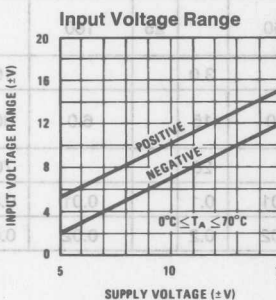
Note 4: Refer to RETS101AX for LM101A military specifications and RETS101X for LM101 military specifications.

Note 5: Human body model, 100 pF discharged through 1.5 k Ω .

Guaranteed Performance Characteristics LM101A/LM201A

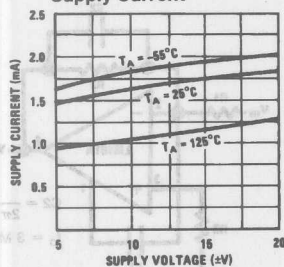


Guaranteed Performance Characteristics LM301A

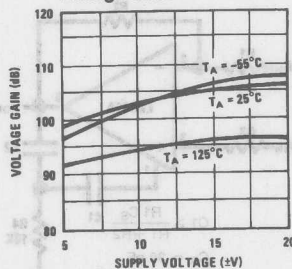


Typical Performance Characteristics

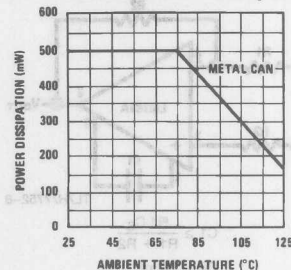
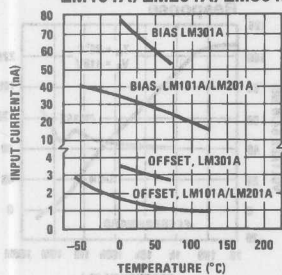
Supply Current



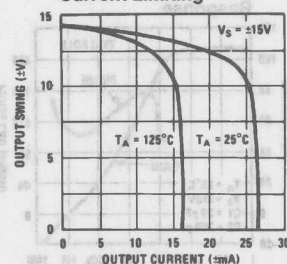
Voltage Gain



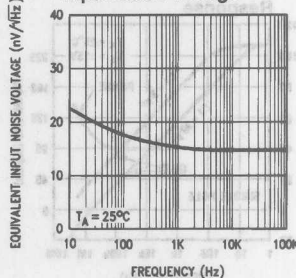
Maximum Power Dissipation

Input Current,
LM101A/LM201A/LM301A

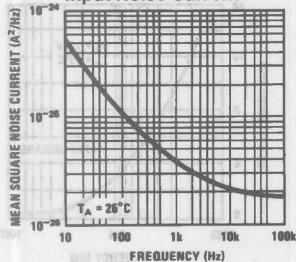
Current Limiting



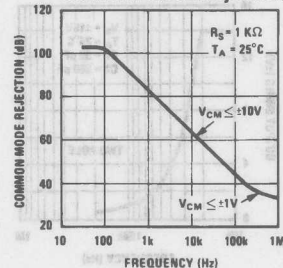
Input Noise Voltage



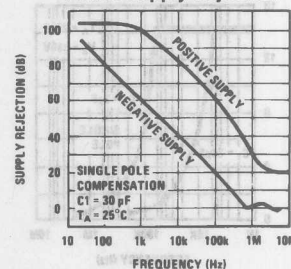
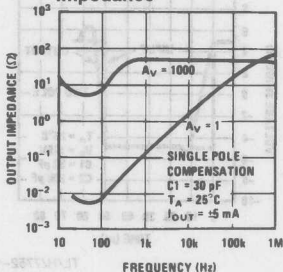
Input Noise Current



Common Mode Rejection



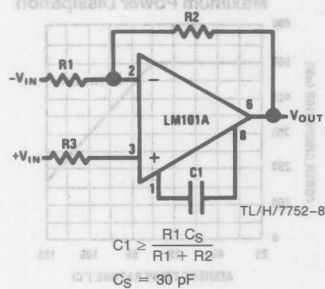
Power Supply Rejection

Closed Loop Output
Impedance

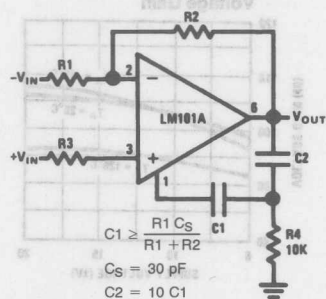
TL/H/7752-7

Typical Performance Characteristics for Various Compensation Circuits**

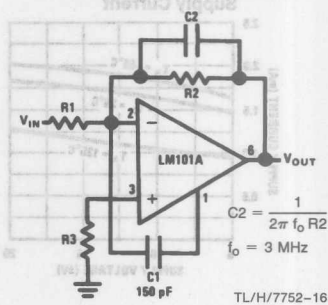
Single Pole Compensation



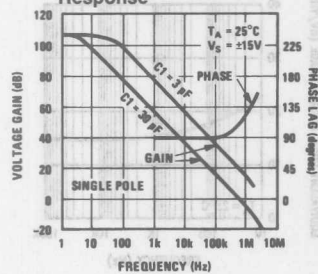
Two Pole Compensation



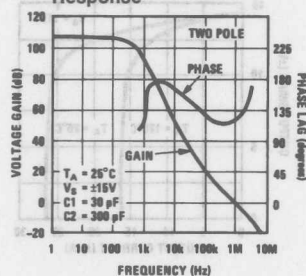
Feedforward Compensation



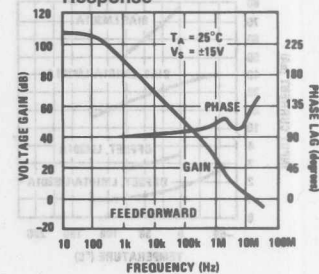
Open Loop Frequency Response



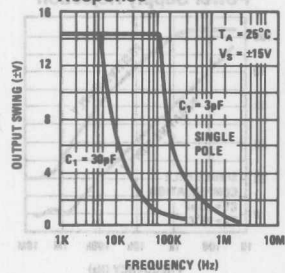
Open Loop Frequency Response



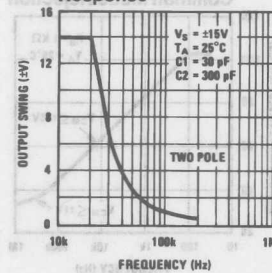
Open Loop Frequency Response



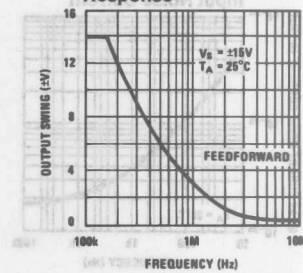
Large Signal Frequency Response



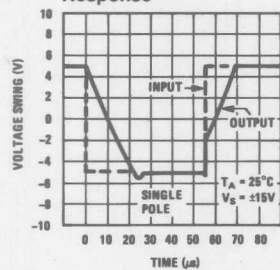
Large Signal Frequency Response



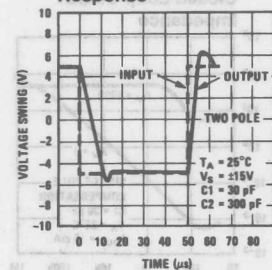
Large Signal Frequency Response



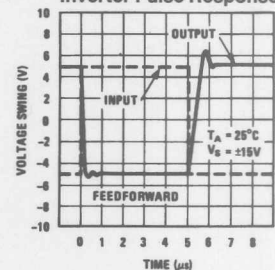
Voltage Follower Pulse Response



Voltage Follower Pulse Response



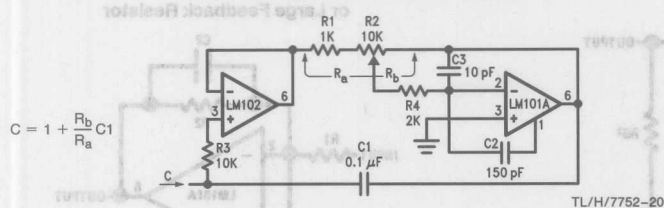
Inverter Pulse Response



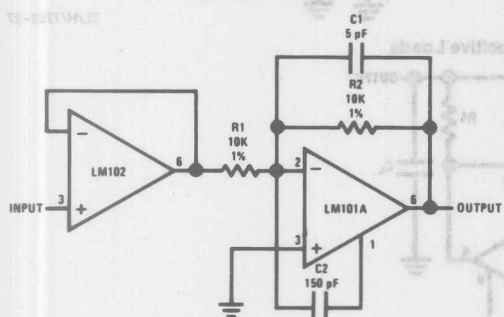
**Pin connections shown are for 8-pin packages.

Typical Applications**

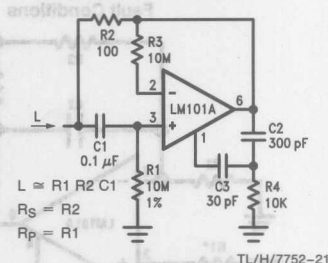
Variable Capacitance Multiplier



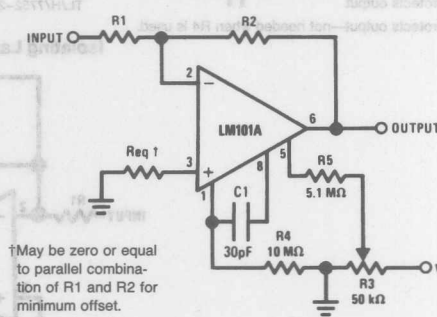
Fast Inverting Amplifier with High Input Impedance



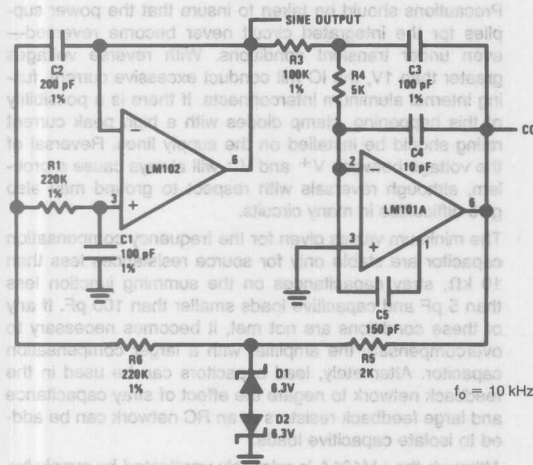
Simulated Inductor



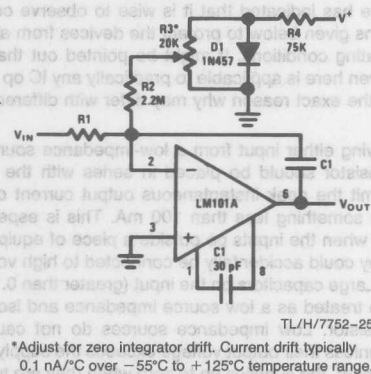
Inverting Amplifier with Balancing Circuit



Sine Wave Oscillator



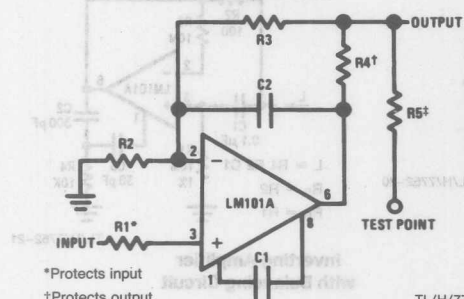
Integrator with Bias Current Compensation



**Pin connections shown are for 8-pin packages.

Application Hints**

Protecting Against Gross Fault Conditions



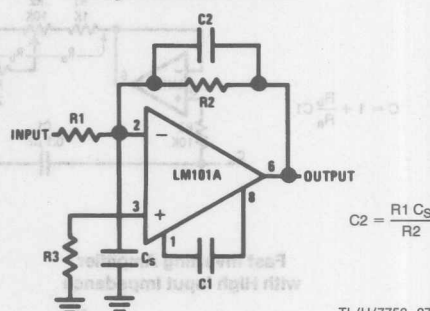
*Protects input

†Protects output

‡Protects output—not needed when R4 is used.

TL/H/7752-26

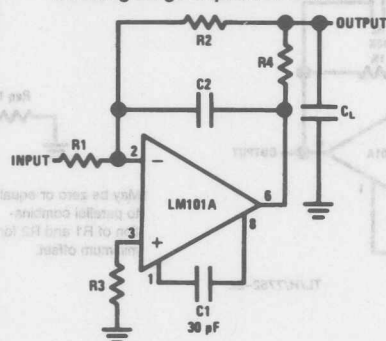
Compensating for Stray Input Capacitances or Large Feedback Resistor



$$C2 = \frac{R1 C_s}{R2}$$

TL/H/7752-27

Isolating Large Capacitive Loads



TL/H/7752-28

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 μ F) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifier drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

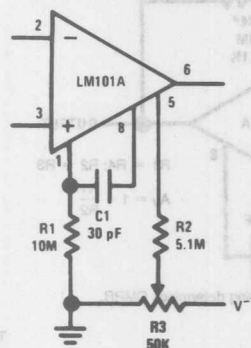
Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed—even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 k Ω , stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

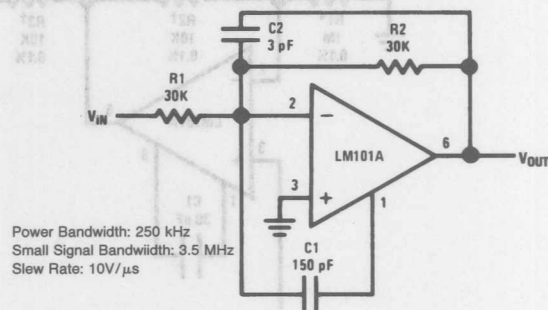
**Pin connections shown are for 8-pin packages.

Standard Compensation and Offset Balancing Circuit



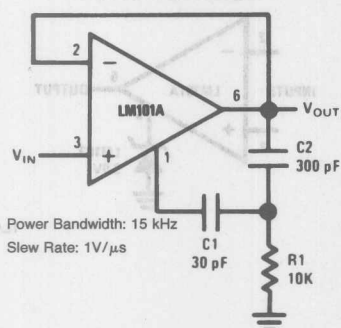
TL/H/7752-29

Fast Summing Amplifier



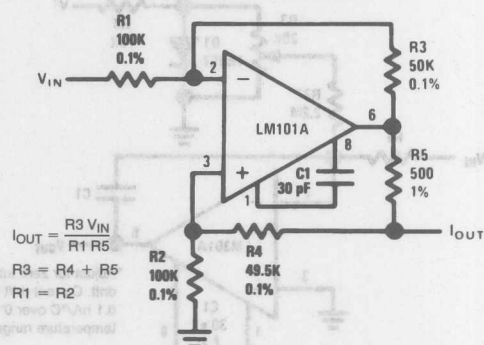
TL/H/7752-30

Fast Voltage Follower



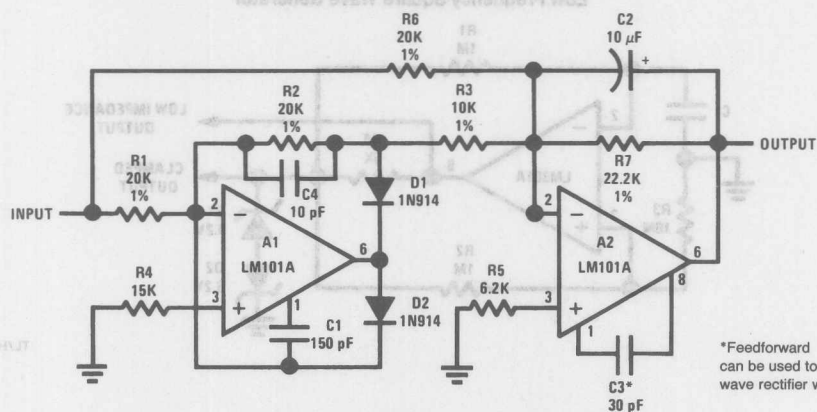
TL/H/7752-31

Bilateral Current Source



TL/H/7752-32

Fast AC/DC Converter*



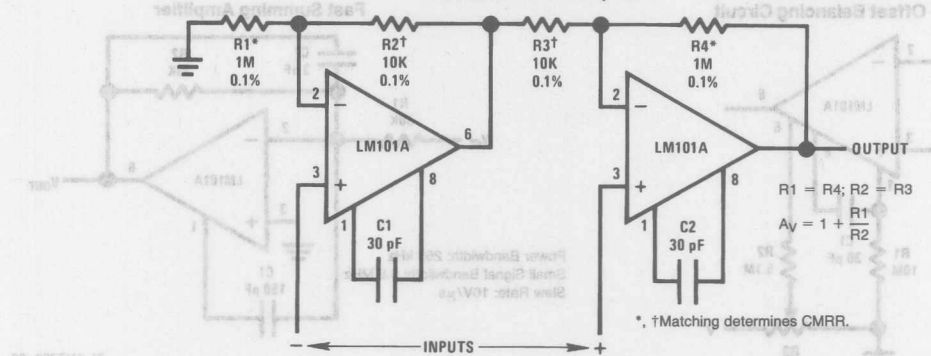
*Feedforward compensation can be used to make a fast full wave rectifier without a filter.

TL/H/7752-33

**Pin connections shown are for 8-pin packages.

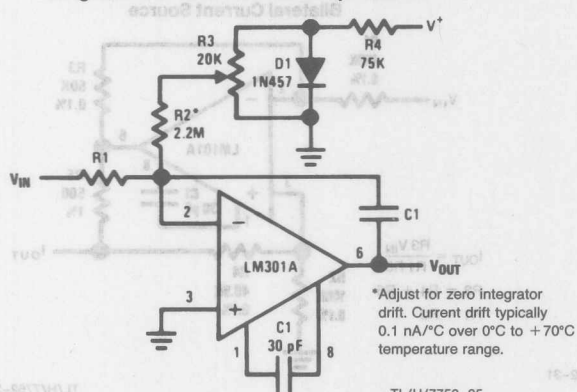
Typical Applications** (Continued)

Instrumentation Amplifier



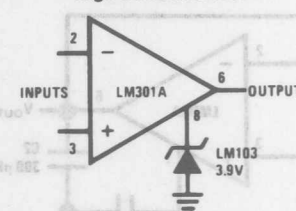
TL/H/7752-34

Integrator with Bias Current Compensation



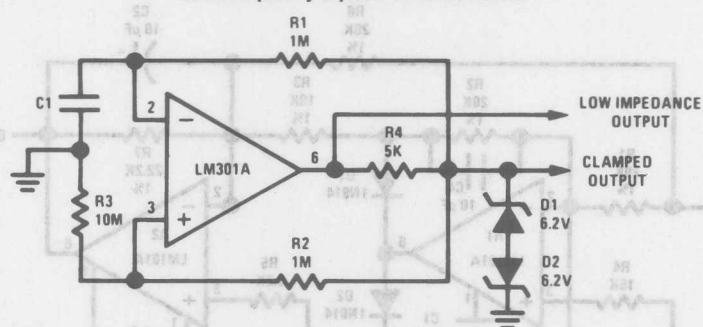
TL/H/7752-35

Voltage Comparator for Driving RTL Logic or High Current Driver



TL/H/7752-37

Low Frequency Square Wave Generator

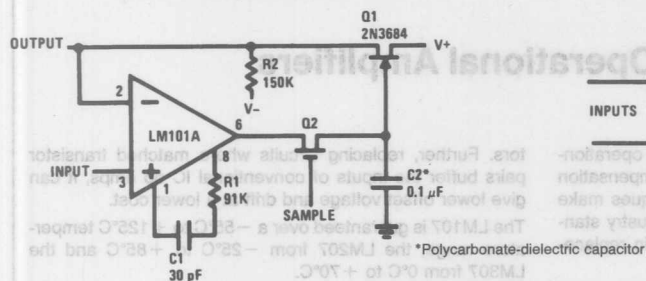


TL/H/7752-36

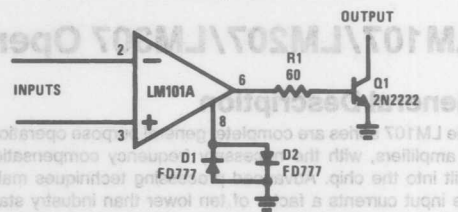
**Pin connections shown are for 8-pin packages.

Typical Applications** (Continued)

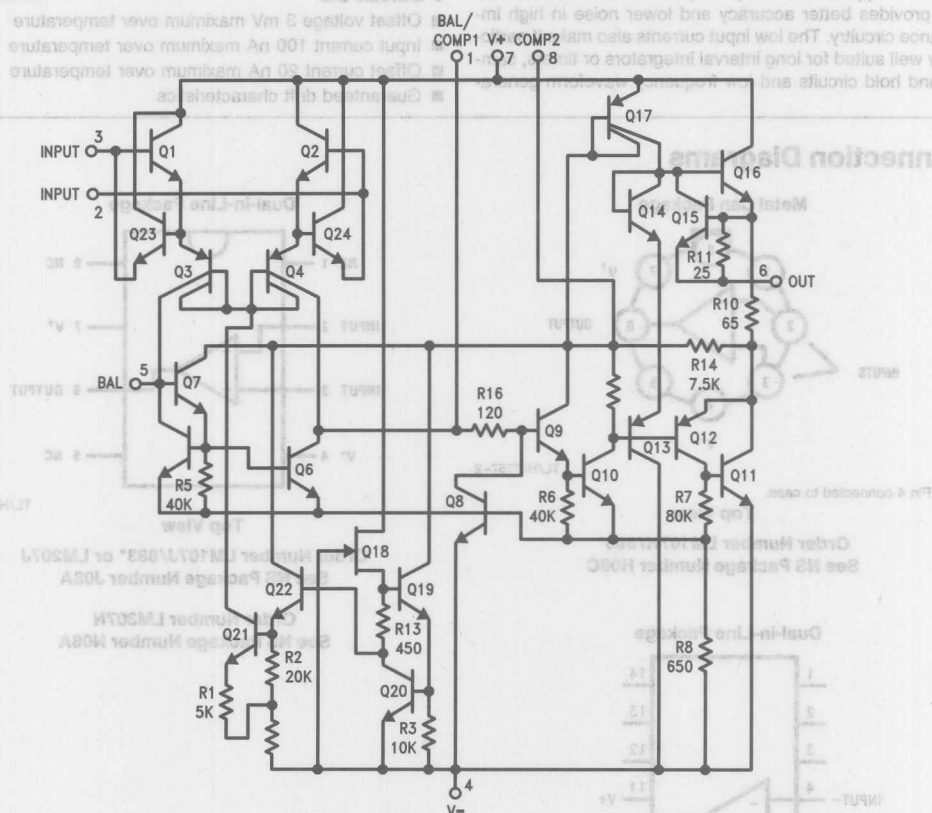
Low Drift Sample and Hold



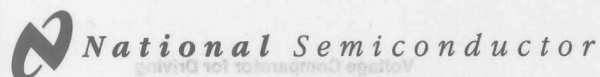
Voltage Comparator for Driving DTL or TTL Integrated Circuits



Schematic**



**Pin connections shown are for 8-pin packages.



LM107/LM207/LM307 Operational Amplifiers

General Description

The LM107 series are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101A and 741.

The LM107 series offers the features of the LM101A, which makes its application nearly foolproof. In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform genera-

tors. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at a lower cost.

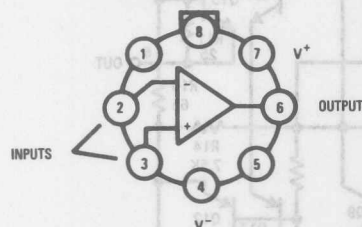
The LM107 is guaranteed over a -55°C to $+125^{\circ}\text{C}$ temperature range, the LM207 from -25°C to $+85^{\circ}\text{C}$ and the LM307 from 0°C to $+70^{\circ}\text{C}$.

Features

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics

Connection Diagrams

Metal Can Package

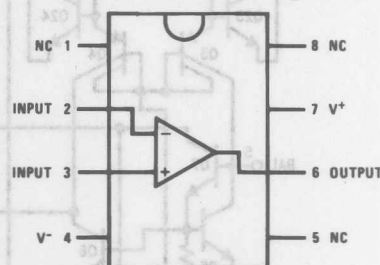


Note: Pin 4 connected to case.

Top View

Order Number LM107H/883*
See NS Package Number H08C

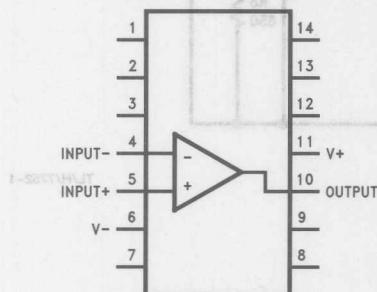
Dual-in-Line Package



Top View

Order Number LM107J/883* or LM207J
See NS Package Number J08A

Dual-in-Line Package



TL/H/7757-13

Order Number LM107J-14/883*
See NS Package Number J14A

*Available per SMD # 5962-8958901.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| Parameter | Conditions | Min | Typ | Max |
|---------------------------------------|------------|-----|-----|-----|
| Supply Voltage | | | | |
| Power Dissipation (Note 1) | | | | |
| Differential Input Voltage | | | | |
| Input Voltage (Note 2) | | | | |
| Output Short Circuit Duration | | | | |
| Operating Temperature Range (T_A) | | | | |
| Storage Temperature Range | | | | |
| Lead Temperature (Soldering, 10 sec) | | | | |

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM107/LM207 | | | LM307 | | | Units |
|---|---|-------------|--------------|------------|-------|--------------|------------|--|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$, $R_S \leq 50\text{ k}\Omega$ | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 1.5 | 10 | | 3.0 | 50 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 30 | 75 | | 70 | 250 | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 1.5 | 4.0 | | 0.5 | 2.0 | | M Ω |
| Supply Current | $T_A = 25^\circ\text{C}$ $V_S = \pm 20\text{V}$ $V_S = \pm 15\text{V}$ | | 1.8 | 3.0 | | 1.8 | 3.0 | mA mA |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{ k}\Omega$ | 50 | 160 | | 25 | 160 | | V/mV |
| Input Offset Voltage | $R_S \leq 50\text{ k}\Omega$ | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 15 | | 6.0 | 30 | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current | | | | 20 | | | 70 | nA |
| Average Temperature Coefficient of Input Offset Current | $25^\circ\text{C} \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25^\circ\text{C}$ | | 0.01 0.02 | 0.1 0.2 | | 0.01 0.02 | 0.3 0.6 | nA/ $^\circ\text{C}$ nA/ $^\circ\text{C}$ |
| Input Bias Current | | | | 100 | | | 300 | nA |
| Supply Current | $T_A = +125^\circ\text{C}$, $V_S = \pm 20\text{V}$ | | 1.2 | 2.5 | | | | mA |

Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM107/LM207 | | | LM307 | | | Units |
|--------------------------------|---|-------------|----------|-----|----------|----------|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2 k\Omega$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V$ $R_L = 10 k\Omega$ $R_L = 2 k\Omega$ | ± 12 | ± 14 | | ± 12 | ± 14 | | V |
| | | ± 10 | ± 13 | | ± 10 | ± 13 | | V |
| Input Voltage Range | $V_S = \pm 20V$ | ± 15 | $+15$ | | ± 12 | $+15$ | | V |
| | $V_S = \pm 15V$ | | -13 | | | -13 | | V |
| Common Mode Rejection Ratio | $R_S \leq 50 k\Omega$ | 80 | 96 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 50 k\Omega$ | 80 | 96 | | 70 | 96 | | dB |

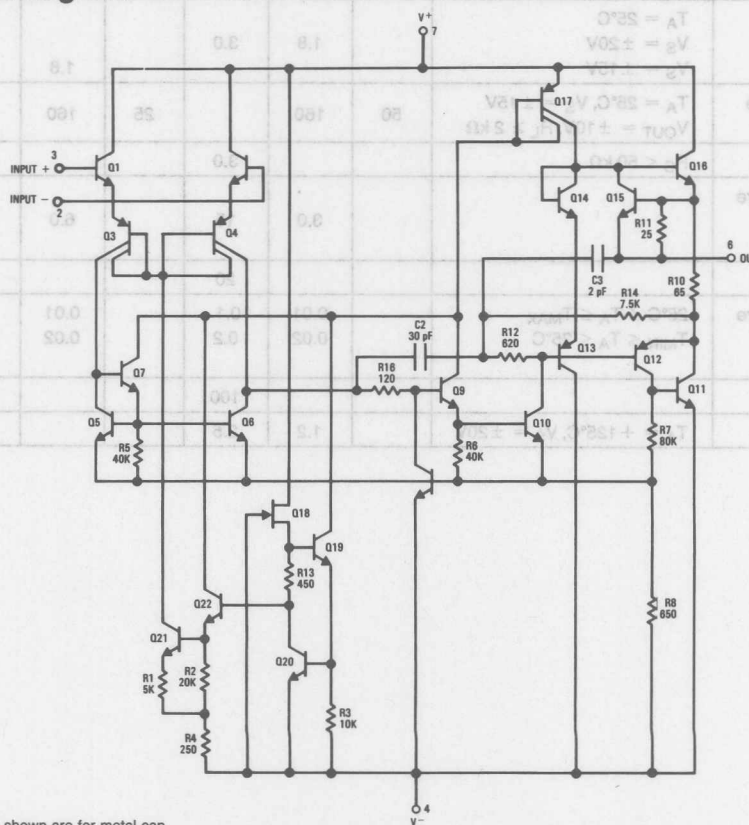
Note 1: The maximum junction temperature of the LM107 is 150°C, and the LM207/LM307 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 30°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$ for the LM107 or $-25^\circ C \leq T_A \leq +85^\circ C$ for the LM207, and $0^\circ C \leq T_A \leq +70^\circ C$ and $\pm 5V \leq V_S \leq \pm 15V$ for the LM307 unless otherwise specified.

Note 4: Refer to RETS107X for LM107H and LM107J military specifications.

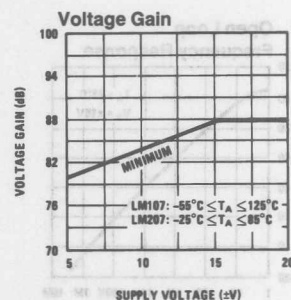
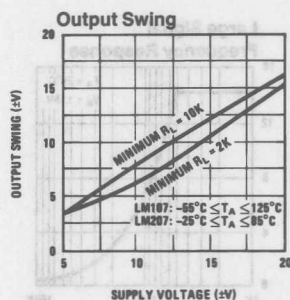
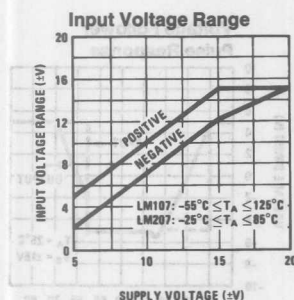
Schematic Diagram*



*Pin connections shown are for metal can.

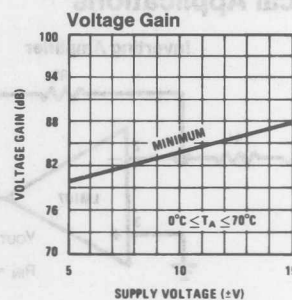
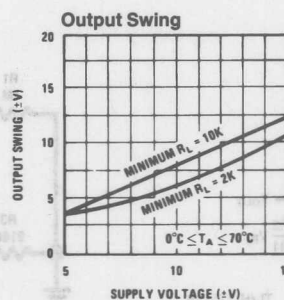
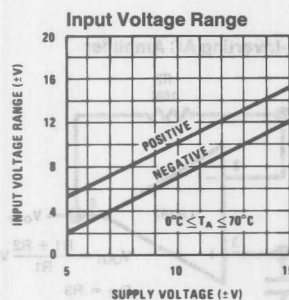
TL/H/7757-1

Guaranteed Performance Characteristics LM107/LM207



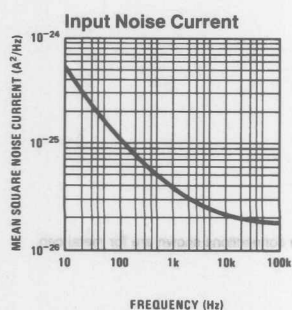
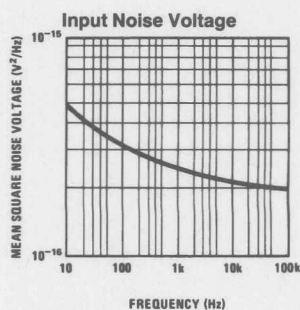
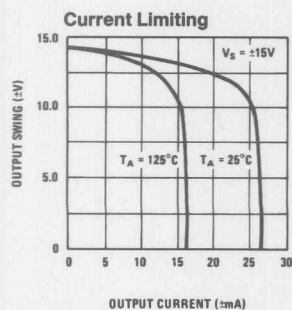
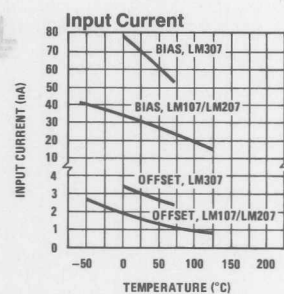
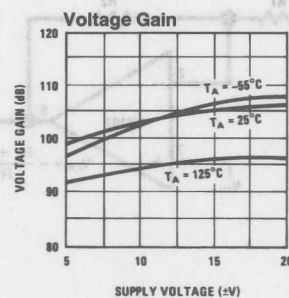
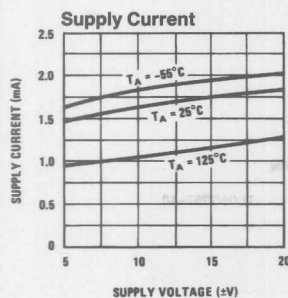
TL/H/7757-4

Guaranteed Performance Characteristics LM307



TL/H/7757-5

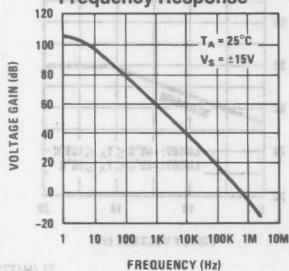
Typical Performance Characteristics



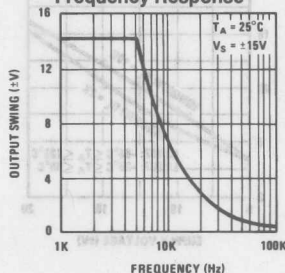
TL/H/7757-6

Typical Performance Characteristics (Continued)

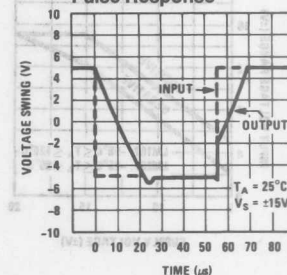
Open Loop Frequency Response



Large Signal Frequency Response



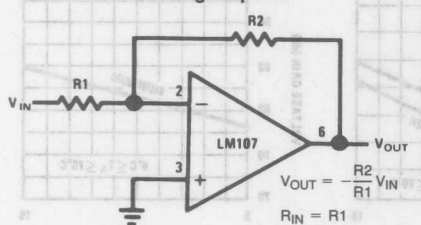
Voltage Follower Pulse Response



TL/H/7757-7

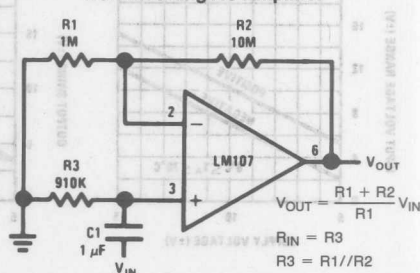
Typical Applications**

Inverting Amplifier



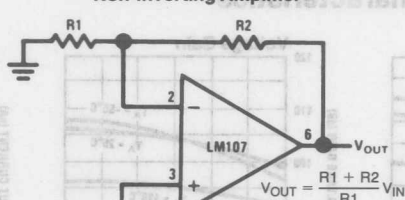
TL/H/7757-8

Non-Inverting AC Amplifier



TL/H/7757-9

Non-Inverting Amplifier



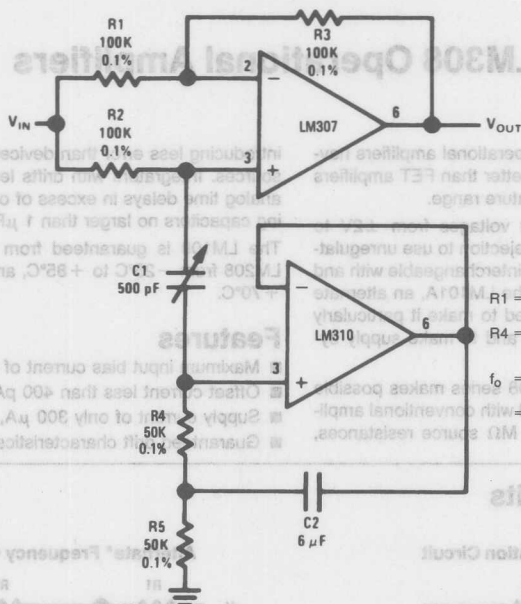
TL/H/7757-10

**Pin connections shown are for metal can.

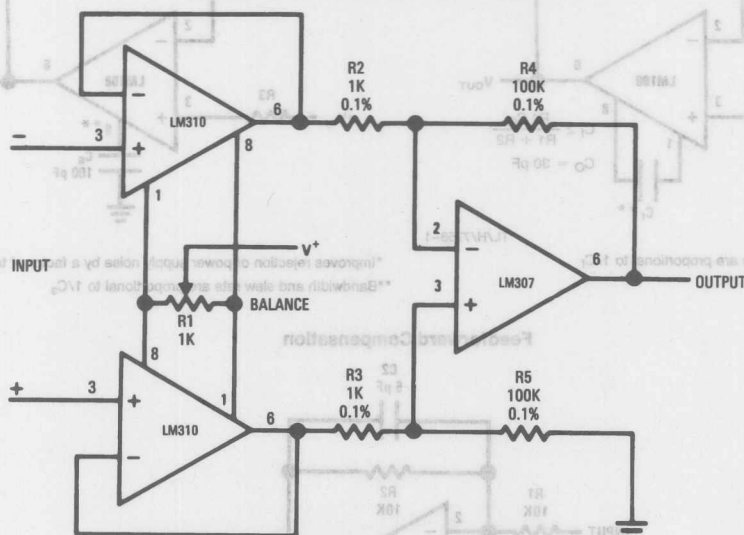
Typical Applications** (Continued)

LM107/LM207/LM307

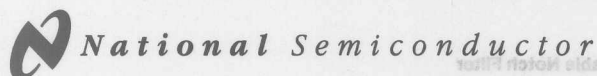
Turntable Notch Filter



Differential Input Instrumentation Amplifier



**Pin connections shown are for metal can.



LM108/LM208/LM308 Operational Amplifiers

General Description

The LM108 series are precision operational amplifiers having specifications a factor of ten better than FET amplifiers over a -55°C to $+125^{\circ}\text{C}$ temperature range.

The devices operate with supply voltages from $\pm 2\text{V}$ to $\pm 20\text{V}$ and have sufficient supply rejection to use unregulated supplies. Although the circuit is interchangeable with and uses the same compensation as the LM101A, an alternate compensation scheme can be used to make it particularly insensitive to power supply noise and to make supply bypass capacitors unnecessary.

The low current error of the LM108 series makes possible many designs that are not practical with conventional amplifiers. In fact, it operates from $10\text{ M}\Omega$ source resistances,

introducing less error than devices like the 709 with $10\text{ k}\Omega$ sources. Integrators with drifts less than $500\text{ }\mu\text{V}/\text{sec}$ and analog time delays in excess of one hour can be made using capacitors no larger than $1\text{ }\mu\text{F}$.

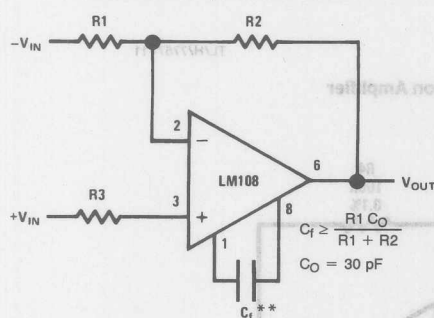
The LM108 is guaranteed from -55°C to $+125^{\circ}\text{C}$, the LM208 from -25°C to $+85^{\circ}\text{C}$, and the LM308 from 0°C to $+70^{\circ}\text{C}$.

Features

- Maximum input bias current of 3.0 nA over temperature
- Offset current less than 400 pA over temperature
- Supply current of only $300\text{ }\mu\text{A}$, even in saturation
- Guaranteed drift characteristics

Compensation Circuits

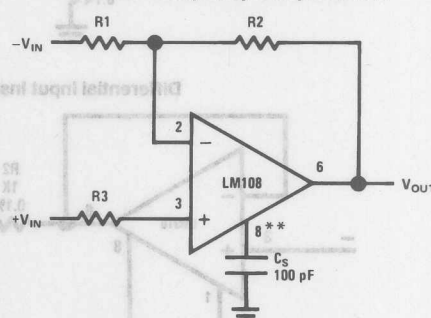
Standard Compensation Circuit



TL/H/7758-1

**Bandwidth and slew rate are proportional to $1/C_1$

Alternate* Frequency Compensation

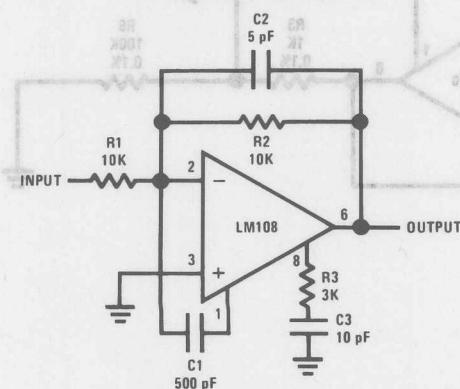


TL/H/7758-2

*Improves rejection of power supply noise by a factor of ten.

**Bandwidth and slew rate are proportional to $1/C_s$

Feedforward Compensation



TL/H/7758-3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 5)

| Parameter | Condition | LM108/LM208 | LM308 |
|---|-----------------|---|---|
| Supply Voltage | $V_S = \pm 15V$ | $\pm 20V$ | $\pm 18V$ |
| Power Dissipation (Note 1) | | 500 mW | 500 mW |
| Differential Input Current (Note 2) | | ± 10 mA | ± 10 mA |
| Input Voltage (Note 3) | | $\pm 15V$ | $\pm 15V$ |
| Output Short-Circuit Duration | | Continuous | Continuous |
| Operating Temperature Range (LM108) | | -55°C to $+125^\circ\text{C}$ | 0°C to $+70^\circ\text{C}$ |
| (LM208) | | -25°C to $+85^\circ\text{C}$ | |
| Storage Temperature Range | | -65°C to $+150^\circ\text{C}$ | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 sec) | | | |
| DIP | | 260°C | 260°C |
| H Package Lead Temp | | | |
| (Soldering 10 seconds) | | 300°C | 300°C |
| Soldering Information | | | |
| Dual-In-Line Package | | | |
| Soldering (10 seconds) | | 260°C | |
| Small Outline Package | | | |
| Vapor Phase (60 seconds) | | 215°C | |
| Infrared (15 seconds) | | 220°C | |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | |
| ESD Tolerance (Note 6) | | 2000V | |

Electrical Characteristics (Note 4)

| Parameter | Condition | LM108/LM208 | | | LM308 | | | Units |
|---|--|-------------|----------|-----|----------|----------|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$ | | 0.7 | 2.0 | | 2.0 | 7.5 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 0.05 | 0.2 | | 0.2 | 1 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 0.8 | 2.0 | | 1.5 | 7 | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 30 | 70 | | 10 | 40 | | M Ω |
| Supply Current | $T_A = 25^\circ\text{C}$ | | 0.3 | 0.6 | | 0.3 | 0.8 | mA |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L \geq 10\text{ k}\Omega$ | 50 | 300 | | 25 | 300 | | V/mV |
| Input Offset Voltage | | | | 3.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 15 | | 6.0 | 30 | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current | | | | 0.4 | | | 1.5 | nA |
| Average Temperature Coefficient of Input Offset Current | | | 0.5 | 2.5 | | 2.0 | 10 | $\text{pA}/^\circ\text{C}$ |
| Input Bias Current | | | | 3.0 | | | 10 | nA |
| Supply Current | $T_A = +125^\circ\text{C}$ | | 0.15 | 0.4 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \geq 10\text{ k}\Omega$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V, R_L = 10\text{ k}\Omega$ | ± 13 | ± 14 | | ± 13 | ± 14 | | V |

Electrical Characteristics (Note 4) (Continued)

| Parameter | Condition | LM108/LM208 | | | LM308 | | | Units |
|--------------------------------|-----------------|-------------|-----|-----|----------|-----|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Voltage Range | $V_S = \pm 15V$ | ± 13.5 | | | ± 14 | | | V |
| Common Mode Rejection Ratio | | 85 | 100 | | 80 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 80 | 96 | | 80 | 96 | | dB |

Note 1: The maximum junction temperature of the LM108 is 150°C, for the LM208, 100°C and for the LM308, 85°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

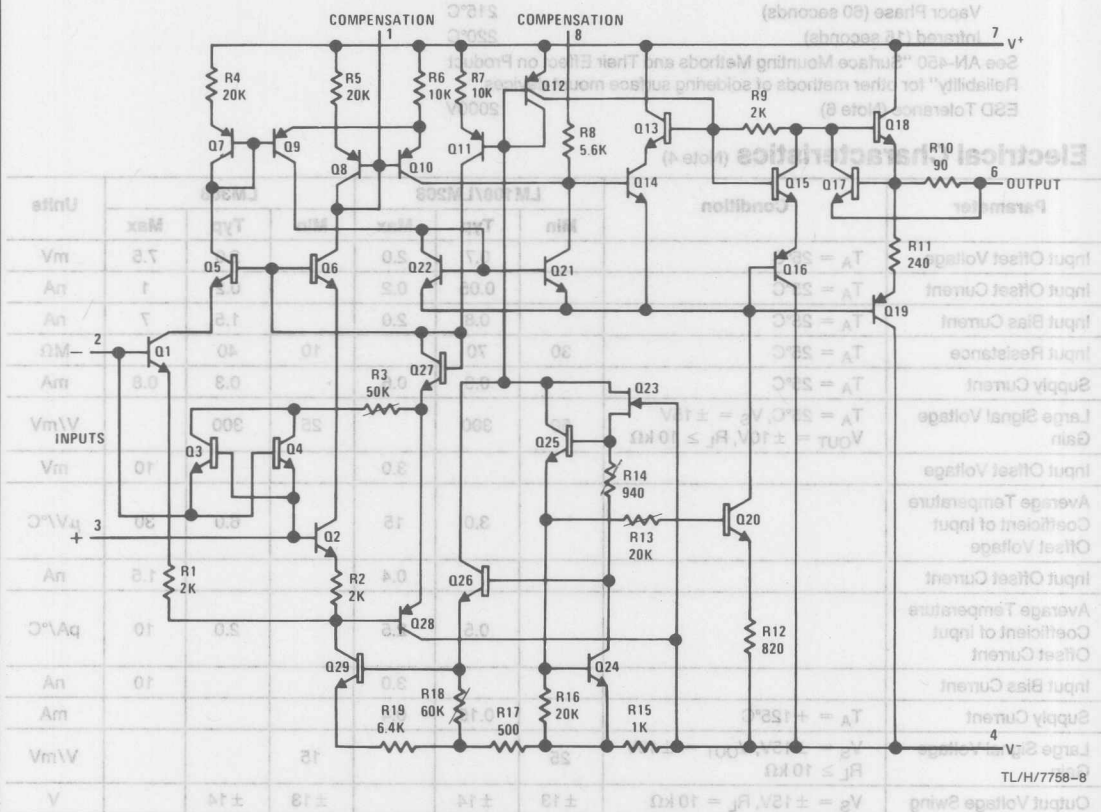
Note 3: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq +125^\circ C$, unless otherwise specified. With the LM208, however, all temperature specifications are limited to $-25^\circ C \leq T_A \leq 85^\circ C$, and for the LM308 they are limited to $0^\circ C \leq T_A \leq 70^\circ C$.

Note 5: Refer to RETS108X for LM108 military specifications and RET's 108AX for LM108A military specifications.

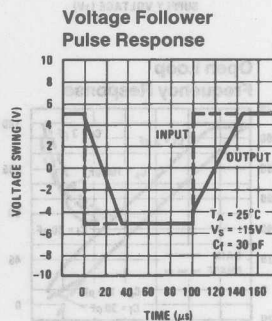
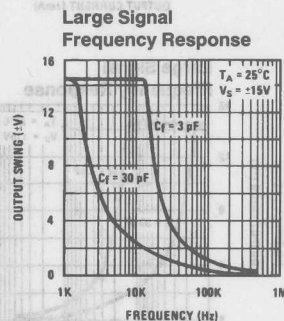
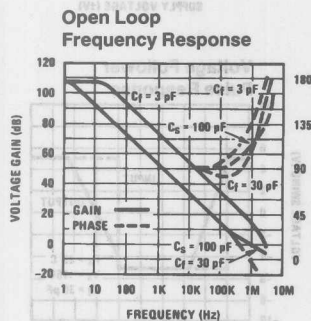
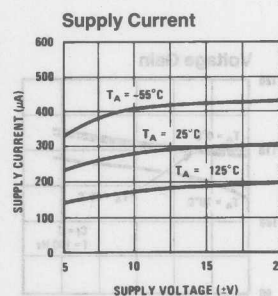
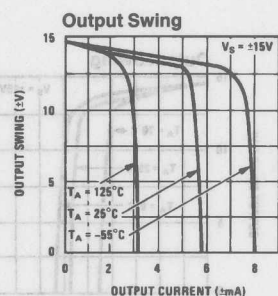
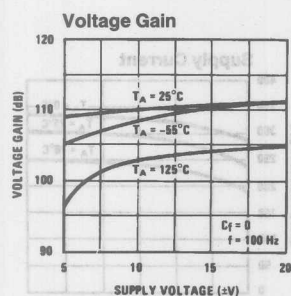
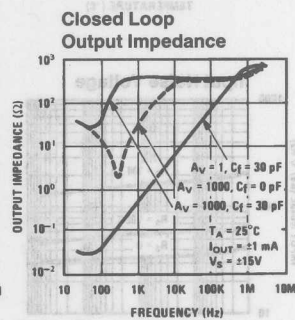
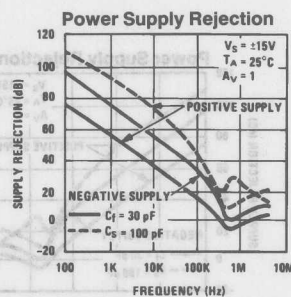
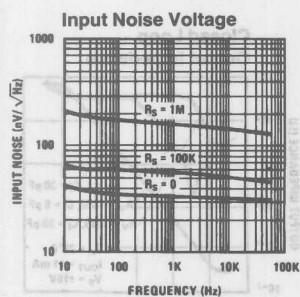
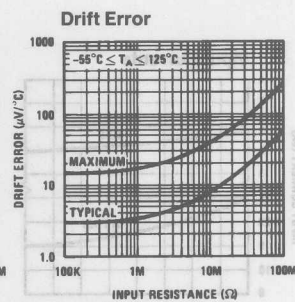
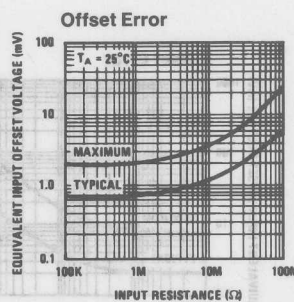
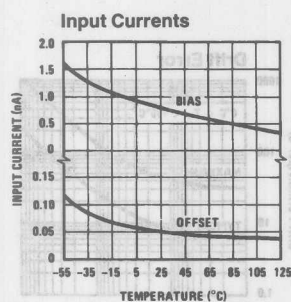
Note 6: Human body model, 1.5 k Ω in series with 100 pF.

Schematic Diagram



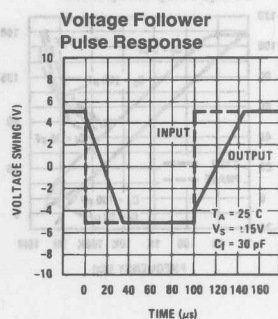
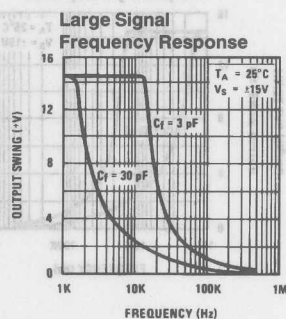
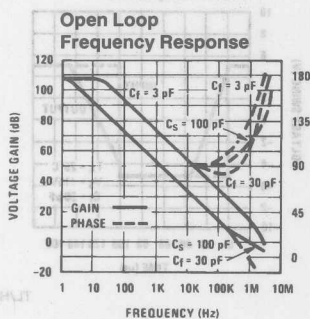
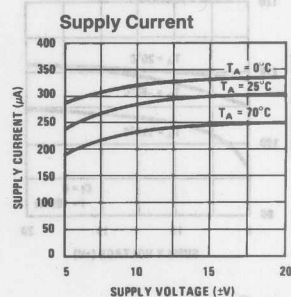
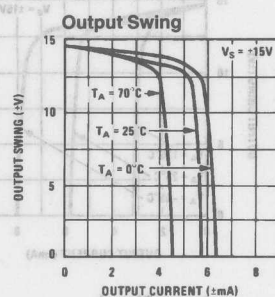
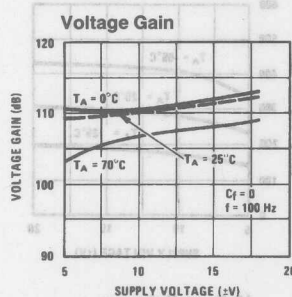
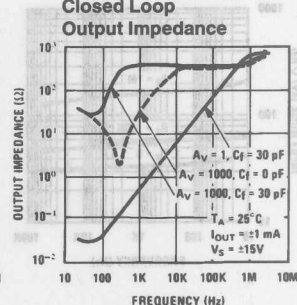
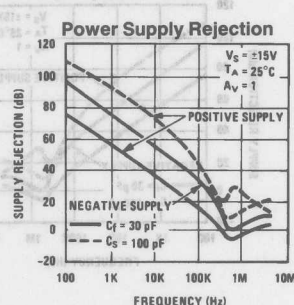
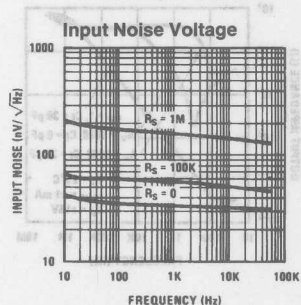
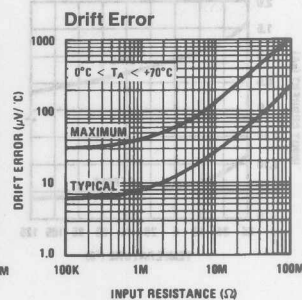
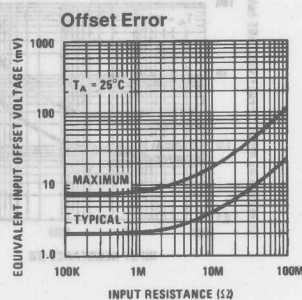
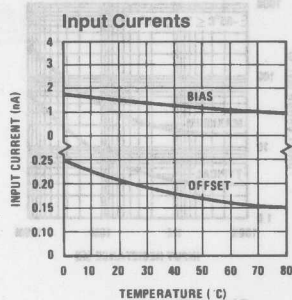
Typical Performance Characteristics LM108/LM208

LM108/LM208/LM308



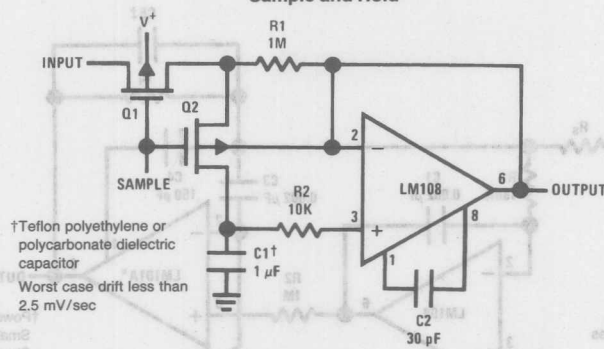
TL/H/7758-6

Typical Performance Characteristics LM308

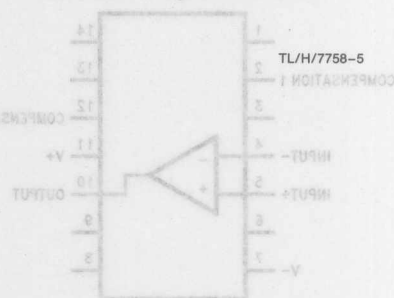
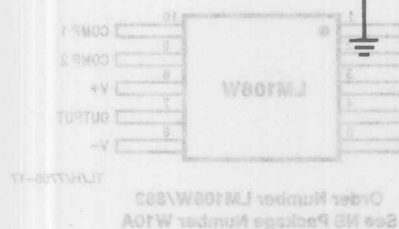
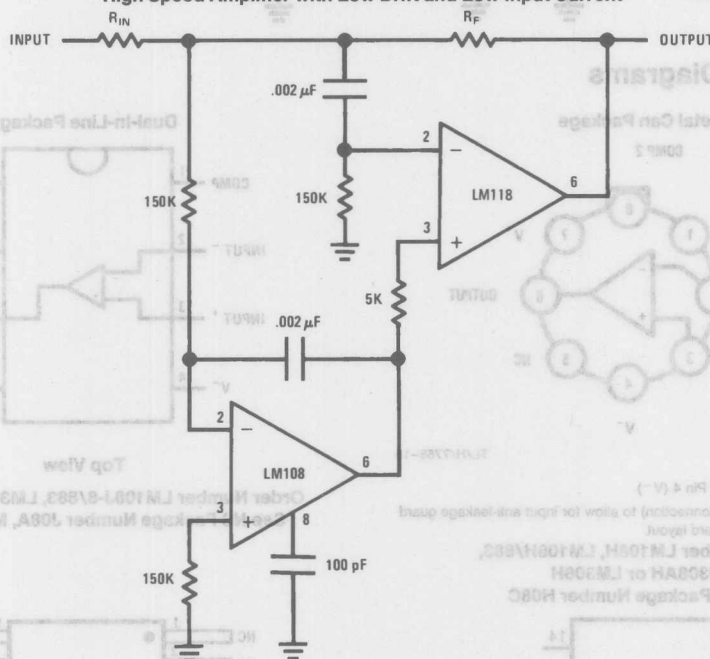


Typical Applications

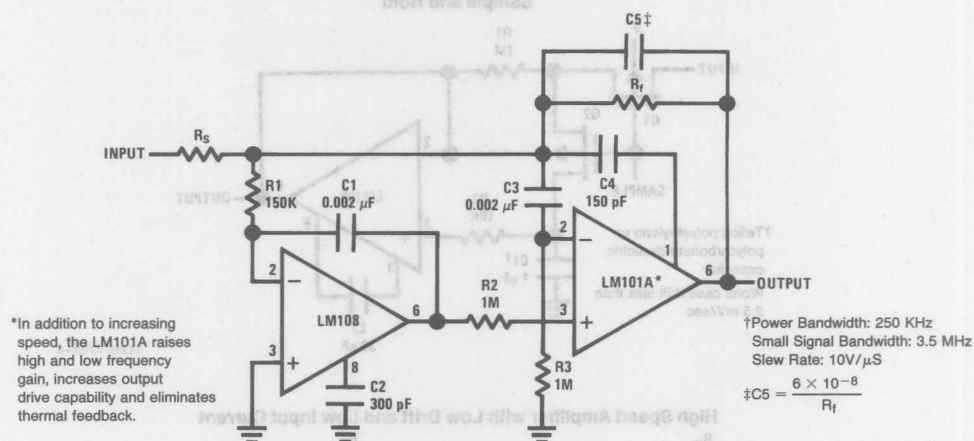
Sample and Hold



High Speed Amplifier with Low Drift and Low Input Current



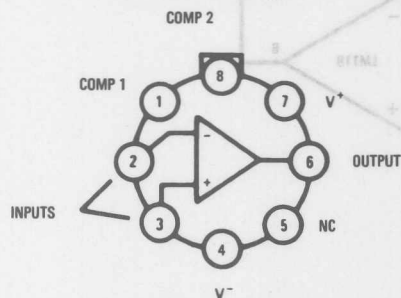
Typical Applications (Continued)

Fast[†] Summing Amplifier

TL/H/7758-12

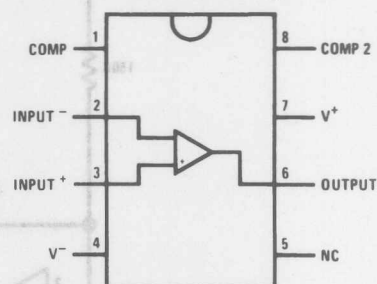
Connection Diagrams

Metal Can Package



TL/H/7758-13

Dual-In-Line Package

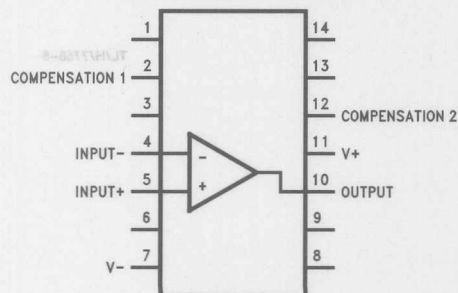


TL/H/7758-15

*Package is connected to Pin 4 (V-)

**Unused pin (no internal connection) to allow for input anti-leakage guard ring on printed circuit board layout.

Order Number LM108H, LM108H/883,
LM308AH or LM308H
See NS Package Number H08C



TL/H/7758-16

Top View

Order Number LM108J/883
See NS Package Number J14A

Top View

Order Number LM108J-8/883, LM308M or LM308N
See NS Package Number J08A, M08A or N08E



TL/H/7758-17

Order Number LM108W/883
See NS Package Number W10A

†Also available per JM38510/10104



LM118/LM218/LM318 Operational Amplifiers

General Description

The LM118 series are precision high speed operational amplifiers designed for applications requiring wide bandwidth and high slew rate. They feature a factor of ten increase in speed over general purpose devices without sacrificing DC performance.

The LM118 series has internal unity gain frequency compensation. This considerably simplifies its application since no external components are necessary for operation. However, unlike most internally compensated amplifiers, external frequency compensation may be added for optimum performance. For inverting applications, feedforward compensation will boost the slew rate to over $150V/\mu s$ and almost double the bandwidth. Overcompensation can be used with the amplifier for greater stability when maximum bandwidth is not needed. Further, a single capacitor can be added to reduce the 0.1% settling time to under $1\mu s$.

The high speed and fast settling time of these op amps make them useful in A/D converters, oscillators, active fil-

ters, sample and hold circuits, or general purpose amplifiers. These devices are easy to apply and offer an order of magnitude better AC performance than industry standards such as the LM709.

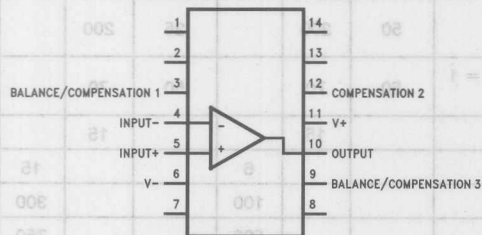
The LM218 is identical to the LM118 except that the LM218 has its performance specified over a $-25^{\circ}C$ to $+85^{\circ}C$ temperature range. The LM318 is specified from $0^{\circ}C$ to $+70^{\circ}C$.

Features

- 15 MHz small signal bandwidth
- Guaranteed $50V/\mu s$ slew rate
- Maximum bias current of 250 nA
- Operates from supplies of $\pm 5V$ to $\pm 20V$
- Internal frequency compensation
- Input and output overload protected
- Pin compatible with general purpose op amps

Connection Diagrams

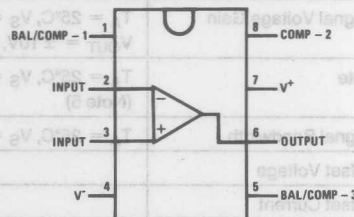
Dual-In-Line Package



Top View

Order Number LM118J/883*
See NS Package Number J14A

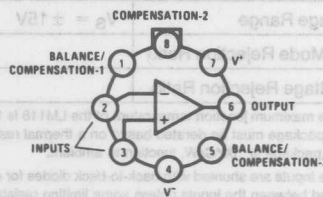
Dual-In-Line Package



Top View

Order Number LM118J-8/883*,
LM318M or LM318N
See NS Package Number J08A, M08A or N08B

Metal Can Package*



Top View

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

Order Number LM118H, LM118H/883*,
LM218H or LM318H
See NS Package Number H08C

*Available per JM38510/10107.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

| | |
|-------------------------------------|------------|
| Supply Voltage | ±20V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Current (Note 2) | ±10 mA |
| Input Voltage (Note 3) | ±15V |
| Output Short-Circuit Duration | Continuous |

Operating Temperature Range

| | |
|-------|-----------------|
| LM118 | −55°C to +125°C |
| LM218 | −25°C to +85°C |
| LM318 | 0°C to +70°C |

Storage Temperature Range

−65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

| | |
|------------------|-------|
| Hermetic Package | 300°C |
| Plastic Package | 260°C |

Soldering Information

| | |
|-----------------------|-------|
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 7)

2000V

Electrical Characteristics (Note 4)

| Parameter | Conditions | LM118/LM218 | | | LM318 | | | Units |
|--------------------------------|---|-------------|-----|-----|-------|-----|-----|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$ | | 2 | 4 | | 4 | 10 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 6 | 50 | | 30 | 200 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 120 | 250 | | 150 | 500 | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 1 | 3 | | 0.5 | 3 | | MΩ |
| Supply Current | $T_A = 25^\circ\text{C}$ | | 5 | 8 | | 5 | 10 | mA |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{ k}\Omega$ | 50 | 200 | | 25 | 200 | | V/mV |
| Slew Rate | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $A_V = 1$ (Note 5) | 50 | 70 | | 50 | 70 | | V/ μs |
| Small Signal Bandwidth | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ | | 15 | | | 15 | | MHz |
| Input Offset Voltage | | | | 6 | | | 15 | mV |
| Input Offset Current | | | | 100 | | | 300 | nA |
| Input Bias Current | | | | 500 | | | 750 | nA |
| Supply Current | $T_A = 125^\circ\text{C}$ | | 4.5 | 7 | | | | mA |
| Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{ k}\Omega$ | 25 | | | 20 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 2\text{ k}\Omega$ | ±12 | ±13 | | ±12 | ±13 | | V |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | ±11.5 | | | ±11.5 | | | V |
| Common-Mode Rejection Ratio | | 80 | 100 | | 70 | 100 | | dB |
| Supply Voltage Rejection Ratio | | 70 | 80 | | 65 | 80 | | dB |

Note 1: The maximum junction temperature of the LM118 is 150°C, the LM218 is 110°C, and the LM318 is 110°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 160°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5\text{V} \leq V_S \leq \pm 20\text{V}$ and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM118), $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ (LM218), and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ (LM318). Also, power supplies must be bypassed with 0.1 μF disc capacitors.

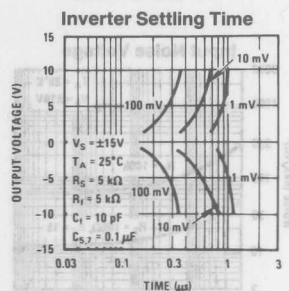
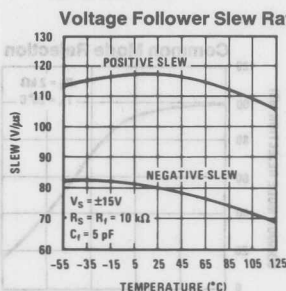
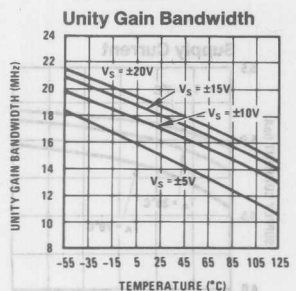
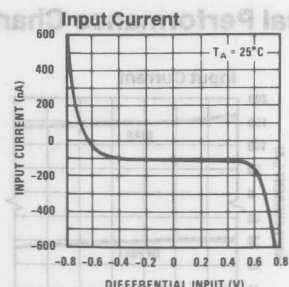
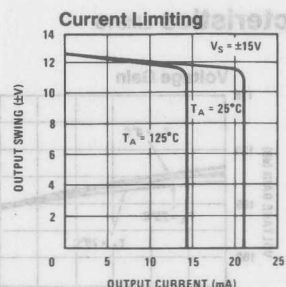
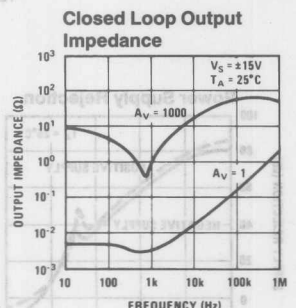
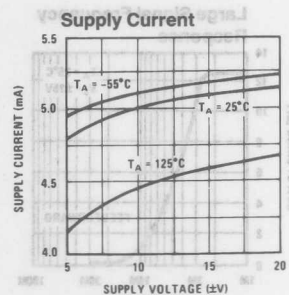
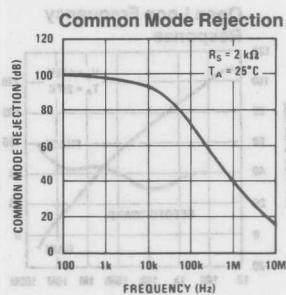
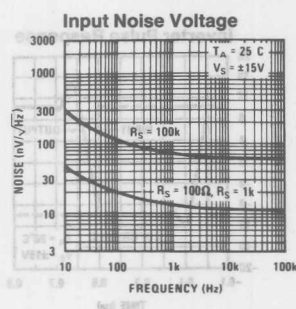
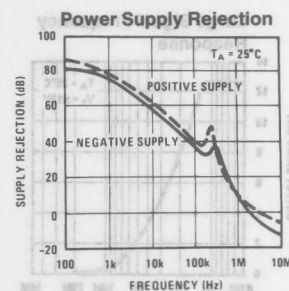
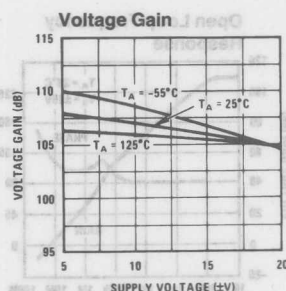
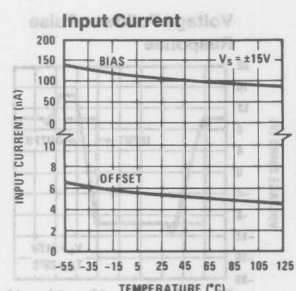
Note 5: Slew rate is tested with $V_S = \pm 15\text{V}$. The LM118 is in a unity-gain non-inverting configuration. V_{IN} is stepped from −7.5V to +7.5V and vice versa. The slew rates between −5.0V and +5.0V and vice versa are tested and guaranteed to exceed 50V/ μs .

Note 6: Refer to RETS118X for LM118H and LM118J military specifications.

Note 7: Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics LM118, LM218

LM118/LM218/LM318

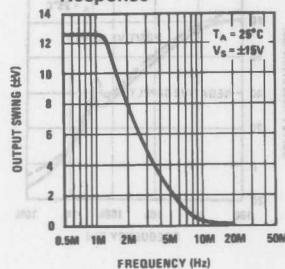


1

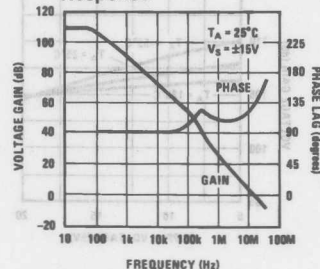
TL/H/7766-4

Typical Performance Characteristics LM118, LM218 (Continued)

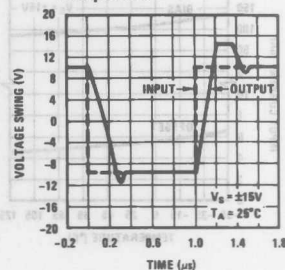
Large Signal Frequency Response



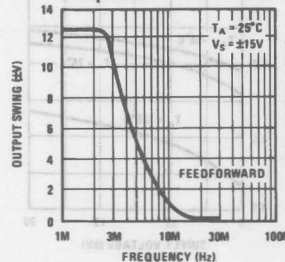
Open Loop Frequency Response



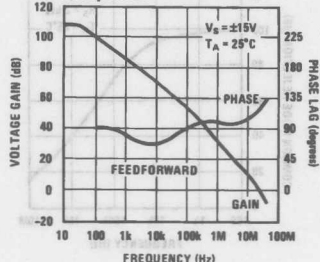
Voltage Follower Pulse Response



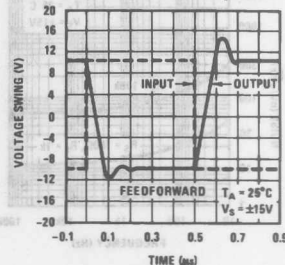
Large Signal Frequency Response



Open Loop Frequency Response



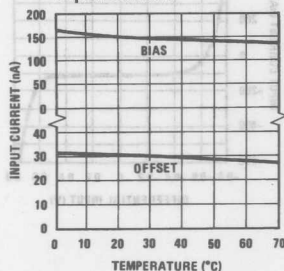
Inverter Pulse Response



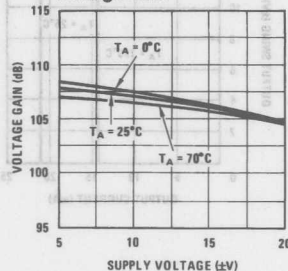
TL/H/7766-5

Typical Performance Characteristics LM318

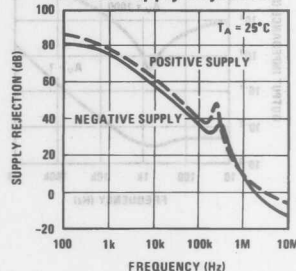
Input Current



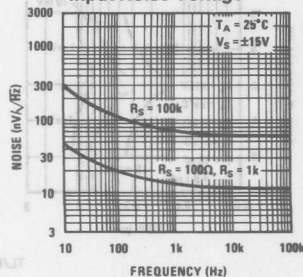
Voltage Gain



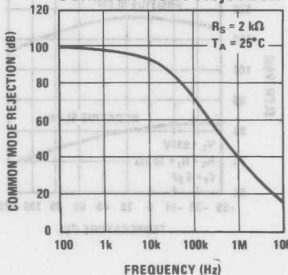
Power Supply Rejection



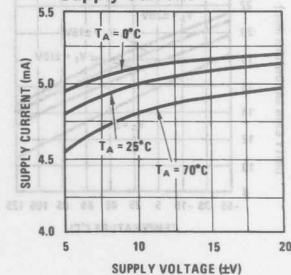
Input Noise Voltage



Common Mode Rejection



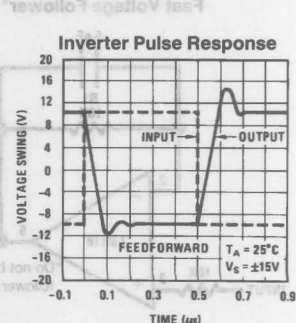
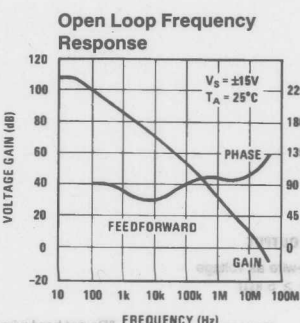
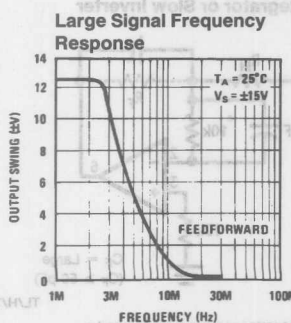
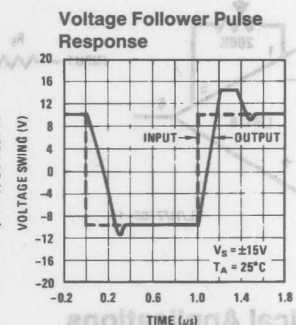
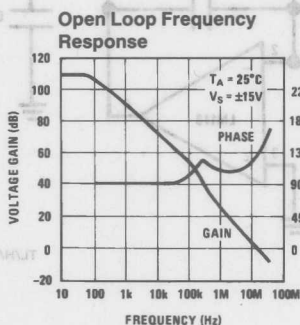
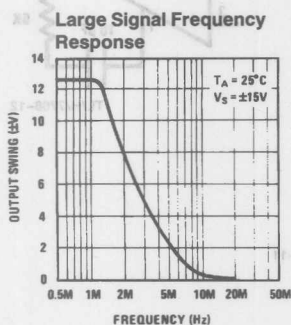
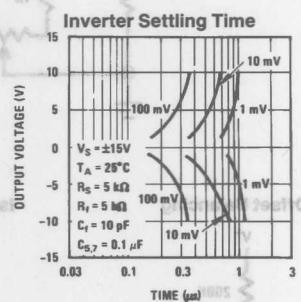
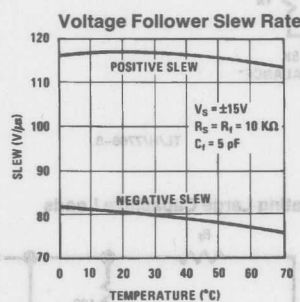
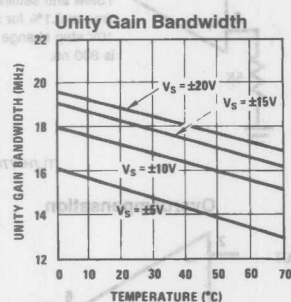
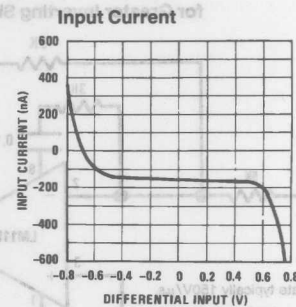
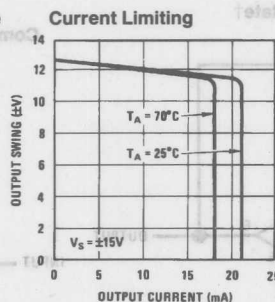
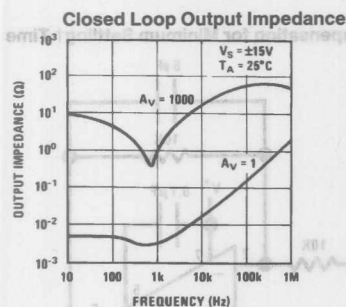
Supply Current



TL/H/7766-6

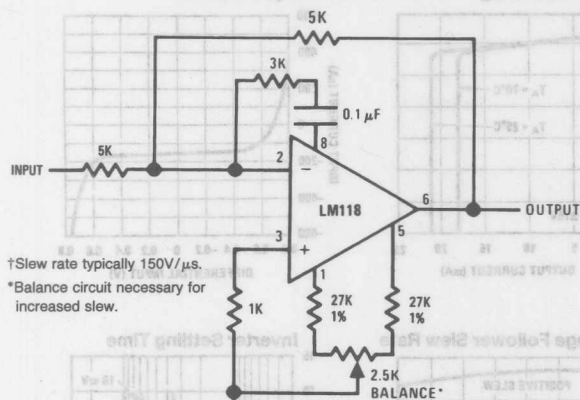
Typical Performance Characteristics LM318 (Continued)

LM118/LM218/LM318



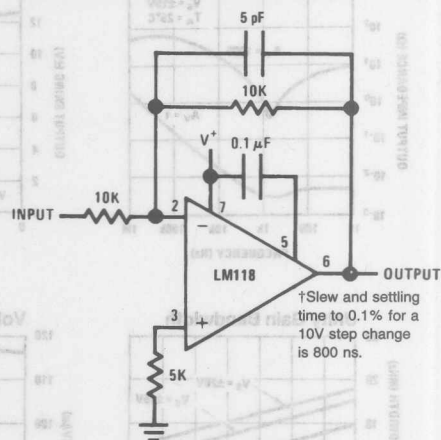
TL/H/7766-7

Feedforward Compensation for Greater Inverting Slew Rate†



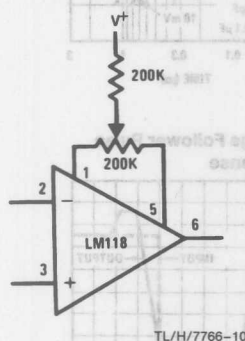
TL/H/7766-8

Compensation for Minimum Settling† Time



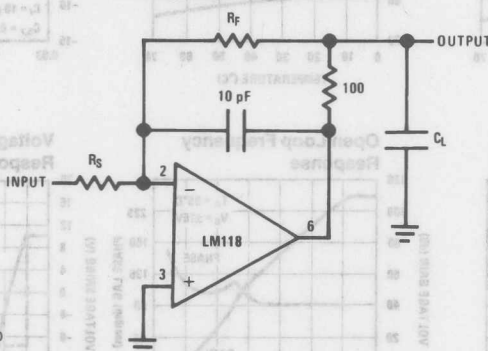
TL/H/7766-9

Offset Balancing



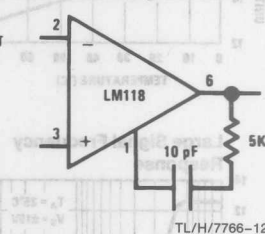
TL/H/7766-10

Isolating Large Capacitive Loads



TL/H/7766-11

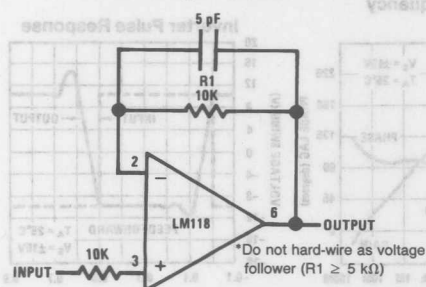
Overcompensation



TL/H/7766-12

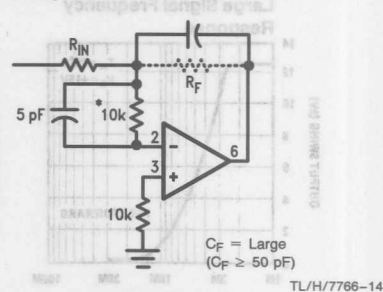
Typical Applications

Fast Voltage Follower*



TL/H/7766-13

Integrator or Slow Inverter

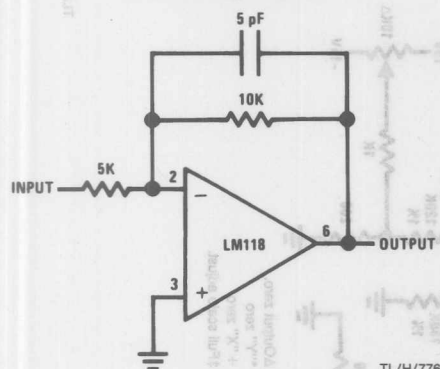


TL/H/7766-14

*Do not hard-wire as integrator or slow inverter; insert a 10k-5 pF network in series with the input, to prevent oscillation.

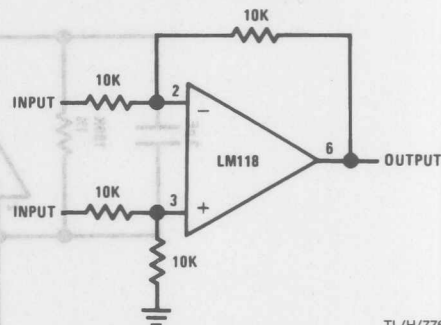
Typical Applications (Continued)

Fast Summing Amplifier



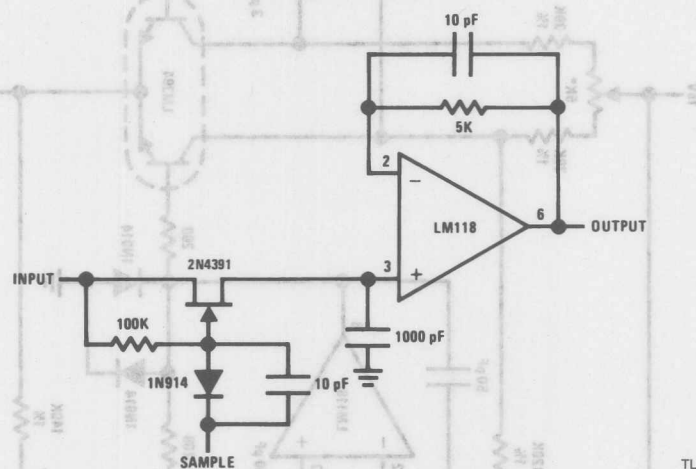
TL/H/7766-15

Differential Amplifier



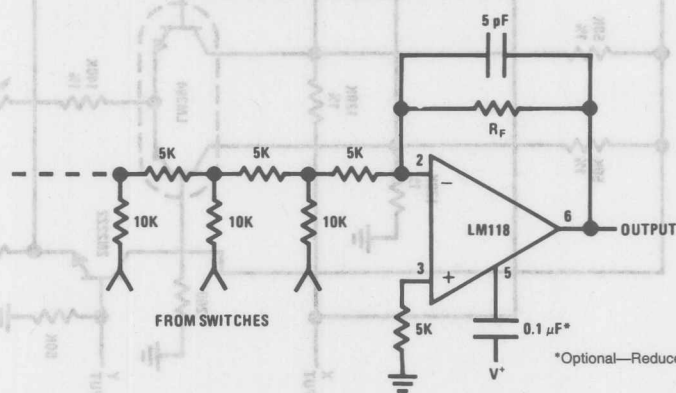
TL/H/7766-16

Fast Sample and Hold



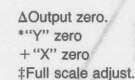
TL/H/7766-18

D/A Converter Using Ladder Network

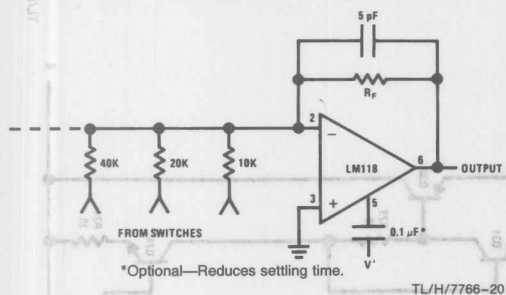


*Optional—Reduces settling time.

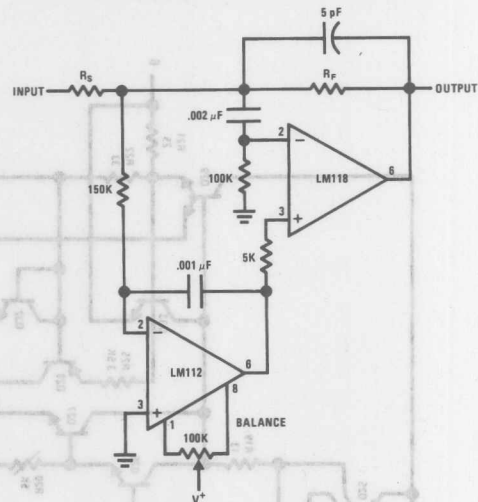
TL/H/7766-19



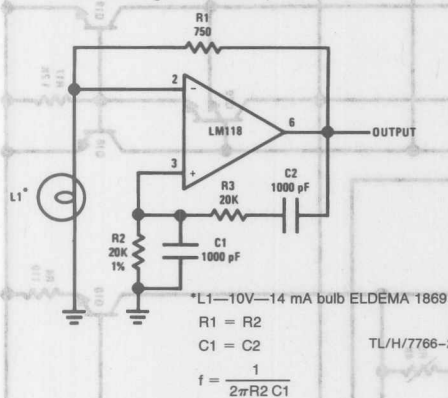
D/A Converter Using Binary Weighted Network



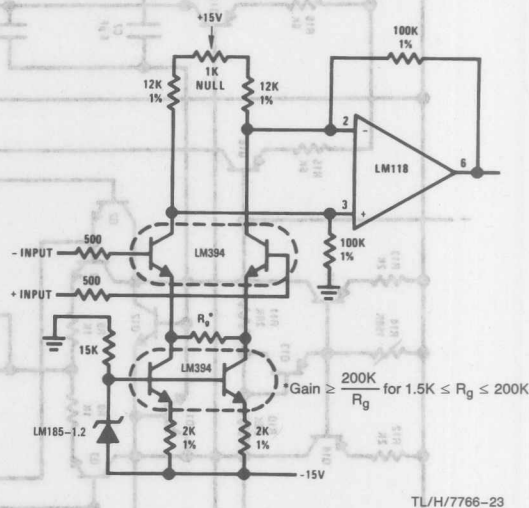
Fast Summing Amplifier with Low Input Current



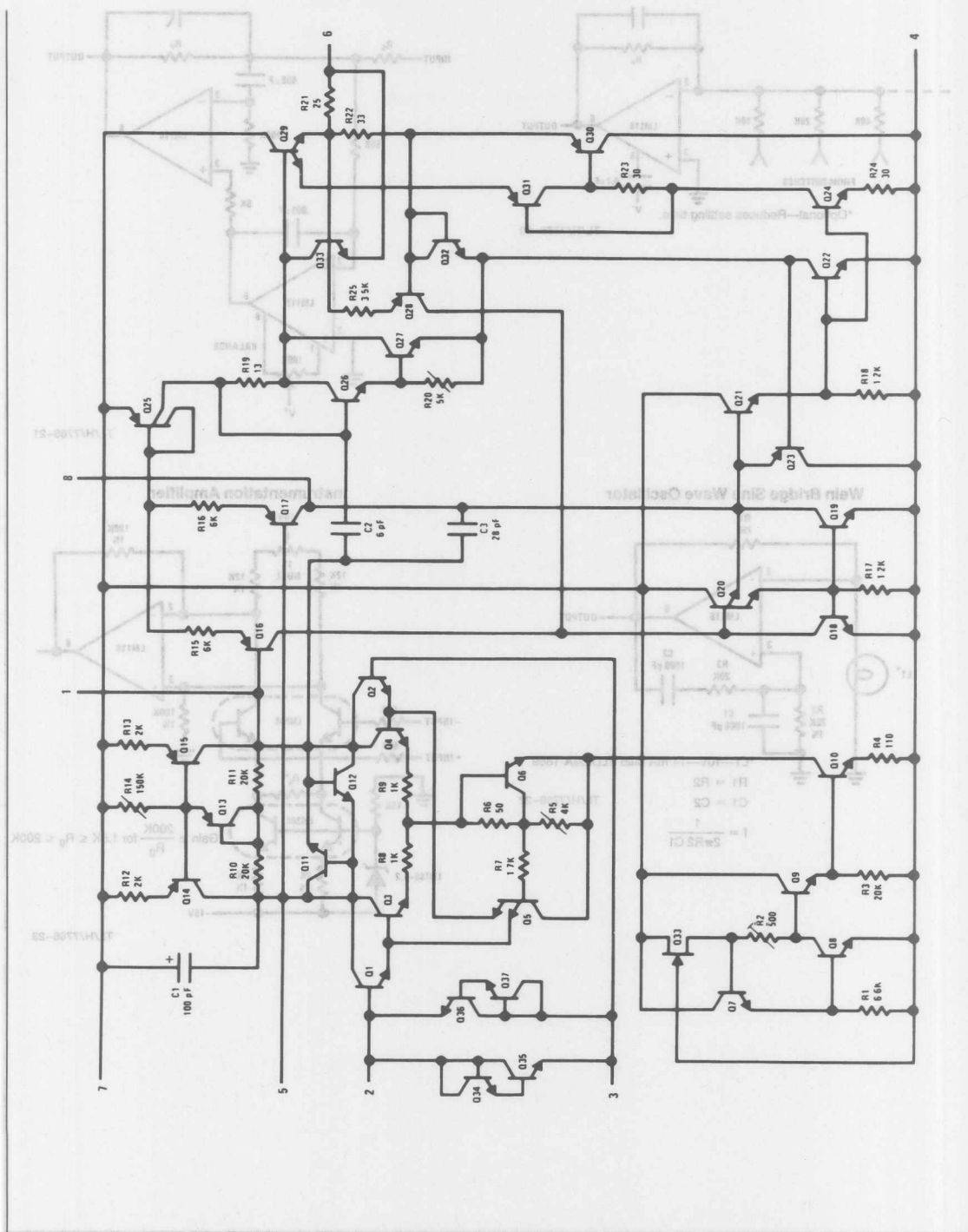
Wein Bridge Sine Wave Oscillator

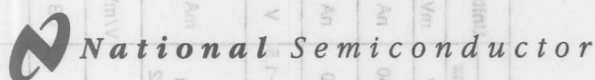


Instrumentation Amplifier



LM218/LM318





LM124/LM224/LM324/LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15V$ power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

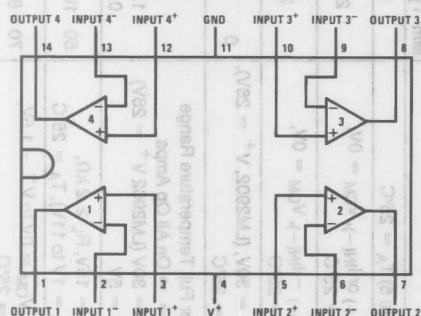
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
Single supply 3V to 32V
or dual supplies $\pm 1.5V$ to $\pm 16V$
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to $V^+ - 1.5V$

Connection Diagram

Dual-In-Line Package



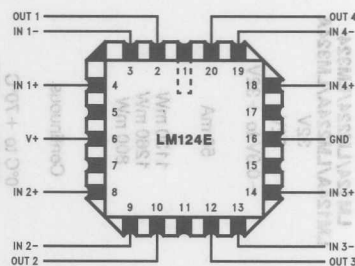
TL/H/9299-1

Top View

Order Number LM124J, LM124AJ, LM124J/883**,
LM124AJ/883*, LM224J, LM224AJ, LM324J, LM324M,
LM324AM, LM2902M, LM324N, LM324AN or LM2902N
See NS Package Number J14A, M14A or N14A

*LM124A available per JM38510/11006

**LM124 available per JM38510/11005



TL/H/9299-32

Order Number LM124AE/883 or LM124E/883

See NS Package Number E20A



TL/H/9299-33

Order Number LM124AW/883 or LM124W/883

See NS Package Number W14B

LM124/LM224/LM324/LM2902

1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

| | LM124/LM224/LM324 LM124A/LM224A/LM324A | LM2902 | LM124/LM224/LM324 LM124A/LM224A/LM324A | LM2902 |
|---|---|----------------|---|-----------------|
| Supply Voltage, V^+ | 32V | 26V | –65°C to +150°C | –65°C to +150°C |
| Differential Input Voltage | 32V | 26V | 260°C | 260°C |
| Input Voltage | –0.3V to +32V | –0.3V to +26V | | |
| Input Current ($V_{IN} < -0.3V$) (Note 3) | 50 mA | 50 mA | | |
| Power Dissipation (Note 1) | | | | |
| Molded DIP | 1130 mW | 1130 mW | | |
| Cavity DIP | 1260 mW | 1260 mW | | |
| Small Outline Package | 800 mW | 800 mW | | |
| Output Short-Circuit to GND (One Amplifier) (Note 2) | | | | |
| $V^+ \leq 15V$ and $T_A = 25^\circ C$ | Continuous | Continuous | | |
| Operating Temperature Range | | –40°C to +85°C | | |
| LM324/LM324A | 0°C to +70°C | | | |
| LM224/LM224A | –25°C to +85°C | | | |
| LM124/LM124A | –55°C to +125°C | | | |
| | | | Storage Temperature Range | –65°C to +150°C |
| | | | Lead Temperature (Soldering, 10 seconds) | 260°C |
| | | | Soldering Information | |
| | | | Dual-In-Line Package | |
| | | | Soldering (10 seconds) | 260°C |
| | | | Small Outline Package | 260°C |
| | | | Vapor Phase (60 seconds) | 215°C |
| | | | Infrared (15 seconds) | 220°C |
| | | | See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | |
| | | | ESD Tolerance (Note 10) | 250V |

Electrical Characteristics $V^+ = +5.0V$, (Note 4), unless otherwise stated

| Parameter | Conditions | LM124A | | LM224A | | LM324A | | LM124/LM224 | | LM324 | | LM2902 | | Units |
|--|---|--------|-----|-------------|-----|--------|-------------|-------------|-----|-------------|-----|--------|-------------|-------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 5) $T_A = 25^\circ C$ | 1 | | 2 | 1 | | 3 | 2 | | 3 | 2 | | 7 | mV |
| Input Bias Current (Note 6) | $I_{IN(+)} \text{ or } I_{IN(-)}, V_{CM} = 0V, T_A = 25^\circ C$ | 20 | | 50 | 40 | | 80 | 45 | | 100 | 45 | | 250 | nA |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}, V_{CM} = 0V, T_A = 25^\circ C$ | 2 | | 10 | 2 | | 15 | 5 | | 30 | 3 | | 50 | nA |
| Input Common-Mode Voltage Range (Note 7) | $V^+ = 30V, (LM2902, V^+ = 26V), T_A = 25^\circ C$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | V |
| Supply Current | Over Full Temperature Range $R_L = \infty$ On All Op Amps $V^+ = 30V$ (LM2902 $V^+ = 26V$) $V^+ = 5V$ | 1.5 | | 3 | 1.5 | | 3 | 1.5 | | 3 | 1.5 | | 3 | mA |
| | | 0.7 | | 1.2 | 0.7 | | 1.2 | 0.7 | | 1.2 | 0.7 | | 1.2 | |
| Large Signal Voltage Gain | $V^+ = 15V, R_L \geq 2 k\Omega, (V_O = 1V \text{ to } 11V), T_A = 25^\circ C$ | 50 | | 100 | 50 | | 100 | 25 | | 100 | 25 | | 100 | V/mV |
| Common-Mode Rejection Ratio | DC, $V_{CM} = 0V \text{ to } V^+ - 1.5V, T_A = 25^\circ C$ | 70 | | 85 | 70 | | 85 | 65 | | 85 | 70 | | 85 | dB |
| Power Supply Rejection Ratio | $V^+ = 5V \text{ to } 30V$ (LM2902, $V^+ = 5V \text{ to } 26V$), $T_A = 25^\circ C$ | 65 | | 100 | 65 | | 100 | 65 | | 100 | 65 | | 100 | dB |

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

| Parameter | Conditions | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|--|--|----------------------------|-----------|-----|-----------|-----|-----------|--------|-----------|-----|-------------|-----|-----------|-------|-----------|-----|-----------|-----|-----------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Amplifier-to-Amplifier Coupling (Note 8) | $f = 1 \text{ kHz to } 20 \text{ kHz}, T_A = 25^\circ\text{C}$ (Input Referred) | -120 | | | -120 | | | -120 | | | -120 | | | -120 | | | -120 | | | dB |
| Output Current | Source $V_{IN}^+ = 1V, V_{IN}^- = 0V,$ $V^+ = 15V, V_O = 2V, T_A = 25^\circ\text{C}$ | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | mA |
| | Sink $V_{IN}^- = 1V, V_{IN}^+ = 0V,$ $V^+ = 15V, V_O = 2V, T_A = 25^\circ\text{C}$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | |
| | $V_{IN}^- = 1V, V_{IN}^+ = 0V,$ $V^+ = 15V, V_O = 200 \text{ mV}, T_A = 25^\circ\text{C}$ | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | μA |
| Short Circuit to Ground | (Note 2) $V^+ = 15V, T_A = 25^\circ\text{C}$ | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | mA |
| Input Offset Voltage | (Note 5) | 4 | | | 4 | | | 5 | | | 7 | | | 9 | | | 10 | | | mV |
| Input Offset Voltage Drift | $R_S = 0\Omega$ | 7 | 20 | | 7 | 20 | | 7 | 30 | | 7 | | | 7 | | | 7 | | | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}, V_{CM} = 0V$ | 30 | | | 30 | | | 75 | | | 100 | | | 150 | | | 45 | 200 | | nA |
| Input Offset Current Drift | $R_S = 0\Omega$ | 10 | 200 | | 10 | 200 | | 10 | 300 | | 10 | | | 10 | | | 10 | | | $\text{pA}/^\circ\text{C}$ |
| Input Bias Current | $I_{IN(+)} \text{ or } I_{IN(-)}$ | 40 | 100 | | 40 | 100 | | 40 | 200 | | 40 | 300 | | 40 | 500 | | 40 | 500 | | nA |
| Input Common-Mode Voltage Range (Note 7) | $V^+ = +30V$ (LM2902, $V^+ = 26V$) | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | 0 | $V^+ - 2$ | V |
| Large Signal Voltage Gain | $V^+ = +15V$ (V_O Swing = 1V to 11V) $R_L \geq 2 \text{ k}\Omega$ | 25 | | | 25 | | | 15 | | | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | V_{OH} $V^+ = 30V$ (LM2902, $V^+ = 26V$) | $R_L = 2 \text{ k}\Omega$ | 26 | | 26 | | | 26 | | | 26 | | | 26 | | | 22 | | | V |
| | V_{OL} $V^+ = 5V, R_L = 10 \text{ k}\Omega$ | $R_L = 10 \text{ k}\Omega$ | 27 | 28 | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 23 | 24 | | mV |

LM124/LM224/LM324/LM2902

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

| Parameter | Conditions | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|----------------|------------|---|-----|-----|--------|-----|-----|--------|-----|-----|-------------|-----|-----|-------|-----|-----|--------|-----|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Current | Source | $V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$ | | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | Sink | $V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$ | | | 10 | 15 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | |

Note 1: For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a $+125^\circ C$ maximum junction temperature and a thermal resistance of $88^\circ C/W$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a $+150^\circ C$ maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+ . At values of supply voltage in excess of $+15V$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$ (at $25^\circ C$).

Note 4: These specifications are limited to $-55^\circ C \leq T_A \leq +125^\circ C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$, the LM324/LM324A temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$, and the LM2902 specifications are limited to $-40^\circ C \leq T_A \leq +85^\circ C$.

Note 5: $V_O = 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range ($0V$ to $V^+ - 1.5V$) for LM2902, V^+ from 5V to 26V.

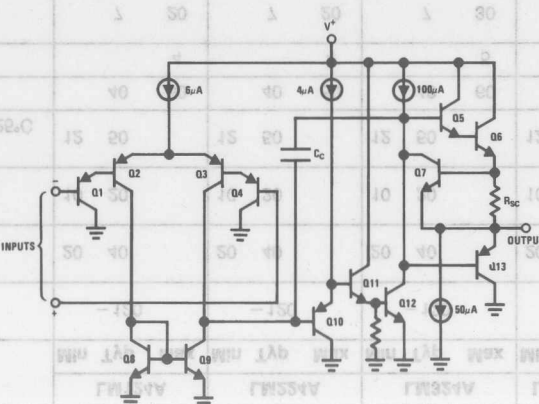
Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than $0.3V$ (at $25^\circ C$). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at $25^\circ C$), but either or both inputs can go to $+32V$ without damage ($+26V$ for LM2902), independent of the magnitude of V^+ .

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

Note 9: Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

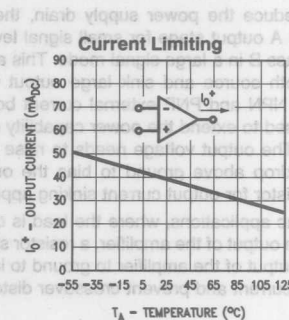
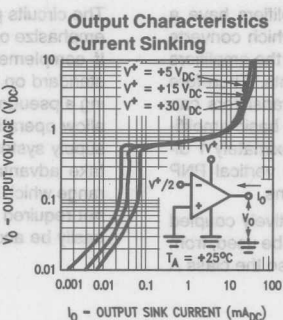
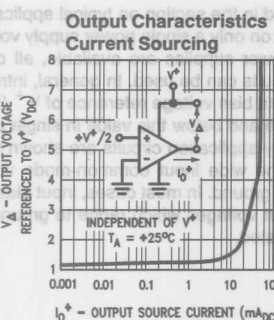
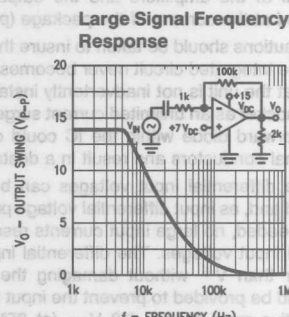
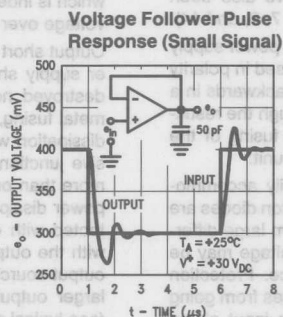
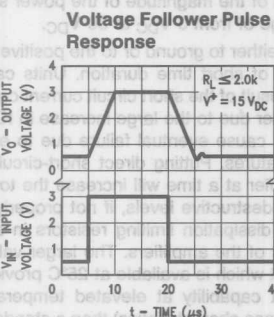
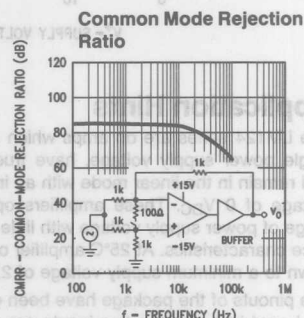
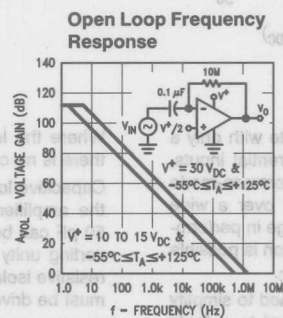
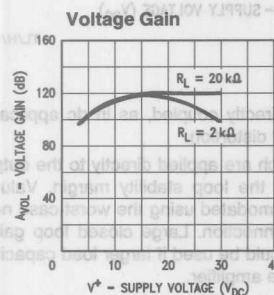
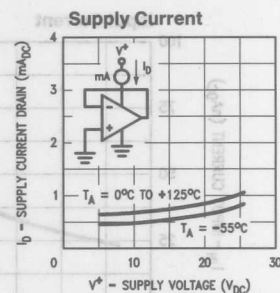
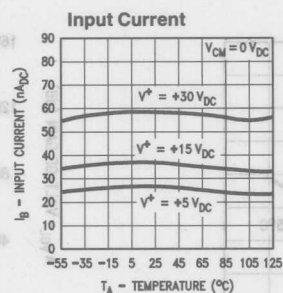
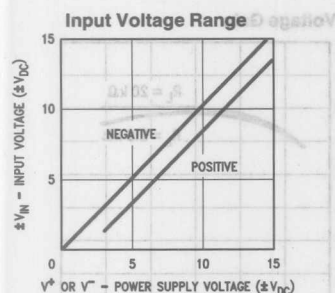
Note 10: Human body model, $1.5 k\Omega$ in series with $100 pF$.

Schematic Diagram (Each Amplifier)

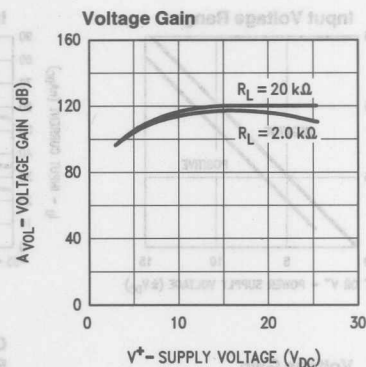
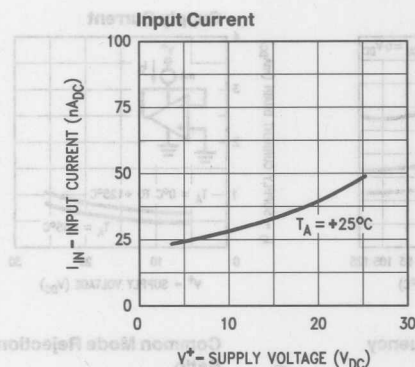
TL/H/9299-2

Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

Typical Performance Characteristics



TL/H/9299-3



TL/H/9299-4

Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC} . These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At $25^\circ C$ amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC} .

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3 V_{DC}$ (at $25^\circ C$). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

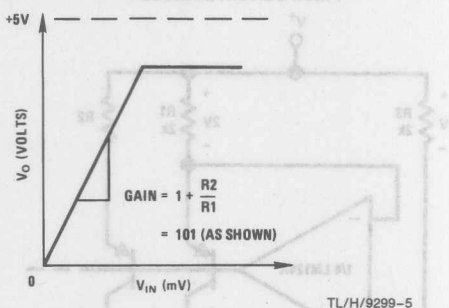
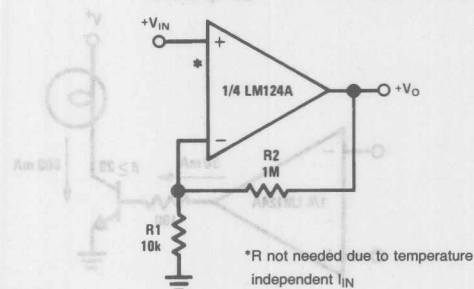
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 V_{DC} to 30 V_{DC} .

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at $25^\circ C$ provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

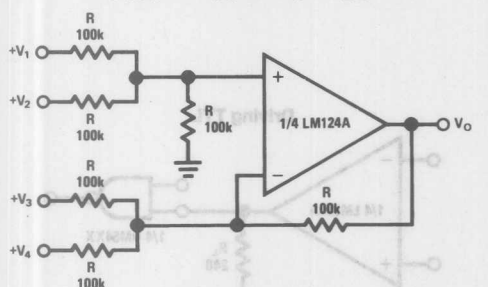
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

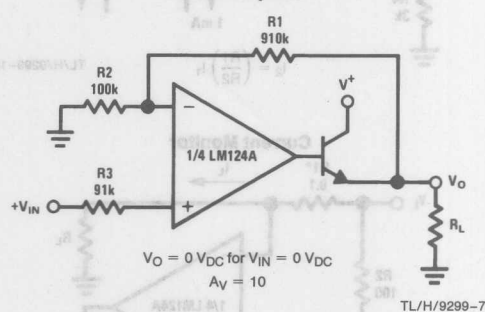


DC Summing Amplifier ($V_{IN'S} \geq 0 V_{DC}$ and $V_O \geq V_{DC}$)

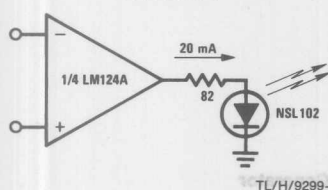


Where: $V_O = V_1 + V_2 - V_3 - V_4$
($V_1 + V_2 \geq (V_3 + V_4)$ to keep $V_O > 0 V_{DC}$)

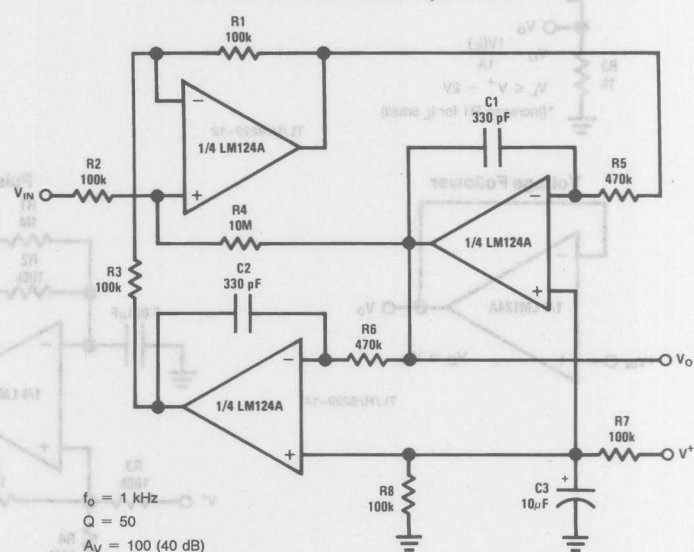
Power Amplifier



LED Driver

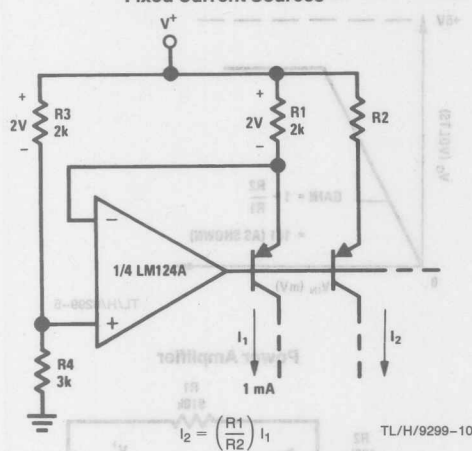


"BI-QUAD" RC Active Bandpass Filter

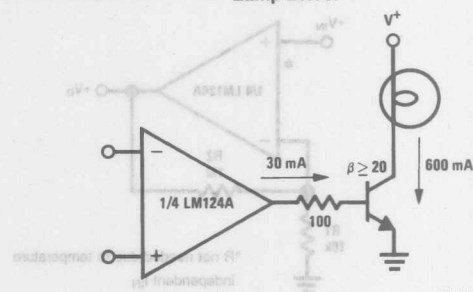


Typical Single-Supply Applications ($V^+ = 5.0 \text{ V}_{\text{DC}}$) (Continued)

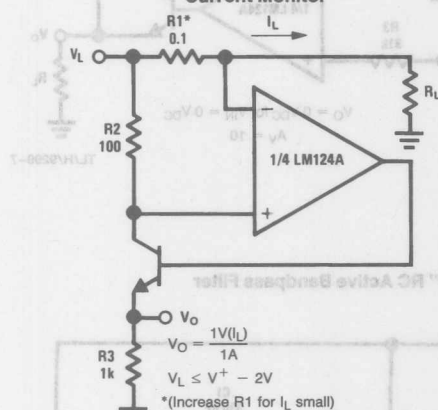
Fixed Current Sources



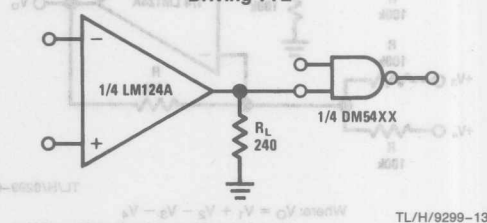
Lamp Driver



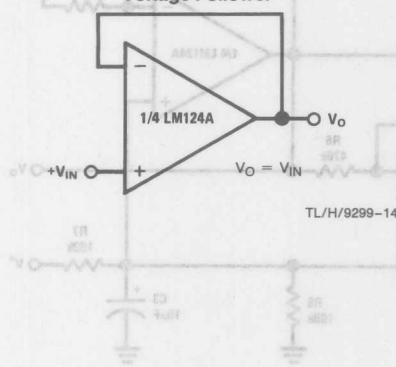
Current Monitor



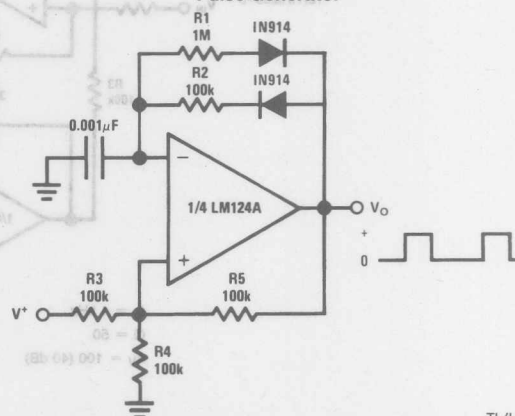
Driving TTL



Voltage Follower

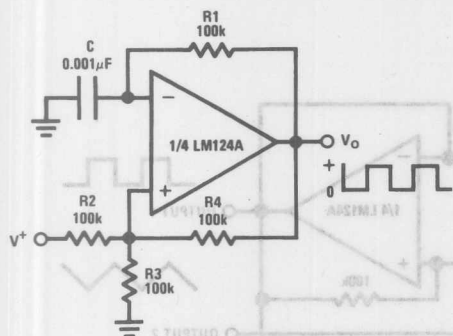


Pulse Generator



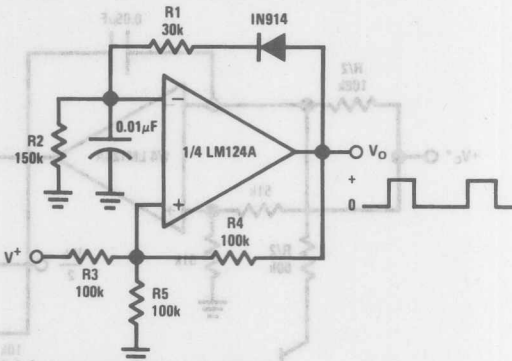
Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

Squarewave Oscillator



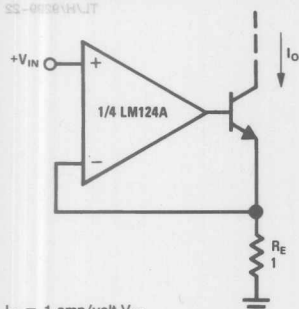
TL/H/9299-16

Pulse Generator



TL/H/9299-17

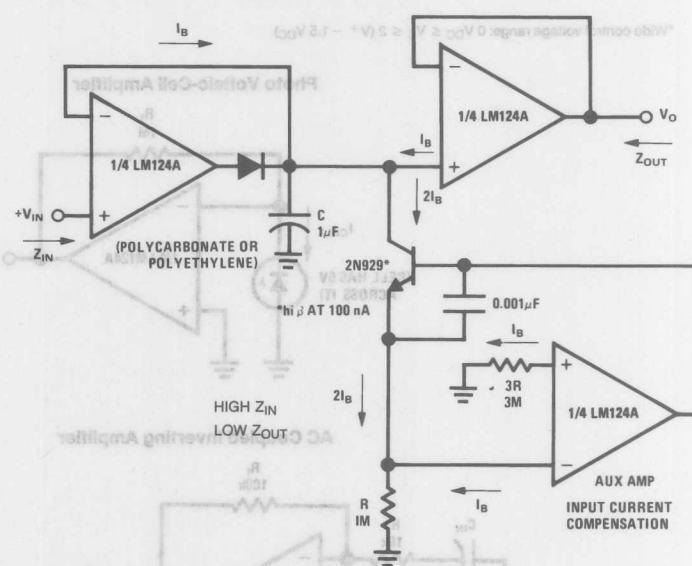
High Compliance Current Sink



$I_O = 1\text{ amp/volt } V_{IN}$
(Increase R_E for I_O small)

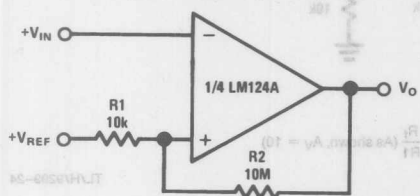
TL/H/9299-18

Low Drift Peak Detector



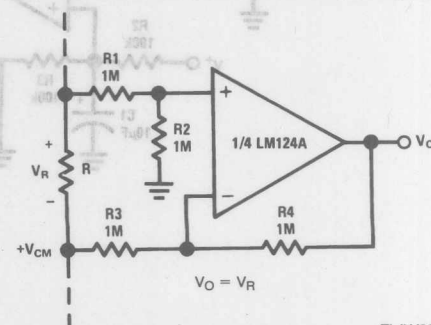
TL/H/9299-19

Comparator with Hysteresis



TL/H/9299-20

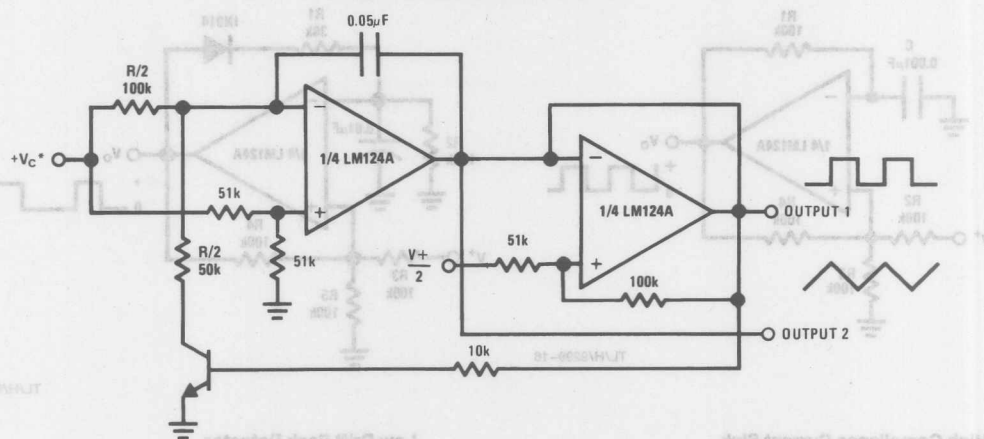
Ground Referencing a Differential Input Signal



TL/H/9299-21

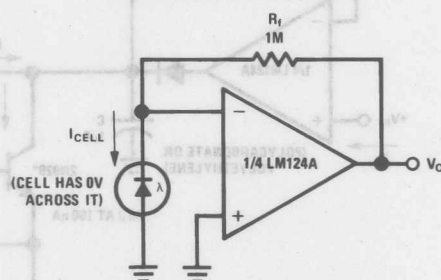
Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

Voltage Controlled Oscillator Circuit



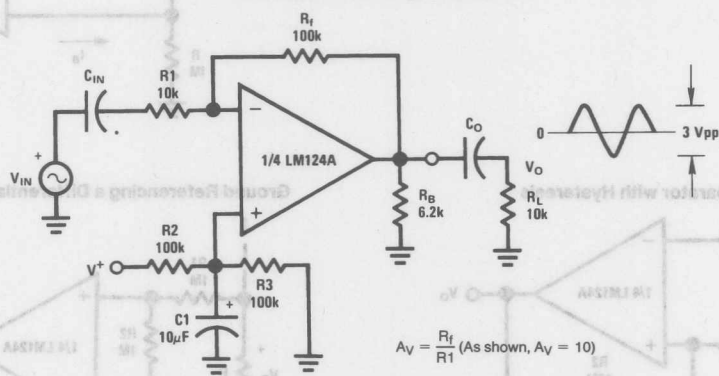
*Wide control voltage range: $0 V_{DC} \leq V_C \leq 2 (V^+ - 1.5 V_{DC})$

Photo Voltaic-Cell Amplifier



TL/H/9299-23

AC Coupled Inverting Amplifier

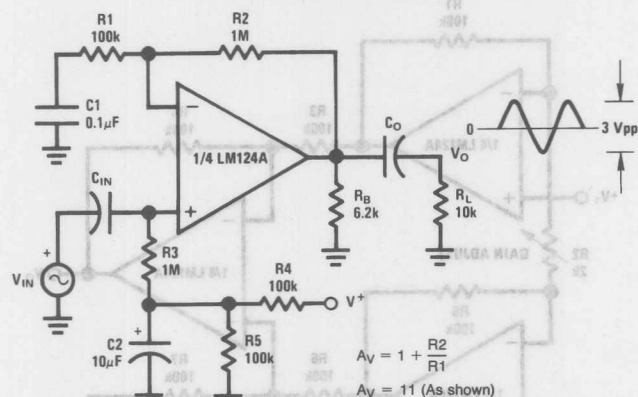


$$A_v = \frac{R_f}{R_1} \text{ (As shown, } A_v = 10 \text{)}$$

TL/H/9299-24

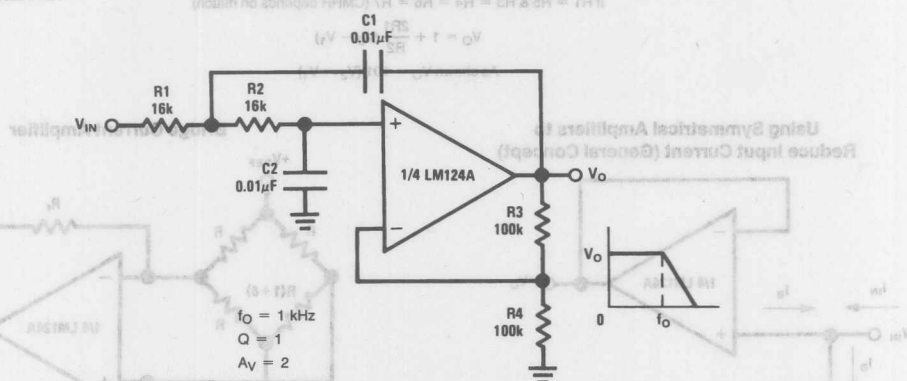
Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

AC Coupled Non-Inverting Amplifier



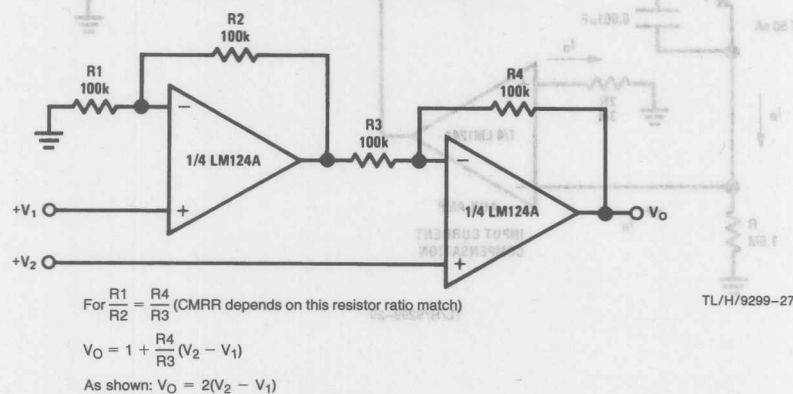
TL/H/9299-25

DC Coupled Low-Pass RC Active Filter

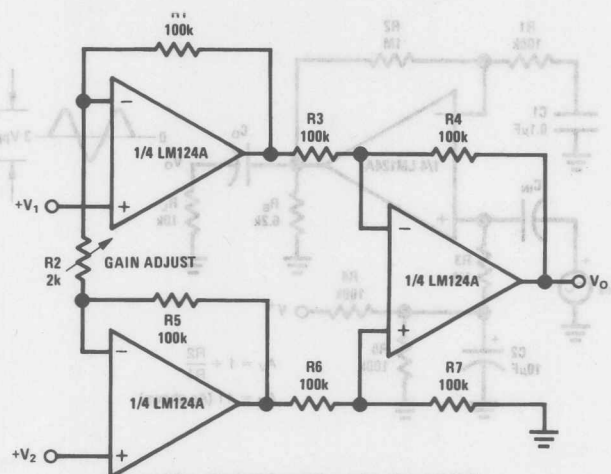


TL/H/9299-26

High Input Z, DC Differential Amplifier



TL/H/9299-27



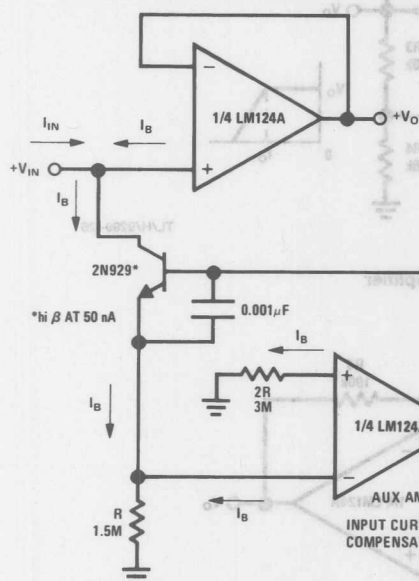
If $R1 = R5$ & $R3 = R4 = R6 = R7$ (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2} (V_2 - V_1)$$

As shown $V_O = 101 (V_2 - V_1)$

TL/H/9299-28

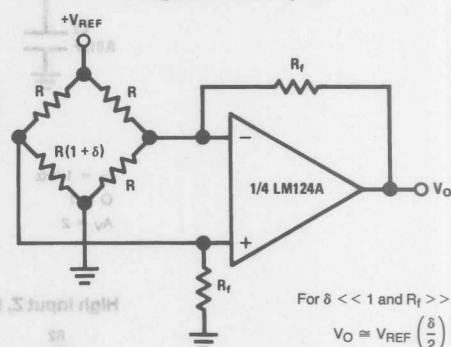
Using Symmetrical Amplifiers to Reduce Input Current (General Concept)



*hi β AT 50 nA

TL/H/9299-29

Bridge Current Amplifier



For $\delta \ll 1$ and $R_f \gg R$

$$V_O \approx V_{REF} \left(\frac{\delta}{2} \right) \frac{R_f}{R}$$

TL/H/9299-30



LM143/LM343 High Voltage Operational Amplifier

General Description

The LM143 is a general purpose high voltage operational amplifier featuring operation to $\pm 40\text{V}$, complete input over-voltage protection up to $\pm 40\text{V}$ and input currents comparable to those of other super- β op amps. Increased slew rate, together with higher common-mode and supply rejection, insure improved performance at high supply voltages. Operating characteristics, in particular supply current, slew rate and gain, are virtually independent of supply voltage and temperature. Furthermore, gain is unaffected by output loading at high supply voltages due to thermal symmetry on the die. The LM143 is pin compatible with general purpose op amps and has offset null capability.

Application areas include those of general purpose op amps, but can be extended to higher voltages and higher output power when externally boosted. For example, when used in audio power applications, the LM143 provides a power bandwidth that covers the entire audio spectrum. In addition, the LM143 can be reliably operated in environments with large overvoltage spikes on the power supplies, where other internally-compensated op amps would suffer catastrophic failure.

The LM343 is similar to the LM143 for applications in less severe supply voltage and temperature environments.

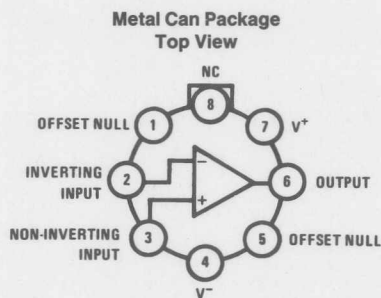
Features

- Wide supply voltage range $\pm 4.0\text{V}$ to $\pm 40\text{V}$
- Large output voltage swing $\pm 37\text{V}$
- Wide input common-mode range $\pm 38\text{V}$
- Input overvoltage protection Full $\pm 40\text{V}$
- Supply current is virtually independent of supply voltage and temperature

Unique Characteristics

- Low input bias current 8.0 nA
- Low input offset current 1.0 nA
- High slew rate—essentially independent of temperature and supply voltage $2.5\text{V}/\mu\text{s}$
- High voltage gain—virtually independent of resistive loading, temperature, and supply voltage 100k min
- Internally compensated for unity gain
- Output short circuit protection
- Pin compatible with general purpose op amps

Connection Diagram



Order Number LM143H, LM143H/883* or LM343H
See NS Package Number H08C

TL/H/7783-1

*Available per SMD# 7800303

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

| | LM143 | LM343 |
|---------------------------------------|-----------------|-----------------|
| Supply Voltage | ±40V | ±34V |
| Power Dissipation (Note 1) | 680 mW | 680 mW |
| Differential Input Voltage (Note 2) | 80V | 68V |
| Input Voltage (Note 2) | ±40V | ±34V |
| Operating Temperature Range | −55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Output Short Circuit Duration | 5 seconds | 5 seconds |
| Lead Temperature (Soldering, 10 sec.) | 300°C | 300°C |
| ESD rating to be determined. | | |

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM143 | | | LM343 | | | Units |
|--------------------------------|--|------------|--------------|------------|------------|--------------|----------|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$ | | 2.0 | 5.0 | | 2.0 | 8.0 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 1.0 | 3.0 | | 1.0 | 10 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 8.0 | 20 | | 8.0 | 40 | nA |
| Supply Voltage Rejection Ratio | $T_A = 25^\circ\text{C}$ | | 10 | 100 | | 10 | 200 | $\mu\text{V/V}$ |
| Output Voltage Swing | $T_A = 25^\circ\text{C}, R_L \geq 5\text{ k}\Omega$ | 22 | 25 | | 20 | 25 | | V |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}, V_{\text{OUT}} = \pm 10\text{V}, R_L \geq 100\text{ k}\Omega$ | 100k | 180k | | 70k | 180k | | V/V |
| Common-Mode Rejection Ratio | $T_A = 25^\circ\text{C}$ | 80 | 90 | | 70 | 90 | | dB |
| Input Voltage Range | $T_A = 25^\circ\text{C}$ | ±24 | ±26 | | ±22 | ±26 | | V |
| Supply Current (Note 5) | $T_A = 25^\circ\text{C}$ | | 2.0 | 4.0 | | 2.0 | 5.0 | mA |
| Short Circuit Current | $T_A = 25^\circ\text{C}$ | | 20 | | | 20 | | mA |
| Slew Rate | $T_A = 25^\circ\text{C}, A_V = 1$ | | 2.5 | | | 2.5 | | V/ μs |
| Power Bandwidth | $T_A = 25^\circ\text{C}, V_{\text{OUT}} = 40\text{ V}_{\text{p-p}}, R_L = 5\text{ k}\Omega, \text{THD} \leq 1\%$ | | 20k | | | 20k | | Hz |
| Unity Gain Frequency | $T_A = 25^\circ\text{C}$ | | 1.0M | | | 1.0M | | Hz |
| Input Offset Voltage | $T_A = \text{Max}$ $T_A = \text{Min}$ | | | 6.0 6.0 | | | 10 10 | mV |
| Input Offset Current | $T_A = \text{Max}$ $T_A = \text{Min}$ | | 0.8 1.8 | 4.5 7.0 | | 0.8 1.8 | 14 14 | nA |
| Input Bias Current | $T_A = \text{Max}$ $T_A = \text{Min}$ | | 5.0 16 | 35 35 | | 5.0 16 | 55 55 | nA |
| Large Signal Voltage Gain | $R_L \geq 100\text{ k}\Omega, T_A = \text{Max}$ $R_L \geq 100\text{ k}\Omega, T_A = \text{Min}$ | 50k 50k | 150k 220k | | 50k 50k | 150k 220k | | V/V |
| Output Voltage Swing | $R_L \geq 5.0\text{ k}\Omega, T_A = \text{Max}$ $R_L \geq 5.0\text{ k}\Omega, T_A = \text{Min}$ | 22 22 | 26 25 | | 20 20 | 26 25 | | V |

Note 1: Absolute maximum ratings are not necessarily concurrent, and care must be taken not to exceed the maximum junction temperature of the LM143 (150°C) or the LM343 (100°C). For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 155°C/W, junction to ambient, or 20°C/W, junction to case.

Note 2: For supply voltage less than ±40V for the LM143 and less than ±34V for the LM343, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 28\text{V}$. For LM143, $T_A = \text{max} = 125^\circ\text{C}$ and $T_A = \text{min} = -55^\circ\text{C}$. For LM343, $T_A = \text{max} = 70^\circ\text{C}$ and $T_A = \text{min} = 0^\circ\text{C}$.

Note 4: Refer to RETS143X for LM143H and LM1536H military specifications.

Note 5: The maximum supply currents are guaranteed at $V_S = \pm 40\text{V}$ for the LM143 and $V_S = \pm 34\text{V}$ for the LM343.

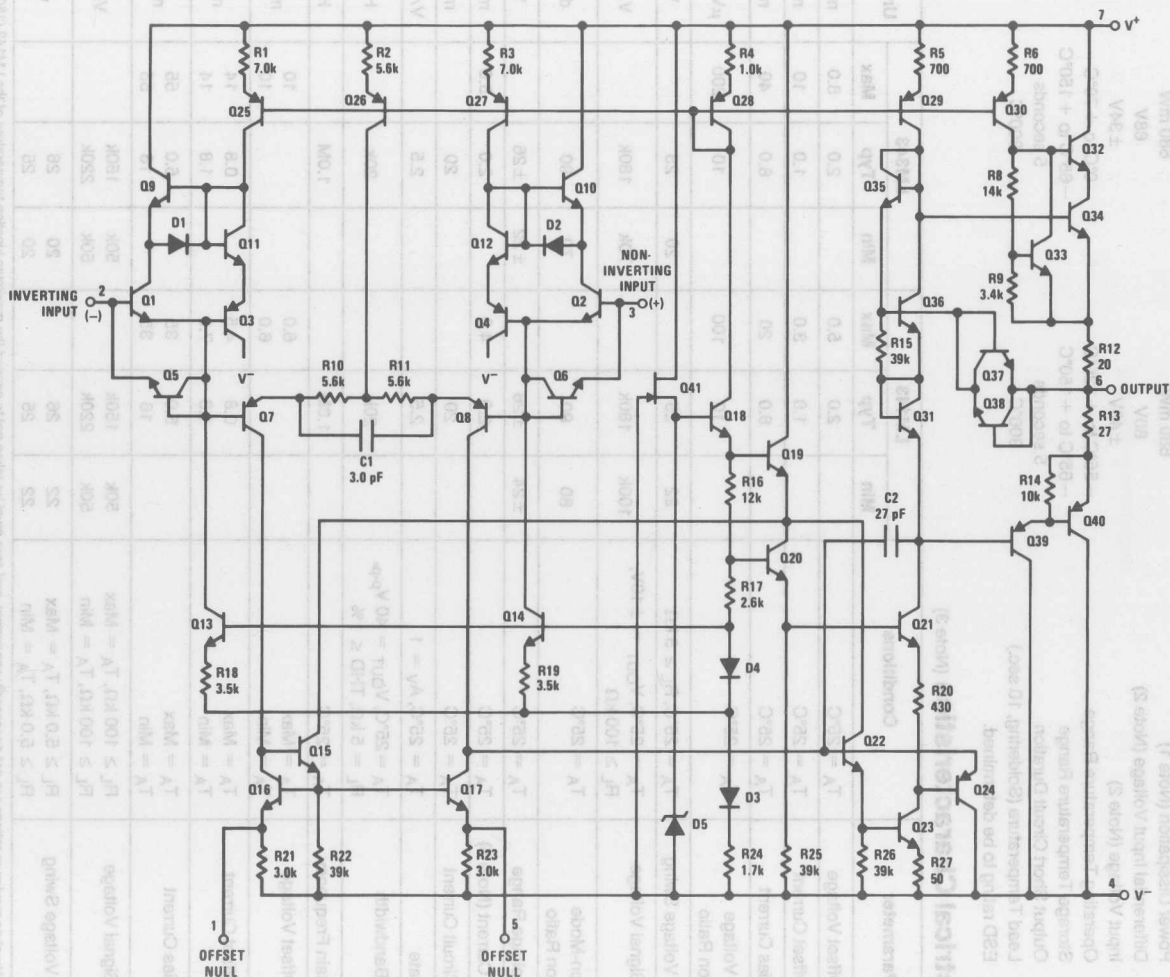
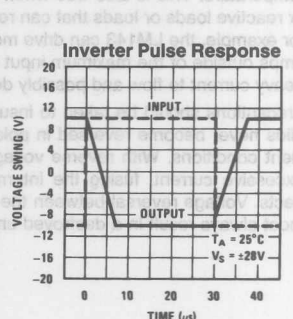
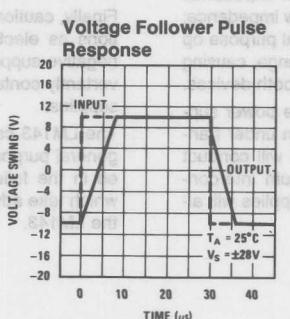
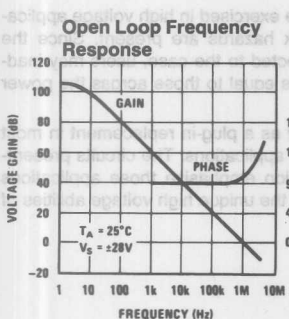
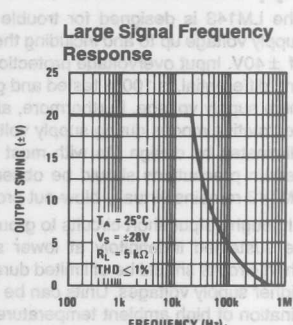
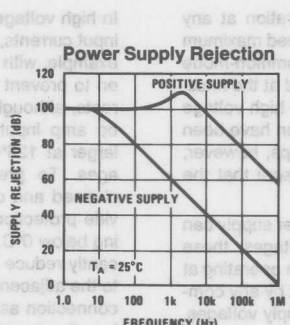
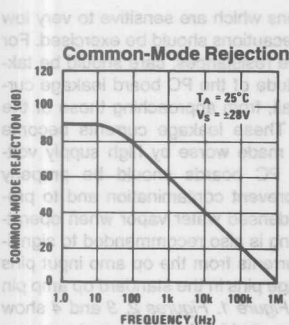
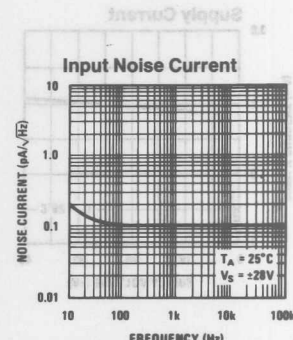
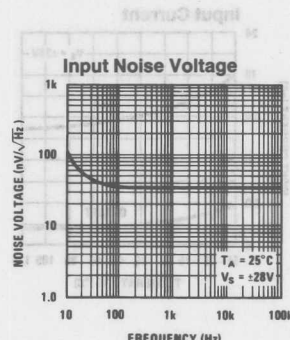
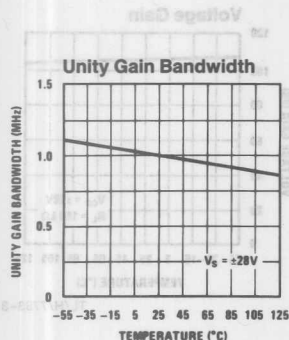
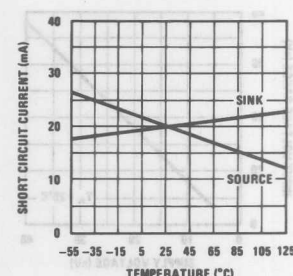
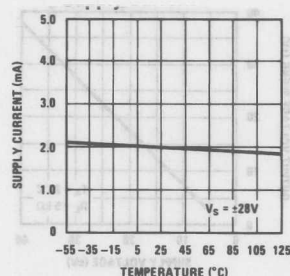
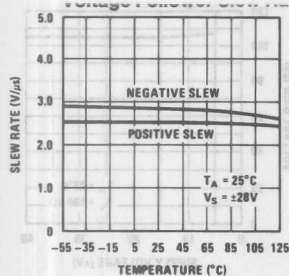
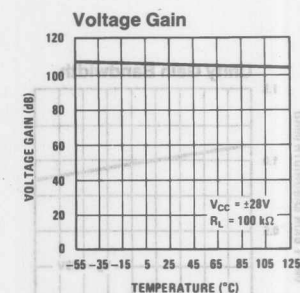
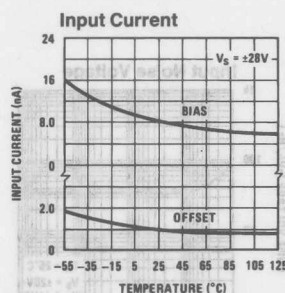
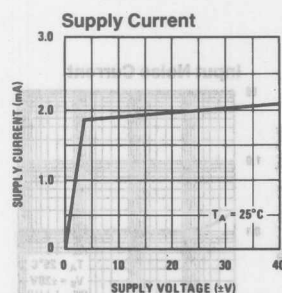
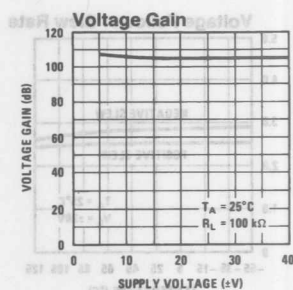
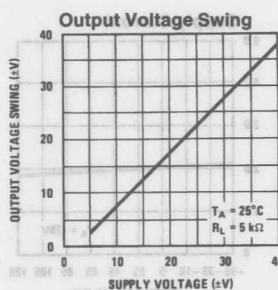
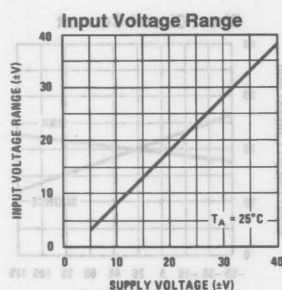


FIGURE 1. Precision centimeter voltmeter circuit. The LM14 is a precision centimeter voltmeter. It is designed to provide a linear output voltage for a given input voltage. The circuit is designed to provide a linear output voltage for a given input voltage. The circuit is designed to provide a linear output voltage for a given input voltage.



TL/H/7783-4

Typical Performance Characteristics (Continued)



TL/H/7783-3

Application Hints (See AN-127)

The LM143 is designed for trouble free operation at any supply voltage up to and including the guaranteed maximum of $\pm 40\text{V}$. Input overvoltage protection, both common-mode and differential, is 100% tested and guaranteed at the maximum supply voltage. Furthermore, all possible high voltage destructive modes during supply voltage turn-on have been eliminated by design. As with most IC op amps, however, certain precautions should be observed to insure that the LM143 remains virtually blow-out proof.

Although output short circuits to ground or either supply can be sustained indefinitely at lower supply voltages, these short circuits should be of limited duration when operating at higher supply voltages. Units can be destroyed by any combination of high ambient temperature, high supply voltages, and high power dissipation which results in excessive die temperature. This is also true when driving low impedance or reactive loads or loads that can revert to low impedance; for example, the LM143 can drive most general purpose op amps outside of the maximum input voltage range, causing heavy current to flow and possibly destroying both devices.

Precautions should be taken to insure that the power supplies never become reversed in polarity—even under transient conditions. With reverse voltage, the IC will conduct excessive current, fusing the internal aluminum interconnects. Voltage reversal between the power supplies will almost always result in a destroyed unit.

In high voltage applications which are sensitive to very low input currents, special precautions should be exercised. For example, with high source resistances, care should be taken to prevent the magnitude of the PC board leakage currents, although quite small, from approaching those of the op amp input currents. These leakage currents become larger at 125°C and are made worse by high supply voltages. To prevent this, PC boards should be properly cleaned and coated to prevent contamination and to provide protection from condensed water vapor when operating below 0°C . A guard ring is also recommended to significantly reduce leakage currents from the op amp input pins to the adjacent high voltage pins in the standard op amp pin connection as shown in Figure 1. Figures 2, 3 and 4 show how the guard ring is connected for the three most common op amp configurations.

Finally, caution should be exercised in high voltage applications as electrical shock hazards are present. Since the negative supply is connected to the case, users may inadvertently contact voltages equal to those across the power supplies.

The LM143 can be used as a plug-in replacement in most general purpose op amp applications. The circuits presented in the following section emphasize those applications which take advantage of the unique high voltage abilities of the LM143.

Application Hints (See AN-127) (Continued)

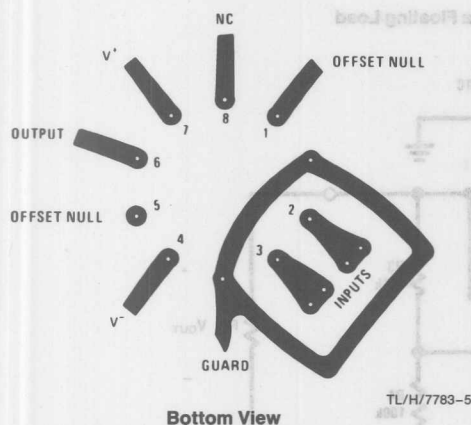


FIGURE 1. Printed Circuit Layout for Input Guarding with TO-5 Package

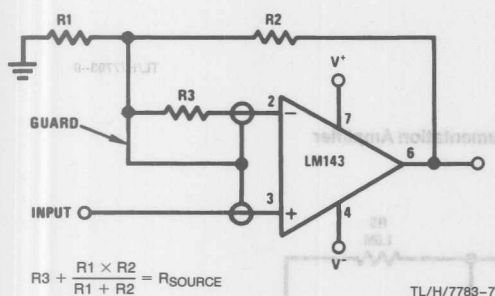


FIGURE 3. Guarded Non-Inverting Amplifier

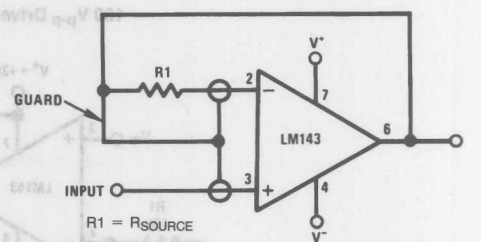


FIGURE 2. Guarded Voltage Follower

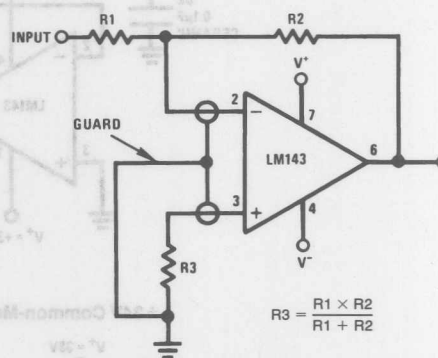


FIGURE 4. Guarded Inverting Amplifier

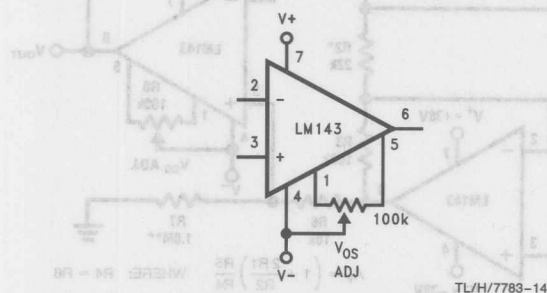
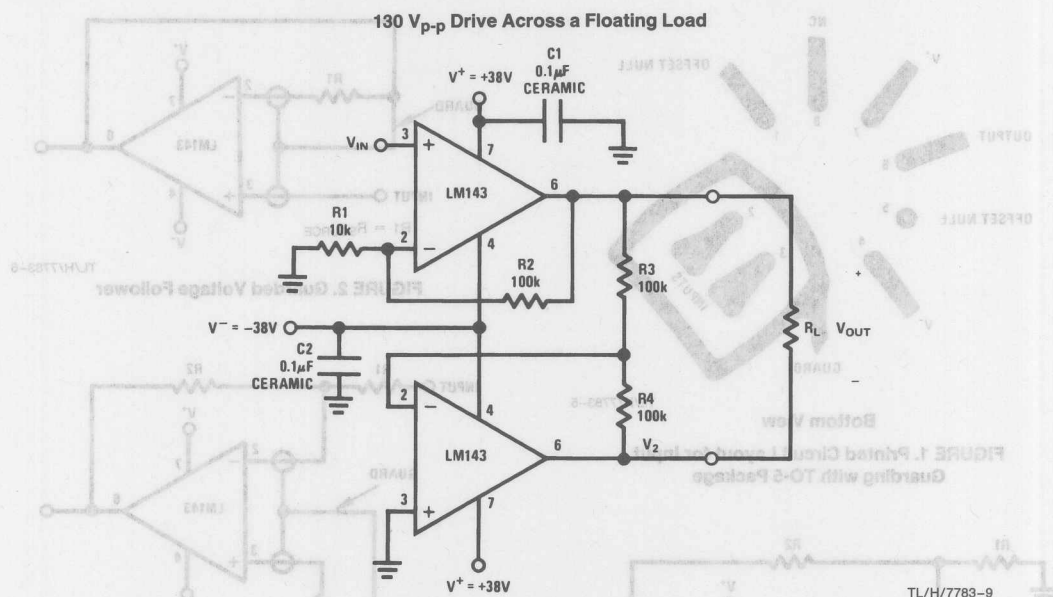


FIGURE 5. Offset Voltage Adjustment

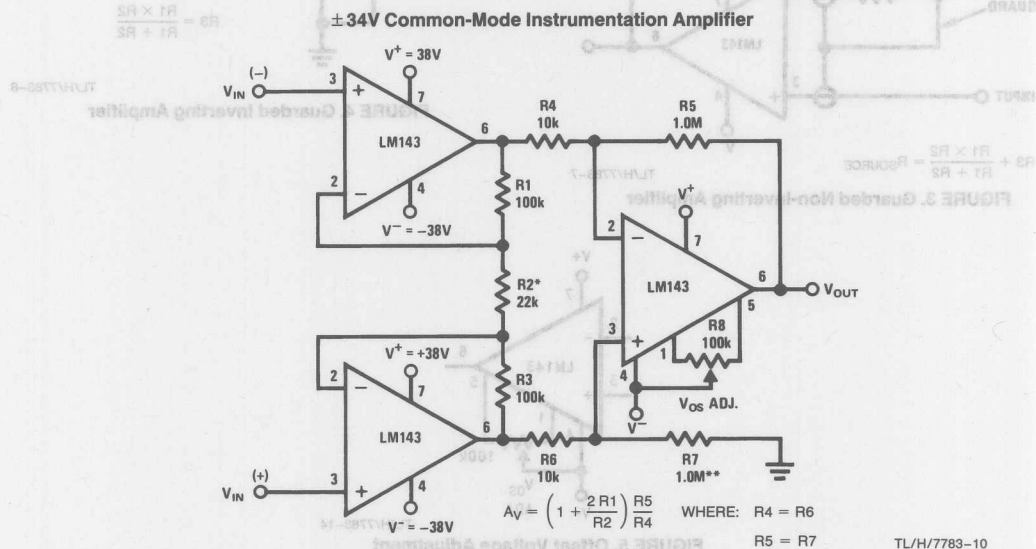
Typical Applications ‡ (For more detail see AN-127)

Application Hints (See AN-127) (Continued)

130 V_{p-p} Drive Across a Floating Load



±34V Common-Mode Instrumentation Amplifier

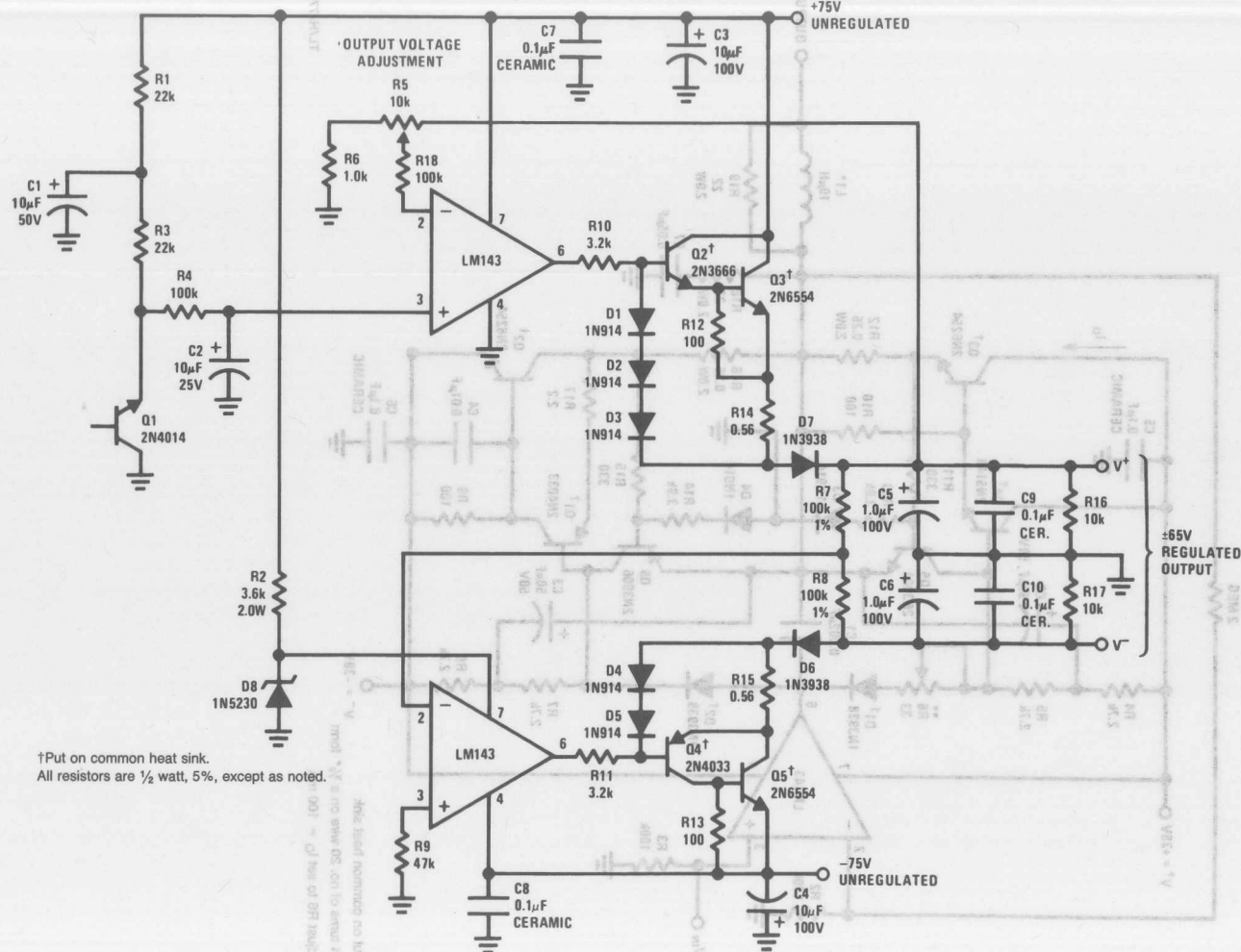


*R2 may be adjustable to trim the gain.

**R7 may be adjusted to compensate for the resistance tolerance of R4-R7 for best CMR.

‡The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

Tracking $\pm 65V$, 1 Amp Power Supply with Short Circuit Protection

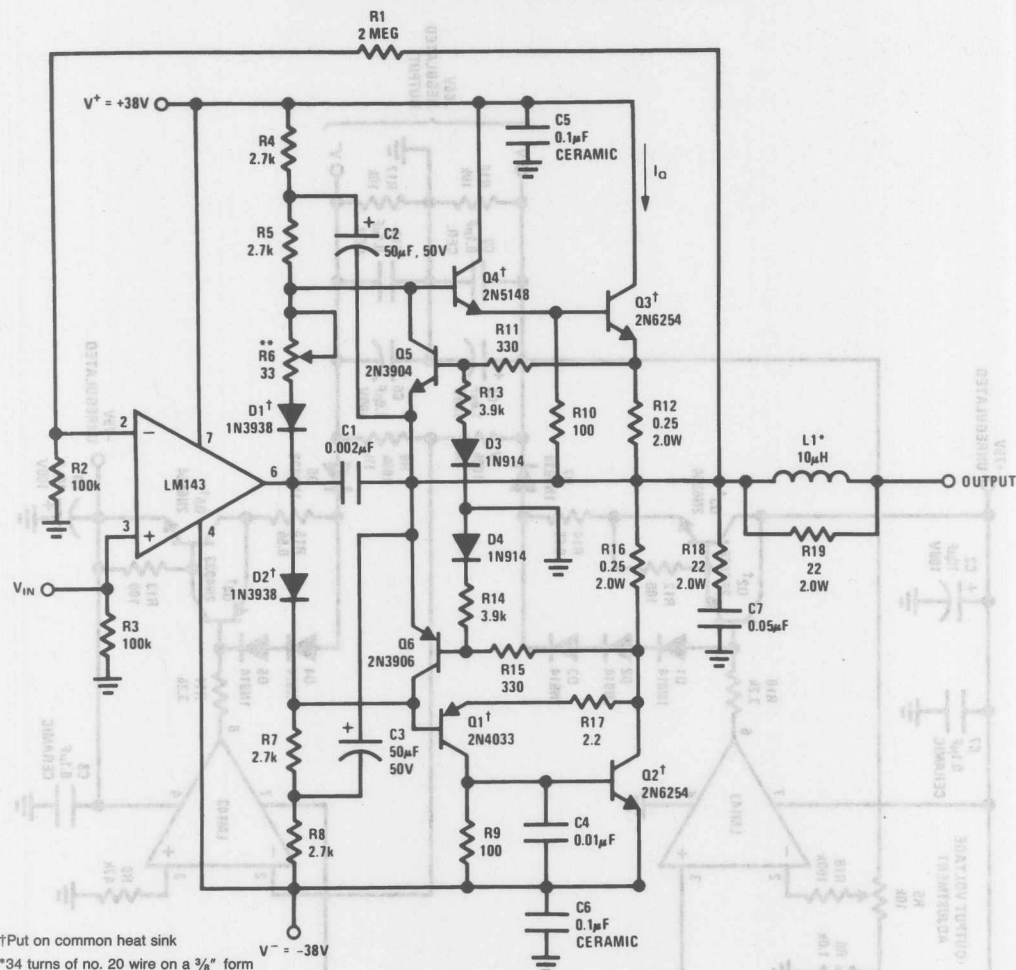


†Put on common heat sink.
All resistors are 1/2 watt, 5%, except as noted.

†The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

TL/H/7783-11

LM143/LM343



† Put on common heat sink

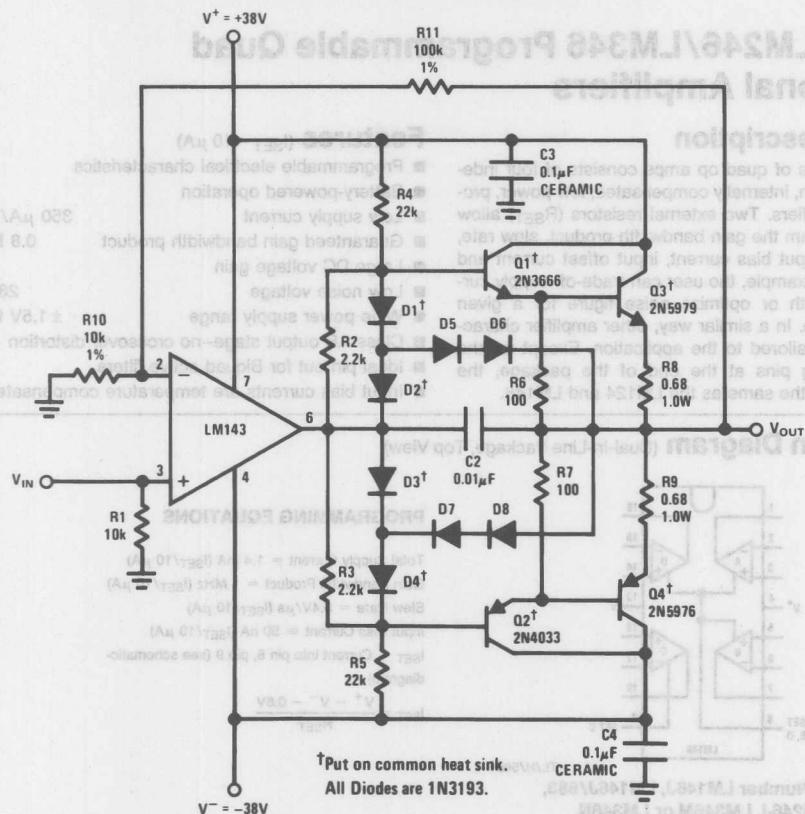
* 34 turns of no. 20 wire on a $\frac{3}{8}$ " form

** Adjust $R6$ to set $I_Q = 100$ mA

TL/H/7783-12

‡ The 38V supplies allow for a 5% voltage tolerance. All resistors are $\frac{1}{2}$ watt, except as noted.

1 Amp Power Amplifier with Short Circuit Protection



†The 38V supplies allow for a 5% voltage tolerance. All resistors are 1/2 watt, except as noted.

TL/H/7783-13

LM343



LM146/LM246/LM346 Programmable Quad Operational Amplifiers

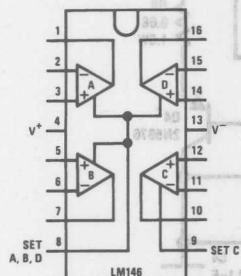
General Description

The LM146 series of quad op amps consists of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

Features ($I_{SET} = 10 \mu A$)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current 350 μA /amplifier
- Guaranteed gain bandwidth product 0.8 MHz min
- Large DC voltage gain 120 dB
- Low noise voltage 28 nV/ \sqrt{Hz}
- Wide power supply range $\pm 1.5V$ to $\pm 22V$
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Input bias currents are temperature compensated

Connection Diagram (Dual-In-Line Package, Top View)



PROGRAMMING EQUATIONS

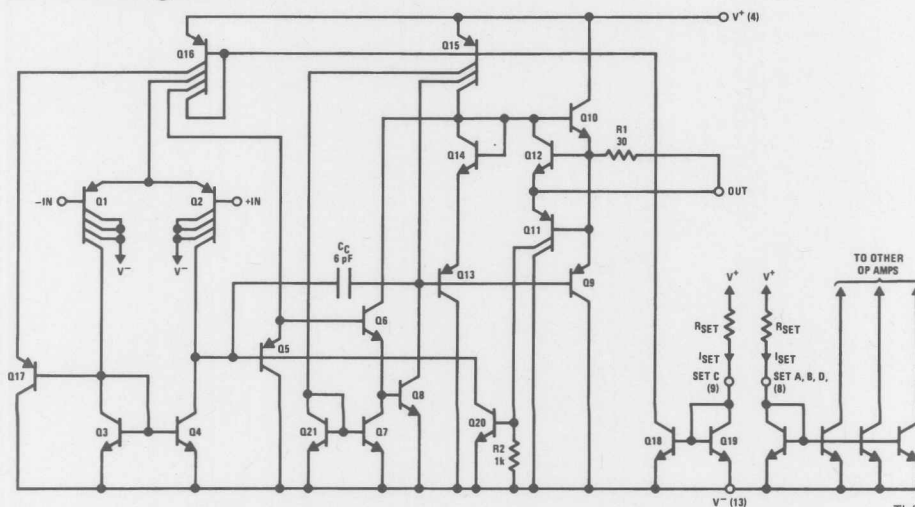
Total Supply Current = 1.4 mA ($I_{SET}/10 \mu A$)
 Gain Bandwidth Product = 1 MHz ($I_{SET}/10 \mu A$)
 Slew Rate = 0.4V/ μs ($I_{SET}/10 \mu A$)
 Input Bias Current ≈ 50 nA ($I_{SET}/10 \mu A$)
 I_{SET} = Current into pin 8, pin 9 (see schematic-diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

Order Number LM146J, LM146J/883,
 LM246J, LM346M or LM346N

See NS Package Number J16A, M16A or N16A

Schematic Diagram



TL/H/5654-2

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 5)

| Parameter | Min | Typ | Max | Parameter | Min | Typ | Max | Parameter | Min | Typ | Max |
|--|---------------|-----|-----------------|-----------|-----|-----|-----------------|-----------|-----|-----|-----------------|
| Supply Voltage | | | ±22V | LM146 | | | ±18V | LM246 | | | ±18V |
| Differential Input Voltage (Note 1) | | | ±30V | | | | ±30V | | | | ±30V |
| CM Input Voltage (Note 1) | | | ±15V | | | | ±15V | | | | ±15V |
| Power Dissipation (Note 2) | | | 900 mW | | | | 500 mW | | | | 500 mW |
| Output Short-Circuit Duration (Note 3) | | | Continuous | | | | Continuous | | | | Continuous |
| Operating Temperature Range | | | -55°C to +125°C | | | | -25°C to +85°C | | | | 0°C to +70°C |
| Maximum Junction Temperature | | | 150°C | | | | 110°C | | | | 100°C |
| Storage Temperature Range | | | -65°C to +150°C | | | | -65°C to +150°C | | | | -65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | | | 260°C | | | | 260°C | | | | 260°C |
| Thermal Resistance (θ_{JA}), (Note 2) | | | | | | | | | | | |
| Cavity DIP (J) | Pd | | 900 mW | | | | 900 mW | | | | 900 mW |
| | θ_{JA} | | 100°C/W | | | | 100°C/W | | | | 100°C/W |
| Small Outline (M) | θ_{JA} | | | | | | | | | | 115°C/W |
| Molded DIP (N) | Pd | | | | | | | | | | 500 mW |
| | θ_{JA} | | | | | | | | | | 90°C/W |
| Soldering Information | | | | | | | | | | | |
| Dual-In-Line Package | | | | | | | | | | | |
| Soldering (10 seconds) | | | +260°C | | | | +260°C | | | | +260°C |
| Small Outline Package | | | | | | | | | | | |
| Vapor Phase (60 seconds) | | | +215°C | | | | +215°C | | | | +215°C |
| Infrared (15 seconds) | | | +220°C | | | | +220°C | | | | +220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating is to be determined.

DC Electrical Characteristics ($V_S = \pm 15V$, $I_{SET} = 10 \mu A$, Note 4)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|------------------------------|--|-------|------|-----|-------------|------|-----|-----------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25^\circ C$ | 0.5 | 5 | | 0.5 | 6 | | mV |
| Input Offset Current | $V_{CM} = 0V$, $T_A = 25^\circ C$ | 2 | 20 | | 2 | 100 | | nA |
| Input Bias Current | $V_{CM} = 0V$, $T_A = 25^\circ C$ | 50 | 100 | | 50 | 250 | | nA |
| Supply Current (4 Op Amps) | $T_A = 25^\circ C$ | 1.4 | 2.0 | | 1.4 | 2.5 | | mA |
| Large Signal Voltage Gain | $R_L = 10 k\Omega$, $\Delta V_{OUT} = \pm 10V$, $T_A = 25^\circ C$ | 100 | 1000 | | 50 | 1000 | | V/mV |
| Input CM Range | $T_A = 25^\circ C$ | ±13.5 | ±14 | | ±13.5 | ±14 | | V |
| CM Rejection Ratio | $R_S \leq 10 k\Omega$, $T_A = 25^\circ C$ | 80 | 100 | | 70 | 100 | | dB |
| Power Supply Rejection Ratio | $R_S \leq 10 k\Omega$, $T_A = 25^\circ C$, $V_S = \pm 5$ to $\pm 15V$ | 80 | 100 | | 74 | 100 | | dB |
| Output Voltage Swing | $R_L \geq 10 k\Omega$, $T_A = 25^\circ C$ | ±12 | ±14 | | ±12 | ±14 | | V |
| Short-Circuit | $T_A = 25^\circ C$ | 5 | 20 | 35 | 5 | 20 | 35 | mA |
| Gain Bandwidth Product | $T_A = 25^\circ C$ | 0.8 | 1.2 | | 0.5 | 1.2 | | MHz |
| Phase Margin | $T_A = 25^\circ C$ | | 60 | | | 60 | | Deg |
| Slew Rate | $T_A = 25^\circ C$ | | 0.4 | | | 0.4 | | V/ μs |
| Input Noise Voltage | $f = 1 kHz$, $T_A = 25^\circ C$ | | 28 | | | 28 | | nV/ \sqrt{Hz} |
| Channel Separation | $R_L = 10 k\Omega$, $\Delta V_{OUT} = 0V$ to $\pm 12V$, $T_A = 25^\circ C$ | | 120 | | | 120 | | dB |
| Input Resistance | $T_A = 25^\circ C$ | | 1.0 | | | 1.0 | | M Ω |
| Input Capacitance | $T_A = 25^\circ C$ | | 2.0 | | | 2.0 | | pF |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$ | | 0.5 | 6 | | 0.5 | 7.5 | mV |
| Input Offset Current | $V_{CM} = 0V$ | | 2 | 25 | | 2 | 100 | nA |
| Input Bias Current | $V_{CM} = 0V$ | | 50 | 100 | | 50 | 250 | nA |
| Supply Current (4 Op Amps) | | | 1.7 | 2.2 | | 1.7 | 2.5 | mA |

DC Electrical Characteristics (Continued) ($V_S = \pm 15V$, $I_{SET} = 10 \mu A$, Note 4)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|------------------------------|--|------------|----------|-----|-------------|----------|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $R_L = 10 k\Omega$, $\Delta V_{OUT} = \pm 10V$ | 50 | 1000 | | 25 | 1000 | | V/mV |
| Input CM Range | | ± 13.5 | ± 14 | | ± 13.5 | ± 14 | | V |
| CM Rejection Ratio | $R_S \leq 50\Omega$ | 70 | 100 | | 70 | 100 | | dB |
| Power Supply Rejection Ratio | $R_S \leq 50\Omega$, $V_S = \pm 5V$ to $\pm 15V$ | 76 | 100 | | 74 | 100 | | dB |
| Output Voltage Swing | $R_L \geq 10 k\Omega$ | ± 12 | ± 14 | | ± 12 | ± 14 | | V |

DC Electrical Characteristic ($V_S = \pm 15V$, $I_{SET} = 1 \mu A$)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|----------------------------|---|-------|-----|-----|-------------|-----|-----|---------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25^\circ C$ | | 0.5 | 5 | | 0.5 | 7 | mV |
| Input Bias Current | $V_{CM} = 0V$, $T_A = 25^\circ C$ | | 7.5 | 20 | | 7.5 | 100 | nA |
| Supply Current (4 Op Amps) | $T_A = 25^\circ C$ | | 140 | 250 | | 140 | 300 | μA |
| Gain Bandwidth Product | $T_A = 25^\circ C$ | 80 | 100 | | 50 | 100 | | kHz |

DC Electrical Characteristics ($V_S = \pm 1.5V$, $I_{SET} = 10 \mu A$)

| Parameter | Conditions | LM146 | | | LM246/LM346 | | | Units |
|----------------------|---|-----------|-----|-----|-------------|-----|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $V_{CM} = 0V$, $R_S \leq 50\Omega$, $T_A = 25^\circ C$ | | 0.5 | 5 | | 0.5 | 7 | mV |
| Input CM Range | $T_A = 25^\circ C$ | ± 0.7 | | | ± 0.7 | | | V |
| CM Rejection Ratio | $R_S \leq 50\Omega$, $T_A = 25^\circ C$ | 80 | | | 80 | | | dB |
| Output Voltage Swing | $R_L \geq 10 k\Omega$, $T_A = 25^\circ C$ | ± 0.6 | | | ± 0.6 | | | V |

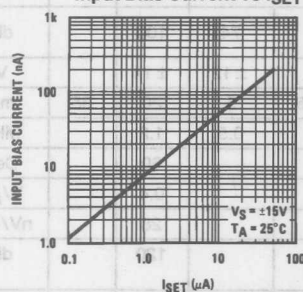
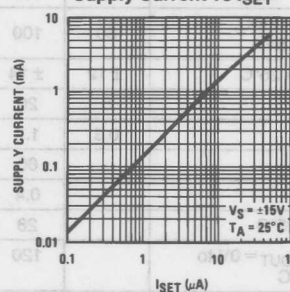
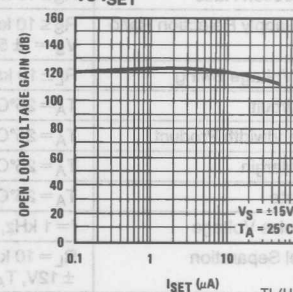
Note 1: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the $25^\circ C$ P_{dMAX} , whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

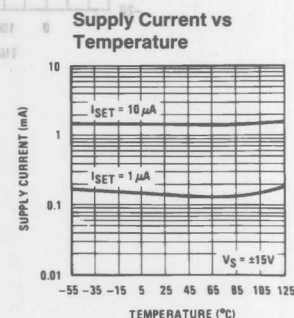
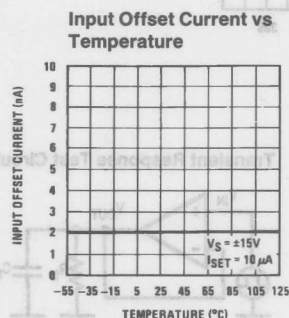
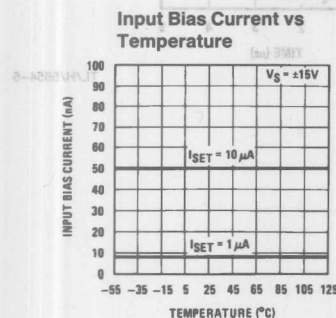
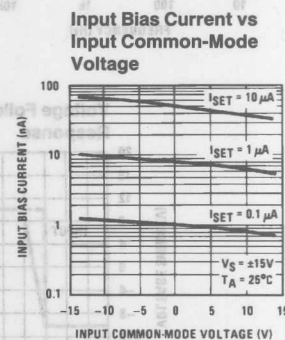
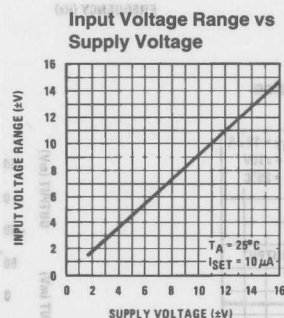
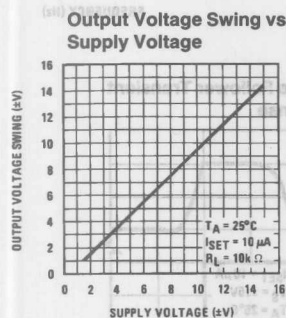
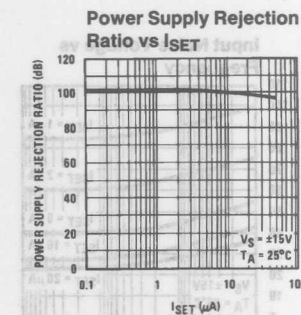
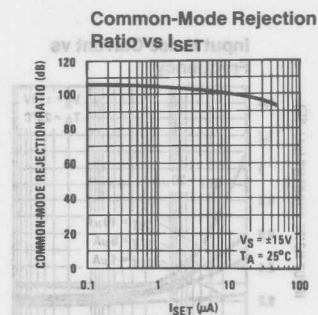
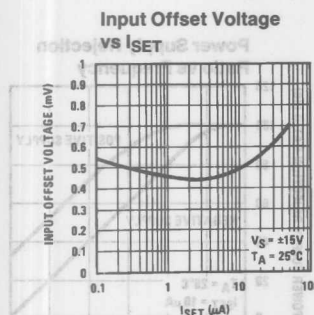
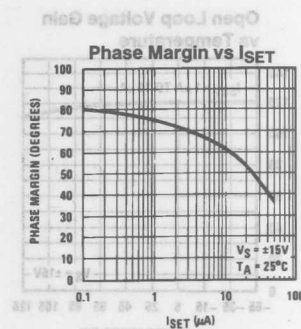
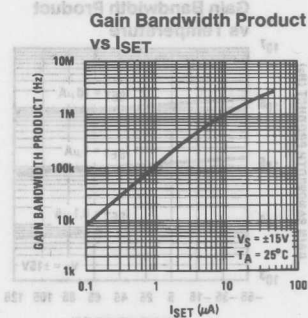
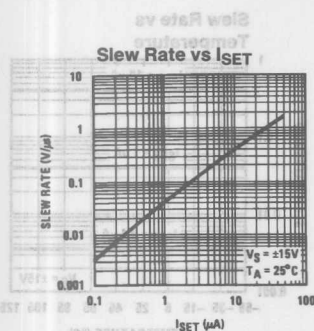
Note 4: These specifications apply over the absolute maximum operating temperature range unless otherwise noted.

Note 5: Refer to RETS146X for LM146J military specifications.

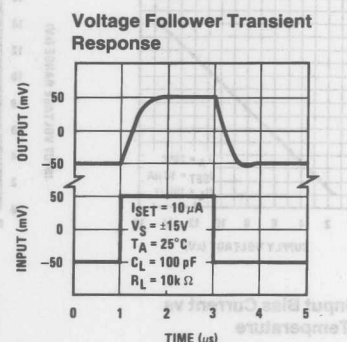
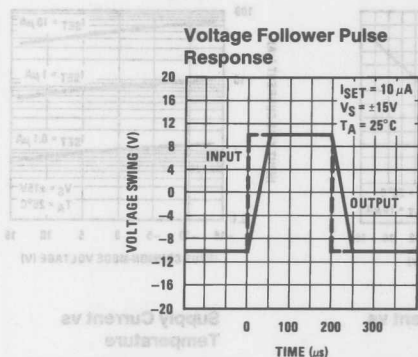
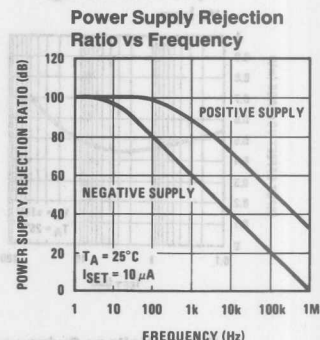
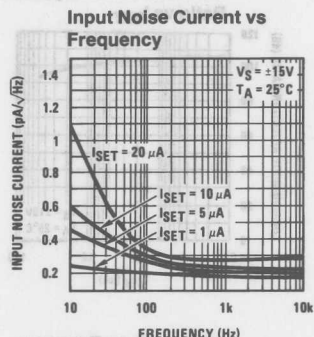
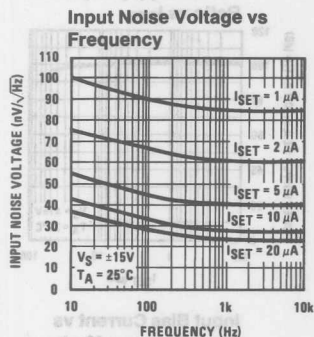
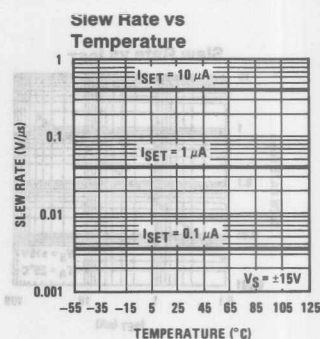
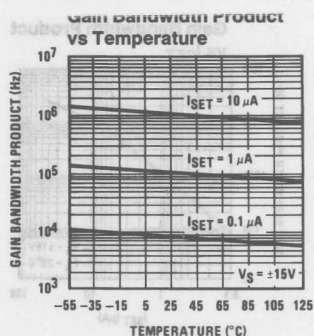
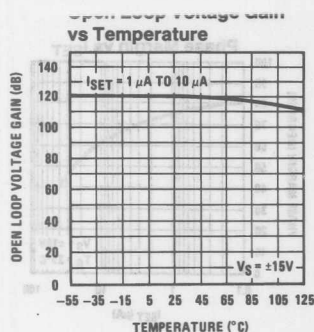
Typical Performance Characteristics**Input Bias Current vs I_{SET}** **Supply Current vs I_{SET}** **Open Loop Voltage Gain vs I_{SET}** 

TL/H/5654-3

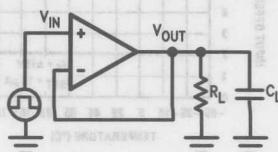
Typical Performance Characteristics



TL/H/5654-4



Transient Response Test Circuit



TL/H/5654-6

TL/H/5654-5

Common-Mode Input Voltage: The negative common-mode voltage limit is one diode drop above the negative supply voltage. Exceeding this limit on either input will result in an output phase reversal. The positive common-mode limit is typically 1V below the positive supply voltage. No output phase reversal will occur if this limit is exceeded by either input.

Output Voltage Swing vs I_{SET} : For a desired output voltage swing the value of the minimum load depends on the positive and negative output current capability of the op amp. The maximum available positive output current, (I_{CL+}), of the device increases with I_{SET} whereas the negative output current (I_{CL-}) is independent of I_{SET} . Figure 1 illustrates the above.

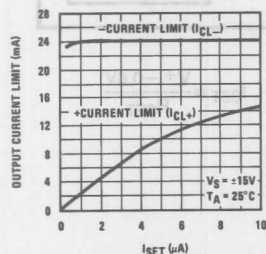


FIGURE 1. Output Current Limit vs I_{SET}

Input Capacitance: The input capacitance, C_{IN} , of the LM146 is approximately 2 pF; any stray capacitance, C_S , (due to external circuit circuit layout) will add to C_{IN} . When resistive or active feedback is applied, an additional pole is added to the open loop frequency response of the device. For instance with resistive feedback (Figure 2), this pole occurs at $1/2\pi (R_1||R_2) (C_{IN} + C_S)$. Make sure that this pole occurs at least 2 octaves beyond the expected -3 dB frequency corner of the closed loop gain of the amplifier; if not, place a lead capacitor in the feedback such that the time constant of this capacitor and the resistance it parallels is equal to the $R_1(C_S + C_{IN})$, where R_1 is the input resistance of the circuit.

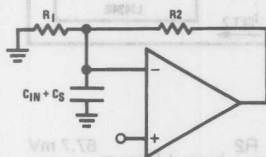


FIGURE 2

Temperature Effect on the GBW: The GBW (gain bandwidth product), of the LM146 is directly proportional to I_{SET} and inversely proportional to the absolute temperature. When using resistors to set the bias current, I_{SET} , of the device, the GBW product will decrease with increasing temperature. Compensation can be provided by creating an I_{SET} current directly proportional to temperature (see typical applications).

is in excess of -105 dB (DC). Optimum isolation (better than -110 dB) occurs between amplifiers A and D, B and C; that is, if amplifier A dissipates power on its output stage, amplifier D is the one which will be affected the least, and vice versa. Same argument holds for amplifiers B and C.

LM146 Typical Performance Summary: The LM146 typical behaviour is shown in Figure 3. The device is fully predictable. As the set current, I_{SET} , increases, the speed, the bias current, and the supply current increase while the noise power decreases proportionally and the V_{OS} remains constant. The usable GBW range of the op amp is 10 kHz to 3.5-4 MHz.

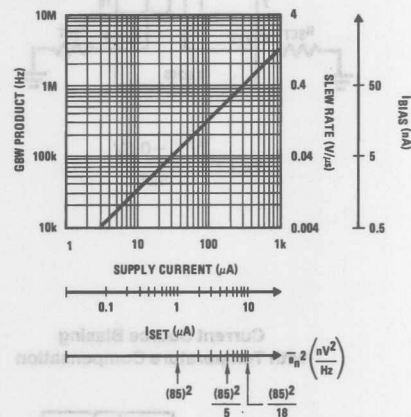


FIGURE 3. LM146 Typical Characteristics

Low Power Supply Operation: The quad op amp operates down to $\pm 1.3V$ supply. Also, since the internal circuitry is biased through programmable current sources, no degradation of the device speed will occur.

Speed vs Power Consumption: LM146 vs LM4250 (single programmable). Through Figure 4, we observe that the LM146's power consumption has been optimized for GBW products above 200 kHz, whereas the LM4250 will reach a GBW of no more than 300 kHz. For GBW products below 200 kHz, the LM4250 will consume less power.

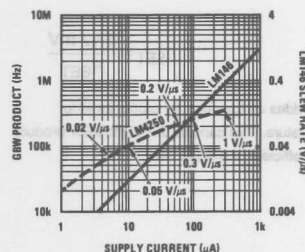
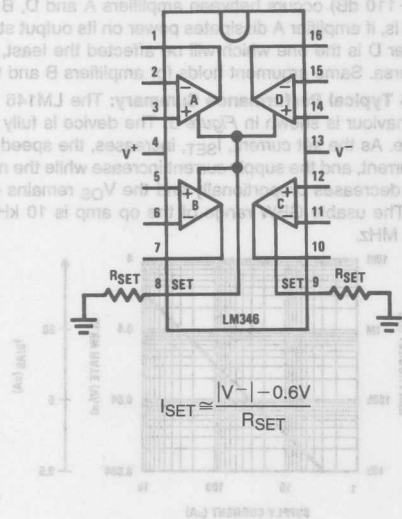


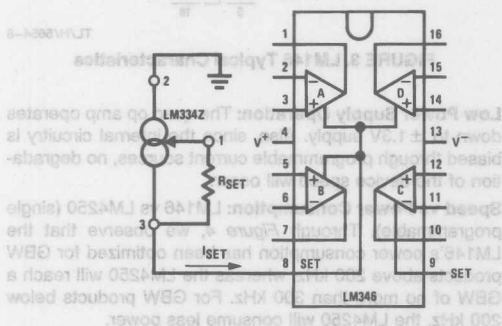
FIGURE 4. LM146 vs LM4250

Typical Applications

Dual Supply or Negative Supply Biasing



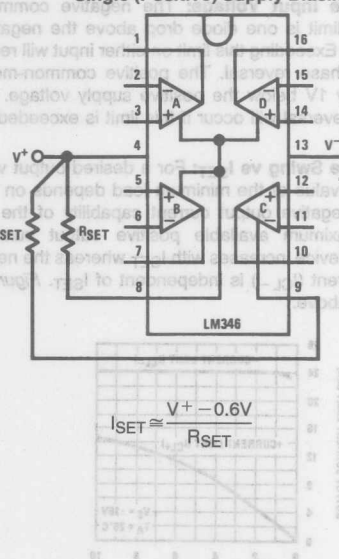
Current Source Biasing with Temperature Compensation



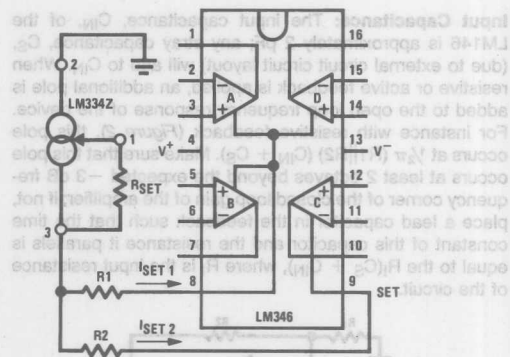
$$I_{SET} = \frac{67.7 \text{ mV}}{R_{SET}}$$

- The LM334 provides an I_{SET} directly proportional to absolute temperature. This cancels the slight GBW product Temperature coefficient of the LM346.

Single (Positive) Supply Biasing



Biasing all 4 Amplifiers with Single Current Source

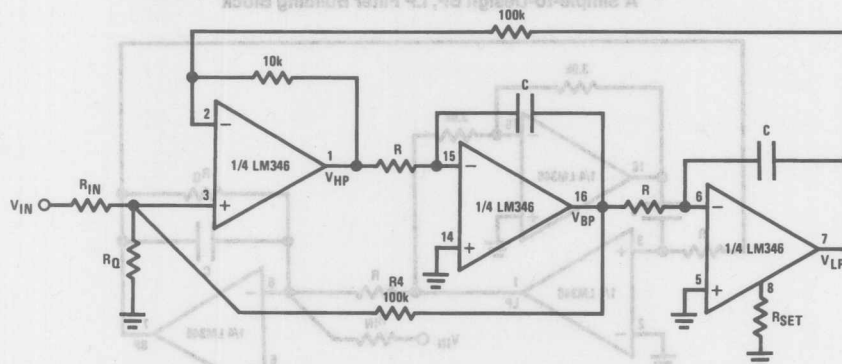


$$\frac{I_{SET1}}{I_{SET2}} = \frac{R_2}{R_1}, I_{SET1} + I_{SET2} = \frac{67.7 \text{ mV}}{R_{SET}}$$

- For $I_{SET1} \approx I_{SET2}$ resistors R1 and R2 are not required if a slight error between the 2 set currents can be tolerated. If not, then use $R1 = R2$ to create a 100 mV drop across these resistors.

Active Filters Applications

Basic (Non-Inverting "State Variable") Active Filter Building Block



TL/H/5654-12

- The LM146 quad programmable op amp is especially suited for active filters because of their adequate GBW product and low power consumption.

Circuit synthesis equations (for circuit analysis equations, consult with the LM148 data sheet).

Need to know desired: f_o = center frequency measured at the BP output

Q_o = quality factor measured at the BP output

H_o = gain at the output of interest (BP or HP or LP or all of them)

- Relation between different gains: $H_o(\text{BP}) = 0.316 \times Q_o \times H_o(\text{LP})$; $H_o(\text{LP}) = 10 \times H_o(\text{HP})$

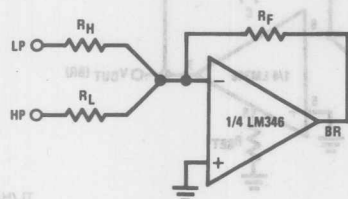
$$R \times C = \frac{5.033 \times 10^{-2}}{f_o} (\text{sec})$$

$$\text{For BP output: } R_Q = \left(\frac{3.478 Q_o - H_o(\text{BP})}{10^5} - \frac{H_o(\text{BP})}{10^5 \times 3.748 \times Q_o} \right)^{-1}; R_{IN} = \frac{(3.478 Q_o - 1)}{\frac{1}{R_Q} + 10^{-5}}$$

$$\text{For HP output: } R_Q = \frac{1.1 \times 10^5}{3.478 Q_o (1.1 - H_o(\text{HP})) - H_o(\text{HP})}; R_{IN} = \frac{1.1}{\frac{1}{R_Q} + 10^{-5}}$$

$$\text{For LP output: } R_Q = \frac{11 \times 10^5}{3.478 Q_o (11 - H_o(\text{LP})) - H_o(\text{LP})}; R_{IN} = \frac{11}{\frac{1}{R_Q} + 10^{-5}}$$

- For BR (notch) output: Use the 4th amplifier of the LM146 to sum the LP and HP outputs of the basic filter.



Note. All resistor values are given in ohms.

$$\sqrt{\frac{R_H}{R_L}} = 0.316 \frac{f_{\text{notch}}}{f_o}$$

TL/H/5654-13

Determine R_F according to the desired gains: $H_o(\text{BR}) \left| \begin{matrix} f < f_{\text{notch}} \\ f > f_{\text{notch}} \end{matrix} \right. = \frac{R_F}{R_L} H_o(\text{LP}), H_o(\text{BR}) \left| \begin{matrix} f < f_{\text{notch}} \\ f > f_{\text{notch}} \end{matrix} \right. = \frac{R_F}{R_H} H_o(\text{HP})$

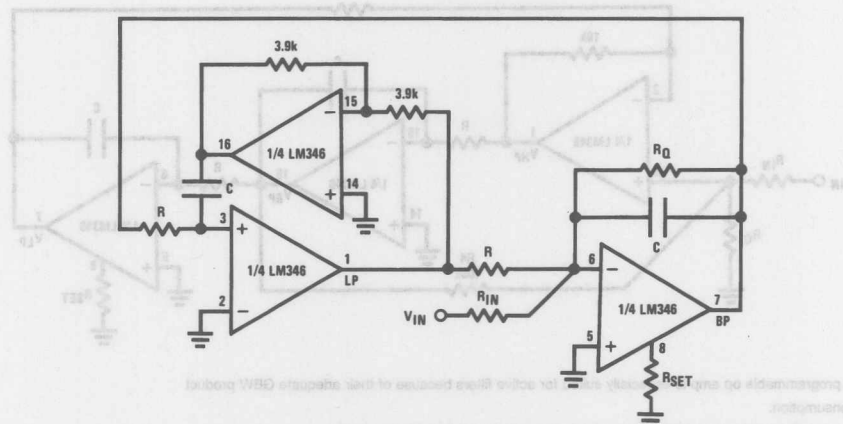
- Where to use amplifier C:** Examine the above gain relations and determine the dynamics of the filter. Do not allow slew rate limiting in any output (V_{HP} , V_{BP} , V_{LP}), that is:

$$V_{IN(\text{peak})} < 63.66 \times 10^3 \times \frac{I_{SET}}{10 \mu A} \times \frac{1}{f_o \times H_o} (\text{Volts})$$

If necessary, use amplifier C, biased at higher I_{SET} , where you get the largest output swing.

Deviation from Theoretical Predictions: Due to the finite GBW products of the op amps the f_o , Q_o will be slightly different from the theoretical predictions.

$$f_{\text{real}} \approx \frac{f_o}{1 + \frac{2 f_o}{GBW}}, Q_{\text{real}} \approx \frac{Q_o}{1 - \frac{3.2 f_o \times Q_o}{GBW}}$$



TL/H/5654-14

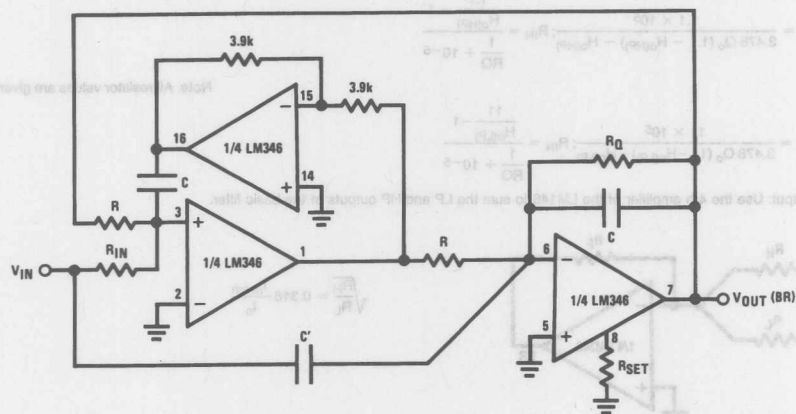
- If resistive biasing is used to set the LM346 performance, the Q_0 of this filter building block is nearly insensitive to the op amp's GBW product temperature drift; it has also better noise performance than the state variable filter.

Circuit Synthesis Equations

$$H_0(BP) = Q_0 H_0(LP); R \times C = \frac{0.159}{f_0}; R_Q = Q_0 \times R; R_{IN} = \frac{R_Q}{H_0(BP)} = \frac{R}{H_0(LP)}$$

- For the eventual use of amplifier C, see comments on the previous page.

A 3-Amplifier Notch Filter (or Elliptic Filter Building Block)



TL/H/5654-15

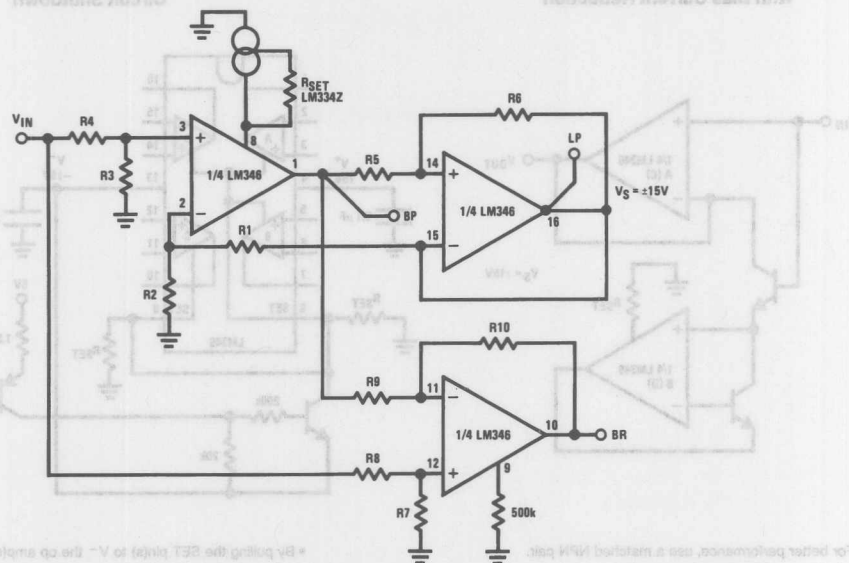
Circuit Synthesis Equations

$$R \times C = \frac{0.159}{f_0}; R_Q = Q_0 \times R; R_{IN} = \frac{0.159 \times f_0}{C' \times f_{notch}^2}$$

$$H_0(BR) \Big|_{f < f_{notch}} = \frac{R}{R_{IN}} H_0(BR) \Big|_{f > f_{notch}} = \frac{C'}{C}$$

- For nothing but a notch output: $R_{IN} = R, C' = C$.

Capacitorless Active Filters (Basic Circuit)



TL/H/5654-16

• This is a BP, LP, BR filter. The filter characteristics are created by using the tunable frequency response of the LM346.

• **Limitations:** $Q_0 < 10$, $f_0 \times Q_0 < 1.5$ MHz, output voltage should not exceed $V_{peak(out)} \leq \frac{63.66 \times 10^3}{f_0} \times \frac{I_{SET}(\mu A)}{10 \mu A}$ (V)

• Design equations: $a = \frac{R_6 + R_5}{R_6}$, $b = \frac{R_2}{R_1 + R_2}$, $c = \frac{R_3}{R_3 + R_4}$, $d = \frac{R_7}{R_8 + R_7}$, $e = \frac{R_{10}}{R_9 + R_{10}}$, $f_0(BP) = f_u \sqrt{\frac{b}{a}}$, $H_0(BP) = a \times c$, $H_0(LP) = \frac{c}{b}$, $Q_0 = \sqrt{a \times b}$

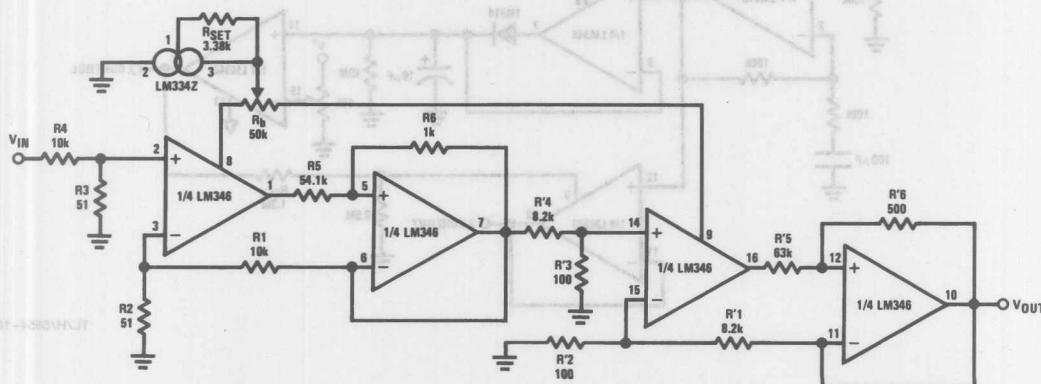
$f_0(BR) = f_0(BP)$, $\left(1 - \frac{c}{b}\right) \approx f_0(BP)$ ($C < 1$) provided that $d = H_0(BP) \times e$, $H_0(BR) = \frac{R_{10}}{R_9}$

• Advantage: f_0 , Q_0 , H_0 can be independently adjusted; that is, the filter is extremely easy to tune.

• Tuning procedure (ex. BP tuning)

1. Pick up a convenient value for b ; ($b < 1$)
2. Adjust Q_0 through R_5
3. Adjust $H_0(BP)$ through R_4
4. Adjust f_0 through R_{SET} . This adjusts the unity gain frequency (f_u) of the op amp.

A 4th Order Butterworth Low Pass Capacitorless Filter



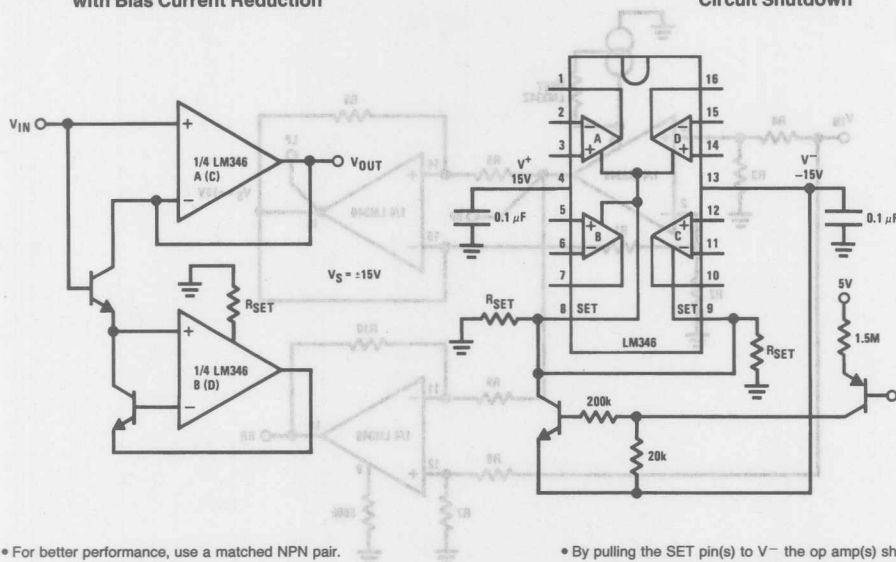
TL/H/5654-17

Ex: $f_c = 20$ kHz, H_0 (gain of the filter) = 1, $Q_{01} = 0.541$, $Q_{02} = 1.306$.

• Since for this filter the GBW product of all 4 amplifiers has been designed to be the same (~ 1 MHz) only one current source can be used to bias the circuit. Fine tuning can be further accomplished through R_b .

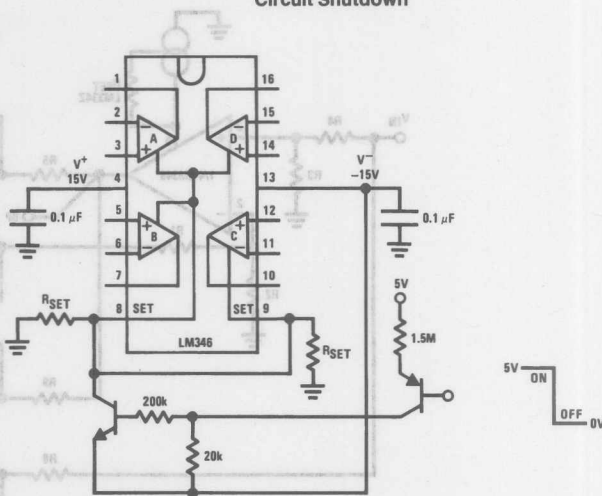
Miscellaneous Applications

A Unity Gain Follower with Bias Current Reduction



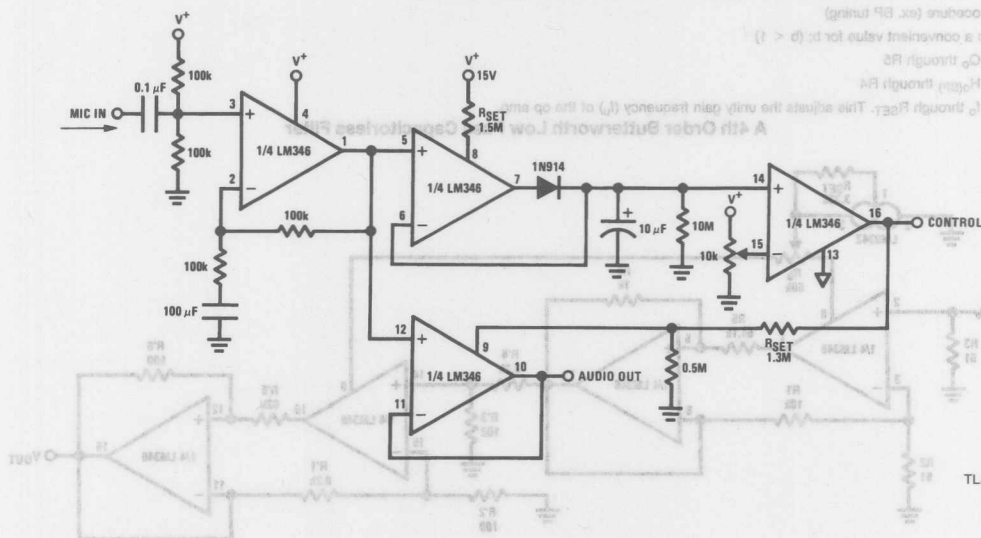
- For better performance, use a matched NPN pair.

Circuit Shutdown



- By pulling the SET pin(s) to V^- the op amp(s) shuts down and its output goes to a high impedance state. According to this property, the LM346 can be used as a very low speed analog switch.

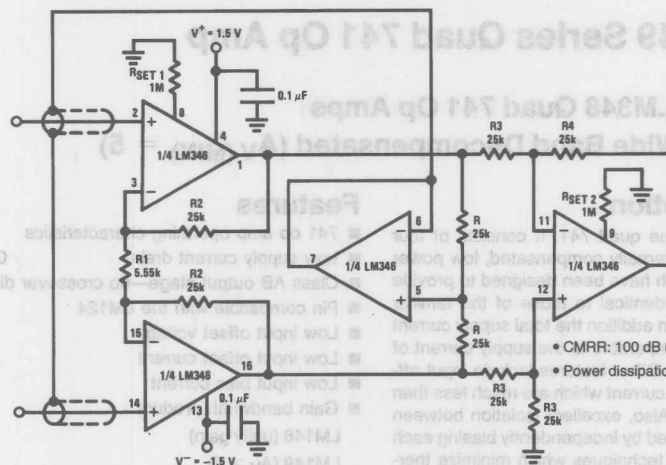
Voice Activated Switch and Amplifier



TL/H/5654-18

Miscellaneous Applications (Continued)

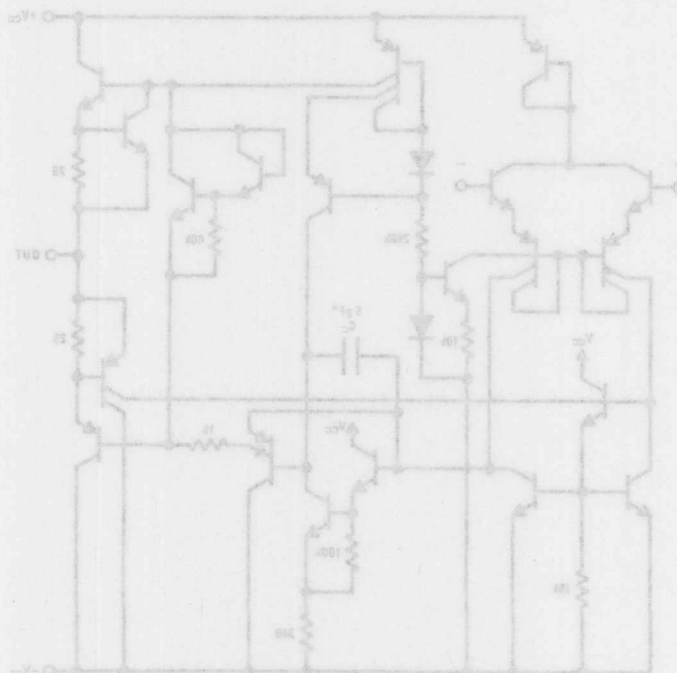
X10 Micropower Instrumentation Amplifier with Buffered Input Guarding



- CMRR: 100 dB (typ)
- Power dissipation: 0.4 mW

TL/H/5654-19

Schematic Diagram



TL/H/5654-19

19 of 19 in the LM348



Miscellaneous Applications (Continued)

X10 Micropower Instrumentation Amplifier with Buffered Input Guarding

LM148/LM149 Series Quad 741 Op Amp

LM148/LM248/LM348 Quad 741 Op Amps

LM149/LM349 Wide Band Decompensated ($A_V(\text{MIN}) = 5$)

General Description

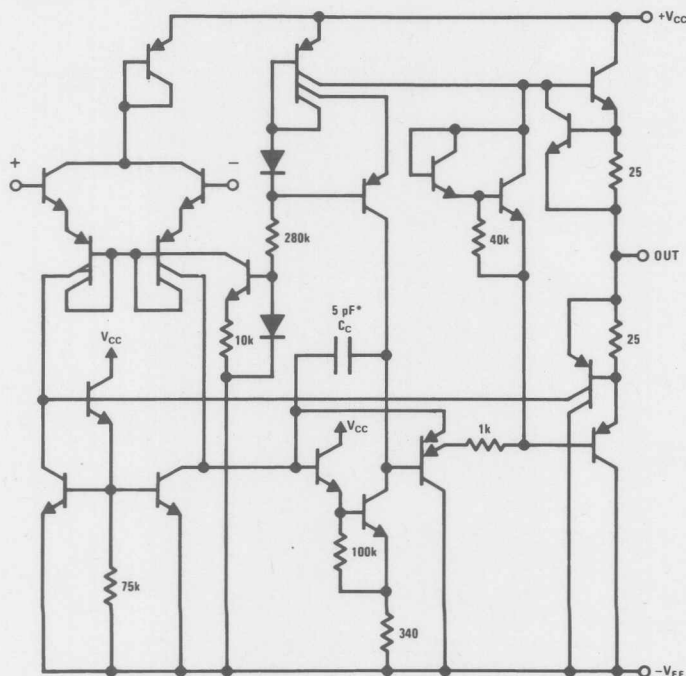
The LM148 series is a true quad 741. It consists of four independent, high gain, internally compensated, low power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias current which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling. The LM149 series has the same features as the LM148 plus a gain bandwidth product of 4 MHz at a gain of 5 or greater.

The LM148 can be used anywhere multiple 741 or 1558 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

Features

- 741 op amp operating characteristics
- Low supply current drain 0.6 mA/Amplifier
- Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage 1 mV
- Low input offset current 4 nA
- Low input bias current 30 nA
- Gain bandwidth product
- LM148 (unity gain) 1.0 MHz
- LM149 ($A_V \geq 5$) 4 MHz
- High degree of isolation between amplifiers 120 dB
- Overload protection for inputs and outputs

Schematic Diagram



*1 pF in the LM149

TL/H/7786-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/
Distributors for availability and specifications.
(Note 4)

| | LM148/LM149 | LM248 | LM348/LM349 |
|---|------------------------|-----------------------|---------------------|
| Supply Voltage | ±22V | ±18V | ±18V |
| Differential Input Voltage | ±44V | ±36V | ±36V |
| Output Short Circuit Duration (Note 1) | Continuous | Continuous | Continuous |
| Power Dissipation (P_D at 25°C) and Thermal Resistance (θ_{JA}), (Note 2) | | | |
| Molded DIP (N) P_D | — | — | 750 mW |
| Cavity DIP (J) P_D | 1100 mW | 800 mW | 700 mW |
| θ_{JA} | 110°C/W | 110°C/W | 110°C/W |
| Maximum Junction Temperature (T_{JMAX}) | 150°C | 110°C | 100°C |
| Operating Temperature Range | −55°C ≤ T_A ≤ +125°C | −25°C ≤ T_A ≤ +85°C | 0°C ≤ T_A ≤ +70°C |
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) Ceramic | 300°C | 300°C | 300°C |
| Lead Temperature (Soldering, 10 sec.) Plastic | — | 260°C | 260°C |
| Soldering Information | | | |
| Dual-In-Line Package | | | |
| Soldering (10 seconds) | 260°C | 260°C | 260°C |
| Small Outline Package | | | |
| Vapor Phase (60 seconds) | 215°C | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C | 220°C |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | |
| ESD tolerance (Note 5) | 500V | 500V | 500V |

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM148/LM149 | | | LM248 | | | LM348/LM349 | | | Units |
|---------------------------------|---|-------------|------|-----|-------|-----|-----|-------------|-----|-----|------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$, $R_S \leq 10\text{ k}\Omega$ | | 1.0 | 5.0 | 1.0 | 6.0 | | 1.0 | 6.0 | | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 4 | 25 | 4 | 50 | | 4 | 50 | | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 30 | 100 | 30 | 200 | | 30 | 200 | | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 0.8 | 2.5 | | 0.8 | 2.5 | | 0.8 | 2.5 | | M Ω |
| Supply Current All Amplifiers | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ | | 2.4 | 3.6 | 2.4 | 4.5 | | 2.4 | 4.5 | | mA |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{ k}\Omega$ | 50 | 160 | | 25 | 160 | | 25 | 160 | | V/mV |
| Amplifier to Amplifier Coupling | $T_A = 25^\circ\text{C}$, $f = 1\text{ Hz to } 20\text{ kHz}$ (Input Referred) See Crosstalk Test Circuit | | −120 | | −120 | | | −120 | | | dB |
| Small Signal Bandwidth | LM148 Series $T_A = 25^\circ\text{C}$ | | 1.0 | | 1.0 | | | 1.0 | | | MHz |
| | LM149 Series | | 4.0 | | 4.0 | | | 4.0 | | | MHz |
| Phase Margin | LM148 Series ($A_V = 1$) $T_A = 25^\circ\text{C}$ | | 60 | | 60 | | | 60 | | | degrees |
| | LM149 Series ($A_V = 5$) | | 60 | | 60 | | | 60 | | | degrees |
| Slew Rate | LM148 Series ($A_V = 1$) $T_A = 25^\circ\text{C}$ | | 0.5 | | 0.5 | | | 0.5 | | | V/ μs |
| | LM149 Series ($A_V = 5$) | | 2.0 | | 2.0 | | | 2.0 | | | V/ μs |
| Output Short Circuit Current | $T_A = 25^\circ\text{C}$ | | 25 | | 25 | | | 25 | | | mA |
| Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | | 6.0 | | 7.5 | | | 7.5 | | mV |
| Input Offset Current | | | | 75 | | 125 | | | 100 | | nA |
| Input Bias Current | | | | 325 | | 500 | | | 400 | | nA |

| Parameter | Conditions | Min | | | Typ | | | Max | | | Units |
|-----------------------------|--|----------|----------|-----|----------|----------|-----|----------|----------|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $V_S = \pm 15V, V_{OUT} = \pm 10V,$ $R_L > 2 k\Omega$ | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15V, R_L = 10 k\Omega$ $R_L = 2 k\Omega$ | ± 12 | ± 13 | | ± 12 | ± 13 | | ± 12 | ± 13 | | V |
| | | ± 10 | ± 12 | | ± 10 | ± 12 | | ± 10 | ± 12 | | V |
| Input Voltage Range | $V_S = \pm 15V$ | ± 12 | | | ± 12 | | | ± 12 | | | V |
| Common-Mode Rejection Ratio | $R_S \leq 10 k\Omega$ | 70 | 90 | | 70 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection | $R_S \leq 10 k\Omega, \pm 5V \leq V_S \leq \pm 15V$ | 77 | 96 | | 77 | 96 | | 77 | 96 | | dB |

Note 1: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

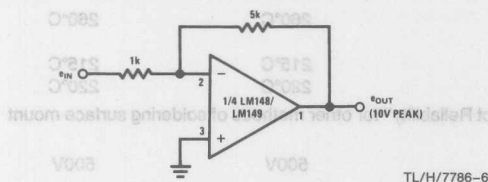
Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum available power dissipation at any temperature is $P_d = (T_{JMAX} - T_A)/\theta_{JA}$ or the $25^\circ C$ P_{dMAX} , whichever is less.

Note 3: These specifications apply for $V_S = \pm 15V$ and over the absolute maximum operating temperature range ($T_L \leq T_A \leq T_H$) unless otherwise noted.

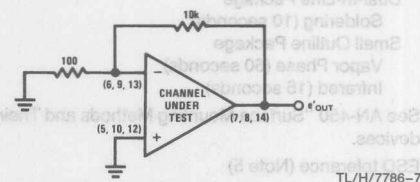
Note 4: Refer to RETS 148X for LM148 military specifications and refer to RETS 149X for LM149 military specifications.

Note 5: Human body model, 1.5 k Ω in series with 100 pF.

Cross Talk Test Circuit



TL/H/7786-6



TL/H/7786-7

$$\text{Crosstalk} = -20 \log \frac{e'_{OUT}}{101 \times e_{OUT}} \text{ (dB)}$$

$$V_S = \pm 15V$$

Application Hints

The LM148 series are quad low power 741 op amps. In the proliferation of quad op amps, these are the first to offer the convenience of familiar, easy to use operating characteristics of the 741 op amp. In those applications where 741 op amps have been employed, the LM148 series op amps can be employed directly with no change in circuit performance.

The LM149 series has the same characteristics as the LM148 except it has been decompensated to provide a wider bandwidth. As a result the part requires a minimum gain of 5.

The package pin-outs are such that the inverting input of each amplifier is adjacent to its output. In addition, the amplifier outputs are located in the corners of the package which simplifies PC board layout and minimizes package related capacitive coupling between amplifiers.

The input characteristics of these amplifiers allow differential input voltages which can exceed the supply voltages. In addition, if either of the input voltages is within the operating common-mode range, the phase of the output remains correct. If the negative limit of the operating common-mode range is exceeded at both inputs, the output voltage will be positive. For input voltages which greatly exceed the maximum supply voltages, either differentially or common-mode, resistors should be placed in series with the inputs to limit the current.

Like the LM741, these amplifiers can easily drive a 100 pF capacitive load throughout the entire dynamic output voltage and current range. However, if very large capacitive loads must be driven by a non-inverting unity gain amplifier,

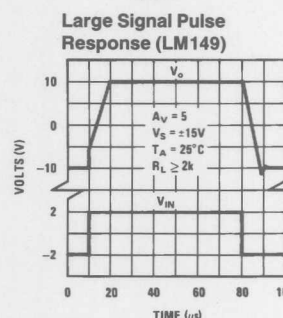
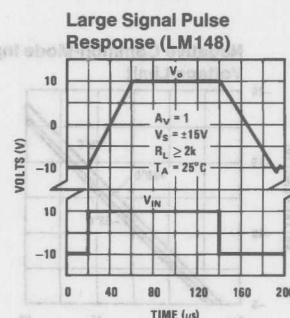
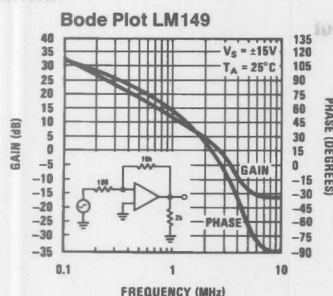
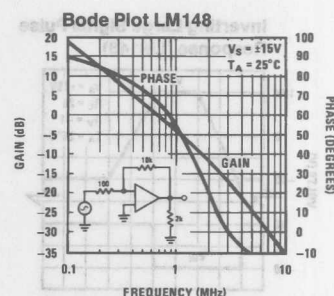
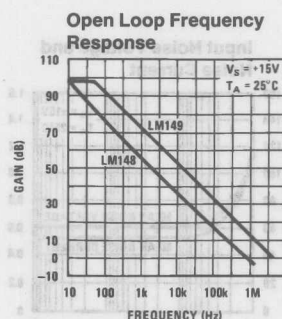
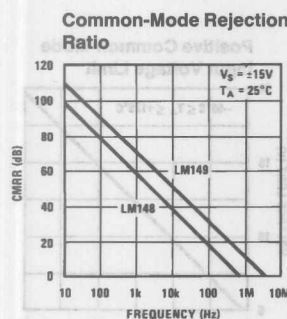
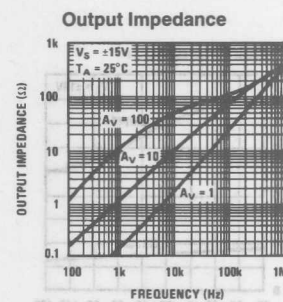
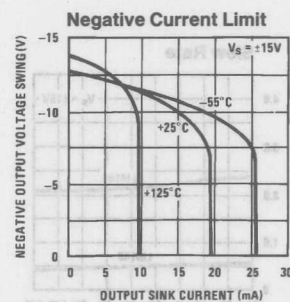
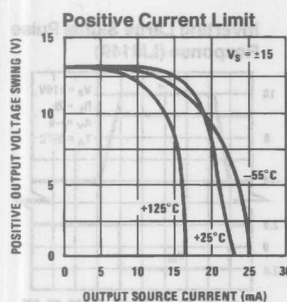
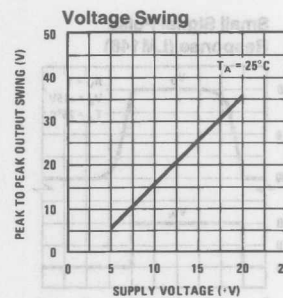
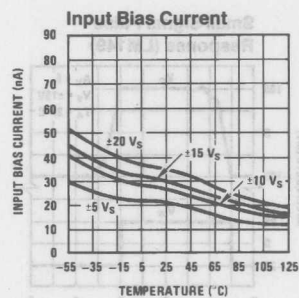
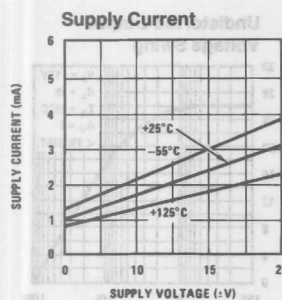
a resistor should be placed between the output (and feedback connection) and the capacitance to reduce the phase shift resulting from the capacitive loading.

The output current of each amplifier in the package is limited. Short circuits from an output to either ground or the power supplies will not destroy the unit. However, if multiple output shorts occur simultaneously, the time duration should be short to prevent the unit from being destroyed as a result of excessive power dissipation in the IC chip.

As with most amplifiers, care should be taken lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole which capacitance from the input to ground creates.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

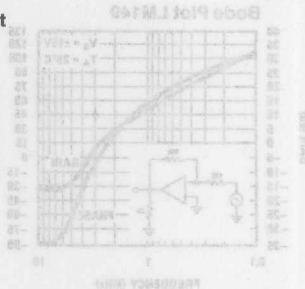
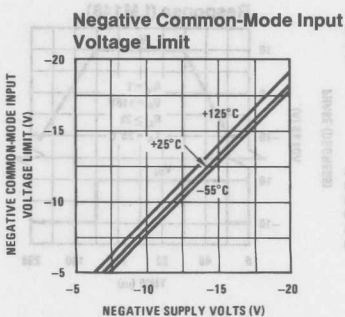
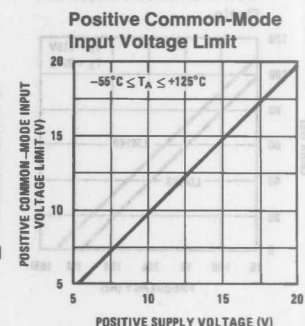
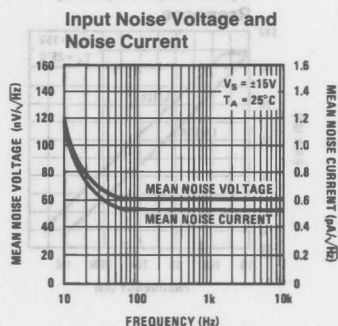
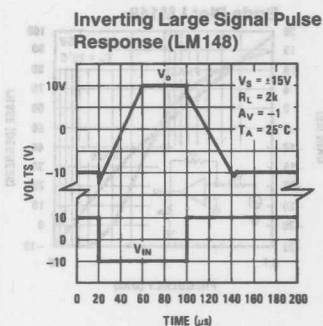
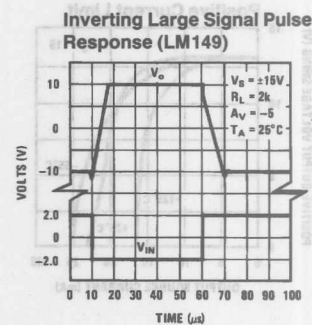
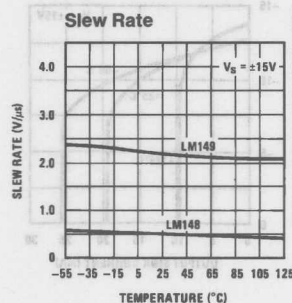
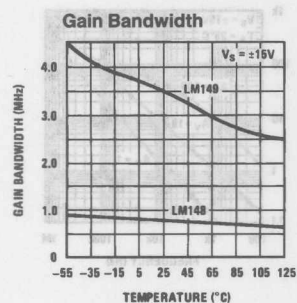
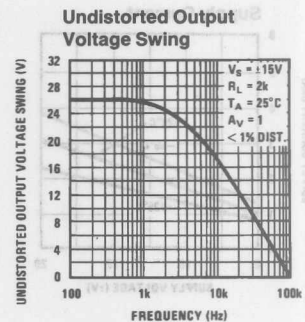
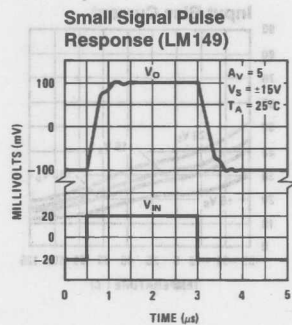
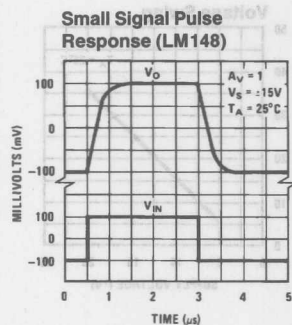
Typical Performance Characteristics



TL/H/7786-3

LM148/LM149/LM248/LM348/LM349

Typical Performance Characteristics (Continued)



TL/H/7786-4

TL/H/7786-5

Low Offset Peak Detector with Bias Current Compensation

TL/H/7786-8

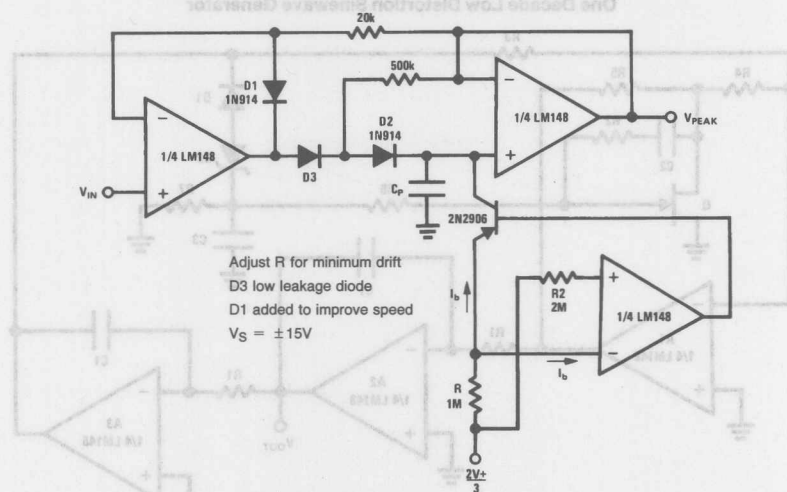
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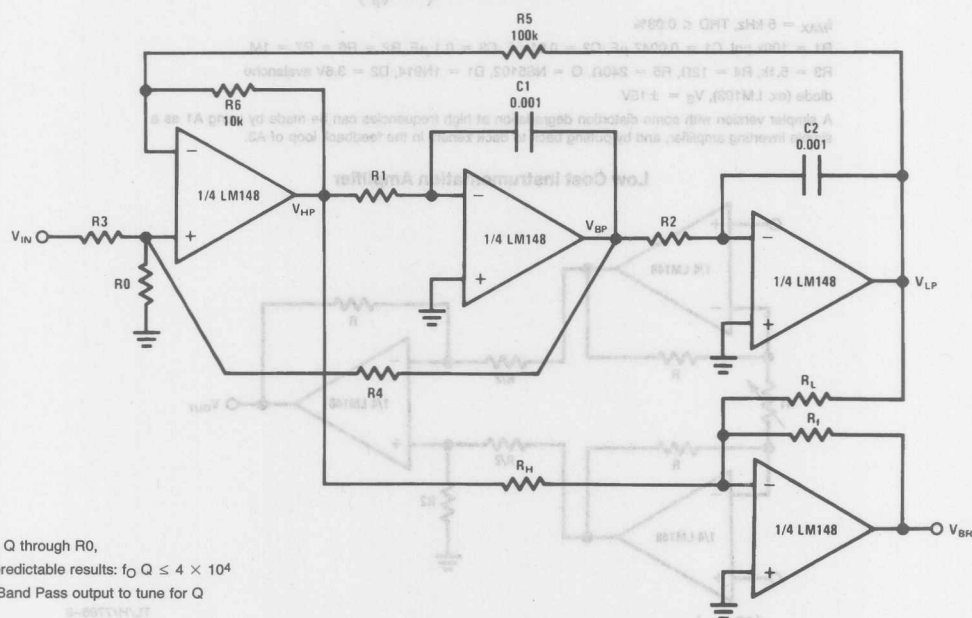
Typical Applications—LM148 (Continued)

Low Drift Peak Detector with Bias Current Compensation



TL/H/7786-10

Universal State-Variable Filter



TL/H/7786-11

Tune Q through R0.

For predictable results: $f_0 Q \leq 4 \times 10^4$

Use Band Pass output to tune for Q

$$\frac{V(s)}{V_{IN}(s)} = \frac{N(s)}{D(s)}, \quad D(s) = s^2 + \frac{S\omega_0}{Q} + \omega_0^2$$

$$N_{HP(s)} = S^2 H_{OHP}, \quad N_{BP(s)} = \frac{-s\omega_0 H_{OBP}}{\Omega} \quad N_{LP} = \omega_0^2 H_{OLP}.$$

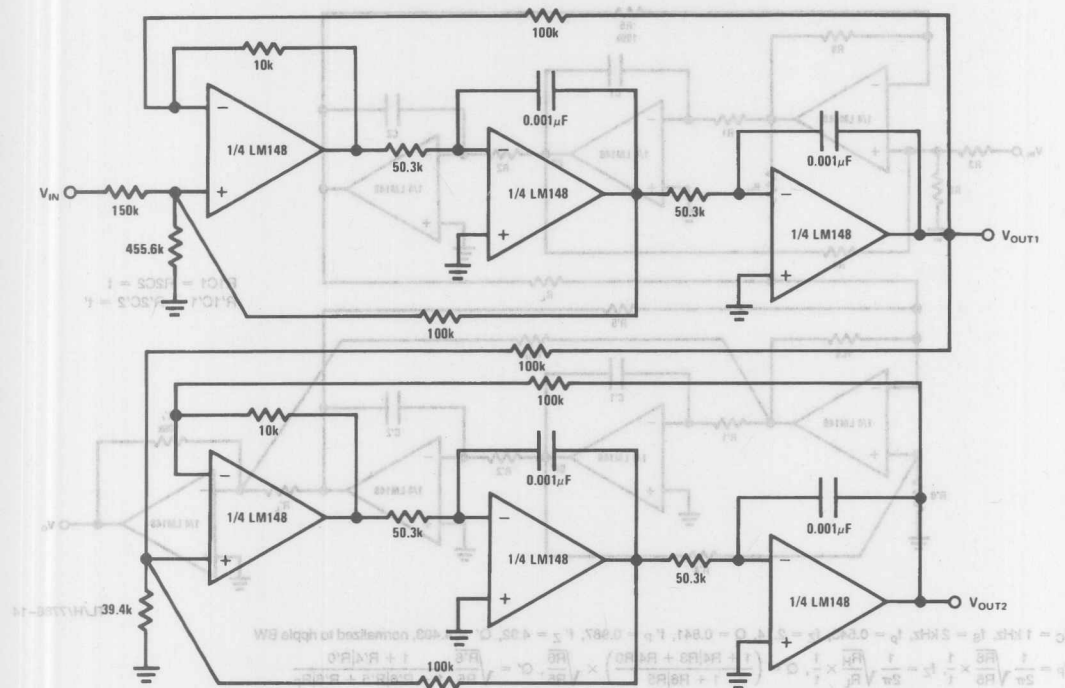
$$f_0 = \frac{1}{2\pi} \sqrt{\frac{R_6}{R_5}} \sqrt{\frac{1}{t_{112}}}, t_1 = R_1 C_1, Q = \left(\frac{1 + R_4/R_3 + R_4/R_0}{1 + R_6/R_5} \right) \left(\frac{R_6 t_1}{R_5 t_2} \right)^{1/2}$$

$$f_{\text{NOTCH}} = \frac{1}{2\pi} \left(\frac{R_H}{R_L t_1 t_2} \right)^{1/2}, \quad H_{\text{OHP}} = \frac{1 + R_6/R_5}{1 + R_3/R_0 + R_3/R_4}, \quad H_{\text{OBP}} = \frac{1 + R_4/R_3 + R_4/R_0}{1 + R_3/R_0 + R_3/R_4}$$

$$H_{OLP} = \frac{1 + R5/R6}{1 + R3/R0 + R3/R4}$$

Typical Applications—LM148 (Continued)

A 1 kHz 4 Pole Butterworth



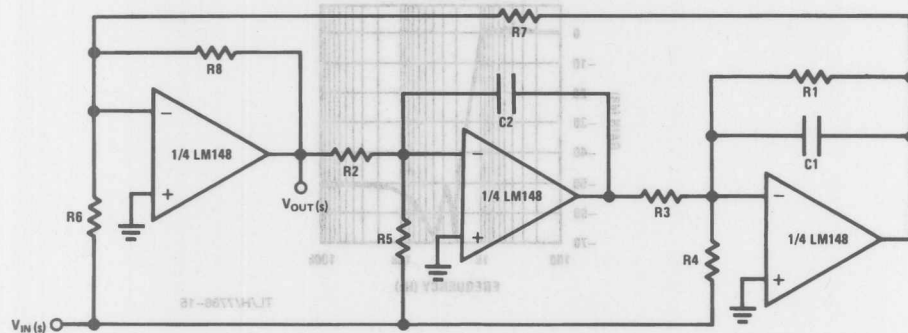
TL/H/7786-12

Use general equations, and tune each section separately

 $Q_{1stSECTION} = 0.541$, $Q_{2ndSECTION} = 1.306$

The response should have 0 dB peaking

A 3 Amplifier Bi-Quad Notch Filter



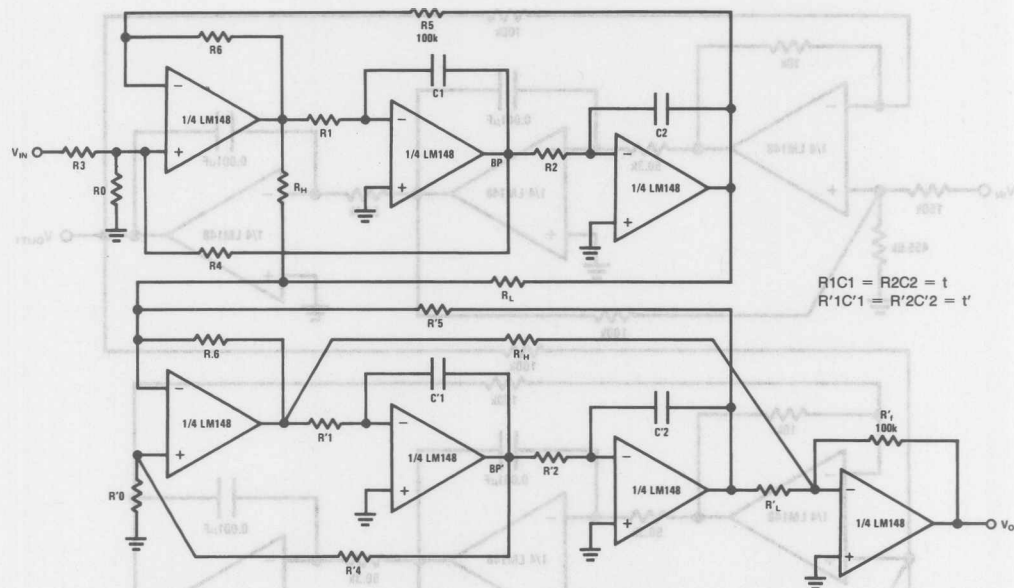
TL/H/7786-13

$$Q = \frac{\sqrt{R_8}}{\sqrt{R_7}} \times \frac{R_1 C_1}{\sqrt{R_3 C_2 R_2 C_1}}, \quad f_0 = \frac{1}{2\pi} \sqrt{\frac{R_8}{R_7}} \times \frac{1}{\sqrt{R_2 R_3 C_1 C_2}}, \quad f_{NOTCH} = \frac{1}{2\pi} \sqrt{\frac{R_6}{R_3 R_5 R_7 C_1 C_2}}$$

$$\text{Necessary condition for notch: } \frac{1}{R_6} = \frac{R_1}{R_4 R_7}$$

Ex: $f_{NOTCH} = 3 \text{ kHz}$, $Q = 5$, $R_1 = 270k$, $R_2 = R_3 = 20k$, $R_4 = 27k$, $R_5 = 20k$, $R_6 = R_8 = 10k$, $R_7 = 100k$, $C_1 = C_2 = 0.001 \mu F$

Better noise performance than the state-space approach.



$$R1C1 = R2C2 = t$$

$$R'1C'1 = R'2C'2 = t'$$

$f_C = 1 \text{ kHz}$, $f_S = 2 \text{ kHz}$, $f_p = 0.543$, $f_z = 2.14$, $Q = 0.841$, $f'_p = 0.987$, $f'_z = 4.92$, $Q' = 4.403$, normalized to ripple BW

$$f_p = \frac{1}{2\pi} \sqrt{\frac{R_6}{R_5}} \times \frac{1}{t}, f_z = \frac{1}{2\pi} \sqrt{\frac{R_H}{R_L}} \times \frac{1}{t'}, Q = \left(\frac{1 + R_4/R_3 + R_4/R_0}{1 + R_6/R_5} \right) \times \sqrt{\frac{R_6}{R_5}}, Q' = \sqrt{\frac{R'_6}{R'_5}} \times \frac{1 + R'_4/R'_0}{1 + R'_6/R'_5 + R'_6/R'_p}$$

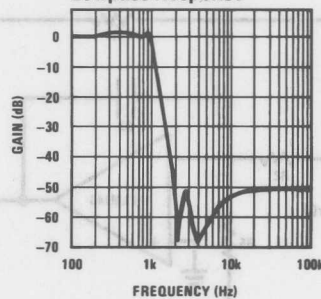
$$R_p = \frac{R_H R_L}{R_H + R_L}$$

Use the BP outputs to tune Q , Q' , tune the 2 sections separately

$R1 = R2 = 92.6k$, $R3 = R4 = R5 = 100k$, $R6 = 10k$, $R0 = 107.8k$, $R_L = 100k$, $R_H = 155.1k$.

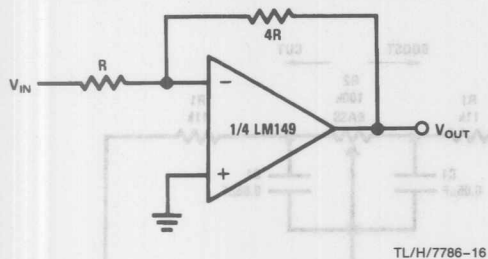
$R'1 = R'2 = 50.9k$, $R'4 = R'5 = 100k$, $R'6 = 10k$, $R'0 = 5.78k$, $R'_L = 100k$, $R'_H = 248.12k$, $R'_f = 100k$. All capacitors are $0.001 \mu F$.

Lowpass Response



TL/H/7786-15

Minimum Gain to Insure LM149 Stability



$$A_{CL}(s) = \frac{V_{OUT}}{V_{IN}} = \frac{-4}{\left(1 + \frac{5}{A_{OL}(s)}\right)} \approx -4$$

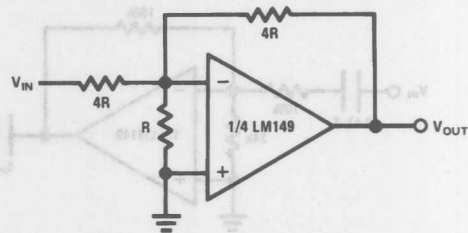
$$V_O \Big|_{V_{IN} = 0} \approx \pm 5 V_{OS}$$

Power BW = 40 kHz

Small Signal BW = G BW/5

TL/H/7786-16

The LM149 as a Unity Gain Inverter



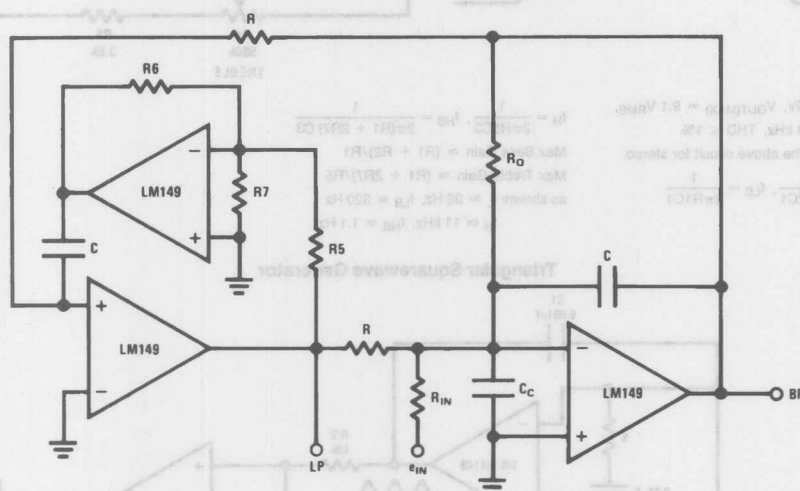
$$A_{CL}(s) = \frac{V_{OUT}}{V_{IN}} = \left(\frac{-1}{1 + \frac{6}{A_{OL}(s)}} \right) \approx -1$$

$$V_O \Big|_{V_{IN} = 0} \approx \pm 5 V_{OS}$$

Small Signal BW = G BW/5

TL/H/7786-17

Non-Inverting-Integrator Bandpass Filter



For stability purposes: $R_7 = R_6/4$, $10R_6 = R_5$, $C_C = 10C$

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{R_5}{R_6}} \times \frac{1}{RC}, Q = \frac{R_Q}{R} \sqrt{\frac{R_5}{R_6}}, H_{oBP} = \frac{R_Q}{R_{IN}}$$

$f_{O(MAX)}, Q_{MAX} = 20 \text{ kHz}, 10$

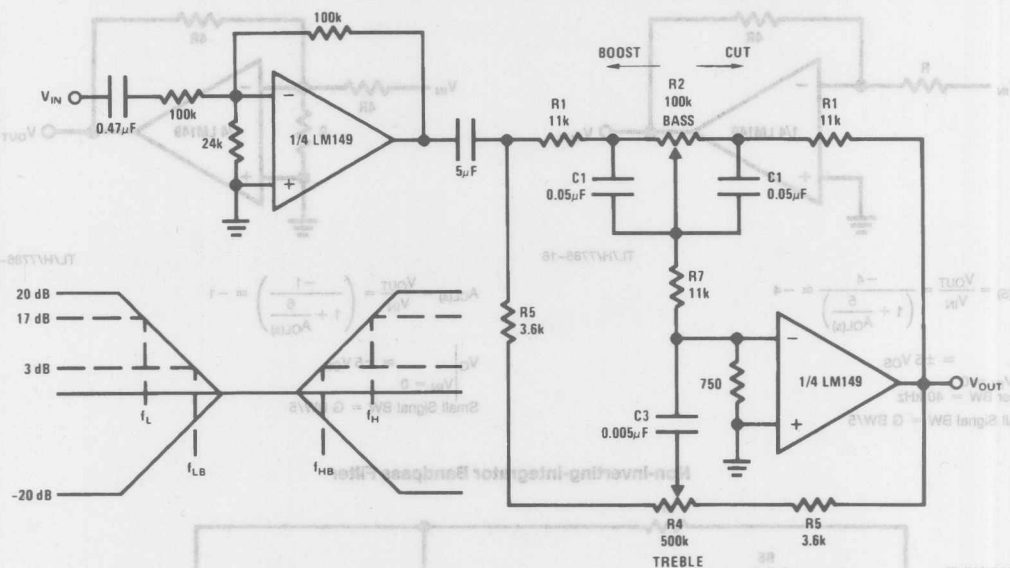
Better Q sensitivity with respect to open loop gain variations than the state variable filter.

R_7, C_C added for compensation

TL/H/7786-18

Typical Applications—LM149 (Continued)

Active Tone Control with Full Output Swing (No Slew Limiting at 20 kHz)



$$V_S = \pm 15V, V_{OUT(MAX)} = 9.1 V_{RMS}$$

$$f_{MAX} = 20 \text{ kHz}, THD \leq 1\%$$

Duplicate the above circuit for stereo

$$f_L = \frac{1}{2\pi R_2 C_1}, f_{LB} = \frac{1}{2\pi R_1 C_1}$$

$$f_H = \frac{1}{2\pi R_5 C_3}, f_{HB} = \frac{1}{2\pi (R_1 + 2R_7) C_3}$$

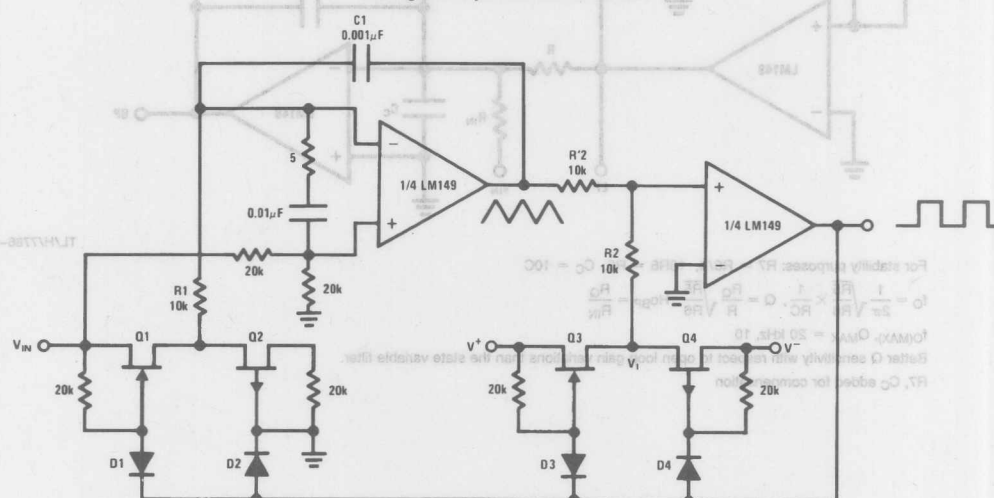
$$\text{Max Bass Gain} \approx (R_1 + R_2)/R_1$$

$$\text{Max Treble Gain} \approx (R_1 + 2R_7)/R_5$$

$$\text{as shown: } f_L \approx 32 \text{ Hz}, f_{LB} \approx 320 \text{ Hz}$$

$$f_H \approx 11 \text{ kHz}, f_{HB} \approx 1.1 \text{ Hz}$$

Triangular Squarewave Generator



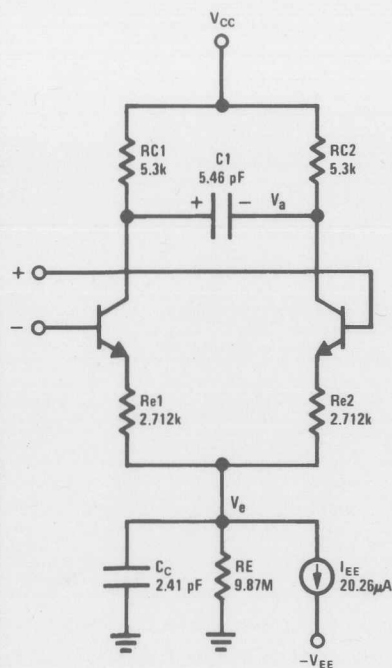
$$f = \frac{K \times V_{IN}}{8V^+ C_1 R_1}, K = R_2/R'_2, \frac{2V_1}{K} \leq 25V, V^+ = V^-, V_S = \pm 15V$$

Use LM125 for $\pm 15V$ supply

The circuit can be used as a low frequency V/F for process control.

Q1, Q3: KE4993, Q2, Q4: P1087E, D1-D4 = 1N914

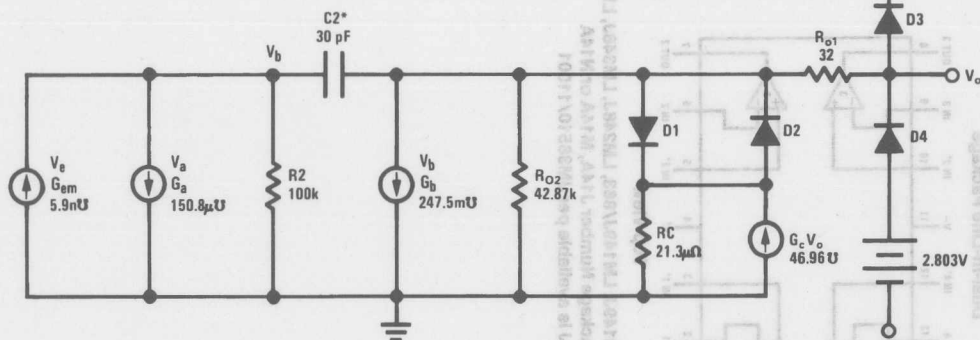
LM148, LM149, LM741 Macromodel for Computer Simulation



TL/H/7786-21

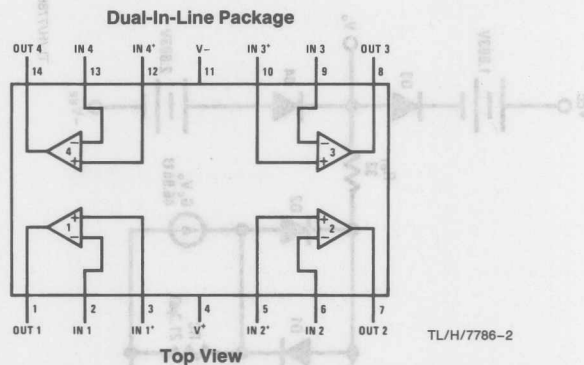
$\beta_{o1} = 112$ $I_S = 8 \times 10^{-16}$
 $\beta_{o2} = 144$ *C2 = 6 pF for LM149

For more details, see IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 6, December 1974



TL/H/7786-22

Connection Diagram



Order Number LM148J, LM148J/883, LM149J, LM149J/883, LM248J, LM348J, LM348M, LM348N or LM349N
See NS Package Number J14A, M14A or N14A
LM148J is available per JM38510/11001

LM158/LM258/LM358/LM2904

Low Power Dual Operational Amplifiers

General Description

The LM158 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM158 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm 15V$ power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.
- The unity gain cross frequency is temperature compensated.
- The input bias current is also temperature compensated.

Advantages

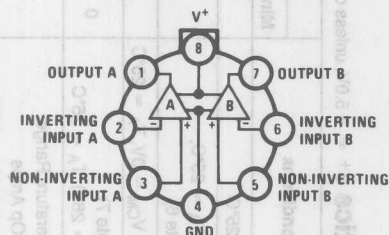
- Two internally compensated op amps in a single package
- Eliminates need for dual supplies
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation
- Pin-out same as LM1558/LM1458 dual operational amplifier

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
 - Single supply 3V to 32V
 - or dual supplies $\pm 1.5V$ to $\pm 16V$
- Very low supply current drain (500 μA)—essentially independent of supply voltage
- Low input offset voltage 2 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to $V^+ - 1.5V$

Connection Diagrams (Top Views)

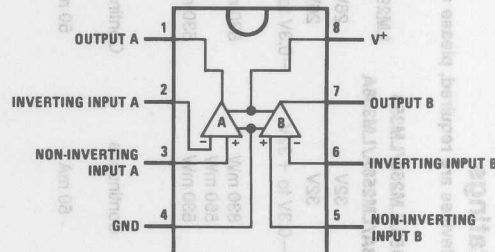
Metal Can Package



TL/H/7787-1

Order Number LM158AH, LM158AH/883*,
LM158H, LM158H/883*, LM258H or LM358H
See NS Package Number H08C

DIP/SO Package



TL/H/7787-2

Order Number LM158J, LM158J/883*,
LM158AJ or LM158AJ/883*
See NS Package Number J08A
Order Number LM358M, LM358AM or LM2904M
See NS Package Number M08A
Order Number LM358AN, LM358N or LM2904N
See NS Package Number N08E

*LM158 is available per SMD #5962-8771001
LM158A is available per SMD #5962-8771002

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.
(Note 9)

| | LM158/LM258/LM358 LM158A/LM258A/LM358A | LM2904 |
|---|---|---------------|
| Supply Voltage, V^+ | 32V | 26V |
| Differential Input Voltage | 32V | 26V |
| Input Voltage | -0.3V to +32V | -0.3V to +26V |
| Power Dissipation (Note 1) | | |
| Molded DIP | 830 mW | 830 mW |
| Metal Can | 550 mW | |
| Small Outline Package (M) | 530 mW | 530 mW |
| Output Short-Circuit to GND (One Amplifier) (Note 2) | | |
| $V^+ \leq 15V$ and $T_A = 25^\circ C$ | Continuous | Continuous |
| Input Current ($V_{IN} < -0.3V$) (Note 3) | 50 mA | 50 mA |

| | LM158/LM258/LM358 LM158A/LM258A/LM358A | LM2904 |
|--|---|-----------------|
| Operating Temperature Range | | |
| LM358 | 0°C to +70°C | -40°C to +85°C |
| LM258 | -25°C to +85°C | |
| LM158 | -55°C to +125°C | |
| Storage Temperature Range | -65°C to +150°C | -65°C to +150°C |
| Lead Temperature, DIP (Soldering, 10 seconds) | 260°C | 260°C |
| Lead Temperature, Metal Can (Soldering, 10 seconds) | 300°C | 300°C |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 10) 250V 250V

Electrical Characteristics $V^+ = +5.0V$, unless otherwise stated

| Parameter | Conditions | LM158A | | | LM358A | | | LM158/LM258 | | | LM358 | | | LM2904 | | |
|------------------------------------|---|----------|-----|-------------|----------|-----|-------------|-------------|-----|-------------|----------|-----|-------------|----------|-----|-------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| Input Offset Voltage | (Note 5), $T_A = 25^\circ C$ | 1 | | 2 | 2 | | 3 | 2 | | 5 | 2 | | 7 | 2 | | 7 |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25^\circ C$, $V_{CM} = 0V$, (Note 6) | 20 | | 50 | 45 | | 100 | 45 | | 150 | 45 | | 250 | 45 | | 250 |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$ | 2 | | 10 | 5 | | 30 | 3 | | 30 | 5 | | 50 | 5 | | 50 |
| Input Common-Mode Voltage Range | $V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$), $T_A = 25^\circ C$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ |
| Supply Current | Over Full Temperature Range $R_L = \infty$ on All Op Amps $V^+ = 30V$ (LM2904 $V^+ = 26V$) $V^+ = 5V$ | 1 0.5 | | 2 1.2 | 1 0.5 | | 2 1.2 | 1 0.5 | | 2 1.2 | 1 0.5 | | 2 1.2 | 1 0.5 | | 2 1.2 |

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

| Parameter | | Conditions | LM158A | | | LM358A | | | LM158/LM258 | | | LM358 | | | LM2904 | | | Units |
|---------------------------------|--------|--|--------|------|-----|--------|------|-----|-------------|------|-----|-------|------|-----|--------|------|-----|------------------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | | $V^+ = 15V$, $T_A = 25^\circ C$, $R_L \geq 2 k\Omega$, (For $V_O = 1V$ to $11V$) | 50 | 100 | | 25 | 100 | | 50 | 100 | | 25 | 100 | | 25 | 100 | | V/mV |
| Common-Mode Rejection Ratio | | $T_A = 25^\circ C$, $V_{CM} = 0V$ to $V^+ - 1.5V$ | 70 | 85 | | 65 | 85 | | 70 | 85 | | 65 | 85 | | 50 | 70 | | dB |
| Power Supply Rejection Ratio | | $V^+ = 5V$ to $30V$ (LM2904, $V^+ = 5V$ to $26V$), $T_A = 25^\circ C$ | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 50 | 100 | | dB |
| Amplifier-to-Amplifier Coupling | | $f = 1 kHz$ to $20 kHz$, $T_A = 25^\circ C$ (Input Referred), (Note 8) | | -120 | | | -120 | | | -120 | | | -120 | | | -120 | | dB |
| Output Current | Source | $V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25^\circ C$ | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | mA |
| | Sink | $V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $T_A = 25^\circ C$, $V_O = 2V$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | | $V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $T_A = 25^\circ C$, $V_O = 200 mV$, $V^+ = 15V$ | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | μA |
| Short Circuit to Ground | | $T_A = 25^\circ C$, (Note 2), $V^+ = 15V$ | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | mA |
| Input Offset Voltage | | (Note 5) | | | 4 | | | 5 | | | 7 | | | 9 | | | 10 | mV |
| Input Offset Voltage Drift | | $R_S = 0\Omega$ | | 7 | 15 | | 7 | 20 | | 7 | | | 7 | | | 7 | | $\mu V/^\circ C$ |
| Input Offset Current | | $I_{IN(+)} - I_{IN(-)}$ | | | 30 | | | 75 | | | 100 | | | 150 | | 45 | 200 | nA |
| Input Offset Current Drift | | $R_S = 0\Omega$ | | 10 | 200 | | 10 | 300 | | 10 | | | 10 | | | 10 | | $pA/^\circ C$ |
| Input Bias Current | | $I_{IN(+)} \text{ or } I_{IN(-)}$ | | 40 | 100 | | 40 | 200 | | 40 | 300 | | 40 | 500 | | 40 | 500 | nA |

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

| Parameter | | Conditions | LM158A | | | LM358A | | | LM158/LM258 | | | LM358 | | | LM2904 | | | Units |
|---------------------------------|----------|--|--------|-----|-----------|--------|-----|-----------|-------------|-----|-----------|-------|-----|-----------|--------|-----|-----------|-------|
| | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Common-Mode Voltage Range | | $V^+ = 30V$, (Note 7) (LM2904, $V^+ = 26V$) | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | V |
| Large Signal Voltage Gain | | $V^+ = +15V$ ($V_O = 1V$ to $11V$) $R_L \geq 2k\Omega$ | 25 | | | 15 | | | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | V_{OH} | $V^+ = +30V$ (LM2904, $V^+ = 26V$) $R_L = 2k\Omega$ | 26 | | | 26 | | | 26 | | | 26 | | | 22 | | | V |
| | | $R_L = 10k\Omega$ | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 23 | 24 | | V |
| | V_{OL} | $V^+ = 5V$, $R_L = 10k\Omega$ | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 100 | | mV |
| Output Current | Source | $V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | Sink | $V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$ | 10 | 15 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | mA |

Note 1: For operating at high temperatures, the LM358/LM358A, LM2904 must be derated based on a $+125^\circ\text{C}$ maximum junction temperature and a thermal resistance of 120°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM258/LM258A and LM158/LM158A can be derated based on a $+150^\circ\text{C}$ maximum junction temperature. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of V^+ . At values of supply voltage in excess of $+15V$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$ (at 25°C).

Note 4: These specifications are limited to $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the LM158/LM158A. With the LM258/LM258A, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, the LM358/LM358A temperature specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, and the LM2904 specifications are limited to $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$.

Note 5: $V_O \approx 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) at 25°C . For LM2904, V^+ from 5V to 26V.

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to $+32V$ without damage ($+26V$ for LM2904), independent of the magnitude of V^+ .

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

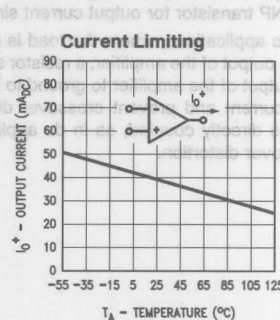
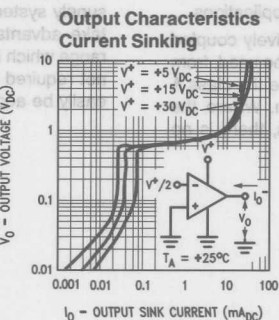
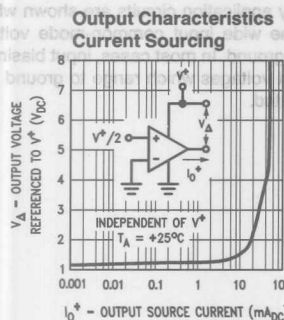
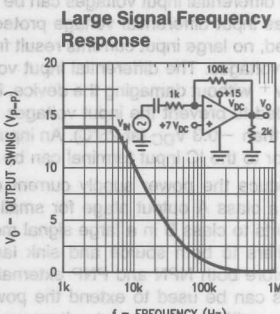
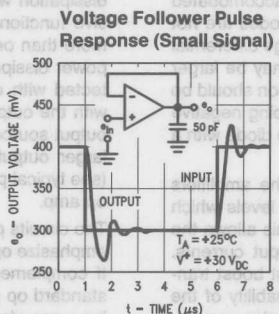
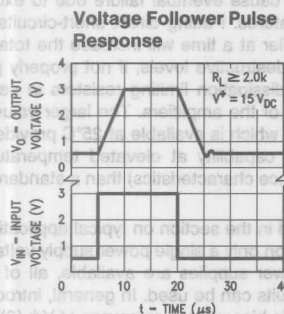
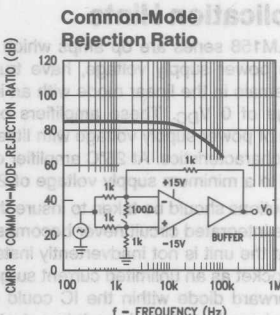
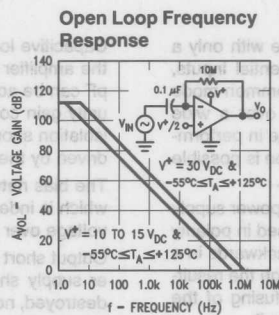
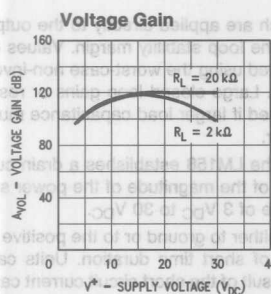
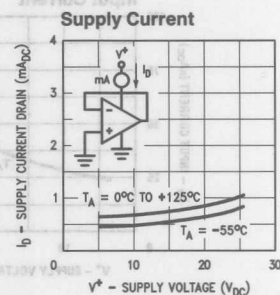
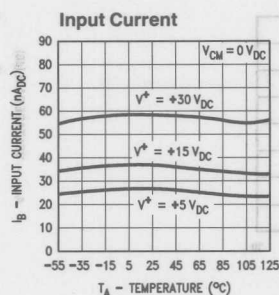
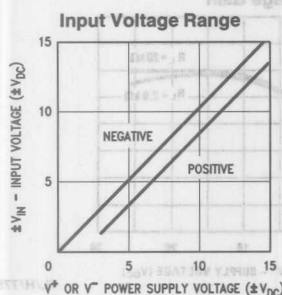
Note 9: Refer to RETS158AX for LM158A military specifications and to RETS158X for LM158 military specifications.

Note 10: Human body model, $1.5k\Omega$ in series with 100 pF.

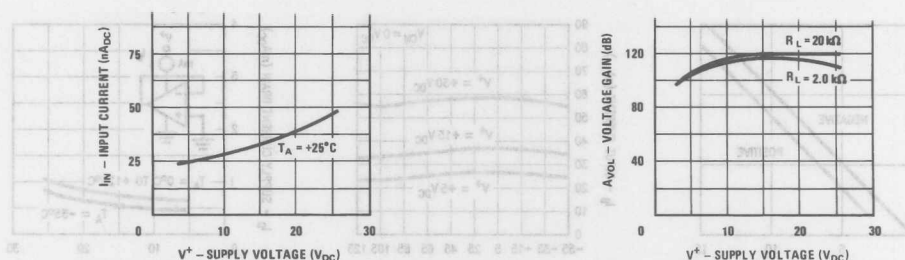
| | | | | | | | | | | | | | | |
|------------------------------|---|--------|-----|-----|--------|-----|-----|-------------|-----|-----|-------|-----|-----|-------|
| Supply range 20mA Voltage | $V^+ > 5V^+ (E_{OL} A^+ = 1A)$ $A^+ = 12A^+ V^+ = 52A^+ C^+$ | 20 | 100 | S2 | 100 | 20 | 100 | S2 | 100 | S2 | 100 | AVm | | |
| Parameter | Conditions | min | typ | max | min | typ | max | min | typ | max | min | typ | max | Units |
| | | LM158A | | | LM358A | | | LM158/LM258 | | | LM358 | | | |

Electrical Characteristics (Continued) $V^+ = +5.0V$, Note 4, unless otherwise stated

Typical Performance Characteristics



TL/H/7787-4



TL/H/7787-5

Application Hints

The LM158 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 V_{DC} . These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 V_{DC} .

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3 V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply current drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion. Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

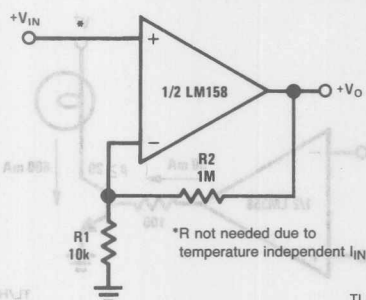
The bias network of the LM158 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 3 V_{DC} to 30 V_{DC} .

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive function temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

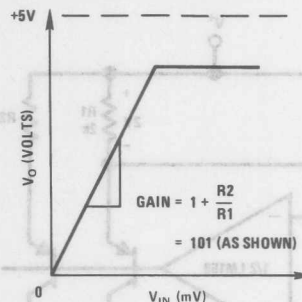
The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

Non-Inverting DC Gain (0V Input = 0V Output)

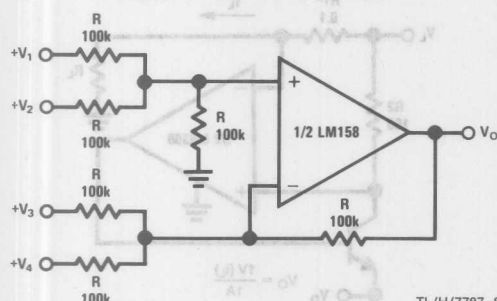


TL/H/7787-6



TL/H/7787-7

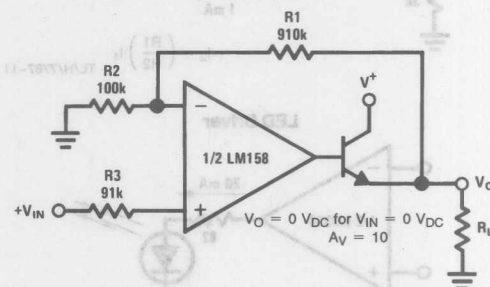
DC Summing Amplifier ($V_{IN'S} \geq 0 V_{DC}$ and $V_O \geq 0 V_{DC}$)



TL/H/7787-8

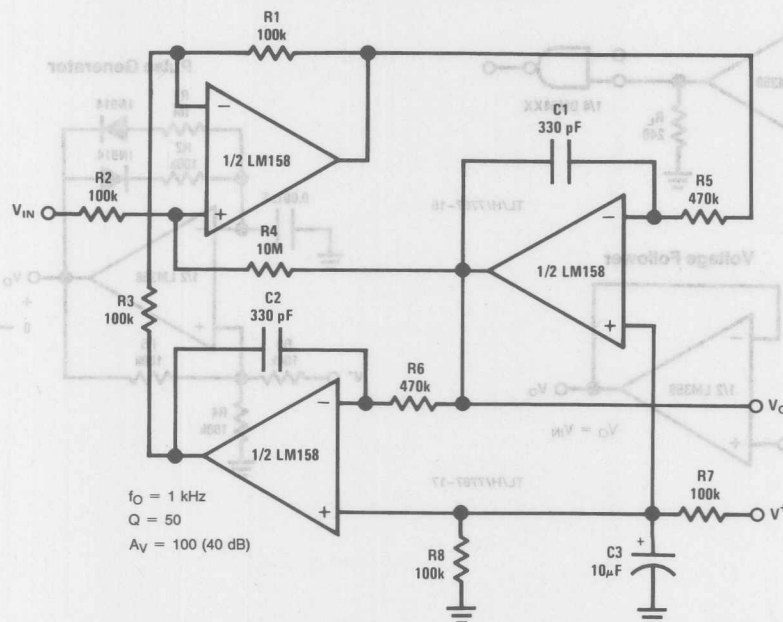
Where: $V_O = V_1 + V_2 + V_3 + V_4$
 $(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0 V_{DC}$

Power Amplifier



TL/H/7787-9

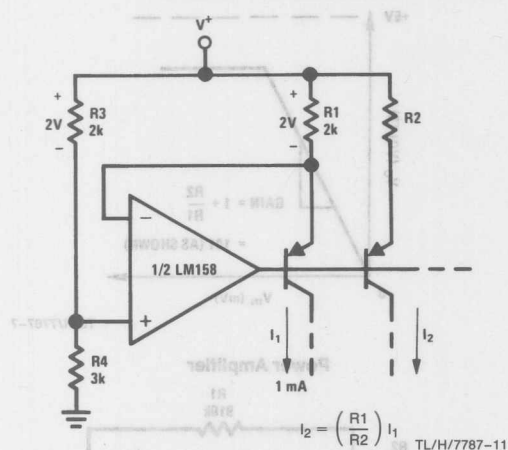
"BI-QUAD" RC Active Bandpass Filter



TL/H/7787-10

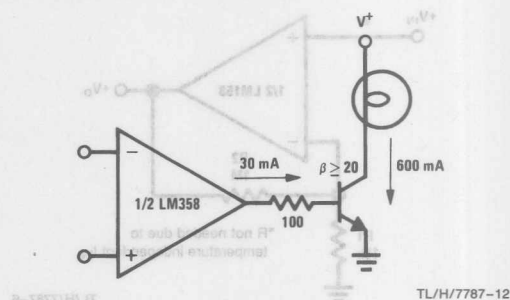
Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DD}}$) (Continued)

Fixed Current Sources



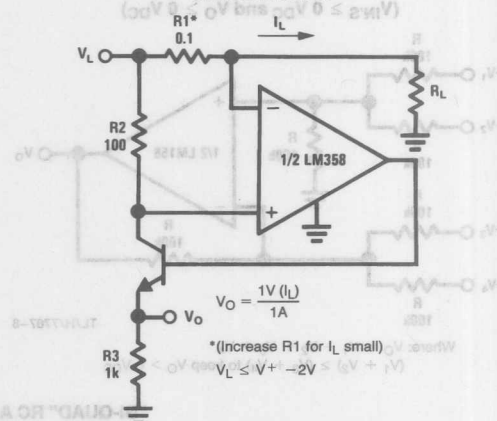
TL/H/7787-11

Lamp Driver



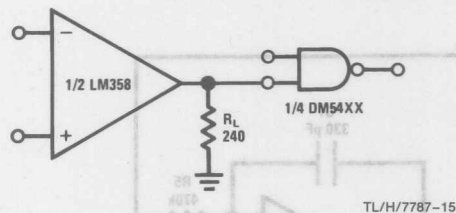
TL/H/7787-12

Current Monitor



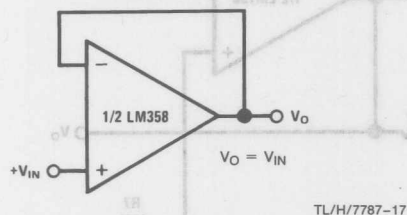
TL/H/7787-14

Driving TTL



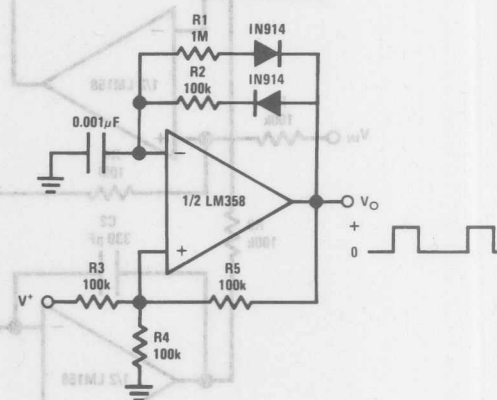
TL/H/7787-15

Voltage Follower



TL/H/7787-17

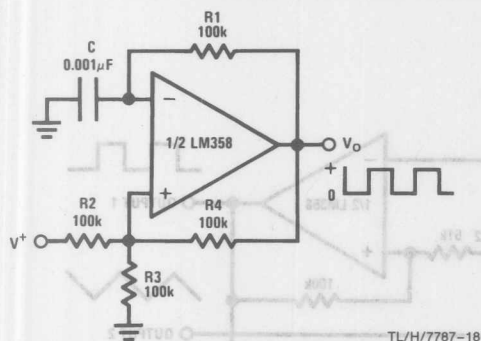
Pulse Generator



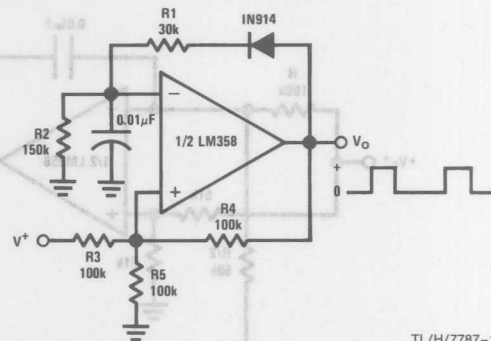
TL/H/7787-16

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

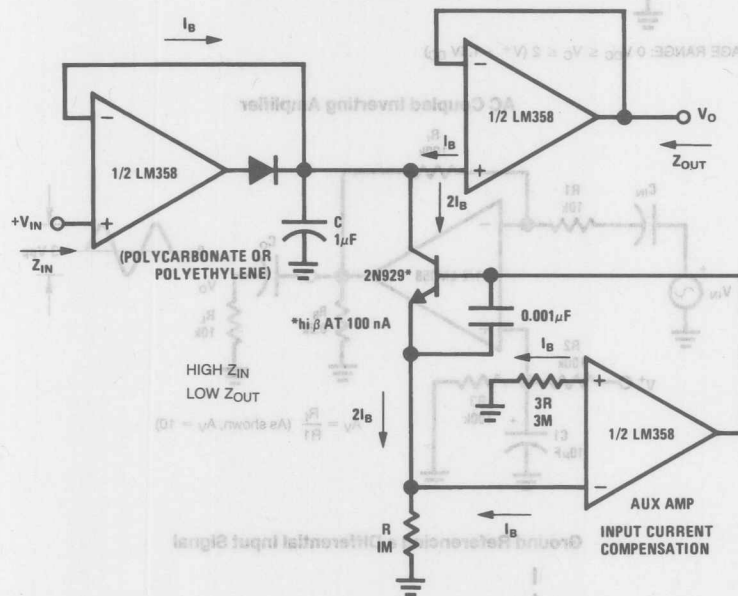
Squarewave Oscillator



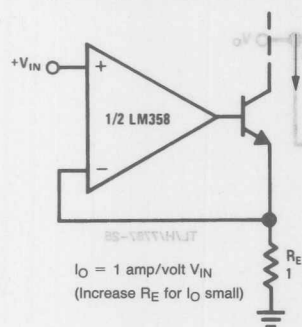
Pulse Generator



Low Drift Peak Detector

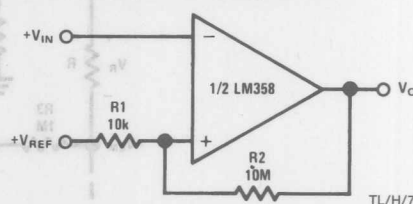


High Compliance Current Sink



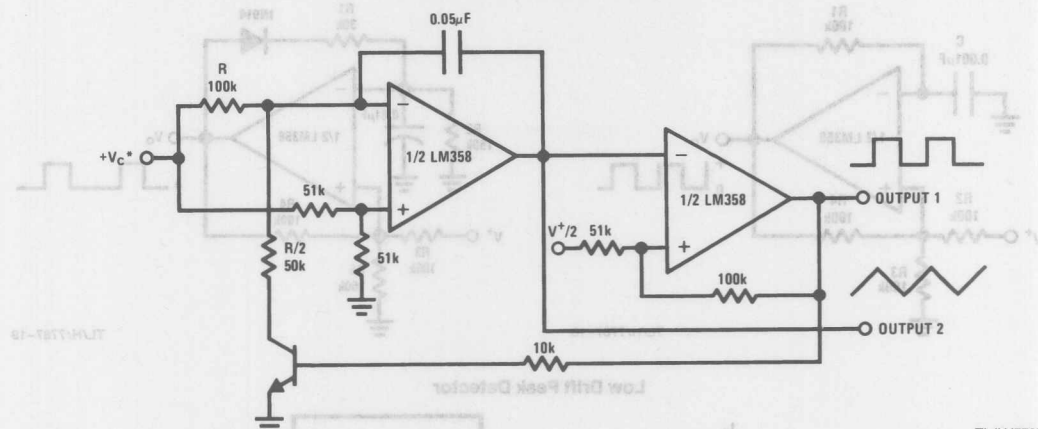
$I_O = 1\text{ amp/volt } V_{IN}$
(Increase R_E for I_O small)

Comparator with Hysteresis



Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

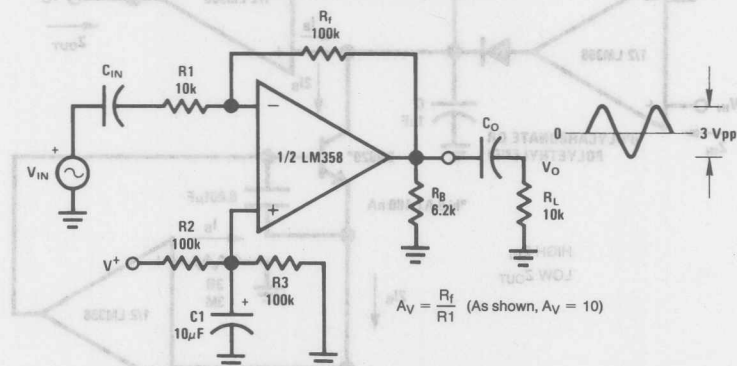
Voltage Controlled Oscillator (VCO)



TL/H/7787-23

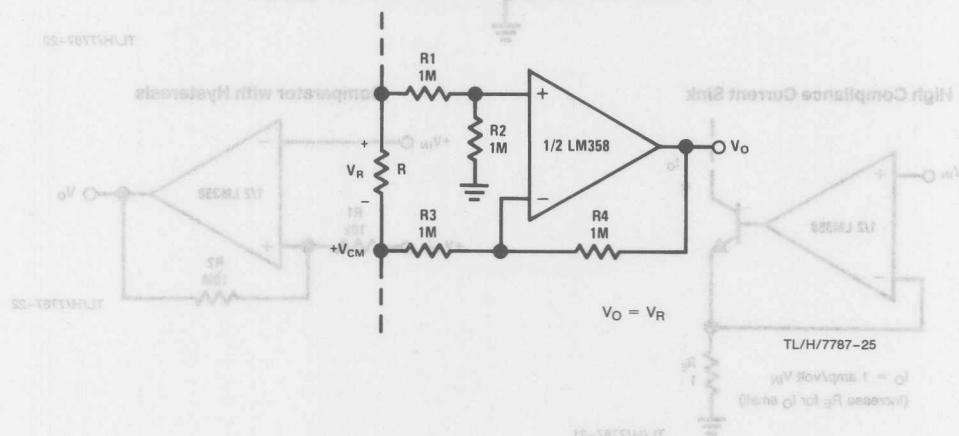
*WIDE CONTROL VOLTAGE RANGE: $0 V_{DC} \leq V_C \leq 2 (V^+ - 1.5V_{DC})$

AC Coupled Inverting Amplifier



TL/H/7787-24

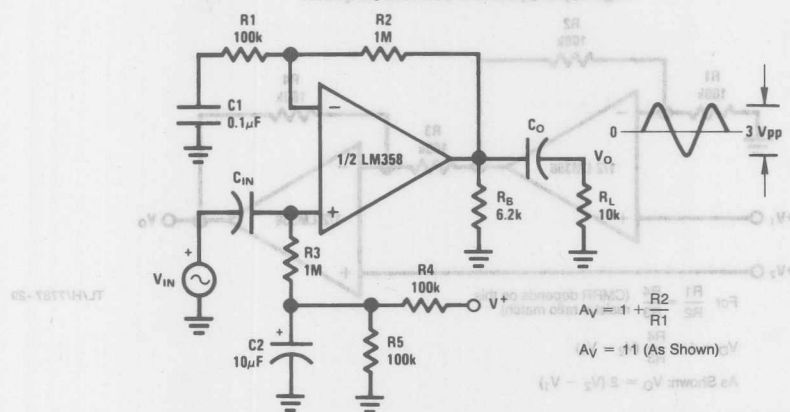
Ground Referencing a Differential Input Signal



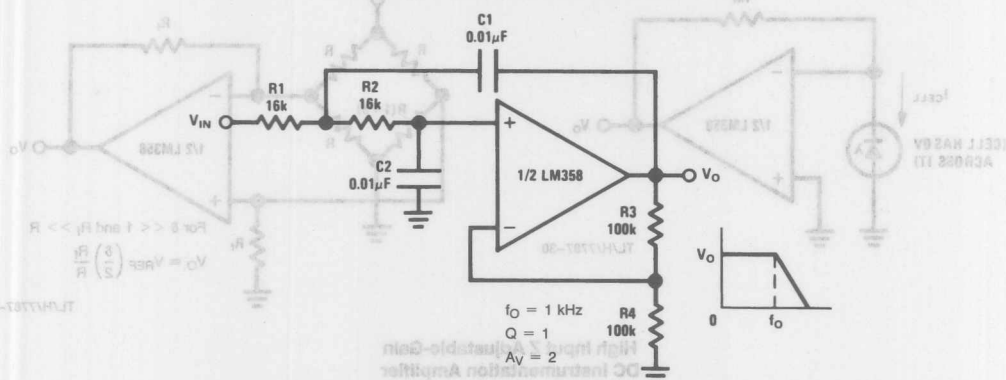
TL/H/7787-25

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

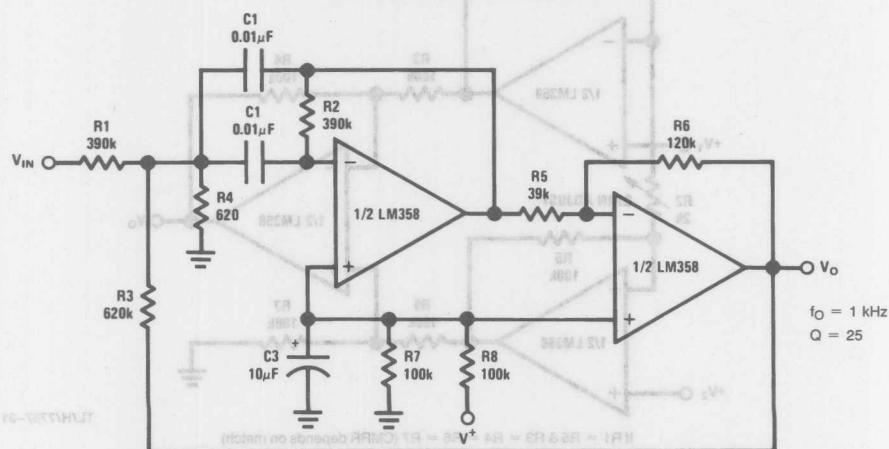
AC Coupled Non-Inverting Amplifier



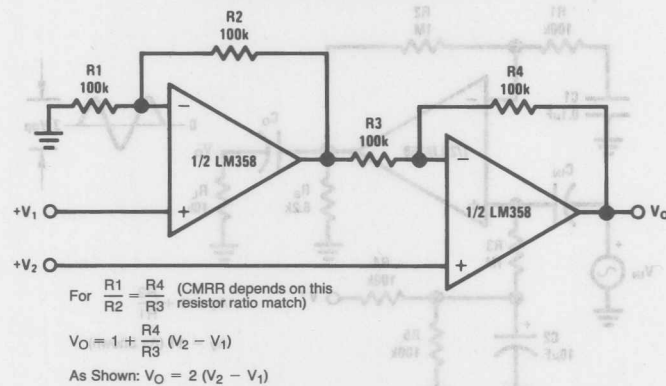
DC Coupled Low-Pass RC Active Filter



Bandpass Active Filter

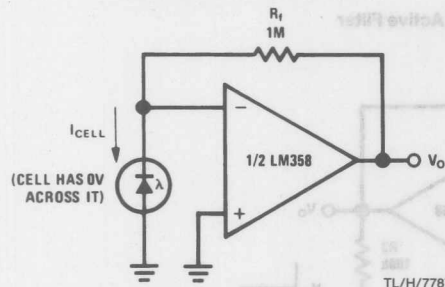


High Input Z, DC Differential Amplifier

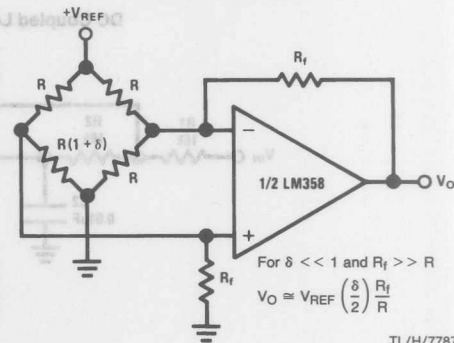


TL/H/7787-29

Photo Voltaic-Cell Amplifier

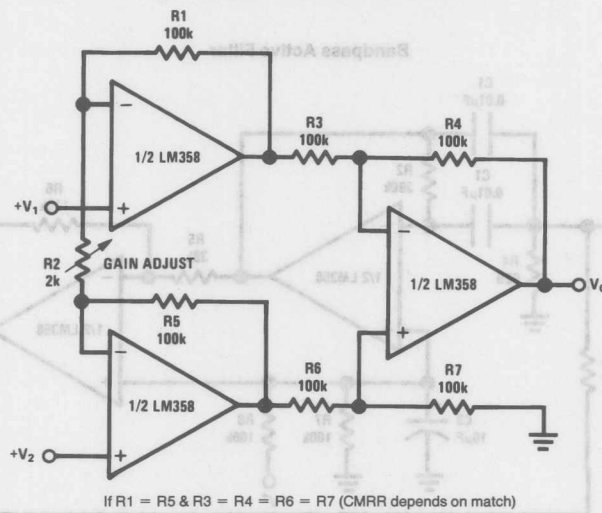


Bridge Current Amplifier



TL/H/7787-33

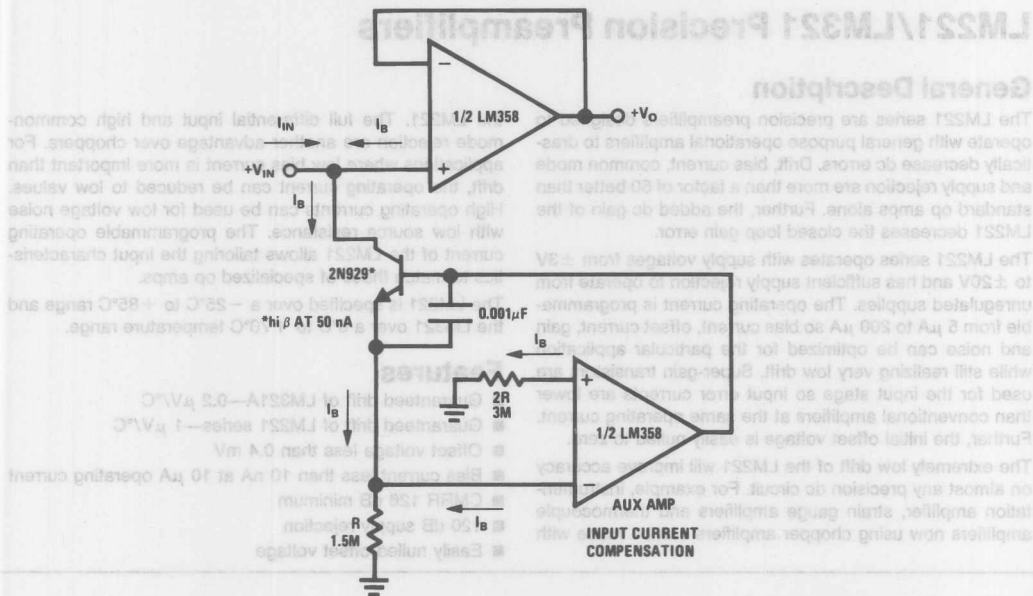
High Input Z Adjustable-Gain DC Instrumentation Amplifier



TL/H/7787-31

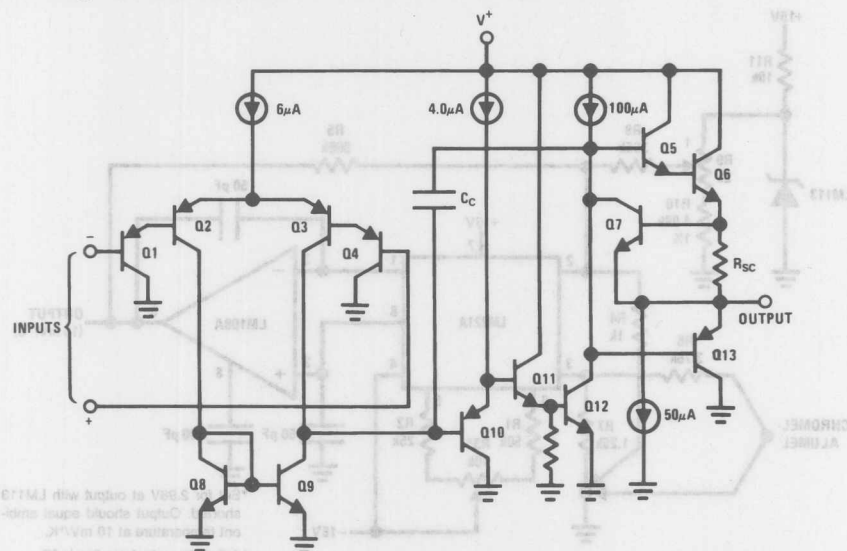
Typical Single-Supply Applications (V⁺ = 5.0 V_{DC}) (Continued)

Using Symmetrical Amplifiers to Reduce Input Current (General Concept)

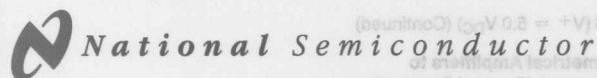


TL/H/7787-32

Schematic Diagram (Each Amplifier)



TL/H/7787-3



LM221/LM321 Precision Preamplifiers

General Description

The LM221 series are precision preamplifiers designed to operate with general purpose operational amplifiers to drastically decrease dc errors. Drift, bias current, common mode and supply rejection are more than a factor of 50 better than standard op amps alone. Further, the added dc gain of the LM221 decreases the closed loop gain error.

The LM221 series operates with supply voltages from $\pm 3V$ to $\pm 20V$ and has sufficient supply rejection to operate from unregulated supplies. The operating current is programmable from $5 \mu A$ to $200 \mu A$ so bias current, offset current, gain and noise can be optimized for the particular application while still realizing very low drift. Super-gain transistors are used for the input stage so input error currents are lower than conventional amplifiers at the same operating current. Further, the initial offset voltage is easily nulled to zero.

The extremely low drift of the LM221 will improve accuracy on almost any precision dc circuit. For example, instrumentation amplifier, strain gauge amplifiers and thermocouple amplifiers now using chopper amplifiers can be made with

the LM221. The full differential input and high common-mode rejection are another advantage over choppers. For applications where low bias current is more important than drift, the operating current can be reduced to low values. High operating currents can be used for low voltage noise with low source resistance. The programmable operating current of the LM221 allows tailoring the input characteristics to match those of specialized op amps.

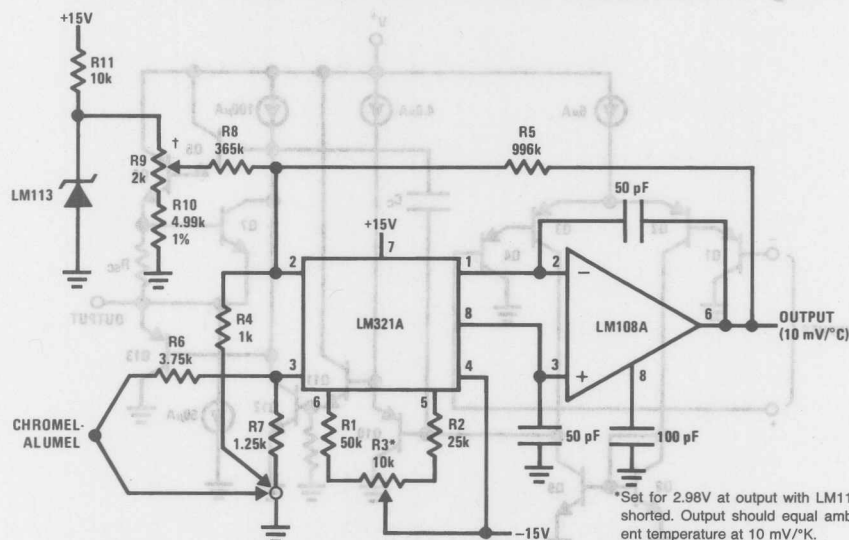
The LM221 is specified over a $-25^{\circ}C$ to $+85^{\circ}C$ range and the LM321 over a $0^{\circ}C$ to $+70^{\circ}C$ temperature range.

Features

- Guaranteed drift of LM321A— $0.2 \mu V/^{\circ}C$
- Guaranteed drift of LM221 series— $1 \mu V/^{\circ}C$
- Offset voltage less than $0.4 mV$
- Bias current less than $10 nA$ at $10 \mu A$ operating current
- CMRR $126 dB$ minimum
- $120 dB$ supply rejection
- Easily nulled offset voltage

Typical Applications

Thermocouple Amplifier with Cold Junction Compensation



*Set for 2.98V at output with LM113 shorted. Output should equal ambient temperature at $10 mV/^{\circ}K$.

†Adjust for output reading in $^{\circ}C$.

TL/H/7769-1

Absolute Maximum Ratings

Supply Voltage $\pm 20V$
 Power Dissipation (Note 1) 500 mW
 Differential Input Voltage (Notes 2 and 3) $\pm 15V$
 Input Voltage (Note 3) $\pm 15V$

Operating Temperature Range LM321A $0^{\circ}C$ to $+70^{\circ}C$
 Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Lead Temperature (Soldering, 10 sec.) $300^{\circ}C$
 ESD rating to be determined.

Electrical Characteristics (Note 4) LM321A

| Parameter | Conditions | LM321A | | | Units |
|-------------------------------------|---|-----------|------|------|-------------------|
| | | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^{\circ}C, 6.4k \leq R_{SET} \leq 70k$ | | 0.2 | 0.4 | mV |
| Input Offset Current | $T_A = 25^{\circ}C,$ $R_{SET} = 70k$ $R_{SET} = 6.4k$ | | 0.3 | 0.5 | nA |
| | | | | 5 | nA |
| Input Bias Current | $T_A = 25^{\circ}C,$ $R_{SET} = 70k$ $R_{SET} = 6.4k$ | | 5 | 15 | nA |
| | | | 50 | 150 | nA |
| Input Resistance | $T_A = 25^{\circ}C,$ $R_{SET} = 70k$ $R_{SET} = 6.4k$ | 2 | 8 | | M Ω |
| | | 0.2 | | | M Ω |
| Supply Current | $T_A = 25^{\circ}C, R_{SET} = 70k$ | | 0.8 | 2.2 | mA |
| Input Offset Voltage | $6.4k \leq R_{SET} \leq 70k$ | | 0.5 | 0.65 | mV |
| Input Bias Current | $R_{SET} = 70k$ $R_{SET} = 6.4k$ | | 15 | 25 | nA |
| | | | 150 | 250 | nA |
| Input Offset Current | $R_{SET} = 70k$ $R_{SET} = 6.4k$ | | 0.5 | 1 | nA |
| | | | 5 | 10 | nA |
| Input Offset Current Drift | $R_{SET} = 70k$ | | 3 | | pA/ $^{\circ}C$ |
| Average Temperature | $R_S \leq 200\Omega, 6.4k \leq R_{SET} \leq 70k$ | | | | |
| Coefficient of Input Offset Voltage | Offset Voltage Nulled | | 0.07 | 0.2 | $\mu V/^{\circ}C$ |
| Long Term Stability | | | 3 | | $\mu V/yr$ |
| Supply Current | | | 1 | 3.5 | mA |
| Input Voltage Range | $V_S = \pm 15V$, (Note 5) $R_{SET} = 70k$ $R_{SET} = 6.4k$ | ± 13 | | | V |
| | | $+7, -13$ | | | V |
| Common-Mode Rejection Ratio | $R_{SET} = 70k$ $R_{SET} = 6.4k$ | 126 | 140 | | dB |
| | | 120 | 130 | | dB |
| Supply Voltage Rejection Ratio | $R_{SET} = 70k$ $R_{SET} = 6.4k$ | 118 | 126 | | dB |
| | | 114 | 120 | | dB |
| Voltage Gain | $T_A = 25^{\circ}C, R_{SET} = 70k,$ $R_L > 3 M\Omega$ | 12 | 20 | | V/V |
| Noise | $R_{SET} = 70k, R_{SOURCE} = 0$ | | 8 | | nV/ \sqrt{Hz} |

Note 1: The maximum junction temperature of the LM321A is $85^{\circ}C$. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of $150^{\circ}C/W$, junction to ambient, or $18^{\circ}C/W$, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of $1V$ is applied between the inputs.

Note 3: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5 \leq V_S \leq \pm 20V$ and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise specified. With the LM221A, however all temperature specifications are limited to $-25^{\circ}C \leq T_A \leq +85^{\circ}C$, and for the LM321A the specifications apply over a $0^{\circ}C$ to $+70^{\circ}C$ temperature range.

Note 5: External precision resistor -0.1% —can be placed from pins 1 and 8 to 7 increase positive common-mode range.

Note 6: See RETS121X for LM121H/883 military specs and RET121AX for LM121AH/883 military specs.

Supply Voltage $\pm 20\text{V}$
 Power Dissipation (Note 1) 500 mW
 Differential Input Voltage (Notes 2 and 3) $\pm 15\text{V}$
 Input Voltage (Note 3) $\pm 15\text{V}$

Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Lead Temperature (Soldering, 10 sec.) 260°C
 ESD rating to be determined.

Electrical Characteristics (Note 4) LM221, LM321

| Parameter | Conditions | LM221 | | | LM321 | | | Units |
|---|--|----------|-----|-----|----------|-----|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$, $6.4\text{k} \leq R_{\text{SET}} \leq 70\text{k}$ | | | 0.7 | | | 1.5 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$, $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | | | 1 | | | 2 | nA |
| | | | | 10 | | | 20 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$, $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | | | 10 | | | 18 | nA |
| | | | | 100 | | | 180 | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$, $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | 4 | | | 2 | | | M Ω |
| | | 0.4 | | | 0.2 | | | M Ω |
| Supply Current | $T_A = 25^\circ\text{C}$, $R_{\text{SET}} = 70\text{k}$ | | | 1.5 | | | 2.2 | mA |
| Input Offset Voltage | $6.4\text{k} \leq R_{\text{SET}} \leq 70\text{k}$ | | | 1.0 | | | 2.5 | mV |
| Input Bias Current | $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | | | 30 | | | 28 | nA |
| | | | | 300 | | | 280 | nA |
| Input Offset Current | $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | | | 3 | | | 4 | nA |
| | | | | 30 | | | 40 | nA |
| Input Offset Current Drift | $R_{\text{SET}} = 70\text{k}$ | | 3 | | | 3 | | pA/ $^\circ\text{C}$ |
| Average Temperature Coefficient of Input Offset Voltage | $R_S \leq 200\Omega$, $6.4\text{k} \leq R_{\text{SET}} \leq 70\text{k}$ Offset Voltage Nulled | | | 1 | | | 1 | $\mu\text{V}/^\circ\text{C}$ |
| Long Term Stability | | | 5 | | | 5 | | $\mu\text{V}/\text{yr}$ |
| Supply Current | | | | 2.5 | | | 3.5 | mA |
| Input Voltage Range | $V_S = \pm 15\text{V}$, (Note 5) $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | ± 13 | | | ± 13 | | | V |
| | | +7, -13 | | | +7, -13 | | | V |
| Common-Mode Rejection Ratio | $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | 120 | | | 114 | | | dB |
| | | 114 | | | 114 | | | dB |
| Supply Voltage Rejection Ratio | $R_{\text{SET}} = 70\text{k}$ $R_{\text{SET}} = 6.4\text{k}$ | 120 | | | 114 | | | dB |
| | | 114 | | | 114 | | | dB |
| Voltage Gain | $T_A = 25^\circ\text{C}$, $R_{\text{SET}} = 70\text{k}$, $R_L > 3\text{M}\Omega$ | 16 | | | 12 | | | V/V |
| | | | | | | | | |
| Noise | $R_{\text{SET}} = 70\text{k}$, $R_{\text{SOURCE}} = 0$ | | 8 | | | 8 | | nV/ $\sqrt{\text{Hz}}$ |

Note 1: The maximum junction temperature of the LM221 is 100°C . The maximum junction temperature of the LM321 is 85°C . For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of $150^\circ\text{C}/\text{W}$, junction to ambient, or $18^\circ\text{C}/\text{W}$, junction to case.

Note 2: The inputs are shunted with back-to-back diodes in series with a 500Ω resistor for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs.

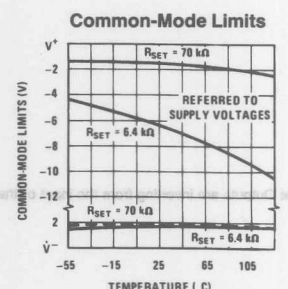
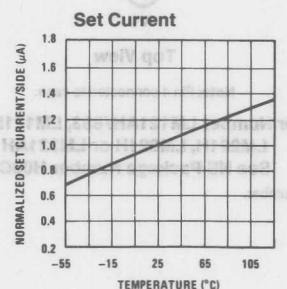
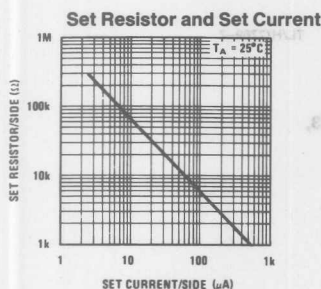
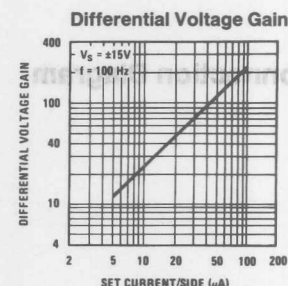
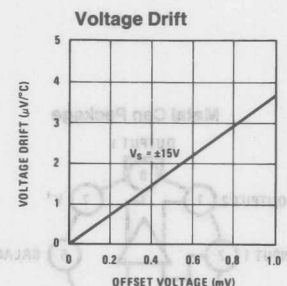
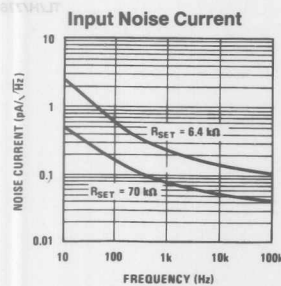
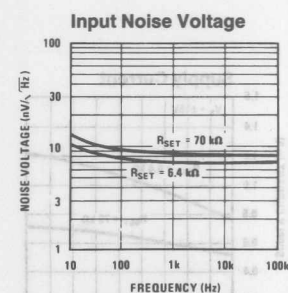
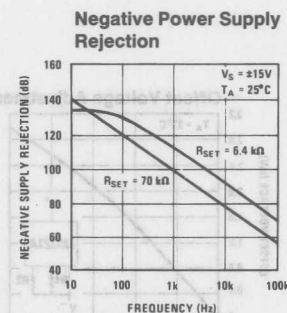
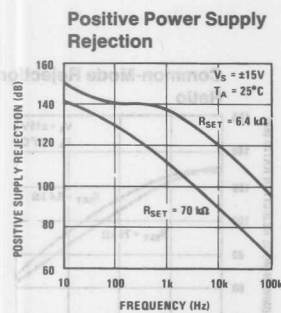
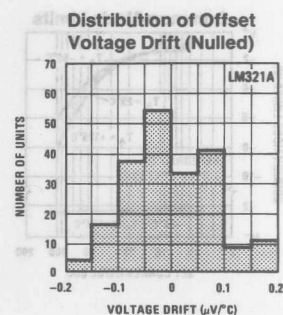
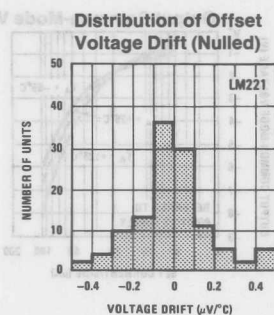
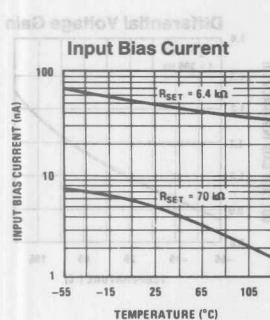
Note 3: For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

Note 4: These specifications apply for $\pm 5 \leq V_S \leq \pm 20\text{V}$ and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise specified. With the LM221, however all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, and for the LM321 the specifications apply over a 0°C to $+70^\circ\text{C}$ temperature range.

Note 5: External precision resistor $<0.1\%$ can be placed from pins 1 and 8 to 7 increase positive common-mode range.

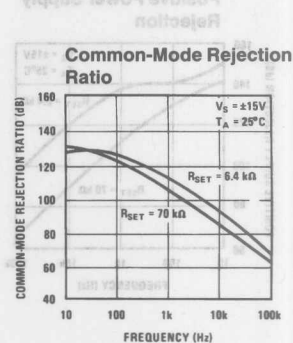
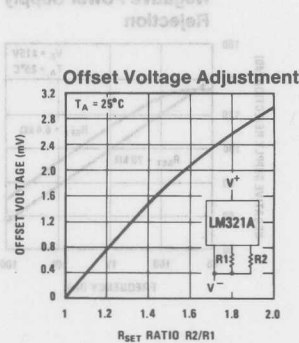
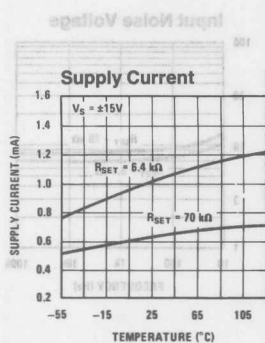
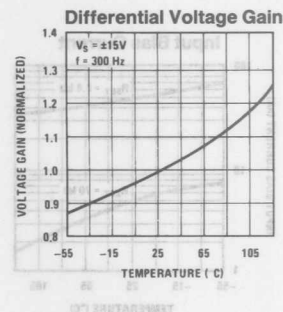
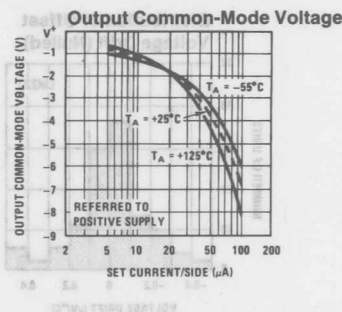
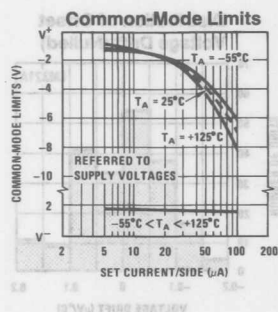
Typical Performance Characteristics

LM221/LM321

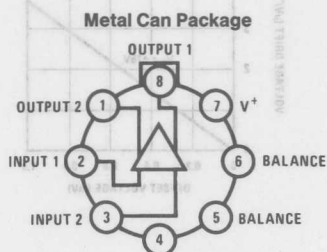


TL/H/7769-9

Typical Performance Characteristics (Continued)



Connection Diagram



Top View

Note: Pin 4 connected to case.

Order Number LM121AH/883, LM121H/883,
LM221H, LM321H or LM321AH
See NS Package Number H08C

Note: Outputs are inverting from the input of the same number.

Frequency Compensation

UNIVERSAL COMPENSATION

The additional gain of the LM321 preamplifier when used with an operational amplifier usually necessitates additional frequency compensation. When the closed loop gain of the op amp with the LM321 is less than the gain of the LM321 alone, more compensation is needed. The worst case situation is when there is 100% feedback—such as a voltage follower or integrator—and the gain of the LM321 is high. When high closed loop gains are used—for example $A_V = 1000$ —and only an addition gain of 200 is inserted by the LM321, the frequency compensation of the op amp will usually suffice.

The frequency compensation shown here is designed to operate with any unity-gain stable op amp. Figure 1 shows the basic configuration of frequency stabilizing network. In operation the output of the LM321 is rendered single ended by a $0.01 \mu\text{F}$ bypass capacitor to ground. Overall frequency compensation then is achieved by an integrating capacitor around the op amp.

$$\text{Bandwidth at unity-gain} \approx \frac{12}{2\pi R_{\text{SET}} C}$$

$$\text{for } 0.5 \text{ MHz bandwidth } C = \frac{4}{10^6 R_{\text{SET}}}$$

For use with higher frequency op amps such as the LM118 the bandwidth may be increased to about 2 MHz.

If the closed loop gain is greater than unity, "C" may be decreased to:

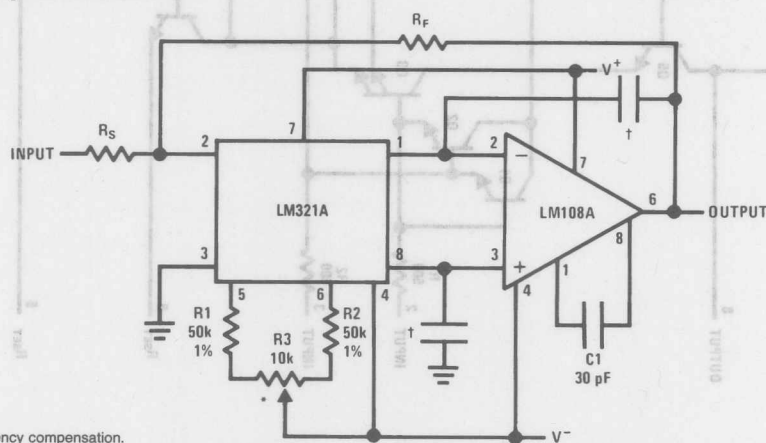
$$C = \frac{4}{10^6 A_{\text{CL}} R_{\text{SET}}}$$

ALTERNATE COMPENSATION

The two compensation capacitors can be made equal for improved power supply rejection. In this case the formula for the compensation capacitor is:

$$C = \frac{8}{10^6 A_{\text{CL}} R_{\text{SET}}}$$

Typical Applications



*Offset adjust.

†See table for frequency compensation.

FIGURE 1. Low Drift Op Amp Using the LM321A as a Preamp

Table I shows typical values for the two compensating capacitors for various gains and operating currents.

TABLE I

| Closed Loop Gain | Current Set Resistor | | | | |
|------------------|----------------------|---------------|---------------|---------------|--------------|
| | 120 k Ω | 60 k Ω | 30 k Ω | 12 k Ω | 6 k Ω |
| $A_V = 1$ | 68 | 130 | 270 | 680 | 1300 |
| $A_V = 5$ | 15 | 27 | 56 | 130 | 270 |
| $A_V = 10$ | 10 | 15 | 27 | 68 | 130 |
| $A_V = 50$ | 1 | 3 | 5 | 15 | 27 |
| $A_V = 100$ | — | 1 | 3 | 5 | 10 |
| $A_V = 500$ | — | — | 1 | 1 | 3 |
| $A_V = 1000$ | — | — | — | — | — |

This table applies for the LM108, LM101A, LM741, LM118. Capacitance is in pF.

DESIGN EQUATIONS FOR THE LM321 SERIES

$$\text{Gain } A_V \approx \frac{1.2 \times 10^6}{R_{\text{SET}}}$$

Null Pot Value should be 10% of R_{SET}

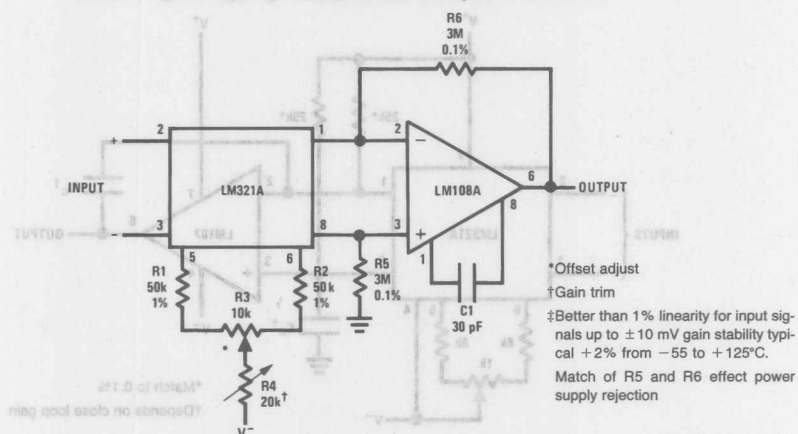
$$\text{Operating Current} \approx \frac{2 \times 0.65V}{R_{\text{SET}}}$$

$$\text{Positive Common-Mode Limit} \approx V^+ - \left[0.6 - \frac{0.65V \times 50k}{R_{\text{SET}}} \right]$$

TL/H/7769-2

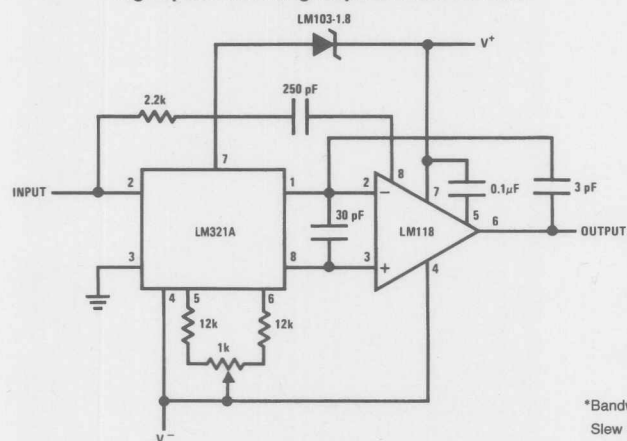
Typical Applications (Continued)

Gain of 1000 Instrumentation Amplifier†

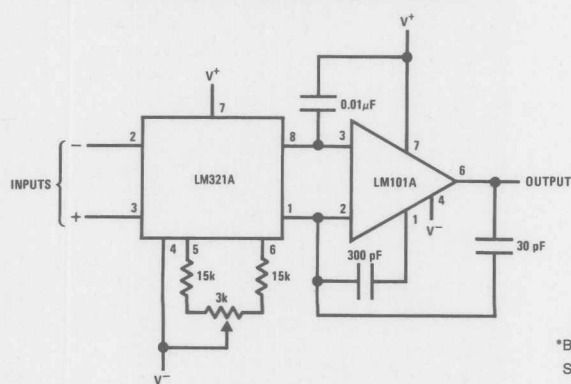


TL/H/7769-3

High Speed* Inverting Amplifier with Low Drift



Medium Speed* General Purpose Amplifier



*Match to 0.1%
†Depends on close loop gain

LM359 Dual, High Speed, Programmable, Current Mode (Norton) Amplifiers

General Description

The LM359 consists of two current differencing (Norton) input amplifiers. Design emphasis has been placed on obtaining high frequency performance and providing user programmable amplifier operating characteristics. Each amplifier is broadbanded to provide a high gain bandwidth product, fast slew rate and stable operation for an inverting closed loop gain of 10 or greater. Pins for additional external frequency compensation are provided. The amplifiers are designed to operate from a single supply and can accommodate input common-mode voltages greater than the supply.

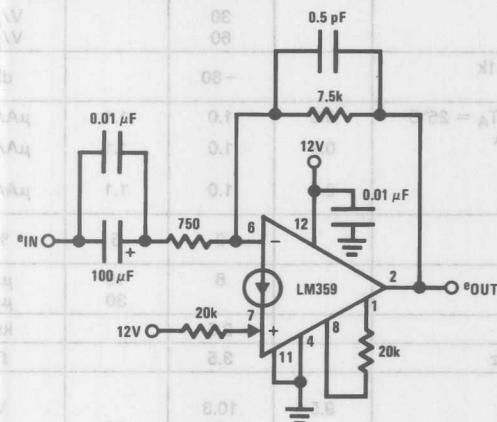
Applications

- General purpose video amplifiers
- High frequency, high Q active filters
- Photo-diode amplifiers
- Wide frequency range waveform generation circuits
- All LM3900 AC applications work to much higher frequencies

Features

- User programmable gain bandwidth product, slew rate, input bias current, output stage biasing current and total device power dissipation
- High gain bandwidth product ($I_{SET} = 0.5 \text{ mA}$)
400 MHz for $A_V = 10$ to 100
30 MHz for $A_V = 1$
- High slew rate ($I_{SET} = 0.5 \text{ mA}$)
60 V/ μs for $A_V = 10$ to 100
30 V/ μs for $A_V = 1$
- Current differencing inputs allow high common-mode input voltages
- Operates from a single 5V to 22V supply
- Large inverting amplifier output swing, 2 mV to $V_{CC} - 2 \text{ V}$
- Low spot noise, 6 nV/ $\sqrt{\text{Hz}}$, for $f > 1 \text{ kHz}$

Typical Application

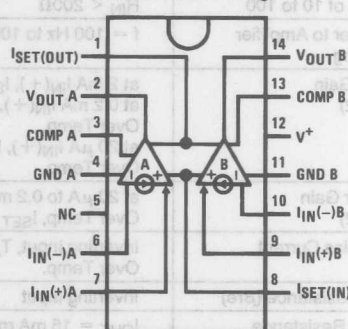


- $A_V = 20 \text{ dB}$
- $-3 \text{ dB bandwidth} = 2.5 \text{ Hz to } 25 \text{ MHz}$
- Differential phase error $< 1^\circ$ at 3.58 MHz
- Differential gain error $< 0.5\%$ at 3.58 MHz

TL/H/7788-1

Connection Diagram

Dual-In-Line Package



Top View

Order Number LM359J, LM359M or LM359N
See NS Package Number J14A, M14A or N14A

TL/H/7788-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|---|
| Supply Voltage | 22 V _{DC} or ± 11 V _{DC} |
| Power Dissipation (Note 1) | |
| J Package | 1 W |
| N Package | 750 mW |
| Maximum T _J | |
| J Package | +150°C |
| N Package | +125°C |
| Thermal Resistance | |
| J Package | |
| θ_{JA} 147°C/W still air | |
| 110°C/W with 400 linear feet/min air flow | |
| N Package | |
| θ_{JA} 100°C/W still air | |
| 75°C/W with 400 linear feet/min air flow | |

| | |
|---|---------------------|
| Input Currents, I _{IN} (+) or I _{IN} (-) | 10 mA _{DC} |
| Set Currents, I _{SET} (IN) or I _{SET} (OUT) | 2 mA _{DC} |
| Operating Temperature Range | |
| LM359 | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | |
| ESD rating to be determined. | |

Electrical Characteristics

I_{SET}(IN) = I_{SET}(OUT) = 0.5 mA, V_{supply} = 12V, T_A = 25°C unless otherwise noted

| Parameter | Conditions | LM359 | | | Units |
|--|---|-------|-----------|-----|--------------------------|
| | | Min | Typ | Max | |
| Open Loop Voltage Gain | V _{supply} = 12V, R _L = 1k, f = 100 Hz T _A = 25°C | 62 | 72 68 | | dB dB |
| Bandwidth Unity Gain | R _{IN} = 1 k Ω , C _{comp} = 10 pF | 15 | 30 | | MHz |
| Gain Bandwidth Product Gain of 10 to 100 | R _{IN} = 50 Ω to 200 Ω | 200 | 400 | | MHz |
| Slew Rate Unity Gain Gain of 10 to 100 | R _{IN} = 1 k Ω , C _{comp} = 10 pF R _{IN} < 200 Ω | | 30 60 | | V/ μ s V/ μ s |
| Amplifier to Amplifier Coupling | f = 100 Hz to 100 kHz, R _L = 1k | | -80 | | dB |
| Mirror Gain (Note 2) | at 2 mA I _{IN} (+), I _{SET} = 5 μ A, T _A = 25°C | 0.9 | 1.0 | 1.1 | μ A/ μ A |
| | at 0.2 mA I _{IN} (+), I _{SET} = 5 μ A Over Temp. | 0.9 | 1.0 | 1.1 | μ A/ μ A |
| | at 20 μ A I _{IN} (+), I _{SET} = 5 μ A Over Temp. | 0.9 | 1.0 | 1.1 | μ A/ μ A |
| Δ Mirror Gain (Note 2) | at 20 μ A to 0.2 mA I _{IN} (+) Over Temp, I _{SET} = 5 μ A | | 3 | 5 | % |
| Input Bias Current | Inverting Input, T _A = 25°C Over Temp. | | 8 30 | 15 | μ A μ A |
| Input Resistance (β re) | Inverting Input | | 2.5 | | k Ω |
| Output Resistance | I _{OUT} = 15 mA rms, f = 1 MHz | | 3.5 | | Ω |
| Output Voltage Swing V _{OUT} High V _{OUT} Low | R _L = 600 Ω I _{IN} (-) and I _{IN} (+) Grounded I _{IN} (-) = 100 μ A, I _{IN} (+) = 0 | 9.5 | 10.3 2 | 50 | V mV |
| Output Currents Source Sink (Linear Region) Sink (Overdriven) | I _{IN} (-) and I _{IN} (+) Grounded, R _L = 100 Ω | 16 | 40 | | mA |
| | V _{comp} - 0.5V = V _{OUT} = 1V, I _{IN} (+) = 0 | | 4.7 | | mA |
| | I _{IN} (-) = 100 μ A, I _{IN} (+) = 0, V _{OUT} Force = 1V | 1.5 | 9 | | mA |
| Supply Current | Non-Inverting Input Grounded, R _L = ∞ | | 18.5 | 22 | mA |
| Power Supply Rejection (Note 3) | f = 120 Hz, I _{IN} (+) Grounded | 40 | 50 | | dB |

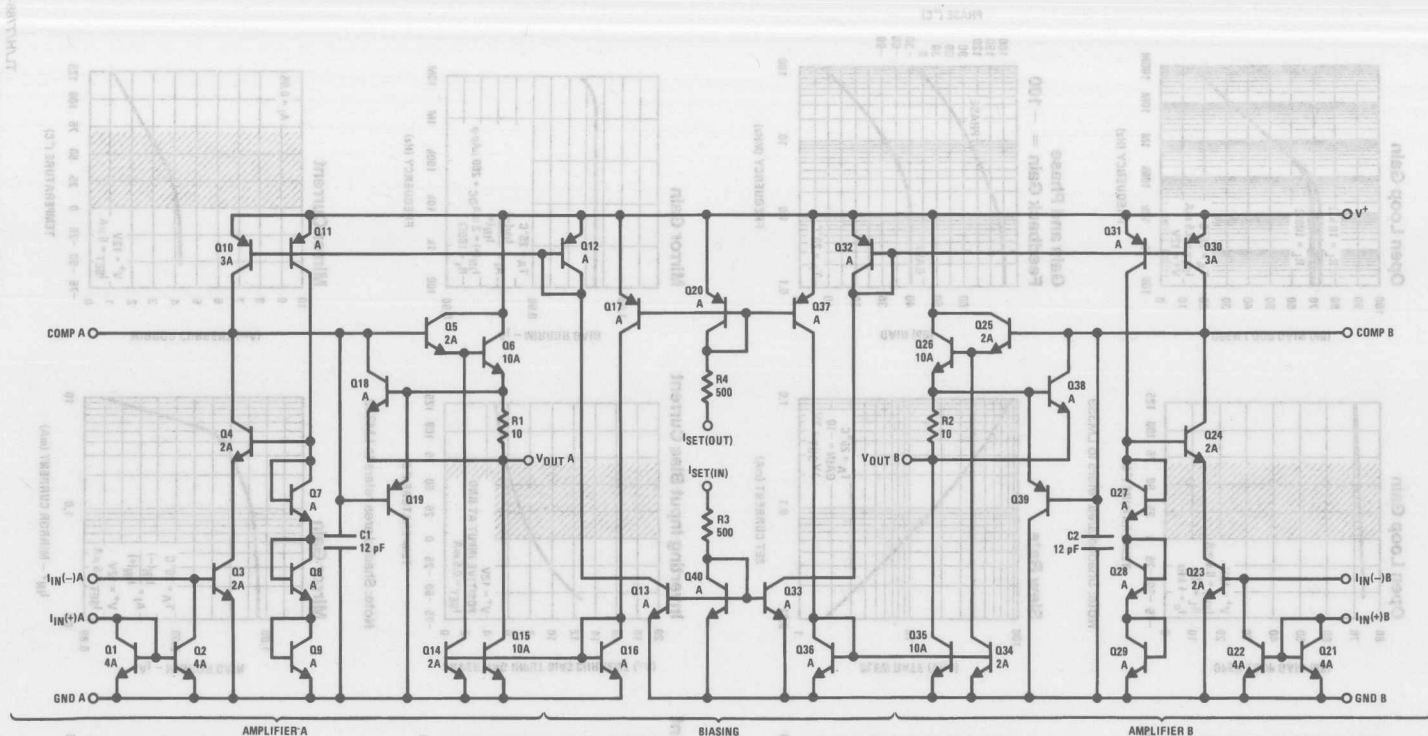
Note 1: See Maximum Power Dissipation graph.

Note 2: Mirror gain is the current gain of the current mirror which is used as the non-inverting input. $(A_i = \frac{I_{IN}(-)}{I_{IN}(+)})$ Δ Mirror Gain is the % change in A_i for two different mirror currents at any given temperature.

Note 3: See Supply Rejection graphs.

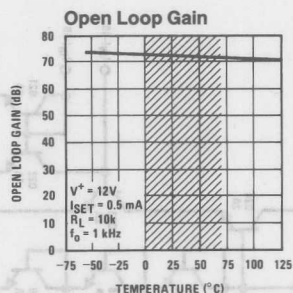
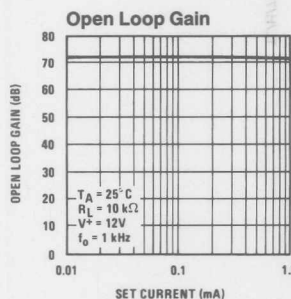
Schematic Diagram

TL/H/7788-3

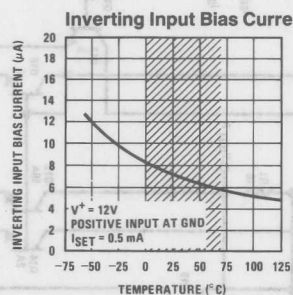
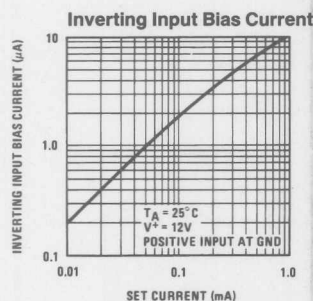
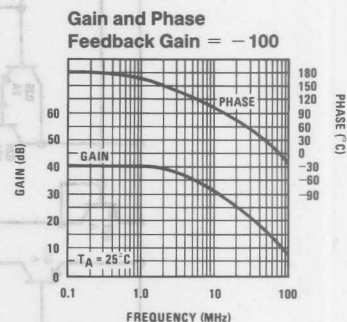
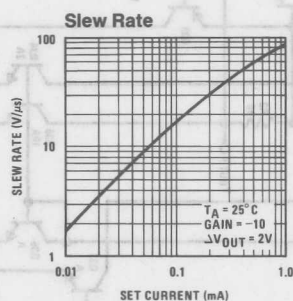
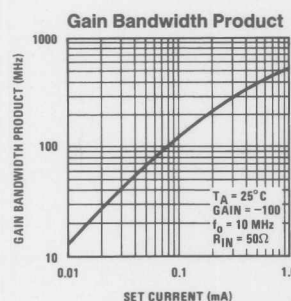
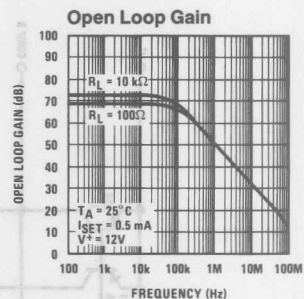


LM3595

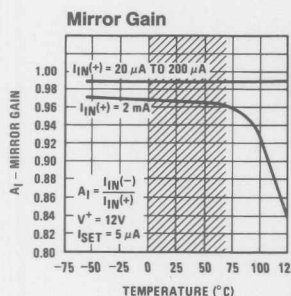
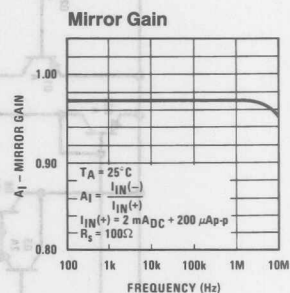
Typical Performance Characteristics



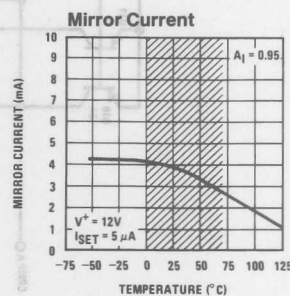
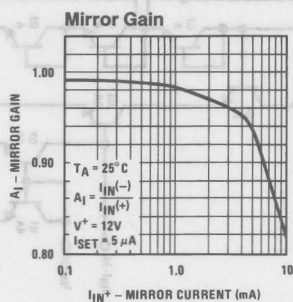
Note: Shaded area refers to LM359



Note: Shaded area refers to LM359



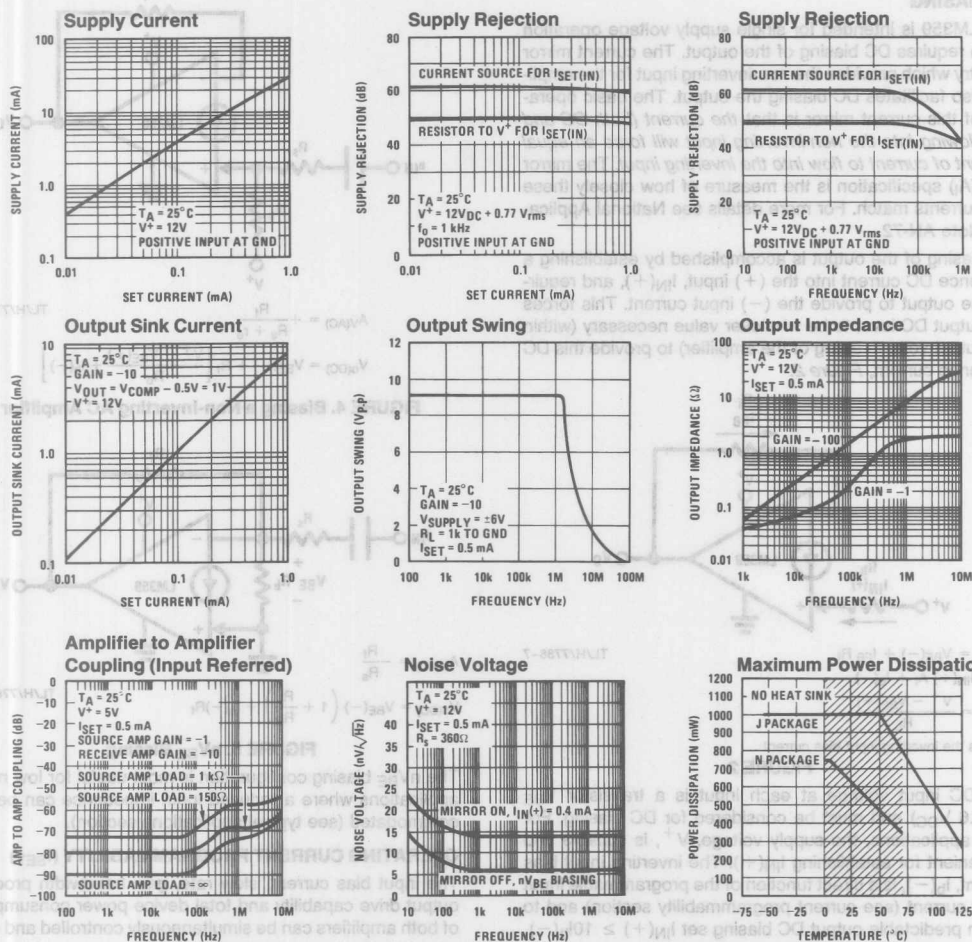
Note: Shaded area refers to LM359



Note: Shaded area refers to LM359

TL/H/7788-4

Typical Performance Characteristics (Continued)



Note: Shaded area refers to LM359J/LM359N
 TL/H/7788-5

Application Hints

The LM359 consists of two wide bandwidth, decompensated current differencing (Norton) amplifiers. Although similar in operation to the original LM3900, design emphasis for these amplifiers has been placed on obtaining much higher frequency performance as illustrated in Figure 1.

This significant improvement in frequency response is the result of using a common-emitter/common-base (cascode) gain stage which is typical in many discrete and integrated video and RF circuit designs. Another versatile aspect of these amplifiers is the ability to externally program many internal amplifier parameters to suit the requirements of a wide variety of applications in which this type of amplifier can be used.

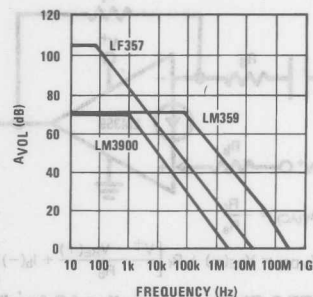


FIGURE 1

TL/H/7788-6

which requires DC biasing of the output. The current mirror circuitry which provides the non-inverting input for the amplifier also facilitates DC biasing the output. The basic operation of this current mirror is that *the current (both DC and AC) flowing into the non-inverting input will force an equal amount of current to flow into the inverting input*. The mirror gain (A_i) specification is the measure of how closely these two currents match. For more details see National Application Note AN-72.

DC biasing of the output is accomplished by establishing a reference DC current into the (+) input, $I_{IN}(+)$, and requiring the output to provide the (-) input current. This forces the output DC level to be whatever value necessary (within the output voltage swing of the amplifier) to provide this DC reference current, Figure 2.

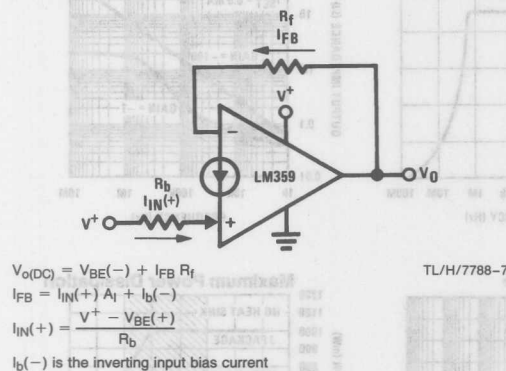


FIGURE 2

The DC input voltage at each input is a transistor V_{BE} ($\approx 0.6 V_{DC}$) and must be considered for DC biasing. For most applications, the supply voltage, V^+ , is suitable and convenient for establishing $I_{IN}(+)$. The inverting input bias current, $I_b(-)$, is a direct function of the programmable input stage current (see current programmability section) and to obtain predictable output DC biasing set $I_{IN}(+) \geq 10 I_b(-)$. The following figures illustrate typical biasing schemes for AC amplifiers using the LM359:

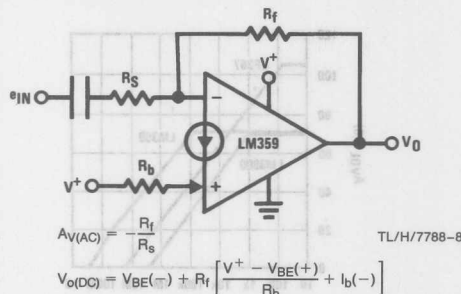


FIGURE 3. Biasing an Inverting AC Amplifier

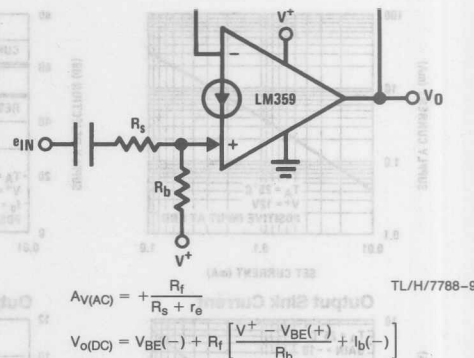


FIGURE 4. Biasing a Non-Inverting AC Amplifier

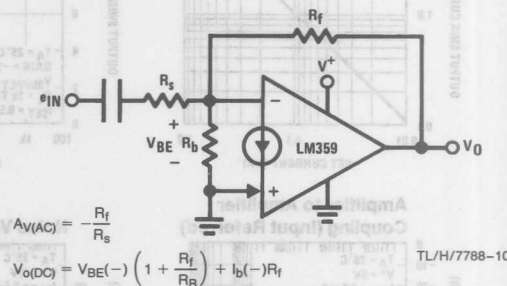


FIGURE 5. nV_{BE} Biasing

The nV_{BE} biasing configuration is most useful for low noise applications where a reduced input impedance can be accommodated (see typical applications section).

OPERATING CURRENT PROGRAMMABILITY (I_{SET})

The input bias current, slew rate, gain bandwidth product, output drive capability and total device power consumption of both amplifiers can be simultaneously controlled and optimized via the two programming pins $I_{SET(OUT)}$ and $I_{SET(IN)}$.

$I_{SET(OUT)}$

The output set current ($I_{SET(OUT)}$) is equal to the amount of current sourced from pin 1 and establishes the class A biasing current for the Darlington emitter follower output stage. Using a single resistor from pin 1 to ground, as shown in Figure 6, this current is equal to:

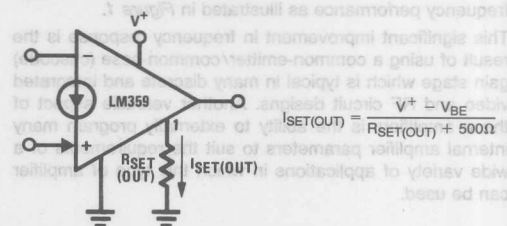


FIGURE 6. Establishing the Output Set Current

Application Hints (Continued)

The output set current can be adjusted to optimize the amount of current the output of the amplifier can sink to drive load capacitance and for loads connected to V^+ . The maximum output sinking current is approximately 10 times $I_{SET(OUT)}$. This set current is best used to reduce the total device supply current if the amplifiers are not required to drive small load impedances.

$I_{SET(IN)}$

The input set current $I_{SET(IN)}$ is equal to the current flowing into pin 8. A resistor from pin 8 to V^+ sets this current to be:

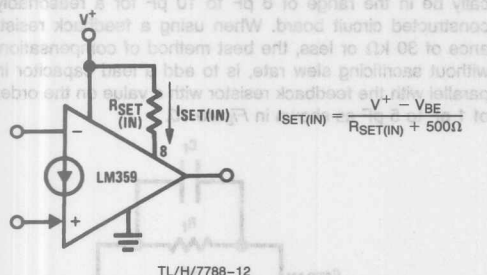


FIGURE 7. Establishing the Input Set Current

$I_{SET(IN)}$ is most significant in controlling the AC characteristics of the LM359 as it directly sets the total input stage current of the amplifiers which determines the maximum slew rate, the frequency of the open loop dominant pole, the input resistance of the (-) input and the biasing current $I_b(-)$. All of these parameters are significant in wide band amplifier design. The input stage current is approximately 3 times $I_{SET(IN)}$ and by using this relationship the following first order approximations for these AC parameters are:

$$S_r(MAX) = \text{max slew rate} \approx \frac{3 I_{SET(IN)} (10^{-6})}{C_{comp}} (V/\mu s)$$

$$\text{frequency of dominant pole} \approx \frac{3 I_{SET(IN)}}{2\pi C_{comp} A_{VOL} (0.026V)} (Hz)$$

$$\text{input resistance} = \beta r_e \approx \frac{150 (0.026V)}{3 I_{SET(IN)}} (\Omega)$$

where C_{comp} is the total capacitance from the compensation pin (pin 3 or pin 13) to ground, A_{VOL} is the low frequency open loop voltage gain in V/V and an ambient tempera-

ture of 25°C is assumed ($KT/q = 26 \text{ mV}$ and $\beta_{typ} = 150$). $I_{SET(IN)}$ also controls the DC input bias current by the expression:

$$I_b(-) = \frac{3 I_{SET}}{\beta} \approx \frac{I_{SET}}{50} \text{ for NPN } \beta = 150$$

which is important for DC biasing considerations.

The total device supply current (for both amplifiers) is also a direct function of the set currents and can be approximated by:

$$I_{supply} \approx 27 \times I_{SET(OUT)} + 11 \times I_{SET(IN)}$$

with each set current programmed by individual resistors.

PROGRAMMING WITH A SINGLE RESISTOR

Operating current programming may also be accomplished using only one resistor by letting $I_{SET(IN)}$ equal $I_{SET(OUT)}$. The programming current is now referred to as I_{SET} and it is created by connecting a resistor from pin 1 to pin 8 (Figure 8).

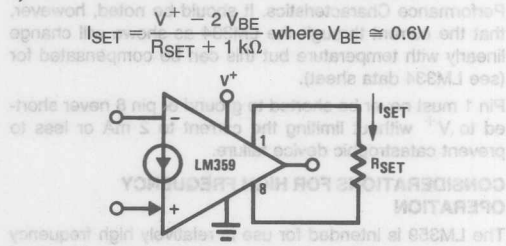


FIGURE 8. Single Resistor Programming of I_{SET}

This configuration does not affect any of the internal set current dependent parameters differently than previously discussed except the total supply current which is now equal to:

$$I_{supply} \approx 37 \times I_{SET}$$

Care must be taken when using resistors to program the set current to prevent significantly increasing the supply voltage above the value used to determine the set current. This would cause an increase in total supply current due to the resulting increase in set current and the maximum device power dissipation could be exceeded. The set resistor value(s) should be adjusted for the new supply voltage.

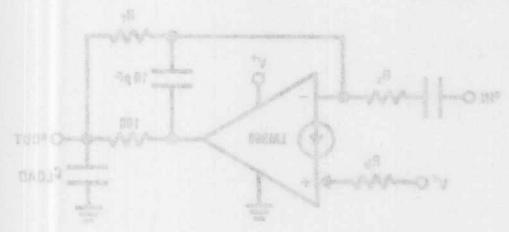


FIGURE 11. Isolating Large Capacitive Loads

Application Hints (Continued)

One method to avoid this is to use an adjustable current source which has voltage compliance to generate the set current as shown in Figure 9.

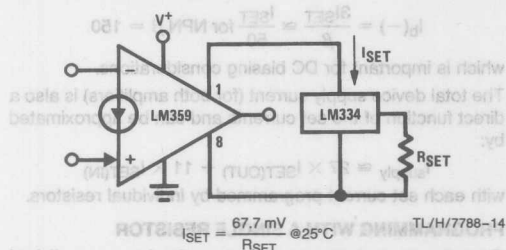


FIGURE 9. Current Source Programming of I_{SET}

This circuit allows I_{SET} to remain constant over the entire supply voltage range of the LM359 which also improves power supply ripple rejection as illustrated in the Typical Performance Characteristics. It should be noted, however, that the current through the LM334 as shown will change linearly with temperature but this can be compensated for (see LM334 data sheet).

Pin 1 must never be shorted to ground or pin 8 never shorted to V^+ without limiting the current to 2 mA or less to prevent catastrophic device failure.

CONSIDERATIONS FOR HIGH FREQUENCY OPERATION

The LM359 is intended for use in relatively high frequency applications and many factors external to the amplifier itself must be considered. Minimization of stray capacitances and their effect on circuit operation are the primary requirements. The following list contains some general guidelines to help accomplish this end:

1. Keep the leads of all external components as short as possible.
2. Place components conducting signal current from the output of an amplifier away from that amplifier's non-inverting input.
3. Use reasonably low value resistances for gain setting and biasing.
4. Use of a ground plane is helpful in providing a shielding effect between the inputs and from input to output. Avoid using vector boards.
5. Use a single-point ground and single-point supply distribution to minimize crosstalk. Always connect the two grounds (one from each amplifier) together.
6. Avoid use of long wires ($> 2''$) but if necessary, use shielded wire.
7. Bypass the supply close to the device with a low inductance, low value capacitor (typically a 0.01 μF ceramic) to create a good high frequency ground. If long supply leads are unavoidable, a small resistor ($\sim 10\Omega$) in series with the bypass capacitor may be needed and using shielded wire for the supply leads is also recommended.

COMPENSATION

The LM359 is internally compensated for stability with closed loop inverting gains of 10 or more. For an inverting gain of less than 10 and all non-inverting amplifiers (the amplifier always has 100% negative current feedback regardless of the gain in the non-inverting configuration) some external frequency compensation is required because the stray capacitance to ground from the (-) input and the feedback resistor add additional lagging phase within the feedback loop. The value of the input capacitance will typically be in the range of 6 pF to 10 pF for a reasonably constructed circuit board. When using a feedback resistance of 30 k Ω or less, the best method of compensation, without sacrificing slew rate, is to add a lead capacitor in parallel with the feedback resistor with a value on the order of 1 pF to 5 pF as shown in Figure 10.

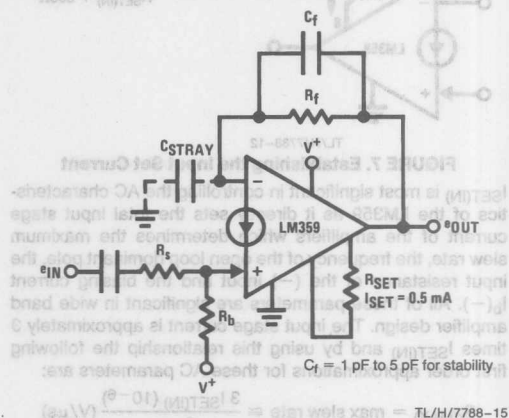


FIGURE 10. Best Method of Compensation

Another method of compensation is to increase the effective value of the internal compensation capacitor by adding capacitance from the COMP pin of an amplifier to ground. An external 20 pF capacitor will generally compensate for all gain settings but will also reduce the gain bandwidth product and the slew rate. These same results can also be obtained by reducing $I_{SET(IN)}$ if the full capabilities of the amplifier are not required. This method is termed over-compensation.

Another area of concern from a stability standpoint is that of capacitive loading. The amplifier will generally drive capacitive loads up to 100 pF without oscillation problems. Any larger C loads can be isolated from the output as shown in Figure 11. Over-compensation of the amplifier can also be used if the corresponding reduction of the GBW product can be afforded.

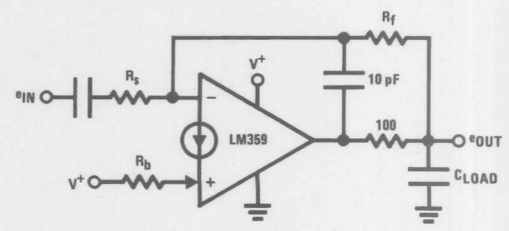


FIGURE 11. Isolating Large Capacitive Loads

Application Hints (Continued)

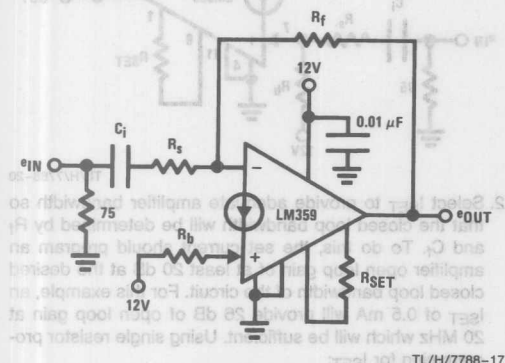
In most applications using the LM359, the input signal will be AC coupled so as not to affect the DC biasing of the amplifier. This gives rise to another subtlety of high frequency circuits which is the effective series inductance (ESL) of the coupling capacitor which creates an increase in the impedance of the capacitor at high frequencies and can cause an unexpected gain reduction. Low ESL capacitors like solid tantalum for large values of C and ceramic for smaller values are recommended. A parallel combination of the two types is even better for gain accuracy over a wide frequency range.

AMPLIFIER DESIGN EXAMPLES

The ability of the LM359 to provide gain at frequencies higher than most monolithic amplifiers can provide makes it most useful as a basic broadband amplification stage. The design of standard inverting and non-inverting amplifiers, though different than standard op amp design due to the current differencing inputs, also entail subtle design differences between the two types of amplifiers. These differences will be best illustrated by design examples. For these examples a practical video amplifier with a passband of 8 Hz to 10 MHz and a gain of 20 dB will be used. It will be assumed that the input will come from a 75Ω source and proper signal termination resistance will be considered. The supply voltage is 12 V_{DC} and single resistor programming of the operating current, I_{SET}, will be used for simplicity.

AN INVERTING VIDEO AMPLIFIER

1. Basic circuit configuration:



2. Determine the required I_{SET} from the characteristic curves for gain bandwidth product.

$$GBW_{MIN} = 10 \times 10 \text{ MHz} = 100 \text{ MHz}$$

For a flat response to 10 MHz a closed loop response to two octaves above 10 MHz (40 MHz) will be sufficient.

$$\text{Actual GBW} = 10 \times 40 \text{ MHz} = 400 \text{ MHz}$$

$$I_{SET} \text{ required} = 0.5 \text{ mA}$$

$$R_{SET} = \frac{V^+ - 2V_{BE}}{I_{SET}} - 1 \text{ k}\Omega = \frac{10.8\text{V}}{0.5 \text{ mA}} - 1 \text{ k}\Omega = 20.6 \text{ k}\Omega$$

3. Determine maximum value for R_f to provide stable DC biasing

$$I_{f(MIN)} \geq 10 \times \frac{3 I_{SET}}{\beta} = 100 \mu\text{A} \text{ minimum DC feedback current}$$

Optimum output DC level for maximum symmetrical swing without clipping is:

$$V_{O(DC)(opt)} = \frac{V_{O(MAX)} - V_{O(MIN)}}{2} + V_{O(MIN)}$$

$$\approx \frac{(V^+ - 3V_{BE}) - 2 \text{ mV}}{2}$$

$$V_{O(DC)(opt)} \approx \frac{12 - 1.8\text{V}}{2} = \frac{10.2\text{V}}{2} = 5.1 \text{ V}_{DC}$$

R_{f(MAX)} can now be found:

$$R_{f(MAX)} = \frac{V_{O(DC)(opt)} - V_{BE(-)}}{I_{f(MIN)}} = \frac{5.1\text{V} - 0.6\text{V}}{100 \mu\text{A}} = 45 \text{ k}\Omega$$

This value should not be exceeded for predictable DC biasing.

4. Select R_s to be large enough so as not to appreciably load the input termination resistance:

$$R_s \geq 750\Omega \text{ Let } R_s = 750\Omega$$

5. Select R_f for appropriate gain:

$$A_v = -\frac{R_f}{R_s} \text{ so; } R_f = 10 R_s = 7.5 \text{ k}\Omega$$

7.5 kΩ is less than the calculated R_{f(MAX)} so DC predictability is insured.

6. Since R_f = 7.5k, for the output to be biased to 5.1 V_{DC}, the reference current I_{N(+)} must be:

$$I_{N(+)} = \frac{5.1\text{V} - V_{BE(-)}}{R_f} = \frac{5.1\text{V} - 0.6\text{V}}{7.5 \text{ k}\Omega} = 600 \mu\text{A}$$

Now R_b can be found by:

$$R_b = \frac{V^+ - V_{BE(+)}}{I_{N(+)}} = \frac{12 - 0.6}{600 \mu\text{A}} = 19 \text{ k}\Omega$$

7. Select C_i to provide the proper gain for the 8 Hz minimum input frequency:

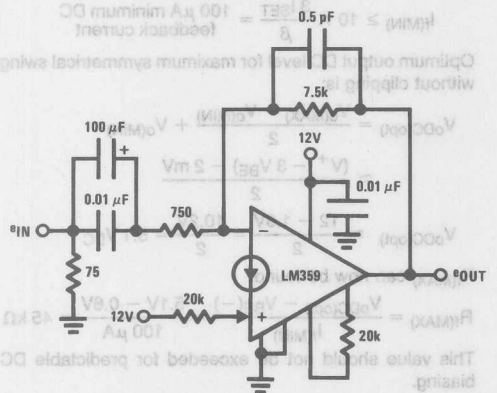
$$C_i \geq \frac{1}{2\pi R_s (f_{low})} = \frac{1}{2\pi (750\Omega) (8 \text{ Hz})} = 26 \mu\text{F}$$

A larger value of C_i will allow a flat frequency response down to 8 Hz and a 0.01 μF ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

8. Test for peaking of the frequency response and add a feedback "lead" capacitor to compensate if necessary.

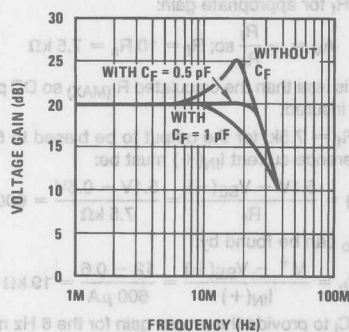
Application Hints (Continued)

Final Circuit Using Standard 5% Tolerance Resistor Values:



TL/H/7788-18

Circuit Performance:



TL/H/7788-19

$$V_{O(DC)} = 5.1V$$

$$\text{Differential phase error} < 1^\circ \text{ for } 3.58 \text{ MHz } f_{IN}$$

$$\text{Differential gain error} < 0.5\% \text{ for } 3.58 \text{ MHz } f_{IN}$$

$$f_{-3 \text{ dB low}} = 2.5 \text{ Hz}$$

A NON-INVERTING VIDEO AMPLIFIER

For this case several design considerations must be dealt with.

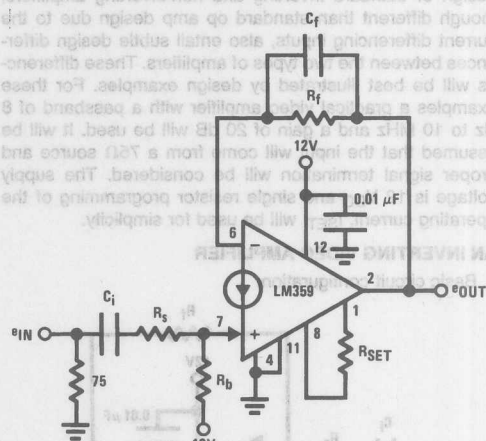
- The output voltage (AC and DC) is strictly a function of the size of the feedback resistor and the sum of AC and DC "mirror current" flowing into the (+) input.

- The amplifier always has 100% current feedback so external compensation is required. Add a small (1 pF–5 pF) feedback capacitance to leave the amplifier's open loop response and slew rate unaffected.
- To prevent saturating the mirror stage the total AC and DC current flowing into the amplifier's (+) input should be less than 2 mA.
- The output's maximum negative swing is one diode above ground due to the V_{BE} diode clamp at the (–) input.

DESIGN EXAMPLE:

$e_{IN} = 50 \text{ mV (MAX)}$, $f_{IN} = 10 \text{ MHz (MAX)}$, desired circuit $BW = 20 \text{ MHz}$, $A_V = 20 \text{ dB}$, driving source impedance = 75Ω , $V^+ = 12V$.

1. Basic circuit configuration:



TL/H/7788-20

- Select I_{SET} to provide adequate amplifier bandwidth so that the closed loop bandwidth will be determined by R_F and C_F . To do this, the set current should program an amplifier open loop gain of at least 20 dB at the desired closed loop bandwidth of the circuit. For this example, an I_{SET} of 0.5 mA will provide 26 dB of open loop gain at 20 MHz which will be sufficient. Using single resistor programming for I_{SET} :

$$R_{SET} = \frac{V^+ - 2V_{BE}}{I_{SET}} - 1 \text{ k}\Omega = 20.6 \text{ k}\Omega$$

- Since the closed loop bandwidth will be determined by

$$R_F \text{ and } C_F \left(f_{-3 \text{ dB}} = \frac{1}{2\pi R_F C_F} \right)$$

of 1 pF to 5 pF for carefully constructed circuit boards to insure stability and allow a flat frequency response. This will limit the value of R_f to be within the range of:

$$\frac{1}{2\pi \cdot 5 \text{ pF} \cdot 20 \text{ MHz}} \leq R_f \leq \frac{1}{2\pi \cdot 1 \text{ pF} \cdot 20 \text{ MHz}}$$

or $1.6 \text{ k}\Omega \leq R_f \leq 7.96 \text{ k}\Omega$

Also, for a closed loop gain of +10, R_f must be 10 times $R_s + r_e$ where r_e is the mirror diode resistance.

4. So as not to appreciably load the 75Ω input termination resistance the value of $(R_s + r_e)$ is set to 750Ω .

5. For $A_v = 10$; R_f is set to $7.5 \text{ k}\Omega$.

6. The optimum output DC level for symmetrical AC swing is:

$$V_{oDC(opt)} = \frac{V_{o(MAX)} - V_{o(MIN)}}{2} + V_{o(MIN)}$$

$$= \frac{(12 - 1.8)V - 0.6V}{2} + 0.6V = 5.4 V_{DC}$$

7. The DC feedback current must be:

$$I_{FB} = \frac{V_{oDC(opt)} - V_{BE(-)}}{R_f} = \frac{5.4V - 0.6V}{7.5k}$$

$$= 640 \mu A = I_{IN(+)}$$

DC biasing predictability will be insured because $640 \mu A$ is greater than the minimum of $I_{SET}/5$ or $100 \mu A$.

AC mirror current will be:

$$\frac{\pm e_{in peak}}{R_s + r_e} = \frac{\pm 50 \text{ mV}}{750\Omega} = \pm 66 \mu A$$

therefore the total mirror current range will be $574 \mu A$ to $706 \mu A$ which will insure gain accuracy.

8. R_b can now be found:

$$R_b = \frac{V^+ - V_{BE(+)}}{I_{IN(+)}} = \frac{12 - 0.6}{640 \mu A} = 17.8 \text{ k}\Omega$$

9. Since $R_s + r_e$ will be 750Ω and r_e is fixed by the DC mirror current to be:

$$r_e = \frac{KT}{q I_{IN(+)}} = \frac{26 \text{ mV}}{640 \mu A} \approx 40\Omega \text{ at } 25^\circ C$$

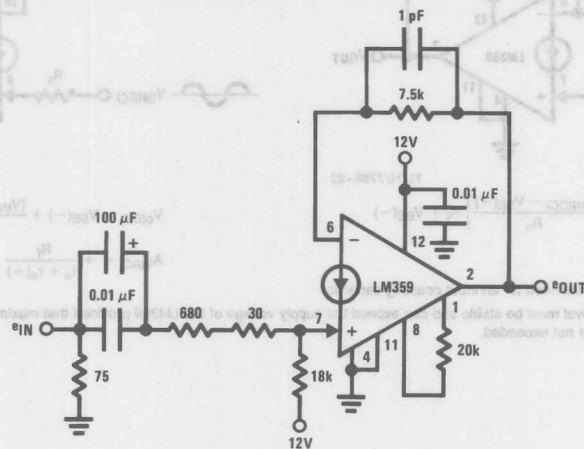
R_s must be $750\Omega - 40\Omega$ or 710Ω which can be a 680Ω resistor in series with a 30Ω resistor which are standard 5% tolerance resistor values.

10. As a final design step, C_i must be selected to pass the lower passband frequency corner of 8 Hz for this example.

$$C_i = \frac{1}{2\pi (R_s + r_e) f_{low}} = \frac{1}{2\pi (750\Omega) (8 \text{ Hz})} = 26.5 \mu F$$

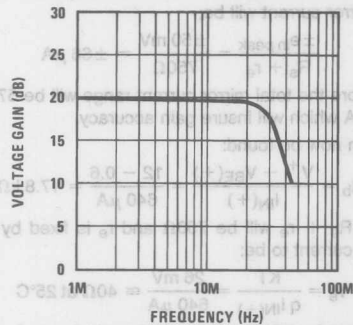
A larger value may be used and a $0.01 \mu F$ ceramic capacitor in parallel with C_i will maintain high frequency gain accuracy.

Final Circuit Using Standard 5% Tolerance Resistor Values



TL/H/7788-21

Circuit Performance



TL/H/7788-22

$$V_o(\text{DC}) = 5.4\text{V}$$

$$\text{Differential phase error} < 0.5^\circ$$

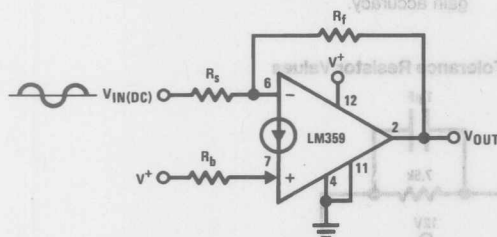
$$\text{Differential gain error} < 2\%$$

$$f_{-3\text{ dB low}} = 2.5\text{ Hz}$$

Typical Applications

DC Coupled Inputs

Inverting



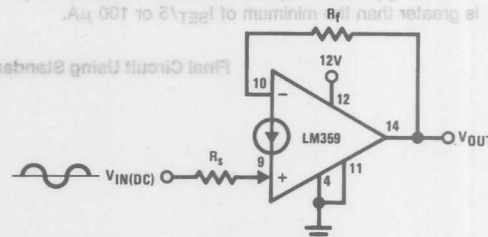
TL/H/7788-23

$$V_o(\text{DC}) = \left[\frac{V^+ - V_{BE}(+)}{R_b} - \frac{V_{IN}(\text{DC}) - V_{BE}(-)}{R_s} \right] R_f + V_{BE}(-)$$

$$A_v(\text{AC}) = \frac{R_f}{R_s}$$

- Eliminates the need for an input coupling capacitor
- Input DC level must be stable and can exceed the supply voltage of the LM359 provided that maximum input currents are not exceeded.

Non-Inverting



TL/H/7788-24

$$V_o(\text{DC}) = V_{BE}(-) + \frac{(V_{IN}(\text{DC}) - V_{BE}(+)) R_f}{R_s}$$

$$A_v(\text{AC}) = + \frac{R_f}{R_s + r_e(+)}$$

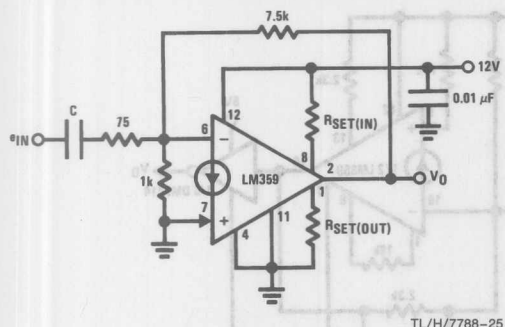
GENERAL PRECAUTIONS

The LM359 is designed primarily for single supply operation but split supplies may be used if the negative supply voltage is well regulated as the amplifiers have no negative supply rejection.

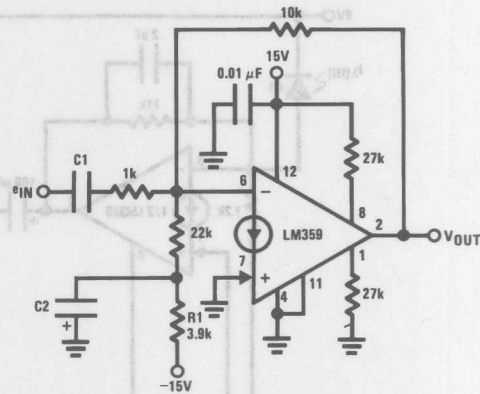
The total device power dissipation must always be kept in mind when selecting an operating supply voltage, the programming current, I_{SET} , and the load resistance, particularly when DC coupling the output to a succeeding stage. To prevent damaging the current mirror input diode, the mirror current should always be limited to 10 mA, or less, which is important if the input is susceptible to high voltage transients. The voltage at any of the inputs must not be forced more negative than -0.7V without limiting the current to 10 mA.

The supply voltage must never be reversed to the device; however, plugging the device into a socket backwards would then connect the positive supply voltage to the pin that has no internal connection (pin 5) which may prevent inadvertent device failure.

Application Hints (Continued)

Noise Reduction using nV_{BE} Biasing

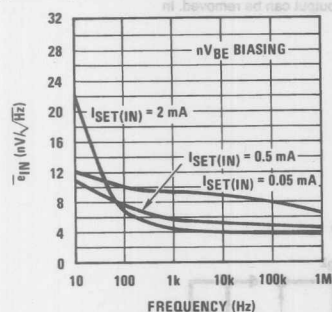
TL/H/7788-25

 nV_{BE} Biasing with a Negative Supply

TL/H/7788-26

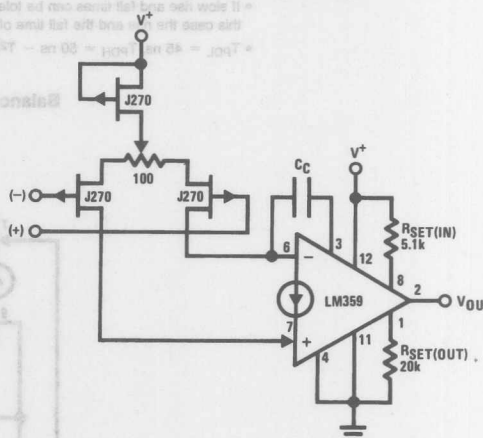
• R1 and C2 provide additional filtering of the negative biasing supply

Typical Input Referred Noise Performance



TL/H/7788-27

Adding a JFET Input Stage

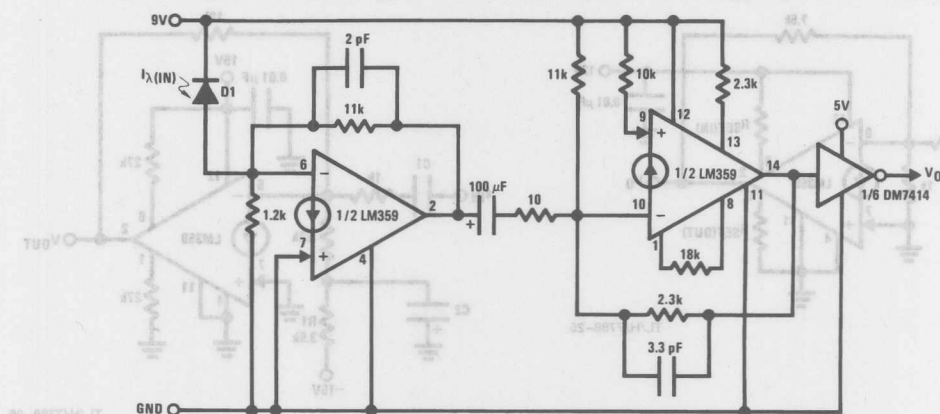


TL/H/7788-28

- FET input voltage mode op amp
- For $A_V = +1$; BW = 40 MHz, $S_r = 60 \text{ V}/\mu\text{s}$; $C_C = 51 \text{ pF}$
- For $A_V = +11$; BW = 24 MHz, $S_r = 130 \text{ V}/\mu\text{s}$; $C_C = 5 \text{ pF}$
- For $A_V = +100$; BW = 4.5 MHz, $S_r = 150 \text{ V}/\mu\text{s}$; $C_C = 2 \text{ pF}$
- V_{OS} is typically <25 mV; 100Ω potentiometer allows a V_{OS} adjust range of $\approx \pm 200 \text{ mV}$
- Inputs must be DC biased for single supply operation

Typical Applications (Continued)

Photo Diode Amplifier

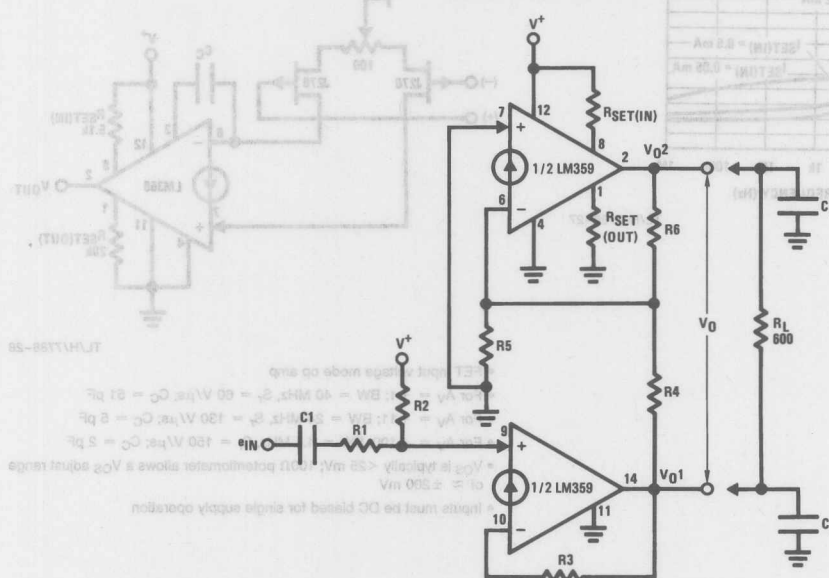


D1 ~ RCA N-Type Silicon P-I-N Photodiode

- Frequency response of greater than 10 MHz
- If slow rise and fall times can be tolerated the gate on the output can be removed. In this case the rise and the fall time of the LM359 is 40 ns.
- $T_{PDL} = 45 \text{ ns}$, $T_{PDH} = 50 \text{ ns}$ – T²L output

TL/H/7788-29

Balanced Line Driver



TL/H/7788-30

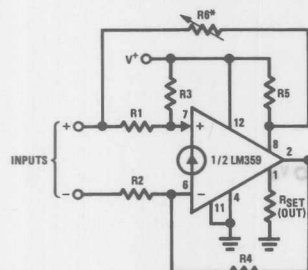
$$\text{For } V_{O1} = V_{O2} = \frac{V^+}{2}, \quad \frac{R3}{R2} = \frac{V^+ - 2\phi}{2(V^+ - \phi)}, \quad \frac{R6}{R5} = \frac{V^+ - 2\phi}{\phi} \text{ where } \phi \approx 0.6V$$

$$A_V = \frac{R_3}{R_1} \left(\frac{R_6}{R_4} + 1 \right)$$

- 1 MHz—3 dB bandwidth with gain of 10 and 0 dbm into 600Ω
- 0.3% distortion at full bandwidth; reduced to 0.05% with bandwidth of 10 kHz
- Will drive $C_L = 1500$ pF with no additional compensation, $\pm 0.01 \mu\text{F}$ with $C_{\text{comp}} = 180$ pF
- 70 dB signal to noise ratio at 0 dbm into 600Ω, 10 kHz bandwidth

Typical Applications (Continued)

Difference Amplifier



$$V_{O(DC)} = \frac{R_4}{R_3} (V^+ - \phi) \text{ where } \phi = 0.6V$$

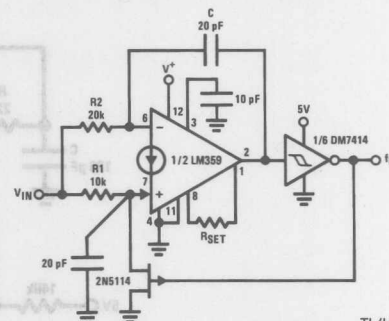
$$A_V = \frac{R_4}{R_1} \text{ for } R_1 = R_2$$

*CMRR is adjusted for max at expected CM input signal

$$R_6 \approx \frac{R_5}{5}, \text{ for } R_5 = 100 \text{ k}\Omega$$

- Wide bandwidth
- 70 dB CMRR typ
- Wide CM input voltage range

Voltage Controlled Oscillator



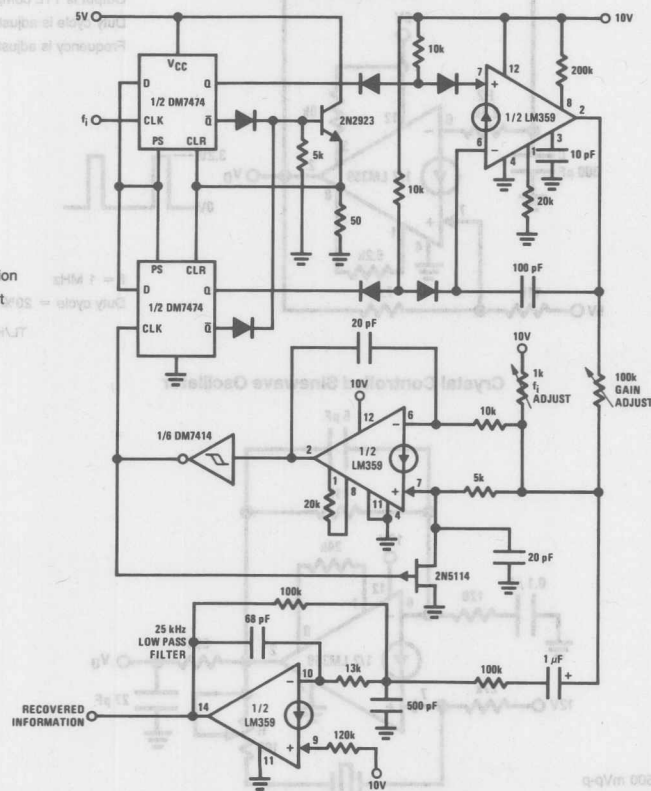
$$f_O = \frac{V_{IN} - \phi}{4 \Delta V R_1}$$

$$\text{where: } R_2 = 2R_1$$

ϕ = amplifier input voltage = 0.6V
 ΔV = DM7414 hysteresis, typ 1V

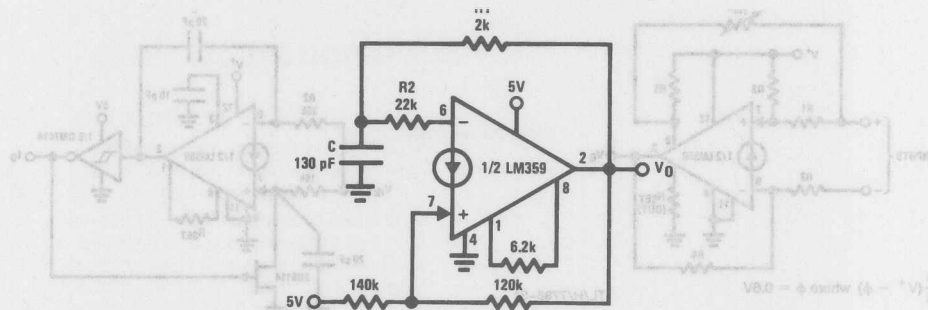
- 5 MHz operation
- T2L output

Phase Locked Loop



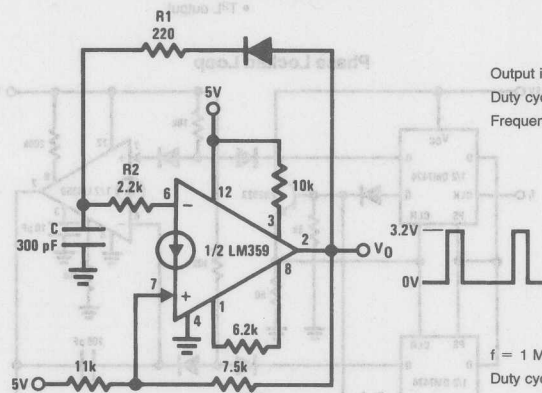
- Up to 5 MHz operation
- T2L compatible input

All diodes = 1N914



$f = 1 \text{ MHz}$
 Output is TTL compatible
 Frequency is adjusted by R1 & C ($R1 \ll R2$)

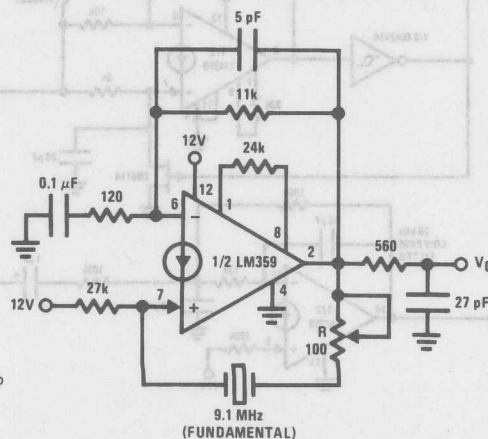
Pulse Generator



Output is TTL compatible
 Duty cycle is adjusted by R1
 Frequency is adjusted by C

$f = 1 \text{ MHz}$
 Duty cycle = 20%

Crystal Controlled Sinewave Oscillator



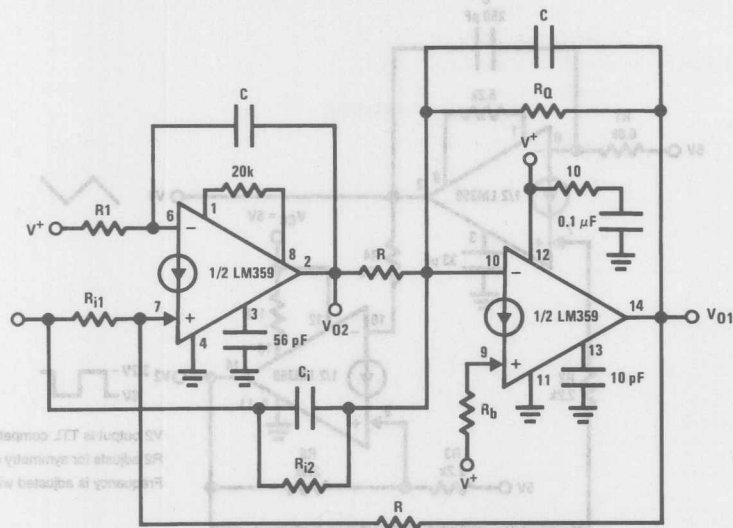
$V_o = 500 \text{ mVp-p}$
 $f = 9.1 \text{ MHz}$
 $\text{THD} < 2.5\%$

9.1 MHz
 (FUNDAMENTAL)

TL/H/7788-37

Typical Applications (Continued)

High Performance 2 Amplifier Biquad Filter(s)



TL/H/7788-35

- The high speed of the LM359 allows the center frequency Q_0 product of the filter to be: $f_o \times Q_0 \leq 5 \text{ MHz}$
- The above filter(s) maintains performance over wide temperature range
- One half of LM359 acts as a true non-inverting integrator so only 2 amplifiers (instead of 3 or 4) are needed for the biquad filter structure

DC Biasing Equations for $V_{O1(DC)} \cong V_{O2(DC)} \cong V^+ / 2$

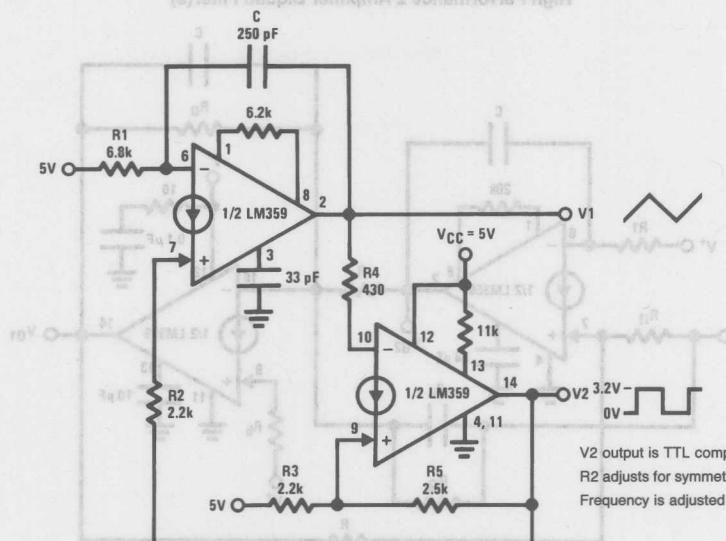
| | |
|----------|---|
| Type I | $\frac{2 V_{IN(DC)}}{V^+ (R_{i2})} + \frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; R_1 = 2R$ |
| Type II | $\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; R_1 = 2R$ |
| Type III | $\frac{1}{R} + \frac{1}{R_Q} = \frac{2}{R_b}; \frac{1}{R_1} = \frac{V_{IN(DC)}}{V^+ (R_{i1})} + \frac{1}{2R}$ |

Analysis and Design Equations

| Type | V_{O1} | V_{O2} | C_i | R_{i2} | R_{i1} | f_o | Q_0 | $f_z(\text{notch})$ | $H_o(LP)$ | $H_o(BP)$ | $H_o(HP)$ | $H_o(BR)$ |
|------|--------------|----------|-------|----------|----------|----------------------|---------|--------------------------------------|------------|----------------|-----------|---|
| I | BP | LP | O | R_{i2} | ∞ | $\frac{1}{2} \pi RC$ | R_Q/R | — | R/R_{i2} | R_Q/R_{i2} | — | — |
| II | HP | BP | C_i | ∞ | ∞ | $\frac{1}{2} \pi RC$ | R_Q/R | — | — | $R_Q C_i / RC$ | C_i / C | — |
| III | Notch/ BR | — | C_i | ∞ | R_{i1} | $\frac{1}{2} \pi RC$ | R_Q/R | $\frac{1}{2} \pi \sqrt{R R_i C C_i}$ | — | — | — | $H_o \Big _{f \rightarrow \infty} = C_i / C$ $H_o \Big _{f \rightarrow 0} = C / R_i$ |

Typical Applications (Continued)

Triangle Waveform Generator



V2 output is TTL compatible
R2 adjusts for symmetry of the triangle waveform
Frequency is adjusted with R5 and C

TL/H/7788-38

LM392/LM2924

Low Power Operational Amplifier/Voltage Comparator

General Description

The LM392 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM392 extremely useful in the design of portable equipment.

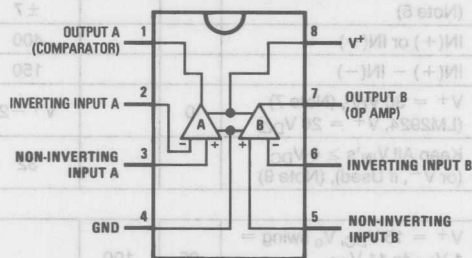
Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM358 dual op amp and the LM393 dual comparator

Connection Diagram (Top View)

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

Dual-In-Line Package



Order Number LM392M or LM2924M

See NS Package Number M08A

Order Number LM392N or LM2924N

See NS Package Number N08E

Features

- Wide power supply voltage range
Single supply 3V to 32V
Dual supply $\pm 1.5V$ to $\pm 16V$
- Low supply current drain—essentially independent of supply voltage 600 μA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to V+ $\pm 1.5V$

ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with all types of logic systems

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | LM392 | LM2924 |
|---|------------------|------------------|
| Supply Voltage, V^+ | 32V or $\pm 16V$ | 26V or $\pm 13V$ |
| Differential Input Voltage | 32V | 26V |
| Input Voltage | -0.3V to +32V | -0.3V to +26V |
| Power Dissipation (Note 1) | | |
| Molded DIP (LM392N, LM2924N) | 820 mW | 820 mW |
| Small Outline Package (LM392M, LM2924M) | 530 mW | 530 mW |
| Output Short-Circuit to Ground (Note 2) | Continuous | Continuous |
| Input Current ($V_{IN} < -0.3 V_{DC}$) (Note 3) | 50 mA | 50 mA |
| Operating Temperature Range | 0°C to +70°C | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C | -65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C |
| ESD rating to be determined. | | |
| Soldering Information | | |
| Dual-in-Line Package | 260°C | 260°C |
| Soldering (10 seconds) | | |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($V^+ = 5 V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

| Parameter | Conditions | LM392 | | | LM2924 | | | Units |
|---------------------------------|--|-------|---------|-------------|--------|---------|-------------|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$, (Note 5) | | ± 2 | ± 5 | | ± 2 | ± 7 | mV |
| Input Bias Current | $IN(+)$ or $IN(-)$, $T_A = 25^\circ\text{C}$, (Note 6), $V_{CM} = 0V$ | | 50 | 250 | | 50 | 250 | nA |
| Input Offset Current | $IN(+)$ - $IN(-)$, $T_A = 25^\circ\text{C}$ | | ± 5 | ± 50 | | ± 5 | ± 50 | nA |
| Input Common-Mode Voltage Range | $V^+ = 30 V_{DC}$, $T_A = 25^\circ\text{C}$, (Note 7) (LM2924, $V^+ = 26 V_{DC}$) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | V |
| Supply Current | $R_L = \infty$, $V^+ = 30V$, (LM2924, $V^+ = 26V$) | | 1 | 2 | | 1 | 2 | mA |
| Supply Current | $R_L = \infty$, $V^+ = 5V$ | | 0.5 | 1 | | 0.5 | 1 | mA |
| Amplifier-to-Amplifier Coupling | $f = 1 \text{ kHz}$ to 20 kHz, $T_A = 25^\circ\text{C}$, Input Referred, (Note 8) | | -100 | | | -100 | | dB |
| Input Offset Voltage | (Note 5) | | | ± 7 | | | ± 10 | mV |
| Input Bias Current | $IN(+)$ or $IN(-)$ | | | 400 | | | 500 | nA |
| Input Offset Current | $IN(+)$ - $IN(-)$ | | | 150 | | | 200 | nA |
| Input Common-Mode Voltage Range | $V^+ = 30 V_{DC}$, (Note 7) (LM2924, $V^+ = 26 V_{DC}$) | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | V |
| Differential Input Voltage | Keep All V_{IN} 's $\geq 0 V_{DC}$ (or V^- , if Used), (Note 9) | | | 32 | | | 26 | V |
| OP AMP ONLY | | | | | | | | |
| Large Signal Voltage Gain | $V^+ = 15 V_{DC}$, V_o swing = $1 V_{DC}$ to $11 V_{DC}$, $R_L = 2 \text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | 25 | 100 | | 25 | 100 | | V/mV |

Electrical Characteristics ($V^+ = 5 V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4) (Continued)

| Parameter | Conditions | LM392 | | | LM2924 | | | Units |
|------------------------------|---|-------|-----|-------------|--------|-----|-------------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| OP AMP ONLY | | | | | | | | |
| Output Voltage Swing | $R_L = 2\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, (LM2924, $R_L \geq 10\text{ k}\Omega$) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | V |
| Common-Mode Rejection Ratio | DC, $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}_{DC}$ to $V^+ - 1.5\text{ V}_{DC}$ | 65 | 70 | | 50 | 70 | | dB |
| Power Supply Rejection Ratio | DC, $T_A = 25^\circ\text{C}$ | 65 | 100 | | 50 | 100 | | dB |
| Output Current Source | $V_{IN(+)} = 1\text{ V}_{DC}$, $V_{IN(-)} = 0\text{ V}_{DC}$, $V^+ = 15\text{ V}_{DC}$, $V_o = 2\text{ V}_{DC}$, $T_A = 25^\circ\text{C}$ | 20 | 40 | | 20 | 40 | | mA |
| Output Current Sink | $V_{IN(-)} = 1\text{ V}_{DC}$, $V_{IN(+)} = 0\text{ V}_{DC}$, $V^+ = 15\text{ V}_{DC}$, $V_o = 2\text{ V}_{DC}$, $T_A = 25^\circ\text{C}$ | 10 | 20 | | 10 | 20 | | mA |
| | $V_{IN(-)} = 1\text{ V}_{DC}$, $V_{IN(+)} = 0\text{ V}_{DC}$, $V^+ = 15\text{ V}_{DC}$, $V_o = 200\text{ mV}$, $T_A = 25^\circ\text{C}$ | 12 | 50 | | 12 | 50 | | μA |
| Input Offset Voltage Drift | $R_S = 0\Omega$ | | 7 | | | 7 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current Drift | $R_S = 0\Omega$ | | 10 | | | 10 | | $\text{pA}/^\circ\text{C}$ |
| COMPARATOR ONLY | | | | | | | | |
| Voltage Gain | $R_L \geq 15\text{ k}\Omega$, $V^+ = 15\text{ V}_{DC}$, $T_A = 25^\circ\text{C}$ | 50 | 200 | | 25 | 100 | | V/mV |
| Large Signal Response Time | $V_{IN} = \text{TTL Logic Swing}$, $V_{REF} = 1.4\text{ V}_{DC}$, $V_{RL} = 5\text{ V}_{DC}$, $R_L = 5.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ | | 300 | | | 300 | | ns |
| Response Time | $V_{RL} = 5\text{ V}_{DC}$, $R_L = 5.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$, (Note 10) | | 1.3 | | | 1.5 | | μs |
| Output Sink Current | $V_{IN(-)} = 1\text{ V}_{DC}$, $V_{IN(+)} = 0\text{ V}_{DC}$, $V_o \geq 1.5\text{ V}_{DC}$, $T_A = 25^\circ\text{C}$ | 6 | 16 | | 6 | 16 | | mA |
| Saturation Voltage | $V_{IN(-)} \geq 1\text{ V}_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\text{ mA}$, $T_A = 25^\circ\text{C}$ | | 250 | 400 | | | 400 | mV |
| | $V_{IN(-)} \geq 1\text{ V}_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\text{ mA}$ | | | 700 | | | 700 | mV |
| Output Leakage Current | $V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\text{ V}_{DC}$, $V_o = 5\text{ V}_{DC}$, $T_A = 25^\circ\text{C}$ | | 0.1 | | | 0.1 | | nA |
| | $V_{IN(-)} = 0$, $V_{IN(+)} \geq 1\text{ V}_{DC}$, $V_o = 30\text{ V}_{DC}$ | | | 1.0 | | | 1.0 | μA |

Note 1: For operating at temperatures above 25°C , the LM392 and the LM2924 must be derated based on a 125°C maximum junction temperature and a thermal resistance of $122^\circ\text{C}/\text{W}$ which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+ . At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V (at 25°C).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

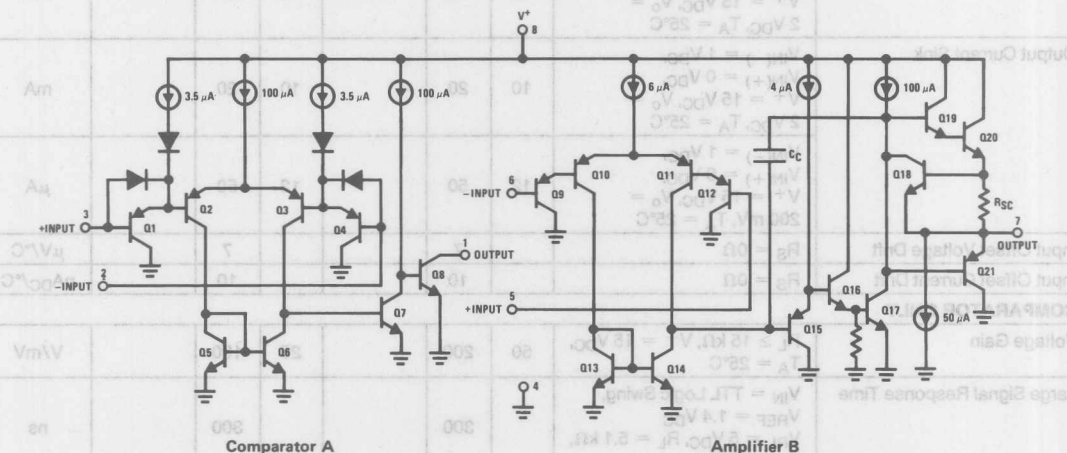
Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to 32V without damage (26V for LM2924).

Note 8: Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

Note 9: Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

Note 10: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Schematic Diagram



Application Hints

Please refer to the application hints section of the LM193 and the LM158 datasheets.

LM611

Operational Amplifier and Adjustable Reference

General Description

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current 300 μ A (op amp)
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to $(V^+ - 1.8V)$
- Wide differential input voltage $\pm 36V$
- Available in low cost 8-pin DIP
- Available in plastic package rated for Military Temperature Range Operation

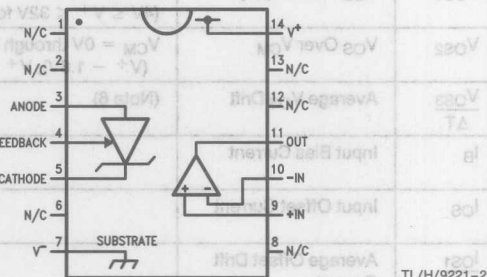
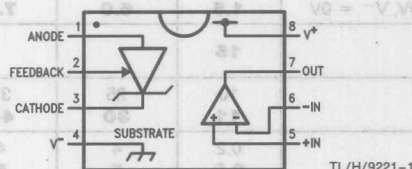
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available $\pm 0.6\%$
- Wide operating current range 17 μ A to 20 mA
- Reference floats above ground
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and Mass Flow Control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



Ordering Information

| Reference Tolerance & V_{OS} | Temperature Range | | | Package | NSC Drawing |
|--|--|---|---|--------------------------------|-------------|
| | Military $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | Industrial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ | Commercial $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | | |
| $\pm 0.6\%$ @ 80 ppm/ $^{\circ}\text{C}$ max $V_{OS} = 3.5$ mV max | LM611AMN | LM611AIN | — | 8-pin molded DIP | N08E |
| | LM611AMJ/883 (Note 12) | — | — | 8-pin ceramic DIP | J08A |
| $\pm 2.0\%$ @ 150 ppm/ $^{\circ}\text{C}$ max $V_{OS} = 5$ mV max | LM611MN | LM611BIN | LM611CN | 8-pin molded DIP | N08E |
| | — | LM611IM | LM611CM | 14-pin Narrow Surface Mount | M14A |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pins Except V_R

(referred to V^- pin)

(Note 2)

36V (Max)

-0.3V (Min)

Current through Any Input Pin and V_R Pin

± 20 mA

Differential Input Voltage

Military and Industrial

Commercial

± 36 V

± 32 V

Storage Temperature Range

$-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$

Maximum Junction Temperature

150°C

Electrical Characteristics

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100\ \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range.

Thermal Resistance, Junction-to-Ambient (Note 3)

N Package

$100^\circ\text{C}/\text{W}$

M Package

$150^\circ\text{C}/\text{W}$

Soldering Information Soldering (10 seconds)

N Package

260°C

M Package

220°C

ESD Tolerance (Note 4)

± 1 kV

Operating Temperature Range

LM611AI, LM611I, LM611BI

$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$

LM611AM, LM611M

$-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

LM611C

$0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$

| Symbol | Parameter | Conditions | Typical (Note 5) | LM611AM LM611AI Limits (Note 6) | LM611M LM611BI LM611I LM611C Limits (Note 6) | Units |
|-----------------------------------|--------------------------------------|--|---------------------|--|---|--|
| I_S | Total Supply Current | $R_{\text{LOAD}} = \infty$, $4\text{V} \leq V^+ \leq 36\text{V}$ (32V for LM611C) | 210 221 | 300 320 | 350 370 | $\mu\text{A max}$ $\mu\text{A max}$ |
| V_S | Supply Voltage Range | | 2.2 2.9 | 2.8 3 | 2.8 3 | V min V min |
| | | | 46 43 | 36 36 | 32 32 | V max V max |
| OPERATIONAL AMPLIFIER | | | | | | |
| V_{OS1} | V_{OS} Over Supply | $4\text{V} \leq V^+ \leq 36\text{V}$ ($4\text{V} \leq V^+ \leq 32\text{V}$ for LM611C) | 1.5 2.0 | 3.5 6.0 | 5.0 7.0 | mV max mV max |
| V_{OS2} | V_{OS} Over V_{CM} | $V_{\text{CM}} = 0\text{V}$ through $V_{\text{CM}} =$ ($V^+ - 1.8\text{V}$), $V^+ = 30\text{V}$, $V^- = 0\text{V}$ | 1.0 1.5 | 3.5 6.0 | 5.0 7.0 | mV max mV max |
| $\frac{V_{\text{OS3}}}{\Delta T}$ | Average V_{OS} Drift | (Note 6) | 15 | | | $\mu\text{V}/^\circ\text{C max}$ |
| I_B | Input Bias Current | | 10 11 | 25 30 | 35 40 | nA max nA max |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA max nA max |
| I_{OS1} ΔT | Average Offset Drift Current | | 4 | | | $\text{pA}/^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 1800 | | | M Ω |
| | | Common-Mode | 3800 | | | M Ω |
| C_{IN} | Input Capacitance | Common-Mode | 5.7 | | | pF |
| e_n | Voltage Noise | $f = 100$ Hz, Input Referred | 74 | | | nV/ $\sqrt{\text{Hz}}$ |
| I_n | Current Noise | $f = 100$ Hz, Input Referred | 58 | | | fA/ $\sqrt{\text{Hz}}$ |
| CMRR | Common-Mode Rejection-Ratio | $V^+ = 30\text{V}$, $0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$ CMRR = $20 \log (\Delta V_{\text{CM}}/\Delta V_{\text{OS}})$ | 95 90 | 80 75 | 75 70 | dB min dB min |
| PSRR | Power Supply Rejection-Ratio | $4\text{V} \leq V^+ \leq 30\text{V}$, $V_{\text{CM}} = V^+/2$, PSRR = $20 \log (\Delta V^+/\Delta V_{\text{OS}})$ | 110 100 | 80 75 | 75 70 | dB min dB min |
| A_V | Open Loop Voltage Gain | $R_L = 10\text{ k}\Omega$ to GND, $V^+ = 30\text{V}$, $5\text{V} \leq V_{\text{OUT}} \leq 25\text{V}$ | 500 50 | 100 40 | 94 40 | V/mV min |
| SR | Slew Rate | $V^+ = 30\text{V}$ (Note 7) | 0.70 0.65 | 0.55 0.45 | 0.50 0.45 | V/ μs |

Electrical Characteristics (Continued)

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range.

| Symbol | Parameter | Conditions | Typical (Note 5) | LM611AM LM611AI Limits (Note 6) | LM611M LM611BI LM611I LM611C Limits (Note 6) | Units |
|--|--|---|--|--|---|------------------------------|
| OPERATIONAL AMPLIFIER (Continued) | | | | | | |
| GBW | Gain Bandwidth | $C_L = 50\text{ pF}$ | 0.80 0.50 | | | MHz |
| V_{O1} | Output Voltage Swing High | $R_L = 10\text{ k}\Omega$ to GND $V^+ = 36\text{V}$ (32V for LM611C) | $V^+ - 1.4$ $V^+ - 1.6$ | $V^+ - 1.7$ $V^+ - 1.9$ | $V^+ - 1.8$ $V^+ - 1.9$ | V min V min |
| V_{O2} | Output Voltage Swing Low | $R_L = 10\text{ k}\Omega$ to V^+ $V^+ = 36\text{V}$ (32V for LM611C) | $V^- + 0.8$ $V^- + 0.9$ | $V^- + 0.9$ $V^- + 1.0$ | $V^- + 0.95$ $V^- + 1.0$ | V max V max |
| I_{OUT} | Output Source Current | $V_{\text{OUT}} = 2.5\text{V}$, $V_{\text{IN}} = 0\text{V}$, $V_{\text{IN}} = -0.3\text{V}$ | 25 15 | 20 13 | 16 13 | mA min mA min |
| I_{SINK} | Output Sink Current | $V_{\text{OUT}} = 1.6\text{V}$, $V_{\text{IN}} = 0\text{V}$, $V_{\text{IN}} = 0.3\text{V}$ | 17 9 | 14 8 | 13 8 | mA min mA min |
| I_{SHORT} | Short Circuit Current | $V_{\text{OUT}} = 0\text{V}$, $V_{\text{IN}} = 3\text{V}$, $V_{\text{IN}} = 2\text{V}$, Source | 30 40 | 50 60 | 50 60 | mA max mA max |
| | | $V_{\text{OUT}} = 5\text{V}$, $V_{\text{IN}} = 2\text{V}$, $V_{\text{IN}} = 3\text{V}$, Sink | 30 32 | 60 80 | 70 90 | mA max mA max |
| VOLTAGE REFERENCE | | | | | | |
| V_R | Reference Voltage | (Note 8) | 1.244 | 1.2365 1.2515 ($\pm 0.6\%$) | 1.2191 1.2689 ($\pm 2.0\%$) | V min V max |
| $\frac{\Delta V_R}{\Delta T}$ | Average Temperature Drift | (Note 9) | 10 | 80 | 150 | PPM/ $^\circ\text{C}$ max |
| $\frac{\Delta V_R}{\Delta T_J}$ | Hysteresis | $\text{Hyst} = (V_{R0}' - V_{R0})/\Delta T_J$ (Note 10) | 3.2 | | | $\mu\text{V}/^\circ\text{C}$ |
| $\frac{\Delta V_R}{\Delta I_R}$ | V_R Change with Current | $V_R(100\text{ }\mu\text{A}) - V_R(17\text{ }\mu\text{A})$ | 0.05 0.1 | 1 1.1 | 1 1.1 | mV max mV max |
| | | $V_R(10\text{ mA}) - V_R(100\text{ }\mu\text{A})$ (Note 11) | 1.5 2.0 | 5 5.5 | 5 5.5 | mV max mV max |
| R | Resistance | $\Delta V_R(10 \rightarrow 0.1\text{ mA})/9.9\text{ mA}$ $\Delta V_R(100 \rightarrow 17\text{ }\mu\text{A})/83\text{ }\mu\text{A}$ | 0.2 0.6 | 0.56 13 | 0.56 13 | Ω max Ω max |
| $\frac{\Delta V_R}{V_{RO}}$ | V_R Change with High V_{RO} | $V_R(V_{RO} = V_R) - V_R(V_{RO} = 6.3\text{V})$ (5.06V between Anode and FEEDBACK) | 2.5 2.8 | 7 10 | 7 10 | mV max mV max |
| $\frac{\Delta V_R}{\Delta V^+}$ | V_R Change with V^+ Change | $V_R(V^+ = 5\text{V}) - V_R(V^+ = 36\text{V})$ ($V^+ = 32\text{V}$ for LM611C) | 0.1 0.1 | 1.2 1.3 | 1.2 1.3 | mV max mV max |
| | | $V_R(V^+ = 5\text{V}) - V_R(V^+ = 3\text{V})$ | 0.01 0.01 | 1 1.5 | 1 1.5 | mV max mV max |
| $\frac{\Delta V_R}{\Delta V_{\text{ANODE}}}$ | V_R Change with V_{ANODE} Change | $V^+ = V^+ \text{ max}$, $\Delta V_R = V_R$ (@ $V_{\text{ANODE}} = V^- = \text{GND}$) - V_R (@ $V_{\text{ANODE}} = V^+ - 1.0\text{V}$) | 0.7 3.3 | 1.5 3.0 | 1.6 3.0 | mV max mV max |
| I_{FB} | FEEDBACK Bias Current | I_{FB} ; $V_{\text{ANODE}} \leq V_{\text{FB}} \leq 5.06\text{V}$ | 22 29 | 35 40 | 50 55 | nA max nA max |
| e_n | V_R Noise | 10 Hz to 10,000 Hz, $V_{RO} = V_R$ | 30 | | | μV_{RMS} |

Electrical Characteristics (Continued)

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 3: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is $90^\circ\text{C}/\text{W}$ for the N package and $135^\circ\text{C}/\text{W}$ for the M package.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Typical values in standard typeface are for $T_J = 25^\circ\text{C}$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 7: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Note 8: V_R is the cathode-feedback voltage, nominally 1.244V.

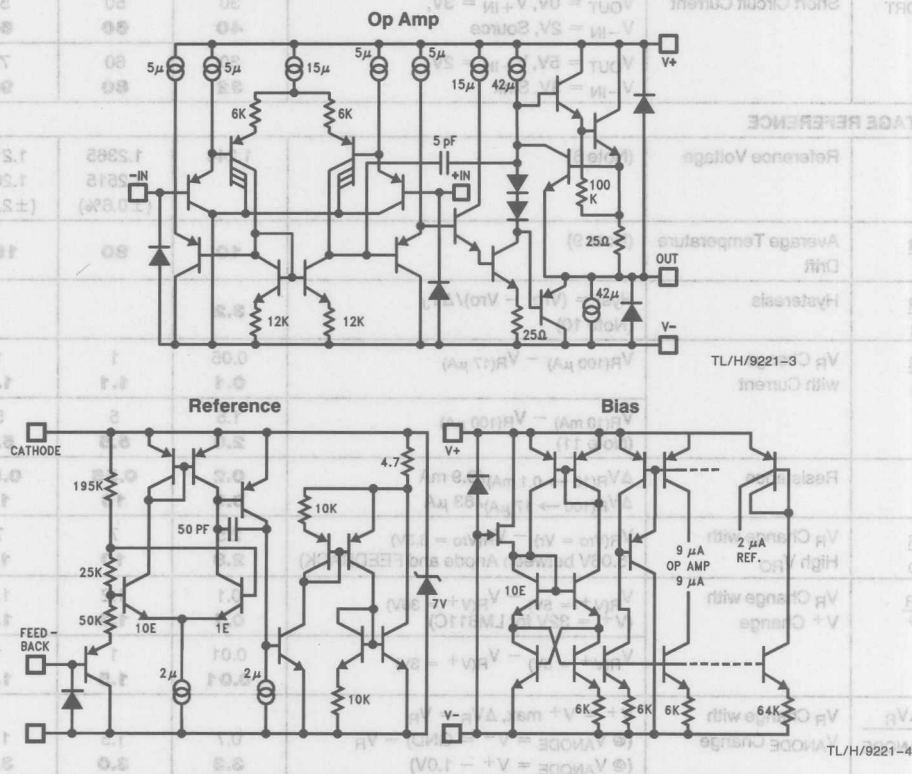
Note 9: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \Delta V_R / (V_R(25^\circ\text{C}) \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_R(25^\circ\text{C})$ is the value at 25°C , and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 10: Hysteresis is the change in V_R caused by a change in T_J , after the reference has been "dehysteresized". To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

Note 11: Low contact resistance is required for accurate measurement.

Note 12: Military RETS 611AMX electrical test specification is available on request. The LM611AMJ/883 can also be procured as a Standard Military Drawing.

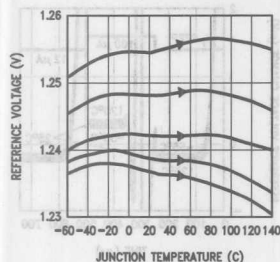
Simplified Schematic Diagrams



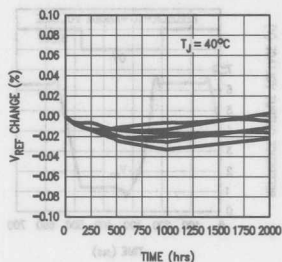
Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V_- = 0\text{V}$, unless otherwise noted

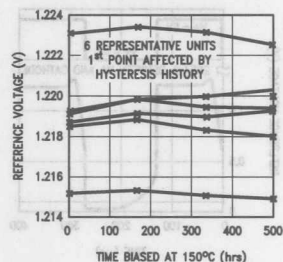
Reference Voltage vs Temp on 5 Representative Units



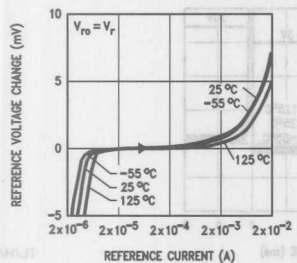
Reference Voltage Drift



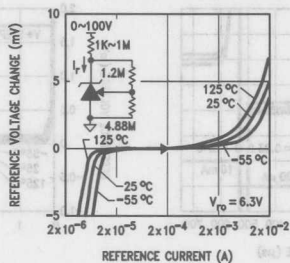
Accelerated Reference Voltage Drift vs Time



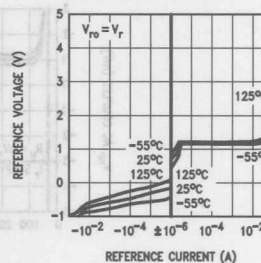
Reference Voltage vs Current and Temperature



Reference Voltage vs Current and Temperature

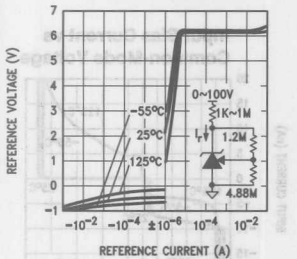


Reference Voltage vs Reference Current

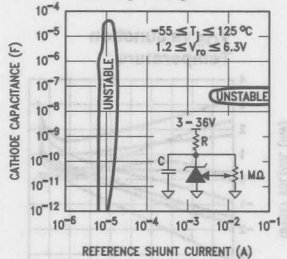


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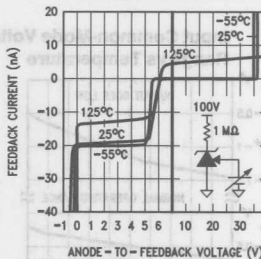
Reference Voltage vs Reference Current



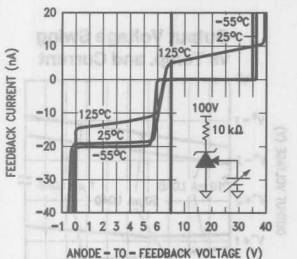
Reference AC Stability Range



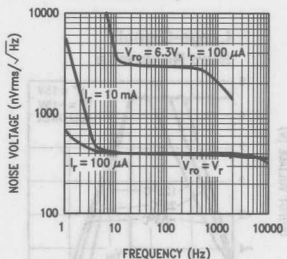
Feedback Current vs Feedback-to-Anode Voltage



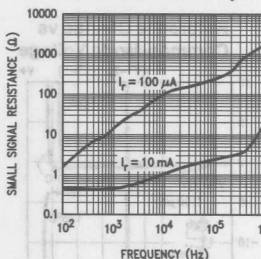
Feedback Current vs Feedback-to-Anode Voltage



Reference Noise Voltage vs Frequency

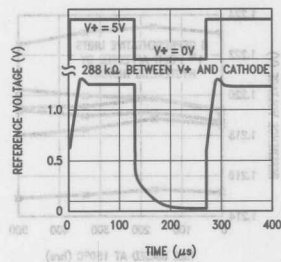


Reference Small-Signal Resistance vs Frequency

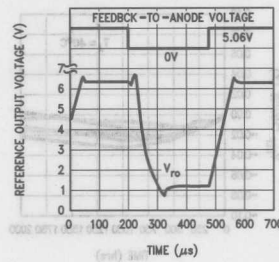


TL/H/9221-6

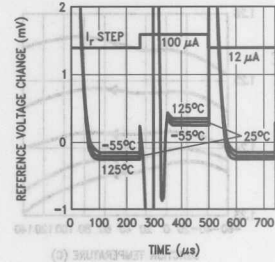
Reference Power-Up Time



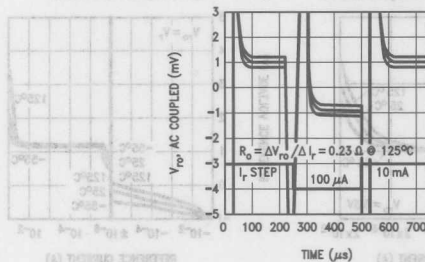
Reference Voltage with Feedback Voltage Step



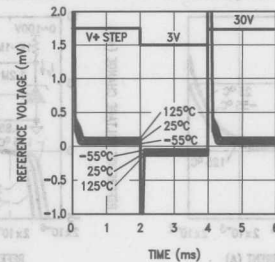
Reference Voltage with 100 ~ 12 μ A Current Step



Reference Step Response for 100 μ A ~ 10 mA Current Step



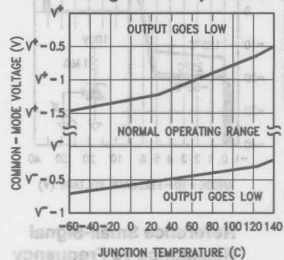
Reference Voltage Change with Supply Voltage Step



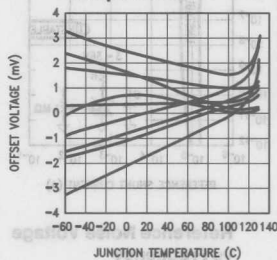
Typical Performance Characteristics (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

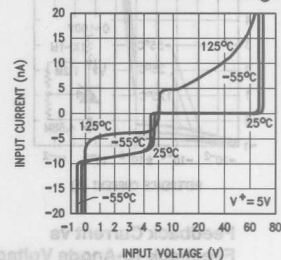
Input Common-Mode Voltage Range vs Temperature



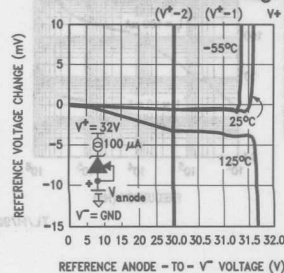
V_{OS} vs Junction Temperature



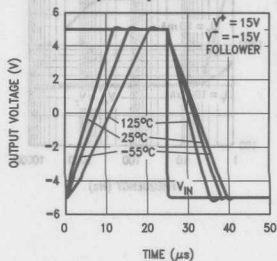
Input Bias Current vs Common-Mode Voltage



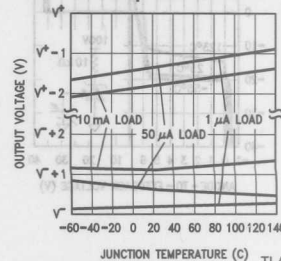
Reference Change vs Common-Mode Voltage



Large-Signal Step Response



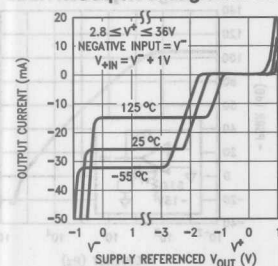
Output Voltage Swing vs Temp. and Current



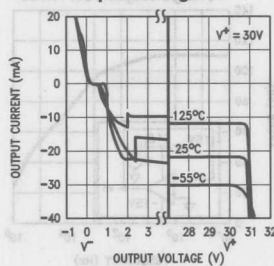
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

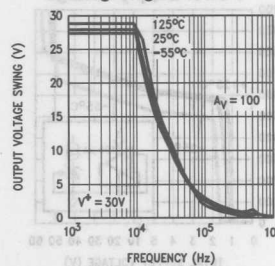
Output Source Current vs Output Voltage and Temp.



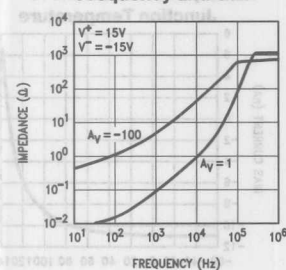
Output Sink Current vs Output Voltage



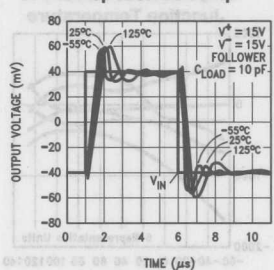
Output Swing, Large Signal



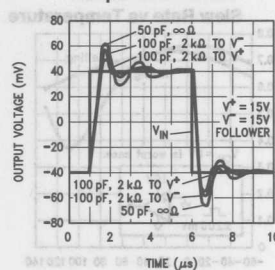
Output Impedance vs Frequency and Gain



Small Signal Pulse Response vs Temp.

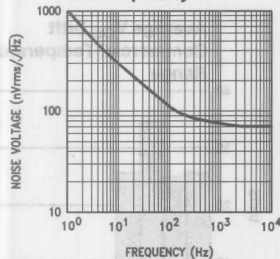


Small-Signal Pulse Response vs Load

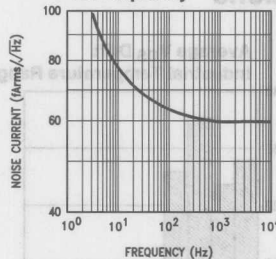


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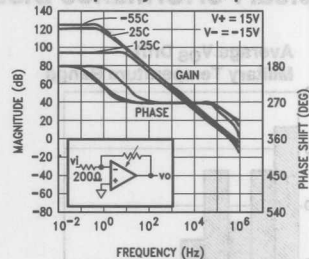
Op Amp Voltage Noise vs Frequency



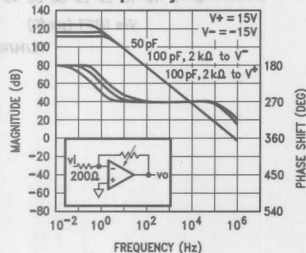
Op Amp Current Noise vs Frequency



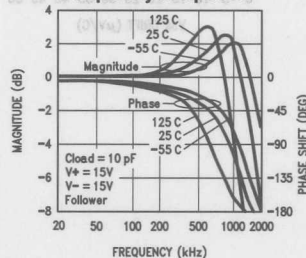
Small-Signal Voltage Gain vs Frequency and Temperature



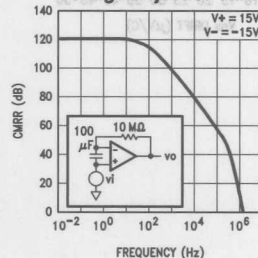
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

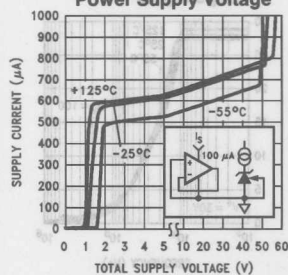


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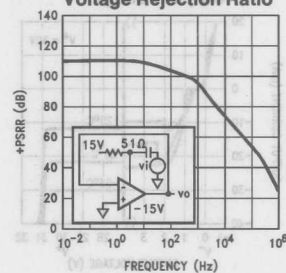
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

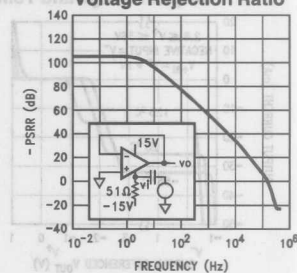
Power Supply Current vs Power Supply Voltage



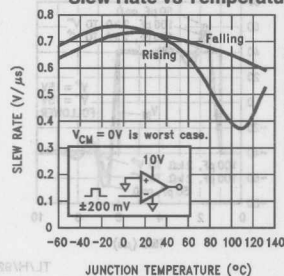
Positive Power Supply Voltage Rejection Ratio



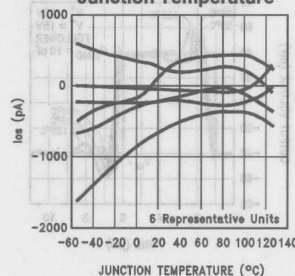
Negative Power Supply Voltage Rejection Ratio



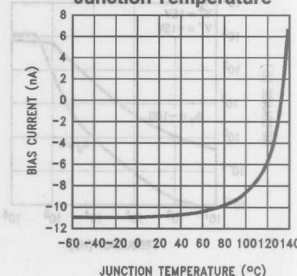
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature

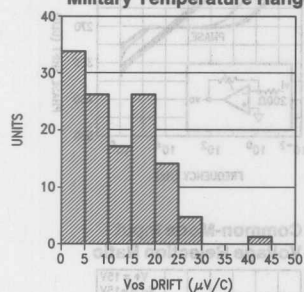


Input Bias Current vs Junction Temperature

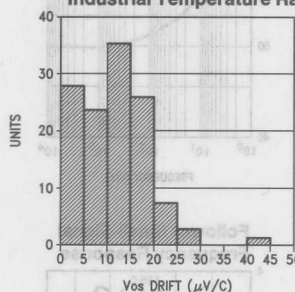


Typical Performance Distributions

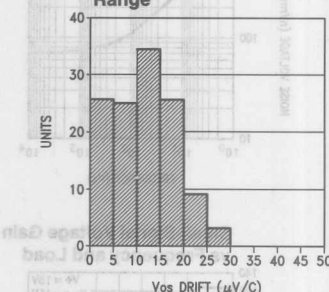
Average V_{OS} Drift Military Temperature Range



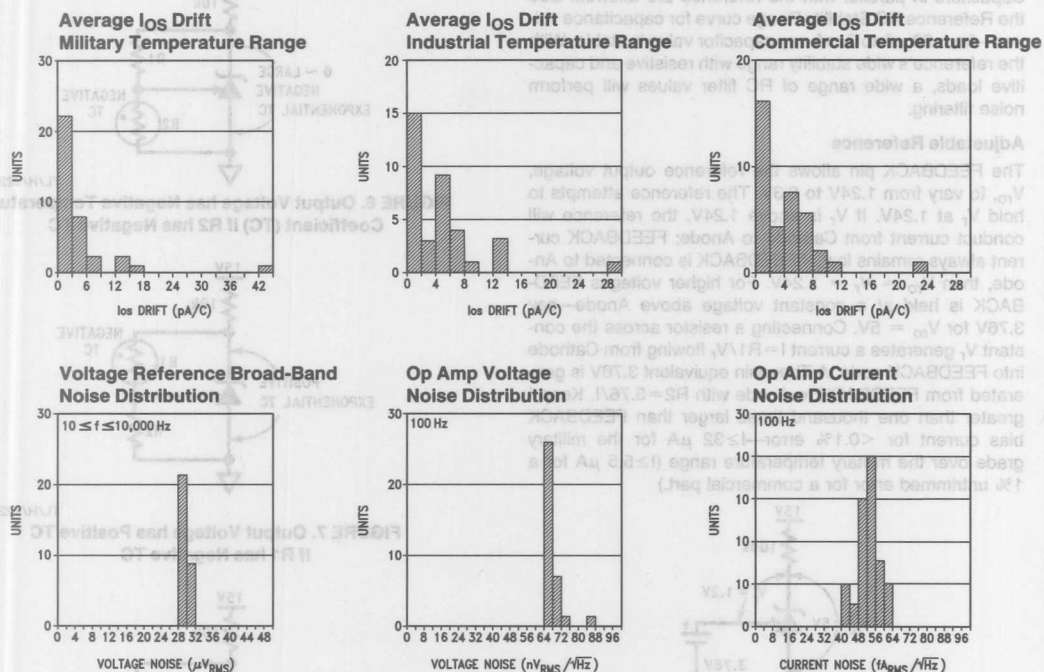
Average V_{OS} Drift Industrial Temperature Range



Average V_{OS} Drift Commercial Temperature Range



Typical Performance Distributions (Continued)



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Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

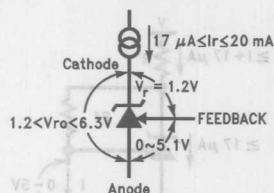


FIGURE 1. Voltages Associated with Reference
(Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the refer-

ence voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r .

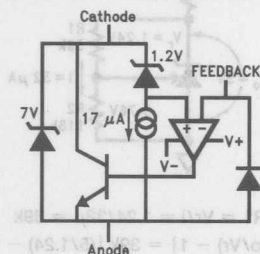


FIGURE 2. Reference Equivalent Circuit

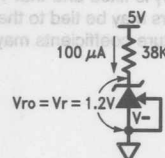


FIGURE 3. 1.2V Reference

the Reference AC Stability Range curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24\text{V}$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5\text{V}$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error— $I \geq 32\text{ }\mu\text{A}$ for the military grade over the military temperature range ($I \geq 5.5\text{ }\mu\text{A}$ for a 1% untrimmed error for a commercial part.)

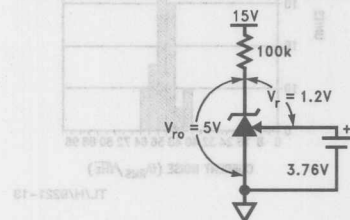
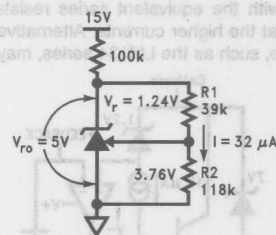


FIGURE 4. Thevenin Equivalent of Reference with 5V Output



$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1 \{ (Vro/Vr) - 1 \} = 39k \{ (5/1.24) - 1 \} = 118k$$

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

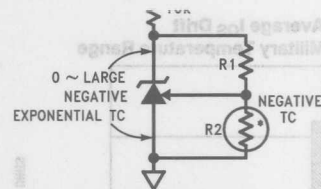


FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

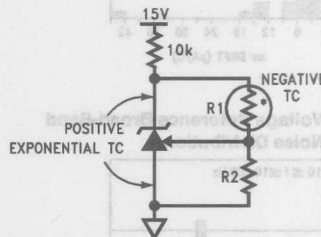


FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

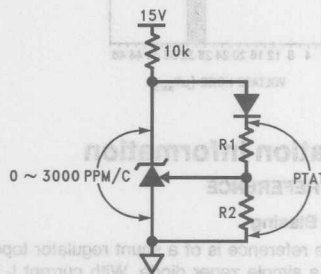


FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.

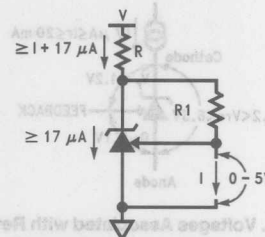


FIGURE 9. Current Source is Programmed by R1

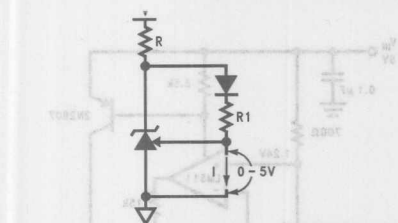


FIGURE 10. Proportional-to-Absolute-Temperature Current Source

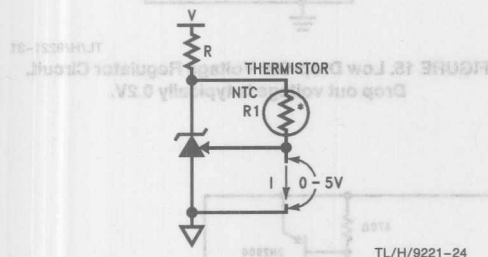


FIGURE 11. Negative -TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

- 1) Output Swing: Unloaded, the $42\ \mu\text{A}$ pull-down will bring the output within $300\ \text{mV}$ of V^- over the military temperature range. If more than $42\ \mu\text{A}$ is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ , at the cost of poorer sinking open-loop voltage gain.

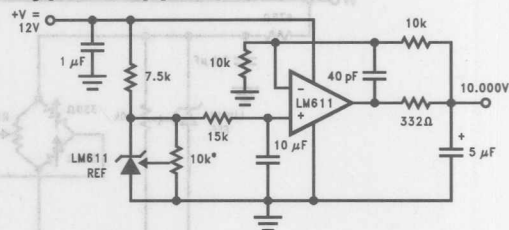
distortion (a $1\ V_{BE}$ deadband versus $3\ V_{BE}$ for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.

- 3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting $1\ \text{mA}$ or more reduces the output stage NPN r_e until the output resistance is that of the current limit $25\ \Omega$. $200\ \text{pF}$ may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



*10k must be low t.c. trim pot.

FIGURE 12. Ultra Low Noise 10.00V Reference.
Total Output Noise is Typically $14\ \mu\text{VRMS}$.
Adjust the 10k pot for 10.000V.

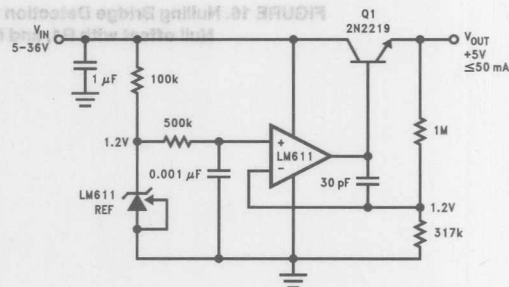
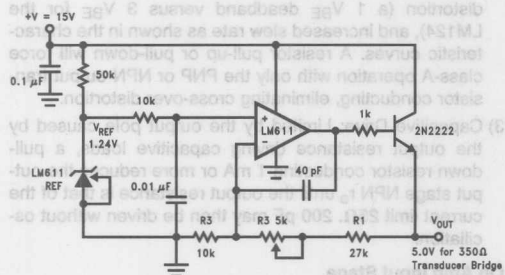


FIGURE 13. Simple Low Quiescent Drain Voltage Regulator. Total Supply Current is approximately $320\ \mu\text{A}$ when $V_{IN} = 5\text{V}$, and output has no load.

Typical Applications (Continued)



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$V_{OUT} = (R_1/R_2 + 1) V_{REF}$
 R1, R2 should be 1% metal film.
 R3 should be low t.c. trim pot.

FIGURE 14. Slow Rise-Time Upon Power-Up, Adjustable Transducer Bridge Driver.
 Rise-time is approximately 0.5 ms.

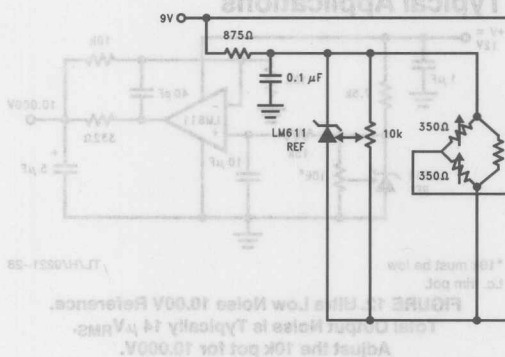
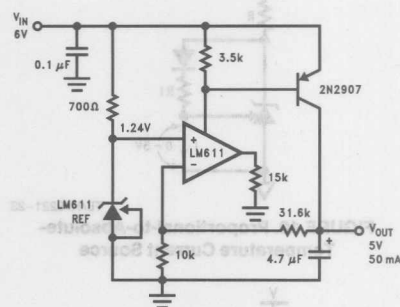


FIGURE 16. Nulling Bridge Detection System. Adjust sensitivity via 400 kΩ pot.
 Null offset with R1, and bridge drive with the 10k pot.

Application Information (Continued)



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FIGURE 15. Low Drop-Out Voltage Regulator Circuit.
 Drop out voltage is typically 0.2V.

Op Amp Output Stages
 The op amp, like the LM124 series, has a flexible and relatively wide-swinging output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability.
 (1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV to V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ at the cost of poorer sinking open-loop voltage gain.



LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current (Op Amp) 300 μ A
- Wide supply voltage range 4V to 36V
- Wide common-mode range V_{-} to $(V_{+} - 1.8V)$
- Wide differential input voltage $\pm 36V$
- Available in plastic package rated for Military Temp. Range Operation

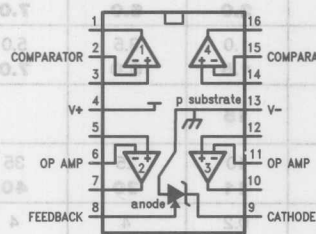
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available $\pm 0.6\%$
- Wide operating current range 17 μ A to 20 mA
- Tolerant of load capacitance

Applications

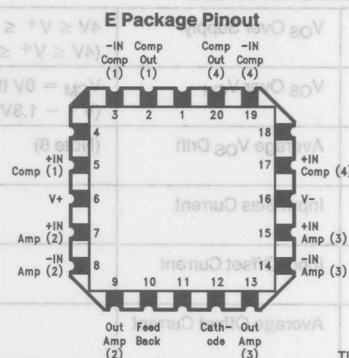
- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



Top View

TL/H/9226-1



E Package Pinout

TL/H/9226-48

Ordering Information

| Reference Tolerance & V_{OS} | Temperature Range | | | Package | NSC Drawing |
|--|--|---|---|------------------------------|----------------|
| | Military $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | Industrial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ | Commercial $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | | |
| $\pm 0.6\%$ 80 ppm/ $^{\circ}\text{C}$ Max. $V_{OS} \leq 3.5 \text{ mV}$ | LM613AMN | LM613AIN | — | 16-Pin Molded DIP | N16E |
| | LM613AMJ/883 (Note 14) | — | — | 16-Pin Ceramic DIP | J16A |
| | LM613AME/883 (Note 14) | — | — | 20-Pin LCC | E20A |
| $\pm 2.0\%$ 150 ppm/ $^{\circ}\text{C}$ Max. $V_{OS} \leq 5.0 \text{ mV}$ Max. | LM613MN | LM613IN | LM613CN | 16-Pin Molded DIP | N16E |
| | — | LM613IWM | — | 16-Pin Wide Surface Mount | M16B |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--|
| Voltage on Any Pin Except V_R (referred to V^- pin) | |
| (Note 2) | 36V (Max) |
| (Note 3) | -0.3V (Min) |
| Current through Any Input Pin & V_R Pin | ± 20 mA |
| Differential Input Voltage | |
| Military and Industrial | ± 36 V |
| Commercial | ± 32 V |
| Storage Temperature Range | $-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ |
| Maximum Junction Temperature (Note 4) | 150°C |

Thermal Resistance, Junction-to-Ambient (Note 5)

| | |
|------------|---------|
| N Package | 100°C/W |
| WM Package | 150°C/W |

Soldering Information (10 Seconds)

| | |
|------------|-------|
| N Package | 260°C |
| WM Package | 220°C |

ESD Tolerance (Note 6)

± 1 kV

Operating Temperature Range

| | |
|------------------|---|
| LM613AI, LM613BI | -40°C to $+85^\circ\text{C}$ |
| LM613AM, LM613M | -55°C to $+125^\circ\text{C}$ |
| LM613C | $0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$ |

Electrical Characteristics These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM613AM LM613AI Limits (Note 8) | LM613M LM613I LM613C Limits (Note 8) | Units |
|--------|----------------------|---|---------------------|--|--|--|
| I_S | Total Supply Current | $R_{\text{LOAD}} = \infty$, $4\text{V} \leq V^+ \leq 36\text{V}$ (32V for LM613C) | 450 550 | 940 1000 | 1000 1070 | μA (Max) μA (Max) |
| V_S | Supply Voltage Range | | 2.2 2.9 | 2.8 3 | 2.8 3 | V (Min) V (Min) |
| | | | 46 43 | 36 36 | 32 32 | V (Max) V (Max) |

OPERATIONAL AMPLIFIERS

| | | | | | | |
|-----------------------------------|--------------------------------------|--|-------------------|-------------------|-------------------|---------------------------------------|
| V_{OS1} | V_{OS} Over Supply | $4\text{V} \leq V^+ \leq 36\text{V}$ ($4\text{V} \leq V^+ \leq 32\text{V}$ for LM613C) | 1.5 2.0 | 3.5 6.0 | 5.0 7.0 | mV (Max) mV (Max) |
| V_{OS2} | V_{OS} Over V_{CM} | $V_{\text{CM}} = 0\text{V}$ through $V_{\text{CM}} =$ ($V^+ - 1.8\text{V}$), $V^+ = 30\text{V}$, $V^- = 0\text{V}$ | 1.0 1.5 | 3.5 6.0 | 5.0 7.0 | mV (Max) mV (Max) |
| $\frac{V_{\text{OS3}}}{\Delta T}$ | Average V_{OS} Drift | (Note 8) | 15 | | | $\mu\text{V}/^\circ\text{C}$ (Max) |
| I_B | Input Bias Current | | 10 11 | 25 30 | 35 40 | nA (Max) nA (Max) |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA (Max) nA (Max) |
| $\frac{I_{\text{OS1}}}{\Delta T}$ | Average Offset Current | | 4 | | | pA/ $^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 1000 | | | M Ω |
| C_{IN} | Input Capacitance | Common-Mode | 6 | | | pF |
| e_n | Voltage Noise | $f = 100\text{ Hz}$, Input Referred | 74 | | | nV/ $\sqrt{\text{Hz}}$ |
| I_n | Current Noise | $f = 100\text{ Hz}$, Input Referred | 58 | | | fA/ $\sqrt{\text{Hz}}$ |
| CMRR | Common-Mode Rejection Ratio | $V^+ = 30\text{V}$, $0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$ CMRR = $20 \log (\Delta V_{\text{CM}} / \Delta V_{\text{OS}})$ | 95 90 | 80 75 | 75 70 | dB (Min) dB (Min) |
| PSRR | Power Supply Rejection Ratio | $4\text{V} \leq V^+ \leq 30\text{V}$, $V_{\text{CM}} = V^+ / 2$, PSRR = $20 \log (\Delta V^+ / V_{\text{OS}})$ | 110 100 | 80 75 | 75 70 | dB (Min) dB (Min) |
| A_v | Open Loop Voltage Gain | $R_L = 10\text{ k}\Omega$ to GND, $V^+ = 30\text{V}$, $5\text{V} \leq V_{\text{OUT}} \leq 25\text{V}$ | 500 50 | 100 40 | 94 40 | V/mV (Min) |

Electrical Characteristics These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in boldface type apply over Operating Temperature Range. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 7) | LM613AM LM613AI Limits (Note 8) | LM613M LM613I Limits (Note 8) | Units |
|---|------------------------------|---|--|--|---|------------------------------------|
| OPERATIONAL AMPLIFIERS (Continued) | | | | | | |
| SR | Slew Rate | $V^+ = 30\text{V}$ (Note 9) | 0.70 0.65 | 0.55 0.45 | 0.50 0.45 | $\text{V}/\mu\text{s}$ |
| GBW | Gain Bandwidth | $C_L = 50\text{ pF}$ | 0.8 0.5 | | | MHz |
| V_{O1} | Output Voltage Swing High | $R_L = 10\text{ k}\Omega$ to GND, $V^+ = 36\text{V}$ (32V for LM613C) | $V^+ - 1.4$ $V^+ - 1.6$ | $V^+ - 1.7$ $V^+ - 1.9$ | $V^+ - 1.8$ $V^+ - 1.9$ | V (Min) |
| V_{O2} | Output Voltage Swing Low | $R_L = 10\text{ k}\Omega$ to V^+ , $V^+ = 36\text{V}$ (32V for LM613C) | $V^- + 0.8$ $V^- + 0.9$ | $V^- + 0.9$ $V^- + 1.0$ | $V^- + 0.95$ $V^- + 1.0$ | V (Max) |
| I_{OUT} | Output Source Current | $V_{\text{OUT}} = 2.5\text{V}$, $V^+_{\text{IN}} = 0\text{V}$, $V^-_{\text{IN}} = -0.3\text{V}$ | 25 15 | 20 13 | 16 13 | mA (Min) |
| I_{SINK} | Output Sink Current | $V_{\text{OUT}} = 1.6\text{V}$, $V^+_{\text{IN}} = 0\text{V}$, $V^-_{\text{IN}} = 0.3\text{V}$ | 17 9 | 14 8 | 13 8 | mA (Min) |
| I_{SHORT} | Short Circuit Current | $V_{\text{OUT}} = 0\text{V}$, $V^+_{\text{IN}} = 3\text{V}$, $V^-_{\text{IN}} = 2\text{V}$ | 30 40 | 50 60 | 50 60 | mA (Max) |
| | | $V_{\text{OUT}} = 5\text{V}$, $V^+_{\text{IN}} = 2\text{V}$, $V^-_{\text{IN}} = 3\text{V}$ | 30 32 | 60 80 | 70 90 | mA (Max) |
| COMPARATORS | | | | | | |
| V_{OS} | Offset Voltage | $4\text{V} \leq V^+ \leq 36\text{V}$ (32V for LM613C), $R_L = 15\text{ k}\Omega$ | 1.0 2.0 | 3.0 6.0 | 5.0 7.0 | mV (Max) |
| V_{OS} | Offset Voltage | $0\text{V} \leq V_{\text{CM}} \leq 36\text{V}$ | 1.0 | 3.0 | 5.0 | mV (Max) |
| V_{CM} | over V_{CM} | $V^+ = 36\text{V}$, (32V for LM613C) | 1.5 | 6.0 | 7.0 | mV (Max) |
| $\frac{V_{\text{OS}}}{\Delta T}$ | Average Offset Voltage Drift | | 15 | | | $\mu\text{V}/^\circ\text{C}$ (Max) |
| I_{B} | Input Bias Current | | 5 8 | 25 30 | 35 40 | nA (Max) |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA (Max) |
| A_V | Voltage Gain | $R_L = 10\text{ k}\Omega$ to 36V (32V for LM613C) $2\text{V} \leq V_{\text{OUT}} \leq 27\text{V}$ | 500 100 | | | V/mV |
| t_r | Large Signal Response Time | $V^+_{\text{IN}} = 1.4\text{V}$, $V^-_{\text{IN}} = \text{TTL Swing}$, $R_L = 5.1\text{ k}\Omega$ | 1.5 2.0 | | | μs |
| I_{SINK} | Output Sink Current | $V^+_{\text{IN}} = 0\text{V}$, $V^-_{\text{IN}} = 1\text{V}$, $V_{\text{OUT}} = 1.5\text{V}$ | 20 13 | 10 8 | 10 8 | mA (Min) |
| | | $V_{\text{OUT}} = 0.4\text{V}$ | 2.8 2.4 | 1.0 0.5 | 0.8 0.5 | mA (Min) |
| I_{LEAK} | Output Leakage Current | $V^+_{\text{IN}} = 1\text{V}$, $V^-_{\text{IN}} = 0\text{V}$, $V_{\text{OUT}} = 36\text{V}$ (32V for LM613C) | 0.1 0.2 | 10 | 10 | μA (Max) |

Electrical Characteristics These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 7) | LM613AM LM613AI Limits (Note 8) | LM613M LM613I LM613C Limits (Note 8) | Units |
|---|---|---|--------------------------|--|--|----------------------------------|
| VOLTAGE REFERENCE | | | | | | |
| V_{R} | Voltage Reference | (Note 10) | 1.244 | 1.2365 1.2515 ($\pm 0.6\%$) | 1.2191 1.2689 ($\pm 2\%$) | V (Min) V (Max) |
| $\frac{\Delta V_{\text{R}}}{\Delta T}$ | Average Temp. Drift | (Note 11) | 10 | 80 | 150 | ppm/ $^\circ\text{C}$ (Max) |
| $\frac{\Delta V_{\text{R}}}{\Delta T_{\text{J}}}$ | Hysteresis | (Note 12) | 3.2 | | | $\mu\text{V}/^\circ\text{C}$ |
| $\frac{\Delta V_{\text{R}}}{\Delta I_{\text{R}}}$ | V_{R} Change with Current | $V_{\text{R}}(100\text{ }\mu\text{A}) - V_{\text{R}}(17\text{ }\mu\text{A})$ | 0.05 0.1 | 1 1.1 | 1 1.1 | mV (Max) mV (Max) |
| | | $V_{\text{R}}(10\text{ mA}) - V_{\text{R}}(100\text{ }\mu\text{A})$ (Note 13) | 1.5 2.0 | 5 5.5 | 5 5.5 | mV (Max) mV (Max) |
| R_{R} | Resistance | $\Delta V_{\text{R}}(10 \rightarrow 0.1\text{ mA})/9.9\text{ mA}$ $\Delta V_{\text{R}}(100 \rightarrow 17\text{ }\mu\text{A})/83\text{ }\mu\text{A}$ | 0.2 0.6 | 0.56 13 | 0.56 13 | Ω (Max) Ω (Max) |
| $\frac{V_{\text{R}}}{\Delta V_{\text{RO}}}$ | V_{R} Change with High V_{RO} | $V_{\text{R}}(V_{\text{RO}} = V_{\text{I}}) - V_{\text{R}}(V_{\text{RO}} = 6.3\text{V})$ (5.06V between Anode and FEEDBACK) | 2.5 2.8 | 7 10 | 7 10 | mV (Max) mV (Max) |
| $\frac{V_{\text{R}}}{\Delta V_{\text{I}}}$ | V_{R} Change with V_{ANODE} Change | $V_{\text{R}}(V^+ = 5\text{V}) - V_{\text{R}}(V^+ = 36\text{V})$ ($V^+ = 32\text{V}$ for LM613C) | 0.1 0.1 | 1.2 1.3 | 1.2 1.3 | mV (Max) mV (Max) |
| | | $V_{\text{R}}(V^+ = 5\text{V}) - V_{\text{R}}(V^+ = 3\text{V})$ | 0.01 0.01 | 1 1.5 | 1 1.5 | mV (Max) mV (Max) |
| I_{FB} | FEEDBACK Bias Current | $V_{\text{ANODE}} \leq V_{\text{FB}} \leq 5.06\text{V}$ | 22 29 | 35 40 | 50 55 | nA (Max) nA (Max) |
| e_{n} | V_{R} Noise | 10 Hz to 10 kHz, $V_{\text{RO}} = V_{\text{R}}$ | 30 | | | μV_{RMS} |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_{\text{J}} = T_{\text{A}} + P_{\text{D}} \theta_{\text{JA}}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is $90^\circ\text{C}/\text{W}$ for the N package, and $135^\circ\text{C}/\text{W}$ for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 7: Typical values in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 10: V_{R} is the Cathode-to-feedback voltage, nominally 1.244V.

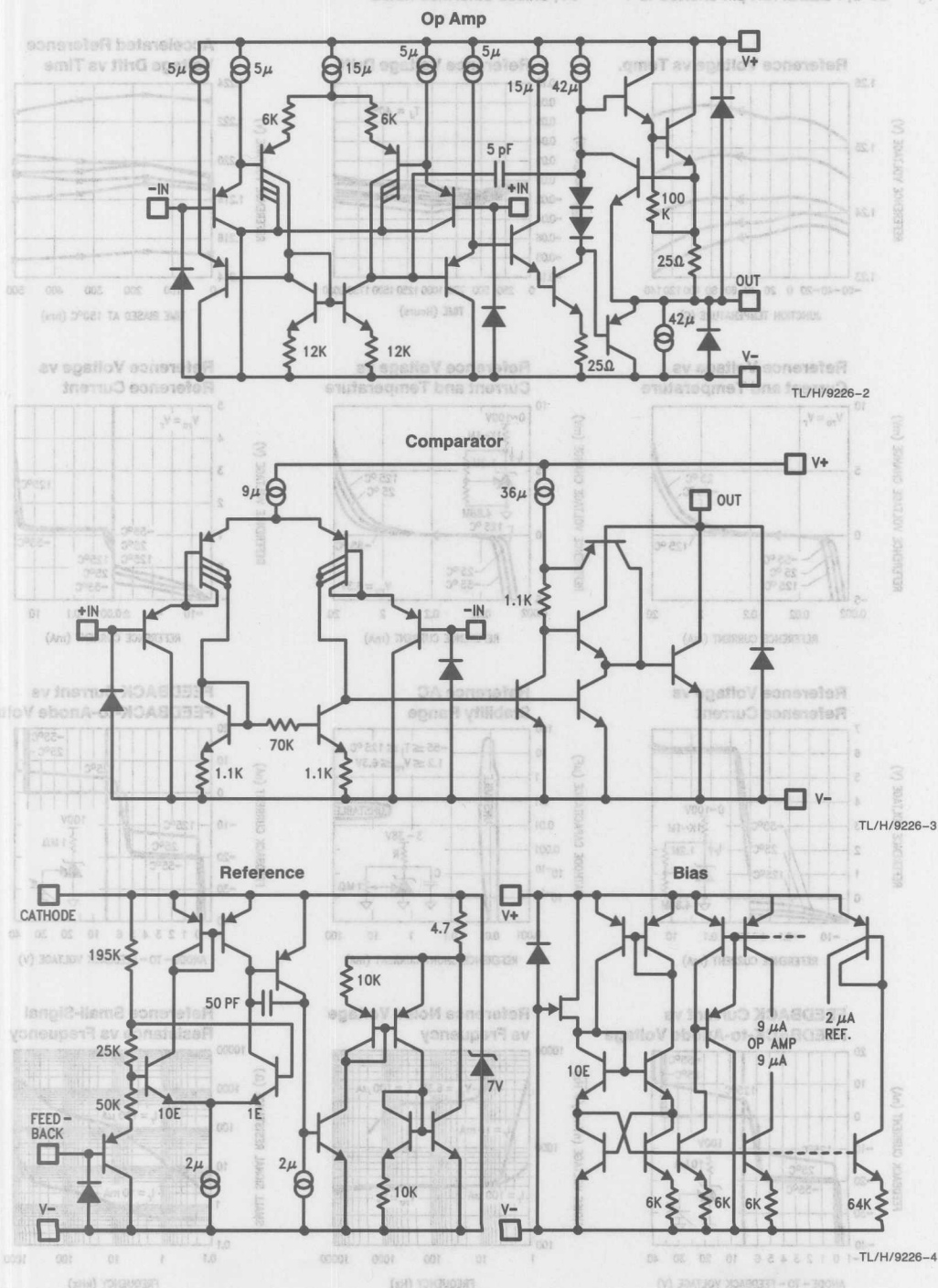
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \Delta V_{\text{R}} / (V_{\text{R}}[25^\circ\text{C}] \Delta T_{\text{J}})$, where ΔV_{R} is the lowest value subtracted from the highest, $V_{\text{R}}[25^\circ\text{C}]$ is the value at 25°C , and ΔT_{J} is the temperature range. This parameter is guaranteed by design and sample testing.

Note 12: Hysteresis is the change in V_{R} caused by a change in T_{J} , after the reference has been "dehysteresized". To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

Note 13: Low contact resistance is required for accurate measurement.

Note 14: A military RETS 613AMX electrical test specification is available on request. The Military screened parts can also be procured as a Standard Military Drawing.

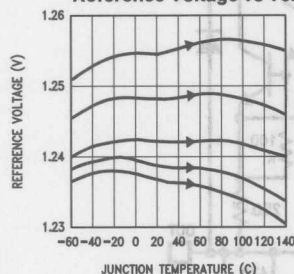
Simplified Schematic Diagrams



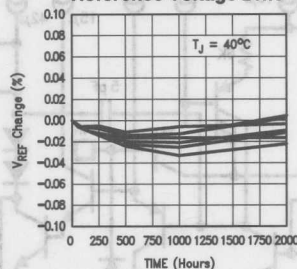
Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

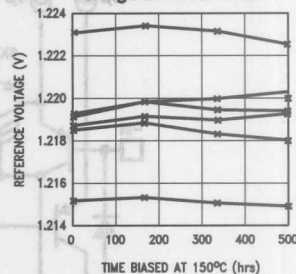
Reference Voltage vs Temp.



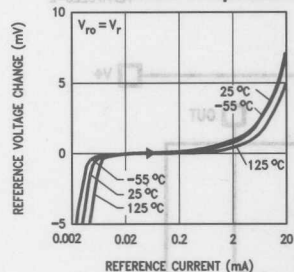
Reference Voltage Drift



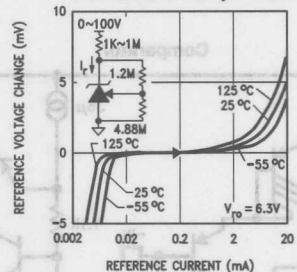
Accelerated Reference Voltage Drift vs Time



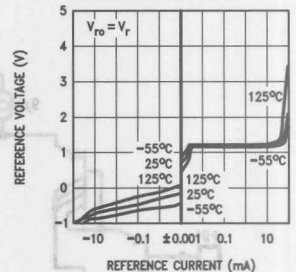
Reference Voltage vs Current and Temperature



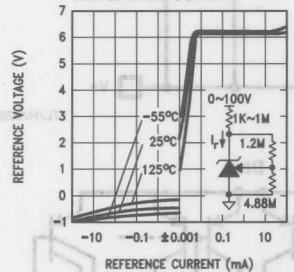
Reference Voltage vs Current and Temperature



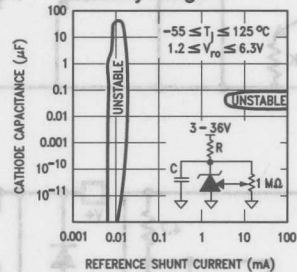
Reference Voltage vs Reference Current



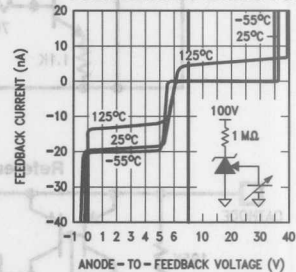
Reference Voltage vs Reference Current



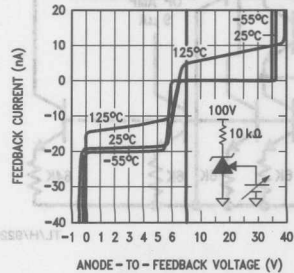
Reference AC Stability Range



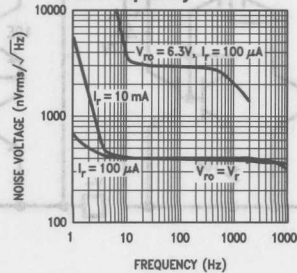
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



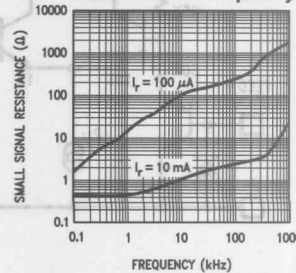
FEEDBACK Current vs FEEDBACK-to-Anode Voltage



Reference Noise Voltage vs Frequency



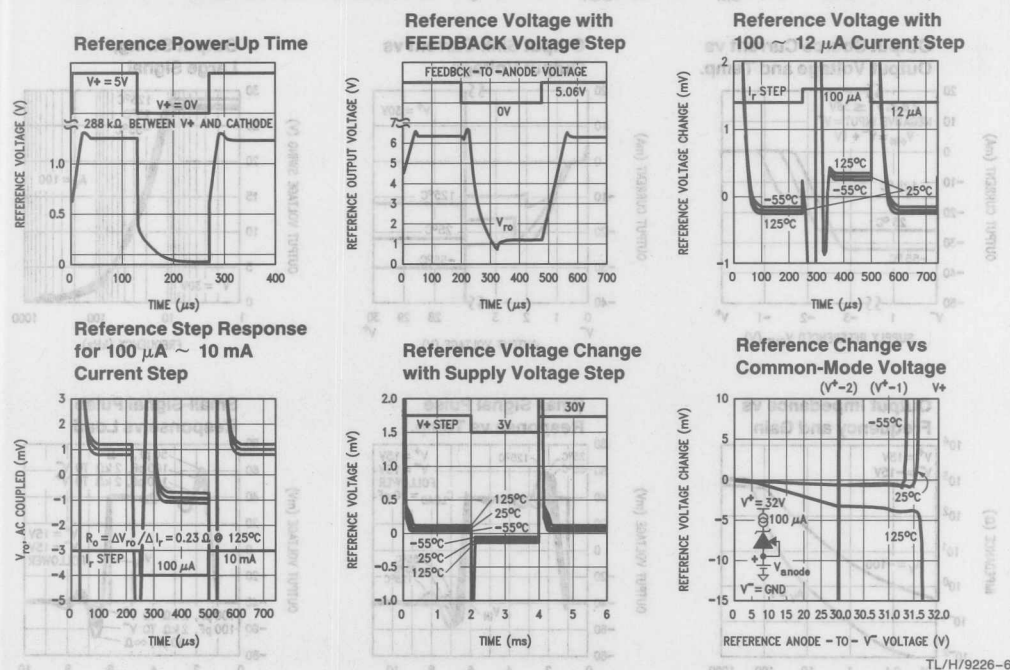
Reference Small-Signal Resistance vs Frequency



TL/H/9226-5

Typical Performance Characteristics (Reference) (Continued)

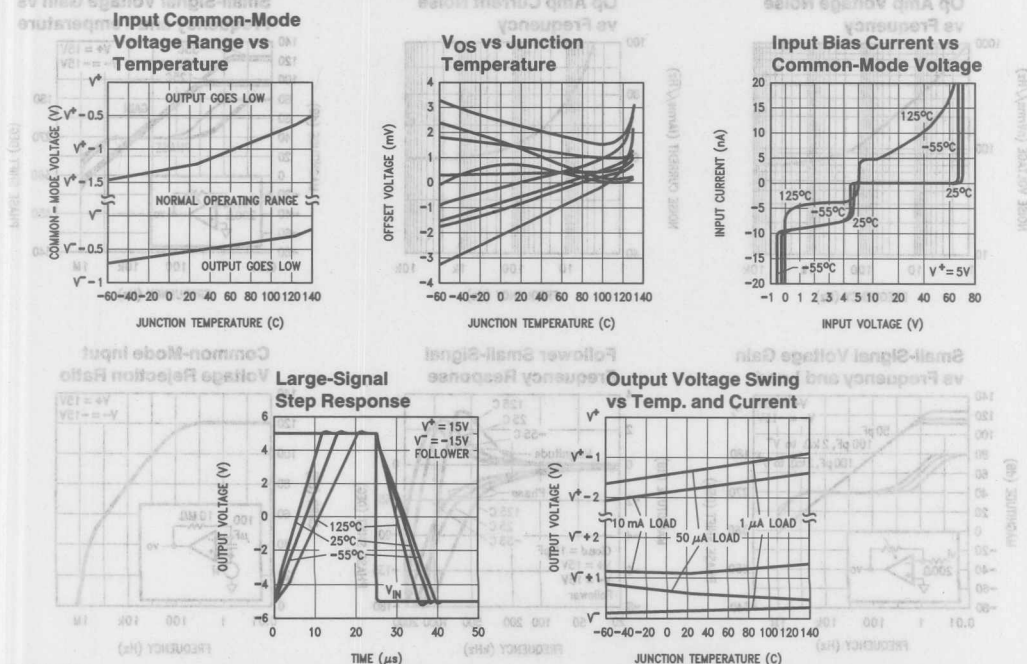
$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted



TL/H/9226-6

Typical Performance Characteristics (Op Amps)

$V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{CM} = V^+ / 2$, $V_{OUT} = V^+ / 2$, $T_J = 25^\circ\text{C}$, unless otherwise noted

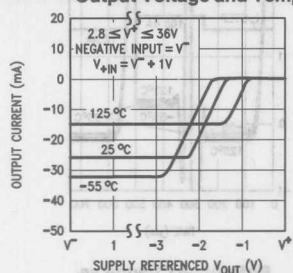


TL/H/9226-7

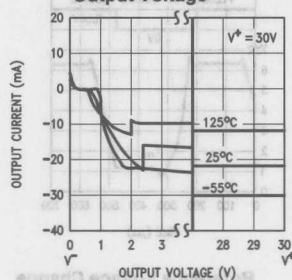
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

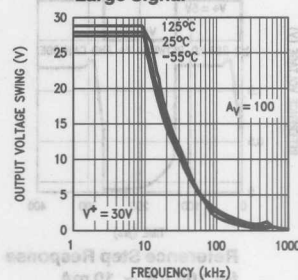
Output Source Current vs Output Voltage and Temp.



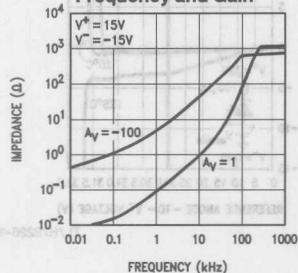
Output Sink Current vs Output Voltage



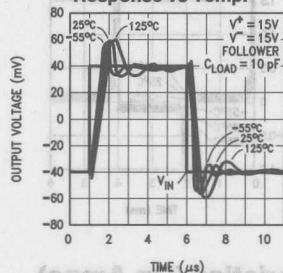
Output Swing, Large Signal



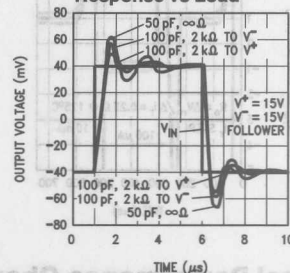
Output Impedance vs Frequency and Gain



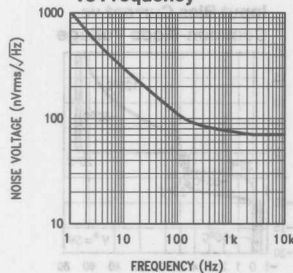
Small Signal Pulse Response vs Temp.



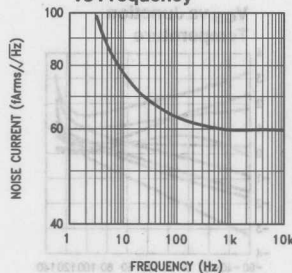
Small-Signal Pulse Response vs Load



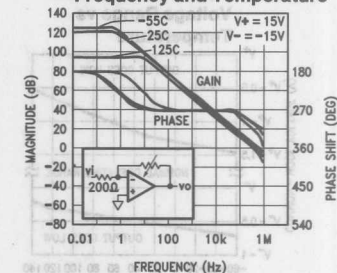
Op Amp Voltage Noise vs Frequency



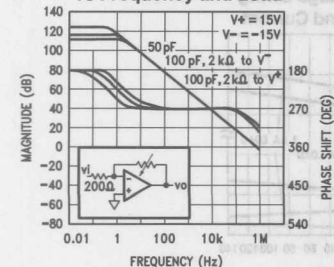
Op Amp Current Noise vs Frequency



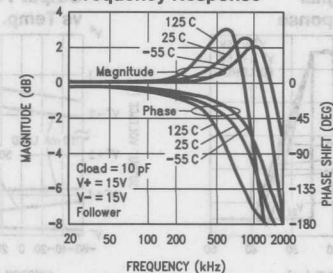
Small-Signal Voltage Gain vs Frequency and Temperature



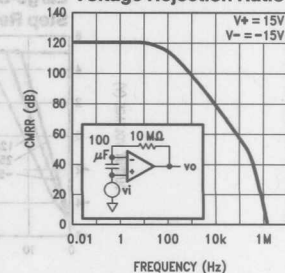
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



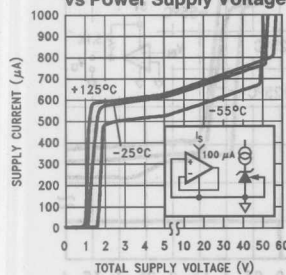
Common-Mode Input Voltage Rejection Ratio



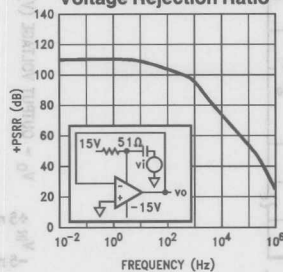
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

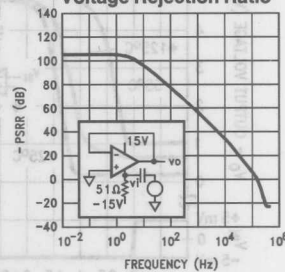
Power Supply Current vs Power Supply Voltage



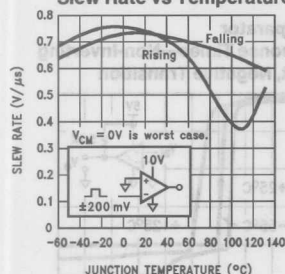
Positive Power Supply Voltage Rejection Ratio



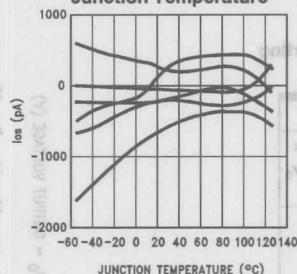
Negative Power Supply Voltage Rejection Ratio



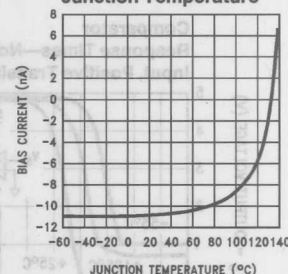
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



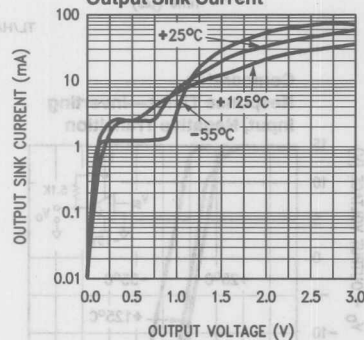
Input Bias Current vs Junction Temperature



TL/H/9226-9

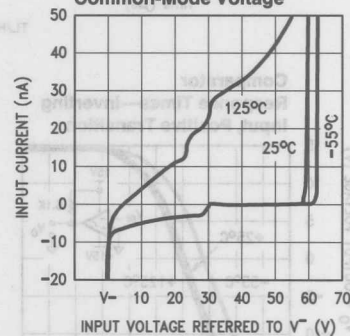
Typical Performance Characteristics (Comparators)

Output Sink Current



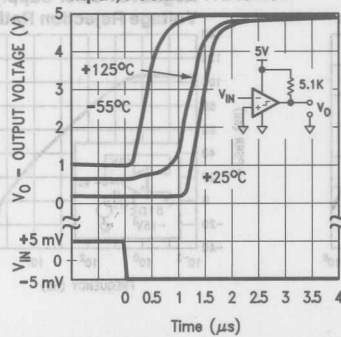
TL/H/9226-10

Input Bias Current vs Common-Mode Voltage



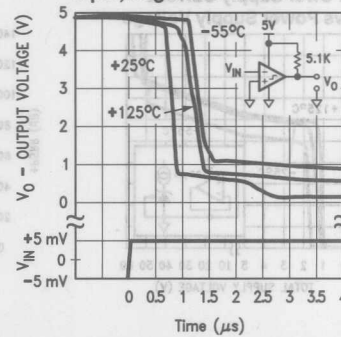
TL/H/9226-11

**Comparator
Response Times—Inverting
Input, Positive Transition**



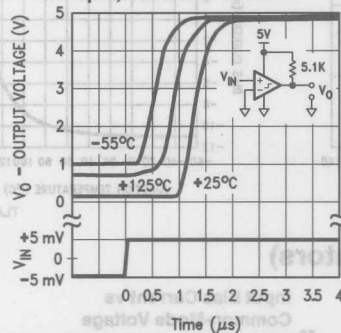
TL/H/9226-12

**Comparator
Response Times—Inverting
Input, Negative Transition**



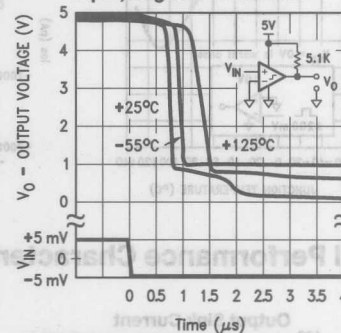
TL/H/9226-13

**Comparator
Response Times—Non-Inverting
Input, Positive Transition**



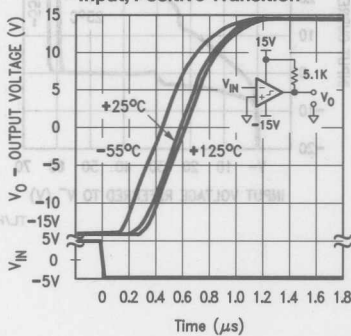
TL/H/9226-14

**Comparator
Response Times—Non-Inverting
Input, Negative Transition**



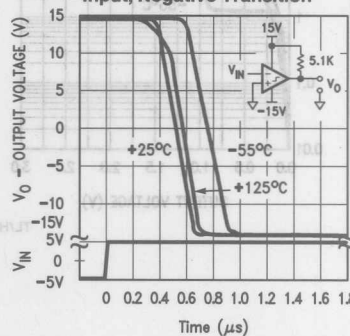
TL/H/9226-15

**Comparator
Response Times—Inverting
Input, Positive Transition**



TL/H/9226-16

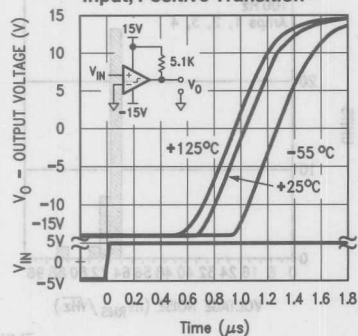
**Comparator
Response Times—Inverting
Input, Negative Transition**



TL/H/9226-17

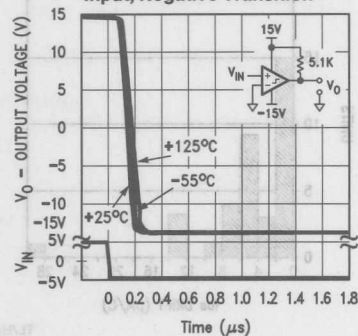
Typical Performance Characteristics (Comparators) (Continued)

Comparator
Response Times—Non-Inverting
Input, Positive Transition



TL/H/9226-18

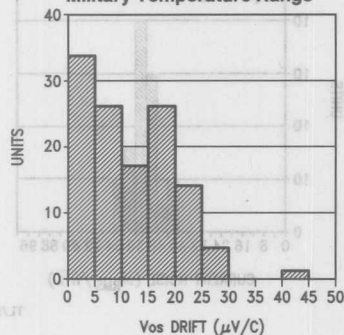
Comparator
Response Times—Non-Inverting
Input, Negative Transition



TL/H/9226-19

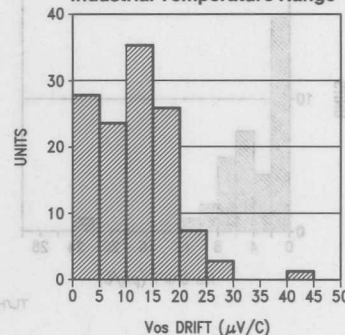
Typical Performance Distributions

Average V_{OS} Drift
Military Temperature Range



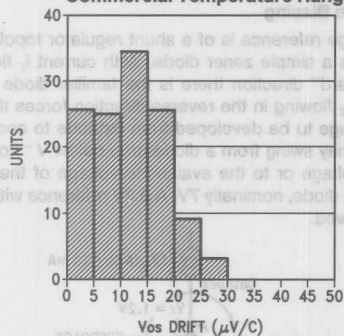
TL/H/9226-20

Average V_{OS} Drift
Industrial Temperature Range



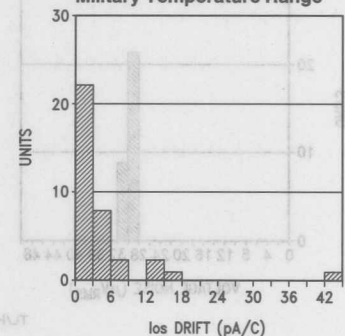
TL/H/9226-21

Average V_{OS} Drift
Commercial Temperature Range



TL/H/9226-22

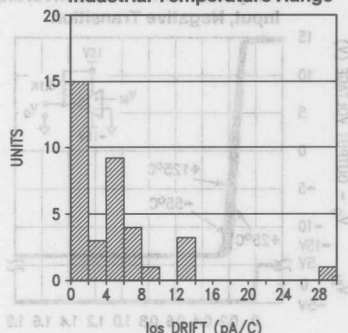
Average I_{OS} Drift
Military Temperature Range



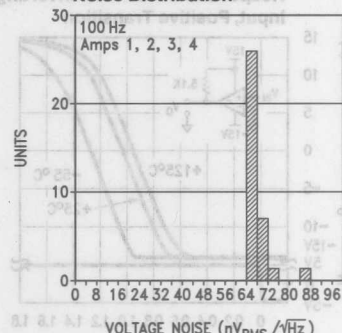
TL/H/9226-23

Typical Performance Distributions (Continued)

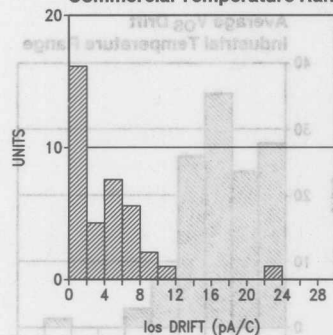
Average I_{OS} Drift
Industrial Temperature Range



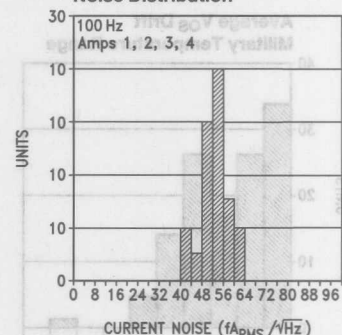
Op Amp Voltage
Noise Distribution



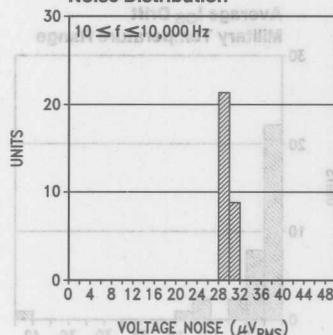
Average I_{OS} Drift
Commercial Temperature Range



Op Amp Current
Noise Distribution



Voltage Reference Broad-Band
Noise Distribution



Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

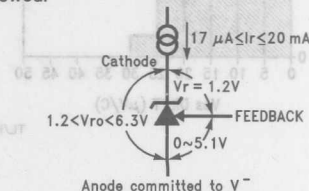


FIGURE 1. Voltage Associated with Reference
(current source I_r is external)

the constant 1.2V by feedback, and now the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r .

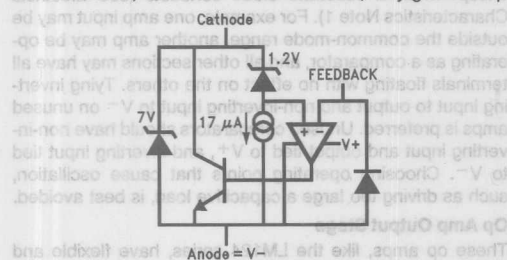


FIGURE 2. Reference Equivalent Circuit

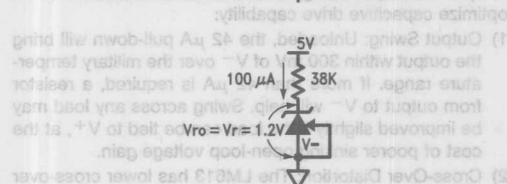


FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μ A to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for $<0.1\%$ error— $I \geq 32 \mu$ A for the military grade over the military temperature range ($I \geq 5.5 \mu$ A for a 1% untrimmed error for a commercial part).

Qp Amp and Comparator Input Stage

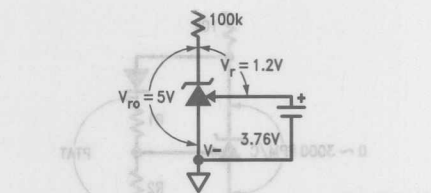


FIGURE 4. Thevenin Equivalent of Reference with 5V Output

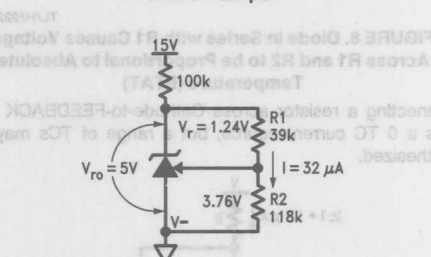


FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1 \{(Vro/Vr) - 1\} = 39k \{(5/1.24) - 1\} = 118k$$

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

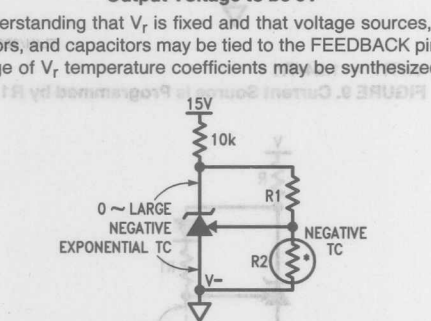


FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

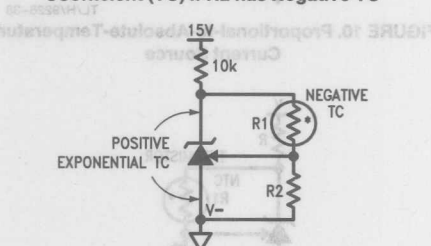
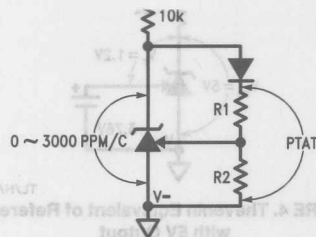


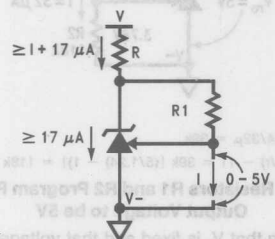
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9226-36

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

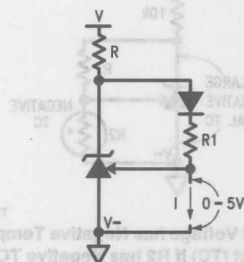
Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/9226-37

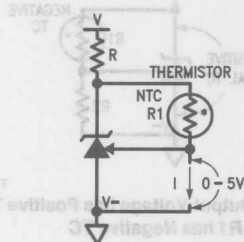
$$I = V_r/R1 = 1.24/R1$$

FIGURE 9. Current Source is Programmed by R1



TL/H/9226-38

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/9226-39

FIGURE 11. Negative-TC Current Source

tory of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+ , and inverting input tied to V^- . Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

- 1) Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ , at the cost of poorer sinking open-loop voltage gain.
- 2) Cross-Over Distortion: The LM613 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
- 3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_o until the output resistance is that of the current limit 25 Ω . 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than 30 μA . Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than 30 μA .

Op Amp and Comparator Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications

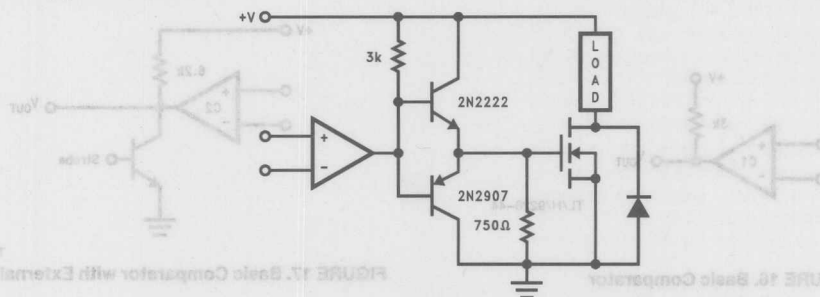


FIGURE 12. High Current, High Voltage Switch

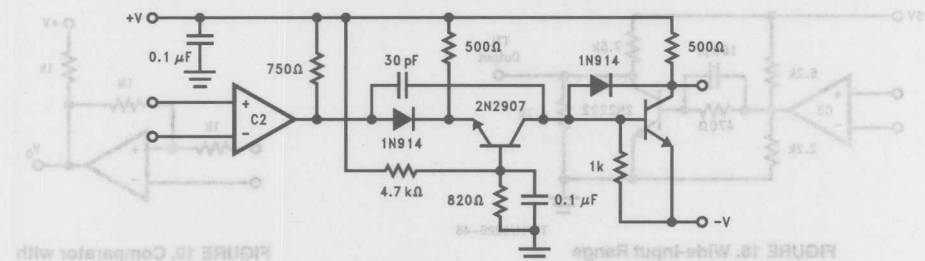


FIGURE 13. High Speed Level Shifter. Response time is approximately $1.5 \mu\text{s}$, where output is either approximately $+V$ or $-V$.

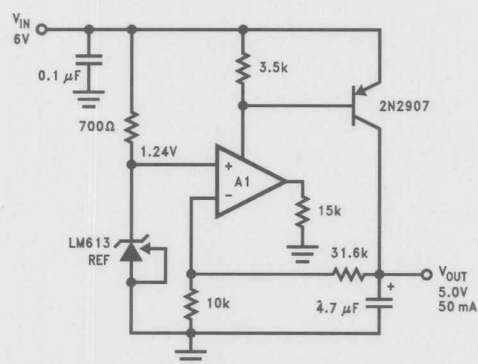
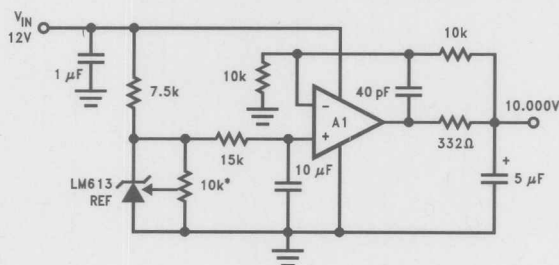


FIGURE 14. Low Voltage Regulator. Dropout voltage is approximately 0.2V.



*10k must be low
t.c. trimpot

Typical Applications (Continued)

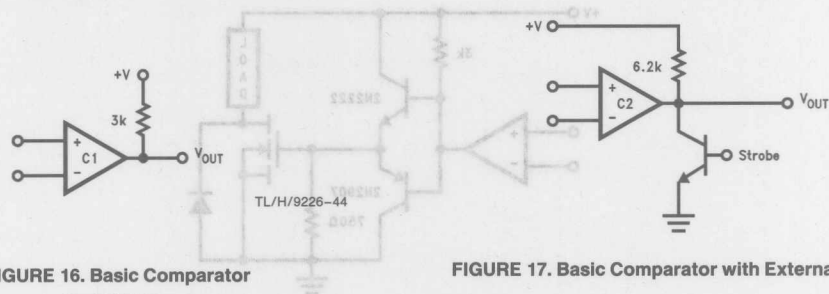
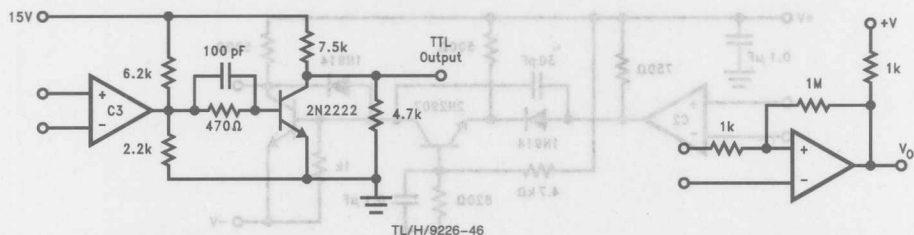


FIGURE 16. Basic Comparator

FIGURE 17. Basic Comparator with External Strobe

TL/H/9226-45

FIGURE 18. Wide-Input Range
Comparator with TTL OutputFIGURE 19. Comparator with
Hysteresis ($\Delta V_H = +V(1k/1M)$)

TL/H/9226-47

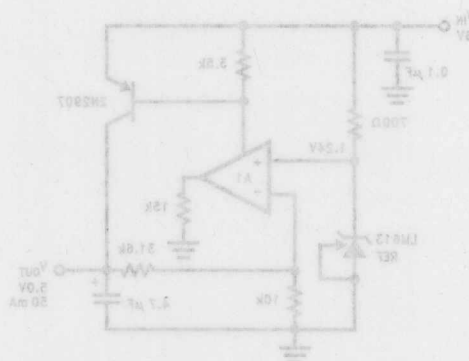
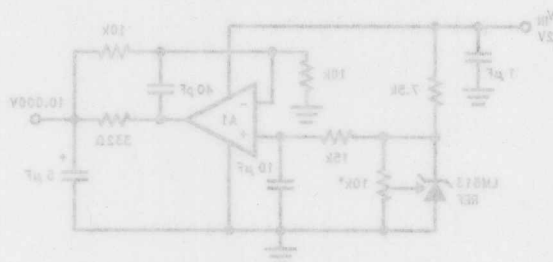


FIGURE 14. Low Voltage Regulator. Dropout voltage is approximately 0.5V.

FIGURE 15. Ultra Low Noise, 10.00V Reference. Total output noise is typically 14 μ Vrms.

LM614 Quad Operational Amplifier and Adjustable Reference

General Description

The LM614 consists of four op-amps and a programmable voltage reference in a 16-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with four wide output swing op-amps makes the LM614 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's new Super-Block™ family, the LM614 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

Op Amp

- Low operating current $300\mu A$
- Wide supply voltage range $4V$ to $36V$
- Wide common-mode range V^- to $(V^+ - 1.8V)$
- Wide differential input voltage $\pm 36V$
- Available in plastic package rated for Military Temperature Range Operation

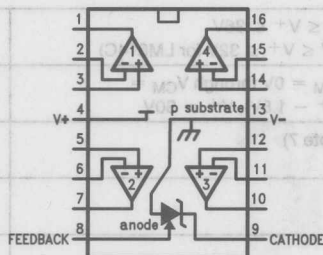
Reference

- Adjustable output voltage $1.2V$ to $6.3V$
- Tight initial tolerance available $\pm 0.6\%$
- Wide operating current range $17\mu A$ to $20mA$
- Tolerant of load capacitance

Applications

- Transducer bridge driver and signal processing
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagram



TL/H/9326-1

Ordering Information

| Reference Tolerance & V_{OS} | Temperature Range | | | Package | NSC Drawing |
|---|--|---|---|------------------------------|-------------|
| | Military $-55^\circ C \leq T_A \leq +125^\circ C$ | Industrial $-40^\circ C \leq T_A \leq +85^\circ C$ | Commercial $0^\circ C \leq T_A \leq +70^\circ C$ | | |
| $\pm 0.6\%$ 80 ppm/ $^\circ C$ max $V_{OS} \leq 3.5$ mV max | LM614AMN | LM614AIN | — | 16-pin Molded DIP | N16E |
| | LM614AMJ/883 (Note 13) | — | — | 16-pin Ceramic DIP | J16A |
| $\pm 2.0\%$ 150 ppm/ $^\circ C$ max $V_{OS} \leq 5.0$ mV | LM614MN | LM614BIN | LM614CN | 16-pin Molded DIP | N16E |
| | — | LM614WWM | LM614CWM | 16-pin Wide Surface Mount | M16B |

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pins except V_R

(referred to V^- pin)

(Note 2)

(Note 3)

36V (Max)

-0.3V (Min)

Current through Any Input Pin & V_R Pin

± 20 mA

Differential Input Voltage

Military and Industrial

± 36 V

Commercial

± 32 V

Storage Temperature Range

$-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$

Maximum Junction Temperature 150°C

Thermal Resistance, Junction-to-Ambient (Note 4)

N Package

100°C

WM Package

150°C

Soldering Information (Soldering, 10 seconds)

N Package

260°C

WM Package

220°C

ESD Tolerance (Note 5)

± 1 kV

Operating Temperature Range

LM614AI, LM614I, LM614BI $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$

LM614AM, LM614M $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

LM614C $0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$

Electrical Characteristics

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range.

| Symbol | Parameter | Conditions | Typical (Note 6) | LM614AM LM614AI Limits (Note 7) | LM614M LM614BI LM614I LM614C Limits (Note 7) | Units |
|-----------------------------------|--------------------------------------|--|---------------------|--|---|--|
| I_S | Total Supply Current | $R_{\text{LOAD}} = \infty$, $4\text{V} \leq V^+ \leq 36\text{V}$ (32V for LM614C) | 450 550 | 940 1000 | 1000 1070 | μA max μA max |
| V_S | Supply Voltage Range | | 2.2 2.9 | 2.8 3 | 2.8 3 | V min V min |
| | | | 46 43 | 36 36 | 32 32 | V max V max |
| OPERATIONAL AMPLIFIER | | | | | | |
| V_{OS1} | V_{OS} Over Supply | $4\text{V} \leq V^+ \leq 36\text{V}$ ($4\text{V} \leq V^+ \leq 32\text{V}$ for LM614C) | 1.5 2.0 | 3.5 6.0 | 5.0 7.0 | mV max mV max |
| V_{OS2} | V_{OS} Over V_{CM} | $V_{\text{CM}} = 0\text{V}$ through $V_{\text{CM}} =$ ($V^+ - 1.8\text{V}$), $V^+ = 30\text{V}$ | 1.0 1.5 | 3.5 6.0 | 5.0 7.0 | mV max mV max |
| $\frac{V_{\text{OS3}}}{\Delta T}$ | Average V_{OS} Drift | (Note 7) | 15 | | | $\mu\text{V}/^\circ\text{C}$ max |
| I_B | Input Bias Current | | 10 11 | 25 30 | 35 40 | nA max nA max |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA max nA max |
| $\frac{I_{\text{OS1}}}{\Delta T}$ | Average Offset Drift Current | | 4 | | | pA/ $^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 1800 | | | M Ω |
| | | Common-Mode | 3800 | | | M Ω |
| C_{IN} | Input Capacitance | Common-Mode Input | 5.7 | | | pF |
| e_n | Voltage Noise | $f = 100\text{ Hz}$, Input Referred | 74 | | | nV/ $\sqrt{\text{Hz}}$ |
| I_n | Current Noise | $f = 100\text{ Hz}$, Input Referred | 58 | | | fA/ $\sqrt{\text{Hz}}$ |
| CMRR | Common-Mode Rejection Ratio | $V^+ = 30\text{V}$, $0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$, CMRR = $20 \log (\Delta V_{\text{CM}} / \Delta V_{\text{OS}})$ | 95 90 | 80 75 | 75 70 | dB min dB min |
| PSRR | Power Supply Rejection Ratio | $4\text{V} \leq V^+ \leq 30\text{V}$, $V_{\text{CM}} = V^+ / 2$, PSRR = $20 \log (\Delta V^+ / \Delta V_{\text{OS}})$ | 110 100 | 80 75 | 75 70 | dB min dB min |
| A_V | Open Loop Voltage Gain | $R_L = 10\text{ k}\Omega$ to GND, $V^+ = 30\text{V}$, $5\text{V} \leq V_{\text{OUT}} \leq 25\text{V}$ | 500 50 | 100 40 | 94 40 | V/mV min |

Electrical Characteristics (Continued)

These specifications apply for $V_- = \text{GND} = 0\text{V}$, $V_+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range.

| Symbol | Parameter | Conditions | Typical (Note 6) | LM614AM LM614AI Limits (Note 8) | LM614M LM614BI LM614I LM614C Limits (Note 8) | Units |
|---|---|---|----------------------------|--|---|--------------------------------|
| SR | Slew Rate | $V^+ = 30\text{V}$ (Note 8) | ± 0.70 ± 0.65 | ± 0.55 ± 0.45 | ± 0.50 ± 0.45 | V/ μs |
| GBW | Gain Bandwidth | $C_L = 50\text{ pF}$ | 0.8 0.52 | | | MHz MHz |
| V_{O1} | Output Voltage Swing High | $R_L = 10\text{ k}\Omega$ to GND $V^+ = 36\text{V}$ (32V for LM614C) | $V^+ - 1.4$ $V^+ - 1.6$ | $V^+ - 1.7$ $V^+ - 1.9$ | $V^+ - 1.8$ $V^+ - 1.9$ | V min V min |
| V_{O2} | Output Voltage Swing Low | $R_L = 10\text{ k}\Omega$ to V^+ $V^+ = 36\text{V}$ (32V for LM614C) | $V^- + 0.8$ $V^- + 0.9$ | $V^- + 0.9$ $V^- + 1.0$ | $V^- + 0.95$ $V^- + 1.0$ | V max V max |
| I_{OUT} | Output Source | $V_{\text{OUT}} = 2.5\text{V}$, $V_{+ \text{IN}} = 0\text{V}$, $V_{- \text{IN}} = -0.3\text{V}$ | 25 15 | 20 13 | 16 13 | mA min mA min |
| I_{SINK} | Output Sink Current | $V_{\text{OUT}} = 1.6\text{V}$, $V_{+ \text{IN}} = 0\text{V}$, $V_{- \text{IN}} = 0.3\text{V}$ | 17 9 | 14 8 | 13 8 | mA min mA min |
| I_{SHORT} | Short Circuit Current | $V_{\text{OUT}} = 0\text{V}$, $V_{+ \text{IN}} = 3\text{V}$, $V_{- \text{IN}} = 2\text{V}$, Source | 30 40 | 50 60 | 50 60 | mA max mA max |
| | | $V_{\text{OUT}} = 5\text{V}$, $V_{+ \text{IN}} = 2\text{V}$, $V_{- \text{IN}} = 3\text{V}$, Sink | 30 32 | 60 80 | 70 90 | mA max mA max |
| VOLTAGE REFERENCE | | | | | | |
| V_R | Voltage Reference | (Note 9) | 1.244 | 1.2365 1.2515 ($\pm 0.6\%$) | 1.2191 1.2689 ($\pm 2.0\%$) | V min V max |
| $\frac{\Delta V_R}{\Delta T}$ | Average Temperature Drift | (Note 10) | 10 | 80 | 150 | PPM/ $^{\circ}\text{C}$ max |
| $\frac{\Delta V_R}{\Delta T_J}$ | Hysteresis | (Note 11) | 3.2 | | | $\mu\text{V}/^{\circ}\text{C}$ |
| $\frac{\Delta V_R}{\Delta I_R}$ | V_R Change with Current | $V_R(100\text{ }\mu\text{A}) - V_R(17\text{ }\mu\text{A})$ | 0.05 0.1 | 1 1.1 | 1 1.1 | mV max mV max |
| | | $V_R(10\text{ mA}) - V_R(100\text{ }\mu\text{A})$ (Note 12) | 1.5 2.0 | 5 5.5 | 5 5.5 | mV max mV max |
| R | Resistance | $\Delta V_R(10 \rightarrow 0.1\text{ mA})/9.9\text{ mA}$ $\Delta V_R(100 \rightarrow 17\text{ }\mu\text{A})/83\text{ }\mu\text{A}$ | 0.2 0.6 | 0.56 13 | 0.56 13 | Ω max Ω max |
| $\frac{\Delta V_R}{\Delta V_{\text{RO}}}$ | V_R Change with High V_{RO} | $V_R(V_{\text{RO}} = V_R) - V_R(V_{\text{RO}} = 6.3\text{V})$ (5.06V between Anode and FEEDBACK) | 2.5 2.8 | 7 10 | 7 10 | mV max mV max |
| $\frac{\Delta V_R}{\Delta V^+}$ | V_R Change with V^+ Change | $V_R(V^+ = 5\text{V}) - V_R(V^+ = 36\text{V})$ ($V^+ = 32\text{V}$ for LM614C) | 0.1 0.1 | 1.2 1.3 | 1.2 1.3 | mV max mV max |
| | | $V_R(V^+ = 5\text{V}) - V_R(V^+ = 3\text{V})$ | 0.01 0.01 | 1 1.5 | 1 1.5 | mV max mV max |
| I_{FB} | FEEDBACK Bias Current | $V_{\text{ANODE}} \leq V_{\text{FB}} \leq 5.06\text{V}$ | 22 29 | 35 40 | 50 55 | nA max nA max |
| e_n | Voltage Noise | BW = 10 Hz to 10 kHz, $V_{\text{RO}} = V_R$ | 30 | | | μV_{RMS} |

device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} are 90°C/W for the N package, WM package.

Note 5: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 6: Typical values in standard typeface are for $T_J = 25^\circ\text{C}$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 7: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 8: Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

Note 9: V_R is the Cathode-feedback voltage, nominally 1.244V.

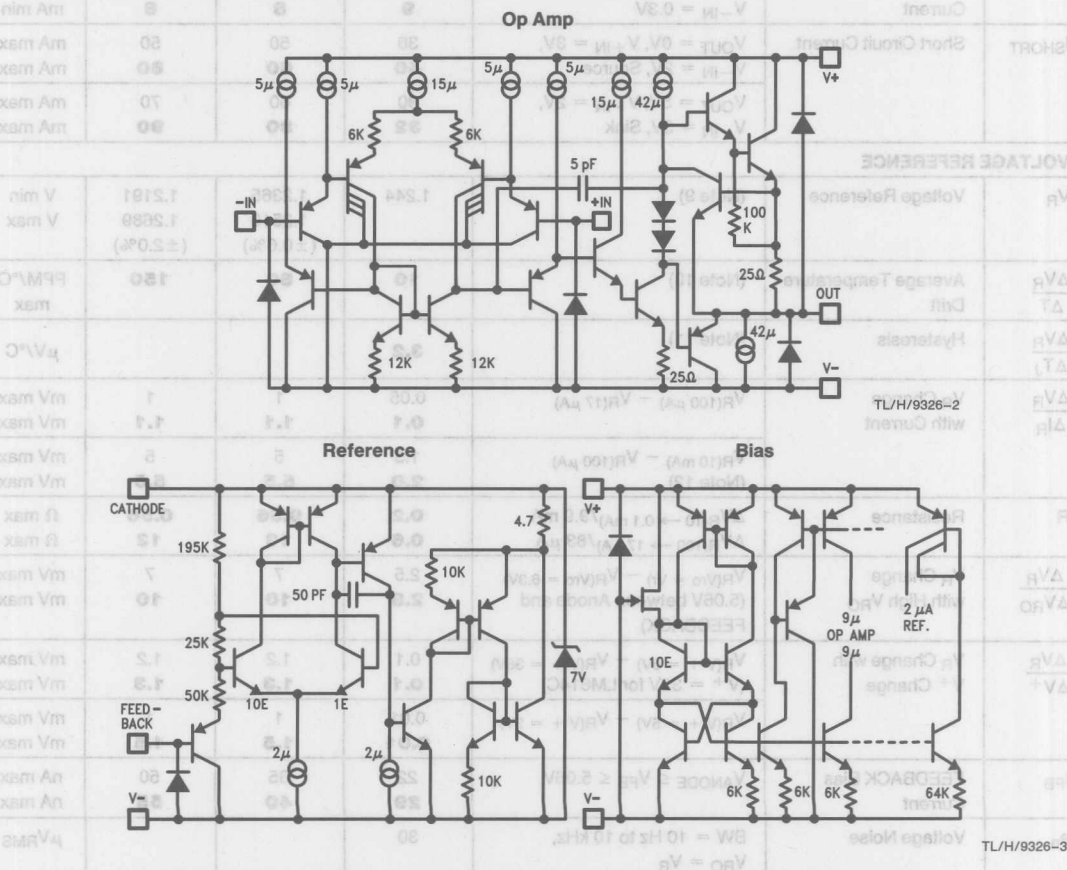
Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \Delta V_R / (V_R[25^\circ\text{C}] \cdot \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_R[25^\circ\text{C}]$ is the value at 25°C , and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 11: Hysteresis is the change in V_R caused by a change in T_J , after the reference has been "dehysteresized". To dehysteresize the reference, that is minimize the hysteresis to the typical value, cycle its junction temperature in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

Note 12: Low contact resistance is required for accurate measurement.

Note 13: A military RETSLM614AMX electrical test specification is available on request. The LM614AMJ/883 can also be procured as a Standard Military Drawing.

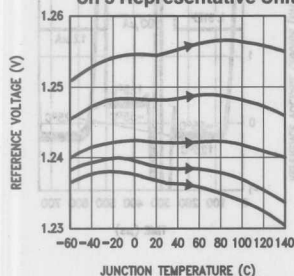
Simplified Schematic Diagrams



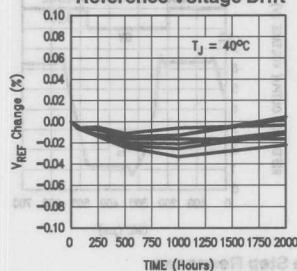
Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

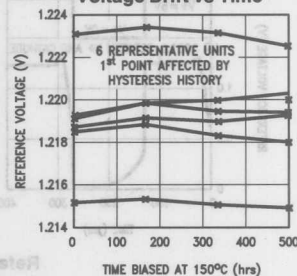
Reference Voltage
vs Temperature
on 5 Representative Units



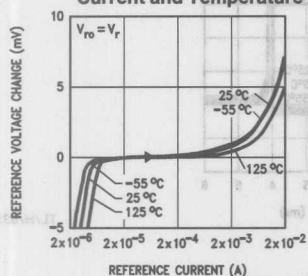
Reference Voltage Drift



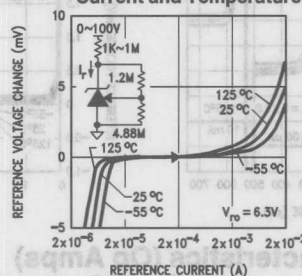
Accelerated Reference
Voltage Drift vs Time



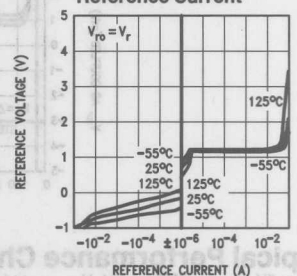
Reference Voltage vs
Current and Temperature



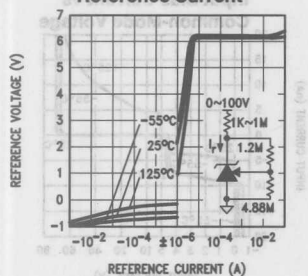
Reference Voltage vs
Current and Temperature



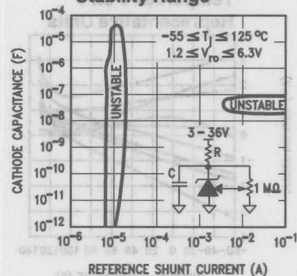
Reference Voltage vs
Reference Current



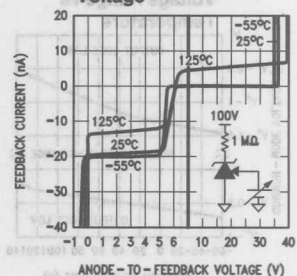
Reference Voltage vs
Reference Current



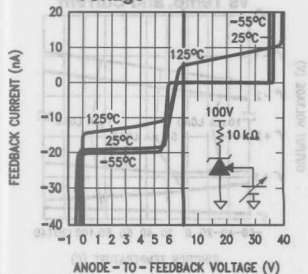
Reference AC
Stability Range



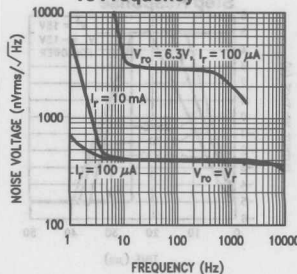
FEEDBACK Current vs
FEEDBACK-to-Anode
Voltage



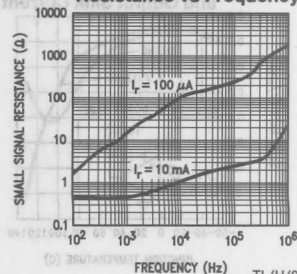
FEEDBACK Current vs
FEEDBACK-to-Anode
Voltage



Reference Noise Voltage
vs Frequency



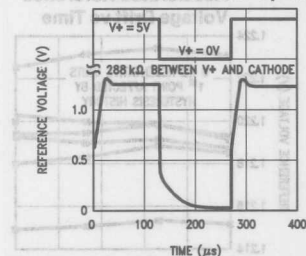
Reference Small-Signal
Resistance vs Frequency



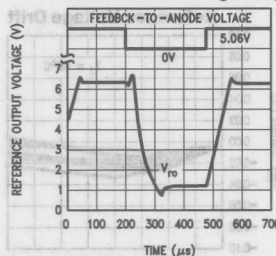
Typical Performance Characteristics (Reference) (Continued)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

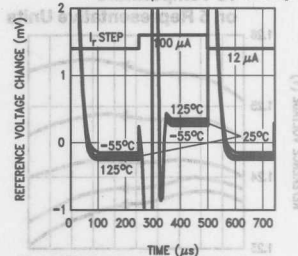
Reference Power-Up Time



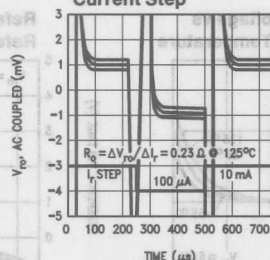
Reference Voltage with FEEDBACK Voltage Step



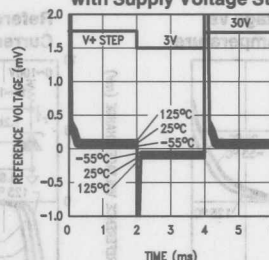
Reference Voltage with 100 ~ 12 μA Current Step



Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step

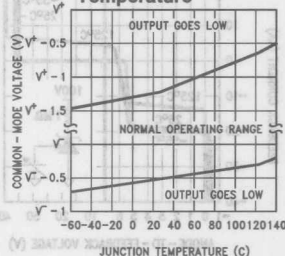


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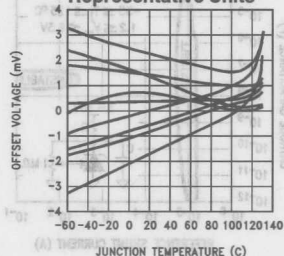
Typical Performance Characteristics (Op Amps)

$V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{CM} = V^+ / 2$, $V_{OUT} = V^+ / 2$, $T_J = 25^\circ\text{C}$, unless otherwise noted

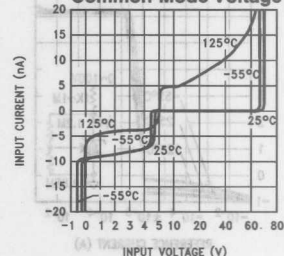
Input Common-Mode Voltage Range vs Temperature



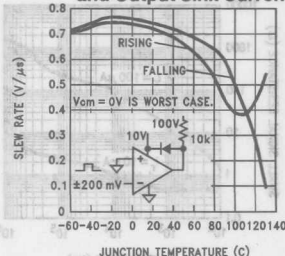
Vos vs Junction Temperature on 9 Representative Units



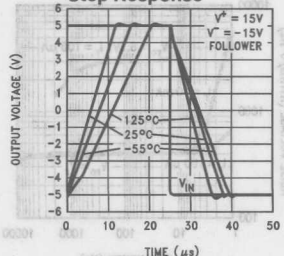
Input Bias Current vs Common-Mode Voltage



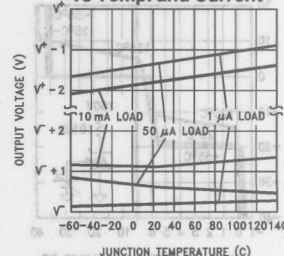
Slew Rate vs Temperature and Output Sink Current



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

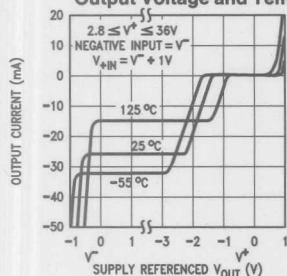


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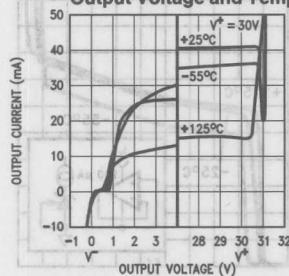
Typical Performance Characteristics (Op Amps) (Continued)

$V_+ = 5V$, $V_- = GND = 0V$, $V_{CM} = V_+/2$, $V_{OUT} = V_+/2$, $T_J = 25^\circ C$, unless otherwise noted

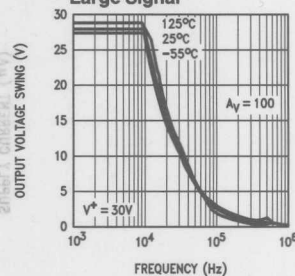
Output Source Current vs Output Voltage and Temp.



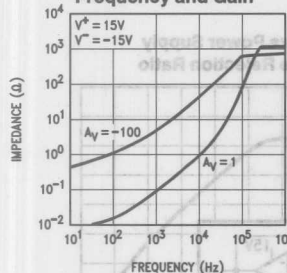
Output Sink Current vs Output Voltage and Temp.



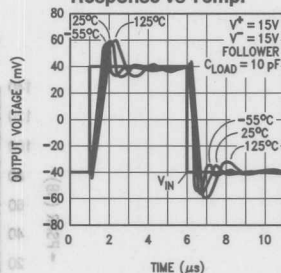
Output Swing, Large Signal



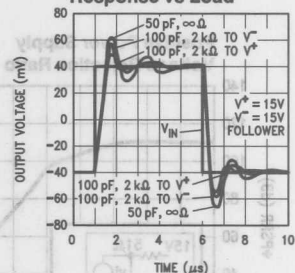
Output Impedance vs Frequency and Gain



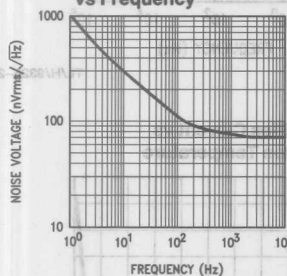
Small-Signal Pulse Response vs Temp.



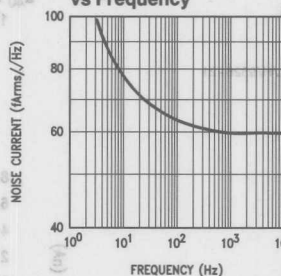
Small-Signal Pulse Response vs Load



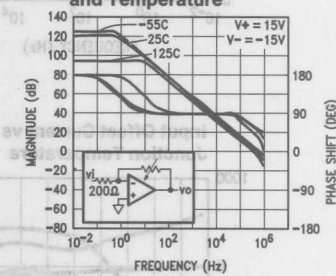
Op Amp Voltage Noise vs Frequency



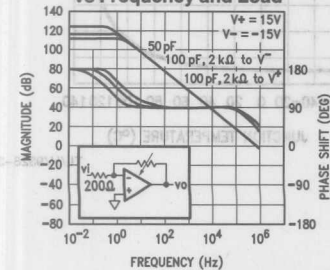
Op Amp Current Noise vs Frequency



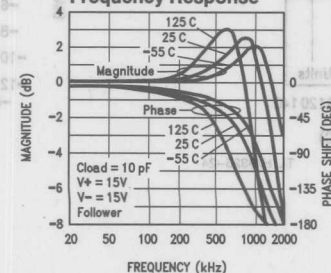
Small-Signal Voltage Gain vs Frequency and Temperature



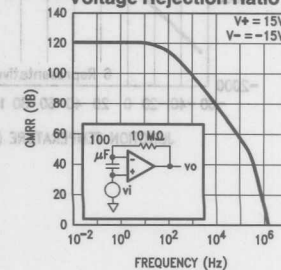
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

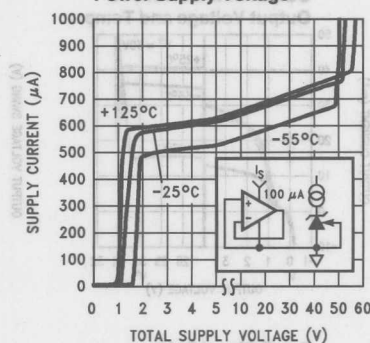


TL/H/9326-6

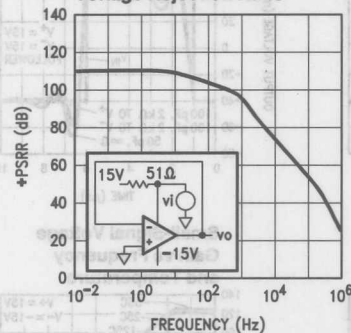
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

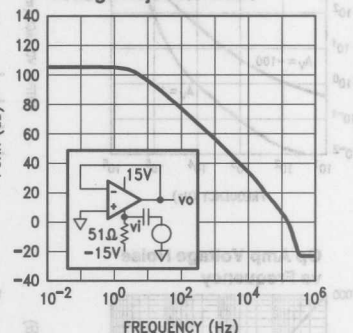
Power Supply Current vs
Power Supply Voltage



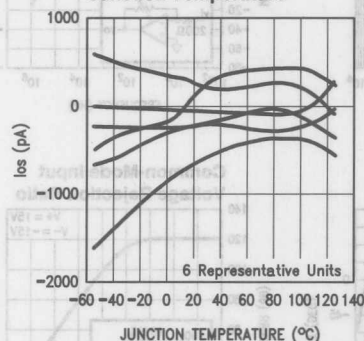
Positive Power Supply
Voltage Rejection Ratio



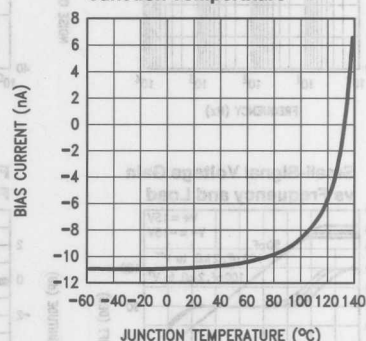
Negative Power Supply
Voltage Rejection Ratio



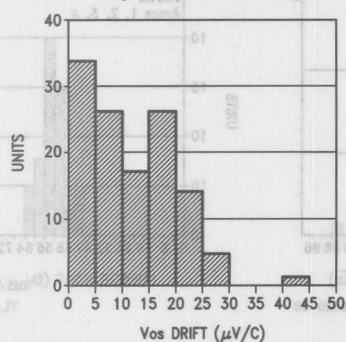
Input Offset Current vs
Junction Temperature



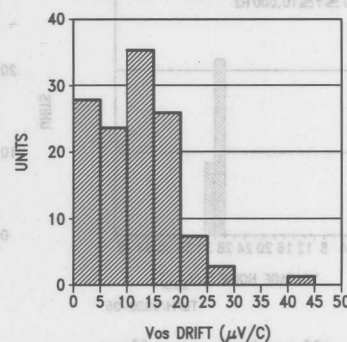
Input Bias Current vs
Junction Temperature



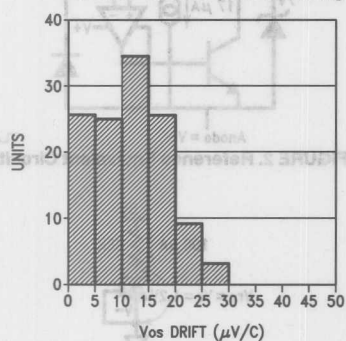
Typical Performance Distributions

Average V_{OS} Drift
Military Temperature Range

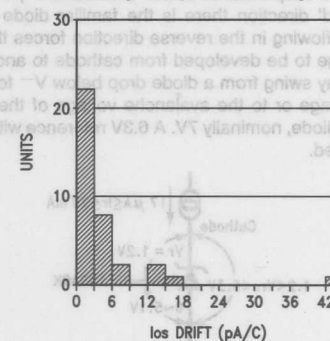
TL/H/9326-29

Average V_{OS} Drift
Industrial Temperature Range

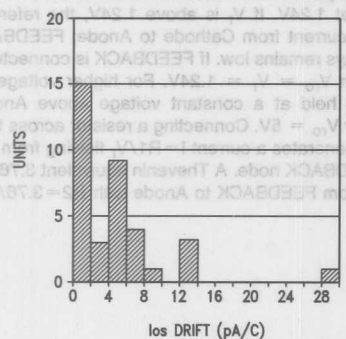
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Average V_{OS} Drift
Commercial Temperature Range

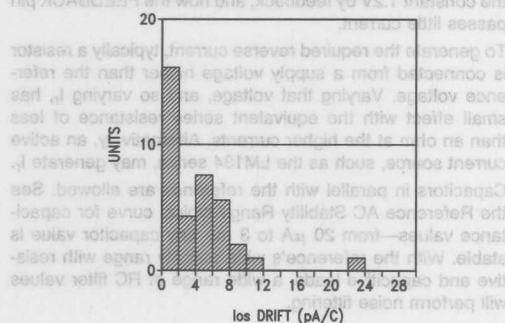
TL/H/9326-31

Average I_{OS} Drift
Military Temperature Range

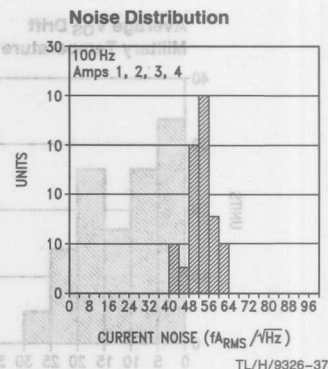
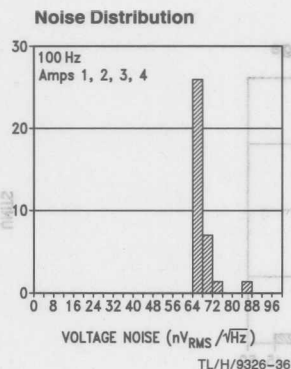
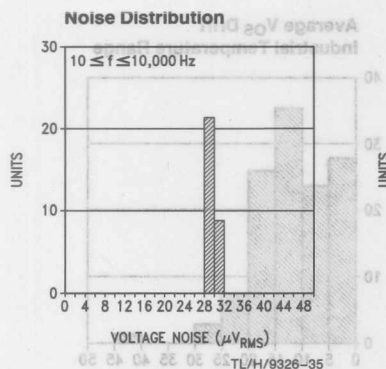
TL/H/9326-32

Average I_{OS} Drift
Industrial Temperature Range

TL/H/9326-33

Average I_{OS} Drift
Commercial Temperature Range

TL/H/9326-34



Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

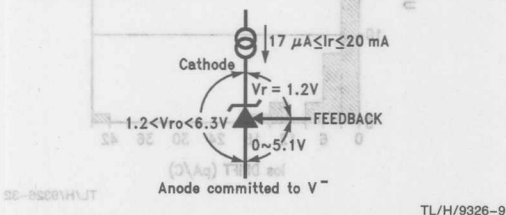


FIGURE 1. Voltages Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r . Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

PS-8526VH/LIT

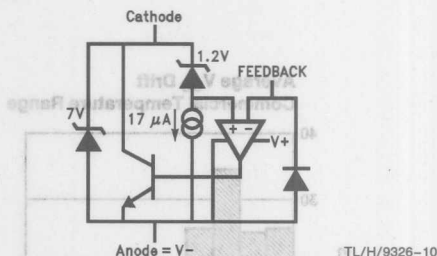


FIGURE 2. Reference Equivalent Circuit

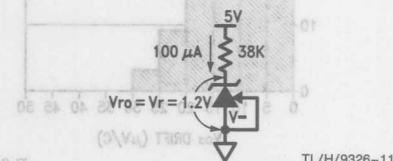


FIGURE 3. 1.2V Reference

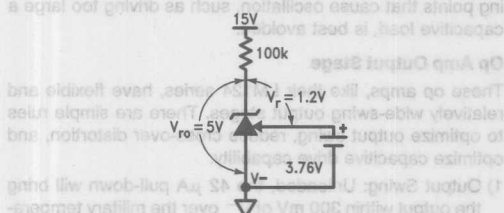
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I

PS-8526VH/LIT

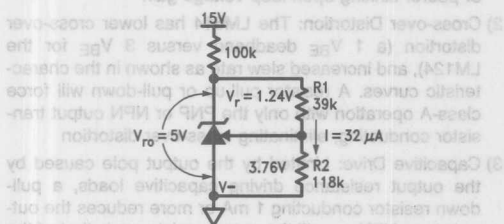
Application Information (Continued)

greater than one thousand times larger than FEEDBACK bias current for $<0.1\%$ error— $\geq 32 \mu\text{A}$ for the military grade over the military temperature range ($\geq 5.5 \mu\text{A}$ for a 1% untrimmed error for a commercial part.)



TL/H/9326-12

FIGURE 4. Thevenin Equivalent of Reference with 5V Output



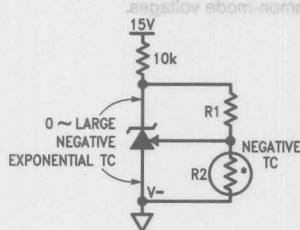
TL/H/9326-13

$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1 \{ (Vro/Vr) - 1 \} = 39k \{ (5/1.24) - 1 \} = 118k$$

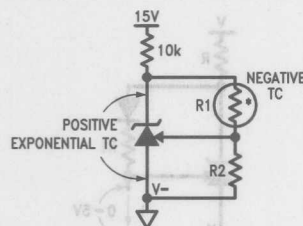
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



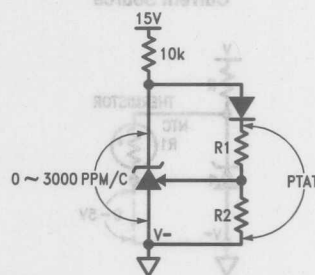
TL/H/9326-14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/9326-15

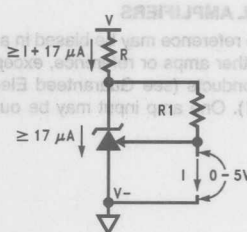
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/9326-16

FIGURE 8. Diode in Series with R1 Causes Voltage across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/9326-17

$$I = Vr/R1 = 1.24/R1$$

FIGURE 9. Current Source is Programmed by R1

Application Information (Continued)

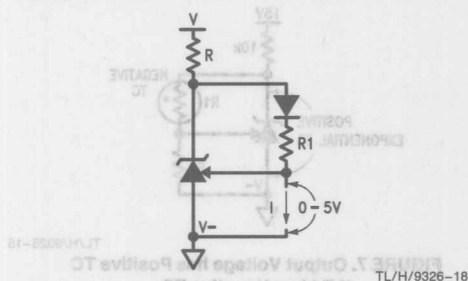


FIGURE 10. Proportional-to-Absolute-Temperature Current Source

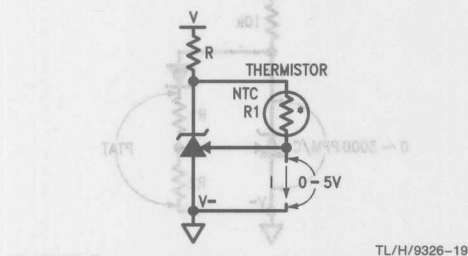


FIGURE 11. Negative-TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS

Any amp or the reference may be biased in any way with no effect on the other amps or reference, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). One amp input may be outside the com-

Application Information (Continued)

mon-mode range, another amp may be operated as a comparator, another with all terminals floating with no effect on the others (tying inverting input to output and non-inverting input to V^- on unused amps is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

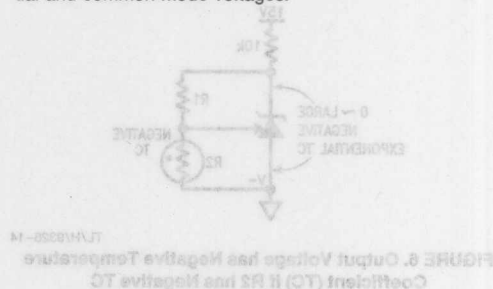
Op Amp Output Stage

These op amps, like their LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

- 1) Output Swing: Unloaded, the $42\ \mu\text{A}$ pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than $42\ \mu\text{A}$ is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ , at the cost of poorer sinking open-loop voltage gain.
- 2) Cross-over Distortion: The LM614 has lower cross-over distortion (a $1\ V_{BE}$ deadband versus $3\ V_{BE}$ for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
- 3) Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit $25\ \Omega$. 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.



Typical Applications

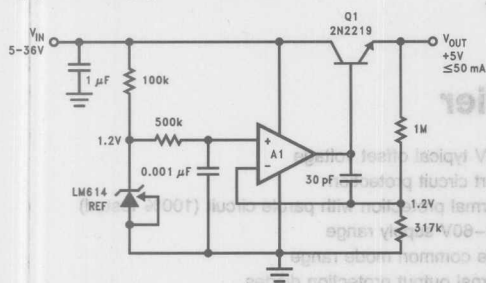
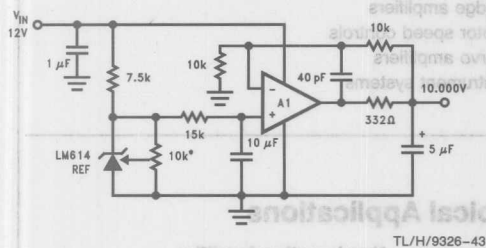


FIGURE 12. Simple Low Quiescent Drain Voltage Regulator. Total supply current approximately 320 μ A, when $V_{IN} = +5V$.



*10k must be low
t.c. trimpot.

FIGURE 13. Ultra Low Noise 10.00V Reference. Total output noise is typically 14 μ V_{RMS}.

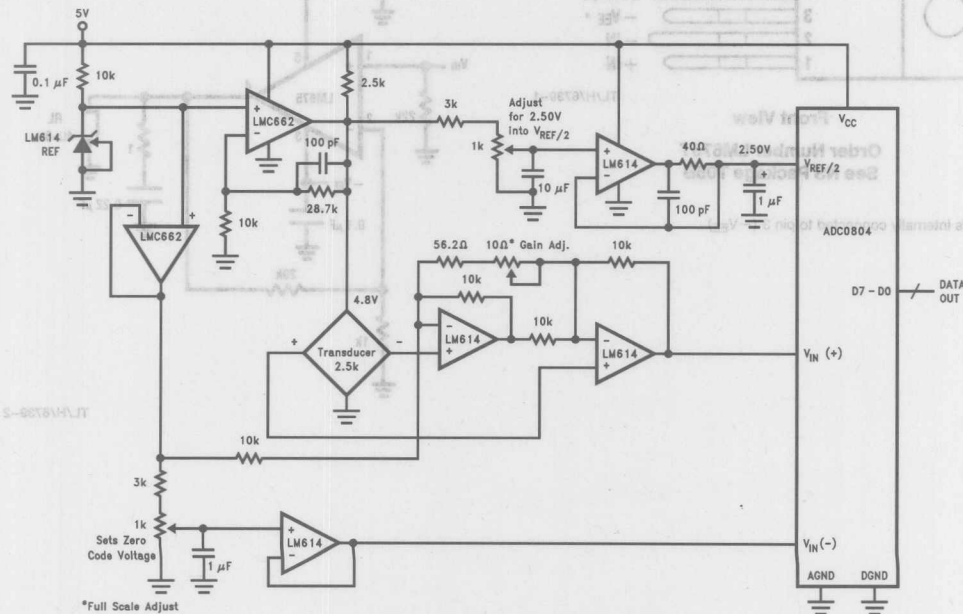


FIGURE 15. Transducer Data Acquisition System. Set zero code voltage, then adjust 10 Ω gain adjust pot for full scale.

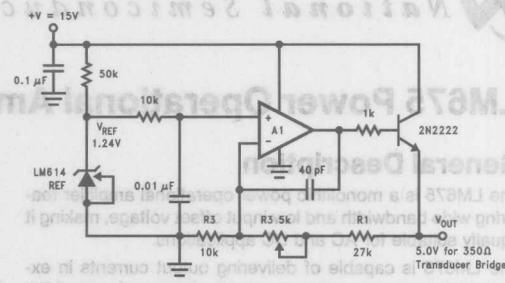


FIGURE 14. Slow Rise Time Upon Power-Up, Adjustable Transducer Bridge Driver. Rise time is approximately 1 ms.

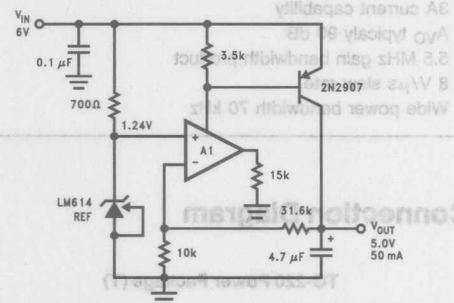


FIGURE 16. Low Drop-Out Voltage Regulator Circuit, drop-out voltage is typically 0.2V.

LM675 Power Operational Amplifier

General Description

The LM675 is a monolithic power operational amplifier featuring wide bandwidth and low input offset voltage, making it equally suitable for AC and DC applications.

The LM675 is capable of delivering output currents in excess of 3 amps, operating at supply voltages of up to 60V. The device overload protection consists of both internal current limiting and thermal shutdown. The amplifier is also internally compensated for gains of 10 or greater.

Features

- 3A current capability
- A_{VO} typically 90 dB
- 5.5 MHz gain bandwidth product
- 8 V/ μ s slew rate
- Wide power bandwidth 70 kHz

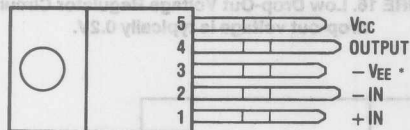
- 1 mV typical offset voltage
- Short circuit protection
- Thermal protection with parol circuit (100% tested)
- 16V–60V supply range
- Wide common mode range
- Internal output protection diodes
- 90 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance power op amp
- Bridge amplifiers
- Motor speed controls
- Servo amplifiers
- Instrument systems

Connection Diagram

TO-220 Power Package (T)



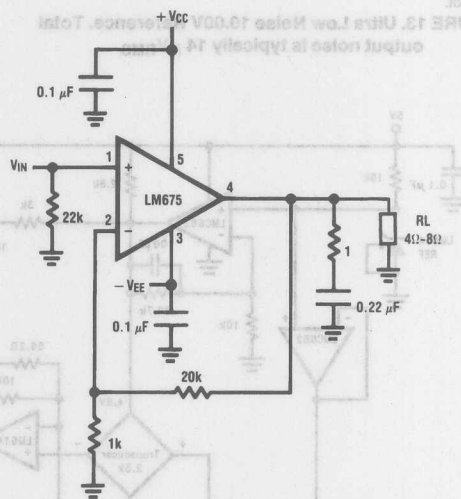
Front View

Order Number LM675T
See NS Package T05B

*The tab is internally connected to pin 3 ($-V_{EE}$)

Typical Applications

Non-Inverting Amplifier



TL/H/6739-2

Office/Distributors for availability and specifications.

Supply Voltage $\pm 30\text{V}$
 Input Voltage $-V_{EE}$ to V_{CC}

Junction Temperature
 Power Dissipation (Note 1)
 Lead Temperature (Soldering, 10 seconds)
 ESD rating to be determined.

150°C
 30W
 260°C

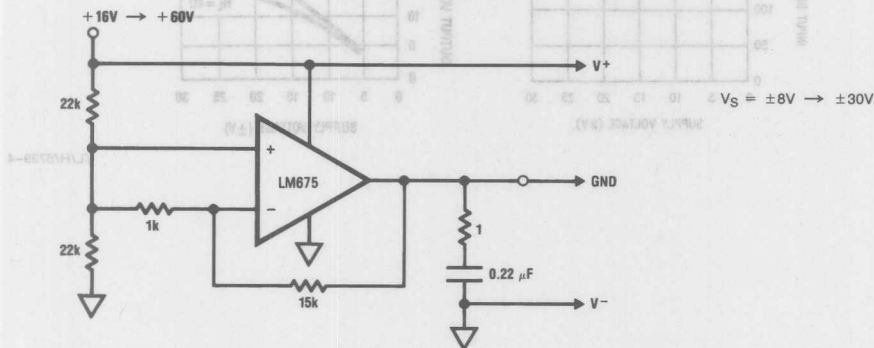
Electrical Characteristics $V_S = \pm 25\text{V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

| Parameter | Conditions | Typical | Tested Limit | Units |
|--|--|----------|----------------|------------------------------|
| Supply Current | $P_{OUT} = 0\text{W}$ | 18 | 50 (max) | mA |
| Input Offset Voltage | $V_{CM} = 0\text{V}$ | 1 | 10 (max) | mV |
| Input Bias Current | $V_{CM} = 0\text{V}$ | 0.2 | 2 (max) | μA |
| Input Offset Current | $V_{CM} = 0\text{V}$ | 50 | 500 (max) | nA |
| Open Loop Gain | $R_L = \infty\Omega$ | 90 | 70 (min) | dB |
| PSRR | $\Delta V_S = \pm 5\text{V}$ | 90 | 70 (min) | dB |
| CMRR | $V_{IN} = \pm 20\text{V}$ | 90 | 70 (min) | dB |
| Output Voltage Swing | $R_L = 8\Omega$ | ± 21 | ± 18 (min) | V |
| Offset Voltage Drift Versus Temperature | $R_S < 100\text{ k}\Omega$ | 25 | | $\mu\text{V}/^\circ\text{C}$ |
| Offset Voltage Drift Versus Output Power | | 25 | | $\mu\text{V}/\text{W}$ |
| Output Power | THD = 1%, $f_O = 1\text{ kHz}$, $R_L = 8\Omega$ | 25 | 20 | W |
| Gain Bandwidth Product | $f_O = 20\text{ kHz}$, $A_{VCL} = 1000$ | 5.5 | | MHz |
| Max Slew Rate | | 8 | | $\text{V}/\mu\text{s}$ |
| Input Common Mode Range | | ± 22 | ± 20 (min) | V |

Note 1: Assumes T_A equal to 70°C . For operation at higher tab temperatures, the LM675 must be derated based on a maximum junction temperature of 150°C .

Typical Applications (Continued)

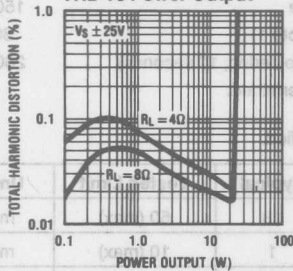
Generating a Split Supply From a Single Supply



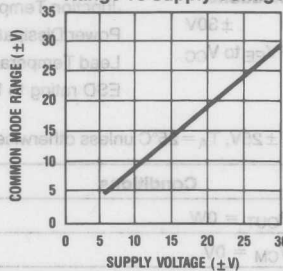
TL/H/6739-3

Typical Performance Characteristics

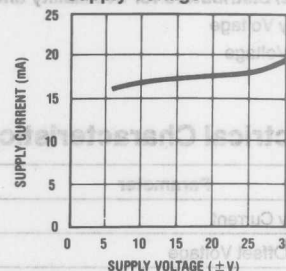
THD vs Power Output



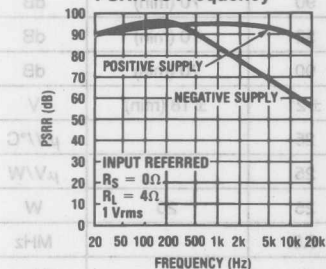
Input Common Mode Range vs Supply Voltage



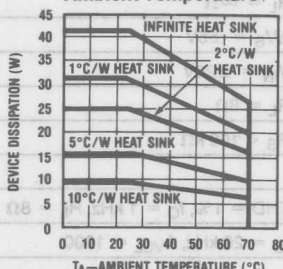
Supply Current vs Supply Voltage



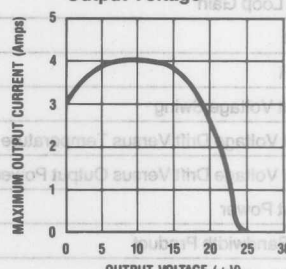
PSRR vs Frequency



Device Dissipation vs Ambient Temperature



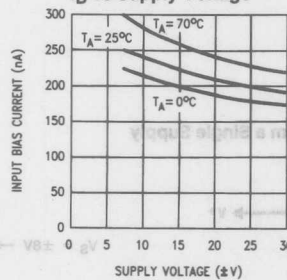
Current Limit vs Output Voltage



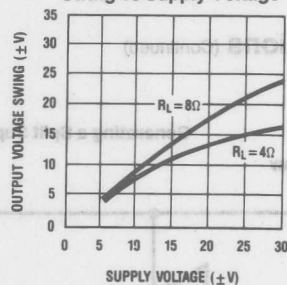
$\dagger \theta$ INTERFACE = $1^{\circ}C/W$.
See Application Hints.

* $V_S = \pm 25V$

IB vs Supply Voltage



Output Voltage Swing vs Supply Voltage

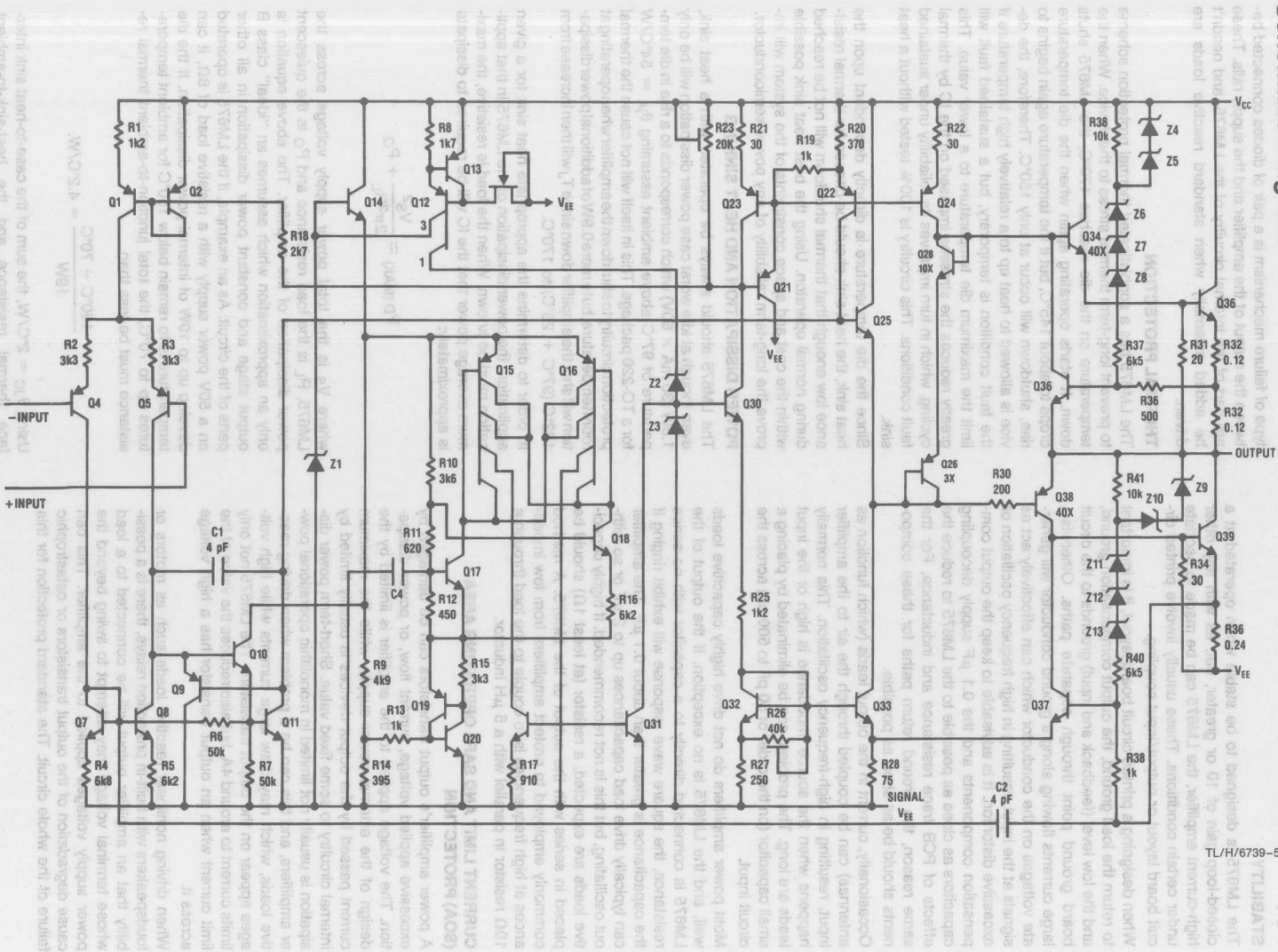


TL/H/6739-4

Schematic Diagram

TL/H/6739-5

TL/H/6739-5



Application Hints

STABILITY

The LM675 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM675 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a printed circuit board layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM675 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM675 is no exception. If the output of the LM675 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF . The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1 Ω) should be placed in series with the output of the LM675. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10 Ω resistor in parallel with a 5 μH inductor.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic operational power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM675 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this

type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM675, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM675 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM675 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions. This circuitry is 100% tested without a heat sink.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor.

POWER DISSIPATION AND HEAT SINKING

The LM675 should always be operated with a heat sink, even though at idle worst case power dissipation will be only 1.8W (30 mA \times 60V) which corresponds to a rise in die temperature of 97°C above ambient assuming $\theta_{JA} = 54^\circ\text{C}/\text{W}$ for a TO-220 package. This in itself will not cause the thermal protection circuitry to shut down the amplifier when operating at room temperature, but a mere 0.9W of additional power dissipation will shut the amplifier down since T_J will then increase from 122°C (97°C + 25°C) to 170°C.

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM675 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_D (\text{MAX}) \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM675, R_L is the load resistance and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. As an example, if the LM675 is operated on a 50V power supply with a resistive load of 8 Ω , it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150^\circ\text{C} - 70^\circ\text{C}}{19\text{W}} = 4.2^\circ\text{C}/\text{W}.$$

Using $\theta_{JC} = 2^\circ\text{C}/\text{W}$, the sum of the case-to-heat sink interface thermal resistance and the heat-sink-to-ambient

Application Hints (Continued)

thermal resistance must be less than $2.2^{\circ}\text{C}/\text{W}$. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about $1^{\circ}\text{C}/\text{W}$ if lubricated, and about $1.2^{\circ}\text{C}/\text{W}$ if dry. If a mica insulator is used, the thermal resistance will be about $1.6^{\circ}\text{C}/\text{W}$ lubricated and $3.4^{\circ}\text{C}/\text{W}$ dry. For this example, we assume a lubricated mica insulator between the LM675 and the heat sink. The heat sink thermal resistance must then be less than

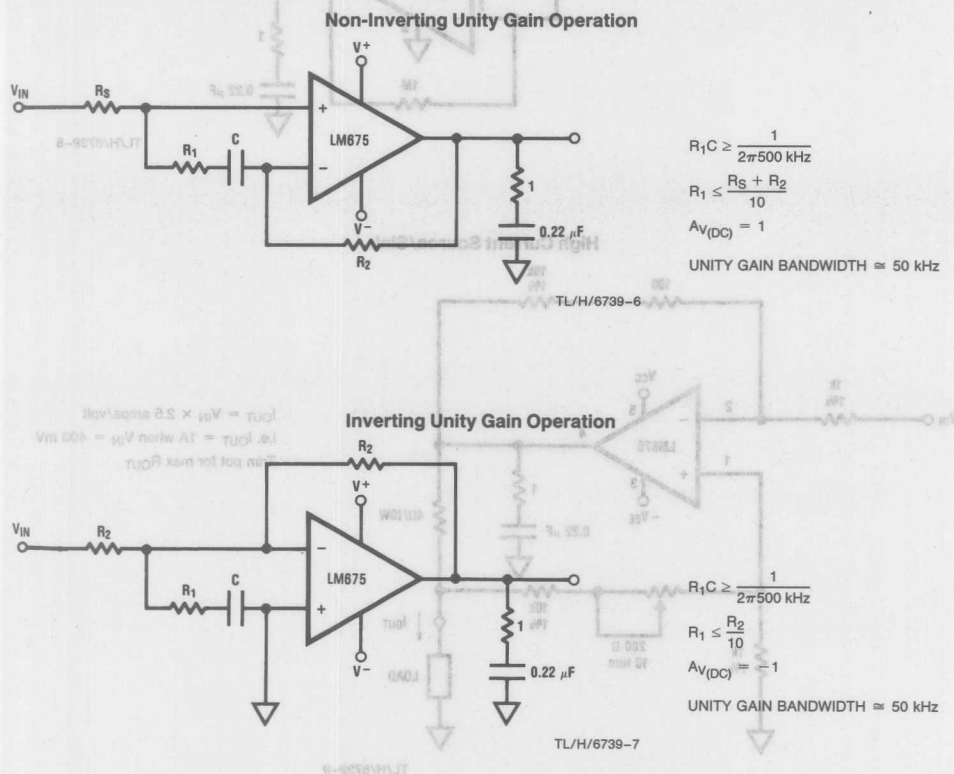
$$4.2^{\circ}\text{C}/\text{W} - 2^{\circ}\text{C}/\text{W} - 1.6^{\circ}\text{C}/\text{W} = 0.6^{\circ}\text{C}/\text{W}.$$

This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be restricted to 50°C (122°F), resulting in a $1.6^{\circ}\text{C}/\text{W}$ heat sink, or the heat

sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a $1.2^{\circ}\text{C}/\text{W}$ unit if the case-to-heat-sink interface is lubricated.

The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load will be roughly that of the same amplifier driving the resistive part of that load. For example, some reactive loads may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60° . The real part of this load will then be $8\Omega \times \cos 60^{\circ}$ or 4Ω , and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Typical Applications (Continued)



Servo Motor Control

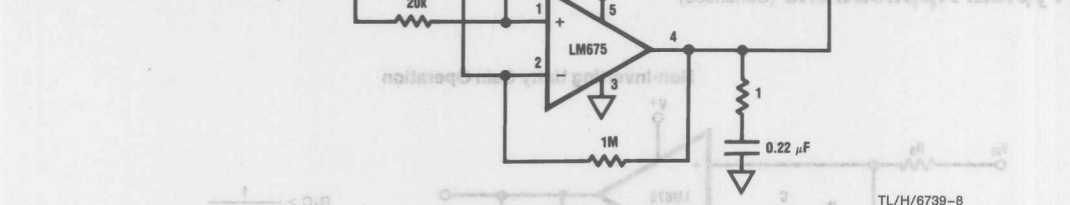
with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.5°C/W if dry. If a mica insulator is used, the thermal resistance will be about 1.8°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM675 and the heat sink. The heat sink thermal resistance must then be less than

$1.5^{\circ}\text{C/W} - 2^{\circ}\text{C/W} = -0.5^{\circ}\text{C/W}$

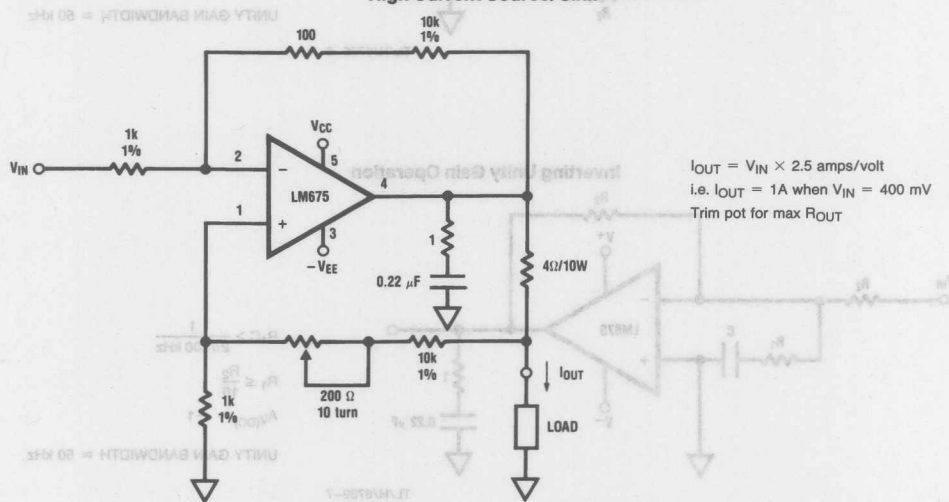
This is a rather large heat sink and not be practical for some applications. If a smaller heat sink is required for some of size or cost, there are two alternatives. The first is to use a mica insulator between the LM675 and the heat sink, or the heat sink must be less than

$1.8^{\circ}\text{C/W} - 2^{\circ}\text{C/W} = -0.2^{\circ}\text{C/W}$

and not be practical for some applications. If a smaller heat sink is required for some of size or cost, there are two alternatives. The first is to use a mica insulator between the LM675 and the heat sink, or the heat sink must be less than



High Current Source/Sink



TL/H/6739-9

LM709 Operational Amplifier

General Description

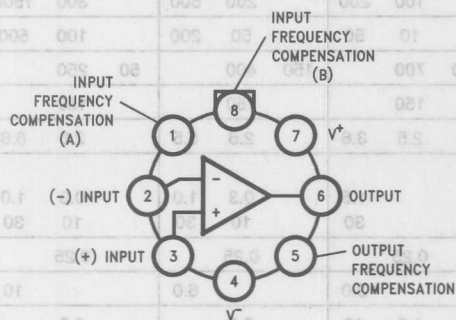
The LM709 series is a monolithic operational amplifier intended for general-purpose applications. Operation is completely specified over the range of voltages commonly used for these devices. The design, in addition to providing high gain, minimizes both offset voltage and bias currents. Further, the class-B output stage gives a large output capability with minimum power drain.

External components are used to frequency compensate the amplifier. Although the unity-gain compensation network specified will make the amplifier unconditionally stable in all feedback configurations, compensation can be tailored to optimize high-frequency performance for any gain setting.

The LM709C is the commercial-industrial version of the LM709. It is identical to the LM709 except that it is specified for operation from 0°C to +70°C.

Connection Diagrams

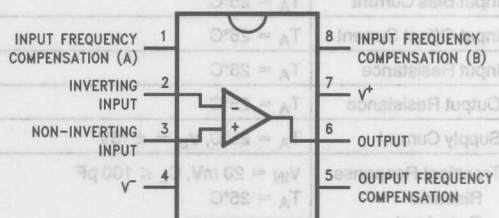
Metal Can Package



Order Number LM709AH, LM709H or LM709CH
See NS Package Number H08C

TL/H/11477-4

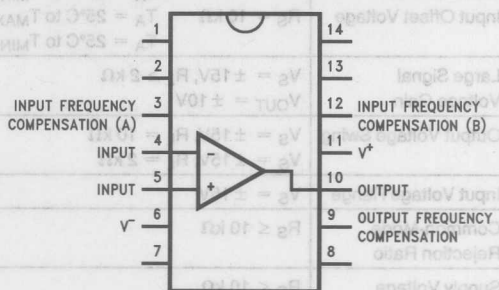
Dual-In-Line Package



TL/H/11477-6

Order Number LM709CN-8
See NS Package Number N08E

Dual-In-Line Package



TL/H/11477-5

Order Number LM709CN
See NS Package Number N14A

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | | |
|---|---------------------|-----------|
| Supply Voltage | LM709/LM709A/LM709C | ±18V |
| Power Dissipation (Note 1) | LM709/LM709A | 300 mW |
| | LM709C | 250 mW |
| Differential Input Voltage | LM709/LM709A/LM709C | ±5V |
| Input Voltage | LM709/LM709A/LM709C | ±10V |
| Output Short-Circuit Duration ($T_A = +25^\circ\text{C}$) | LM709/LM709A/LM709C | 5 seconds |

| | | |
|---------------------------------------|---------------------|-----------------|
| Storage Temperature Range | LM709/LM709A/LM709C | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | LM709/LM709A/LM709C | 300°C |

Operating Ratings (Note 3)

| | | |
|--------------------------------------|------------------|-----------------------------------|
| Junction Temperature Range (Note 1) | LM709/LM709A | -55°C to +150°C |
| | LM709C | 0°C to +100°C |
| Thermal Resistance (θ_{JA}) | H Package | 150°C/W, (θ_{JC}) 45°C/W |
| | 8-Pin N Package | 134°C/W |
| | 14-Pin N Package | 109°C/W |

Electrical Characteristics (Note 2)

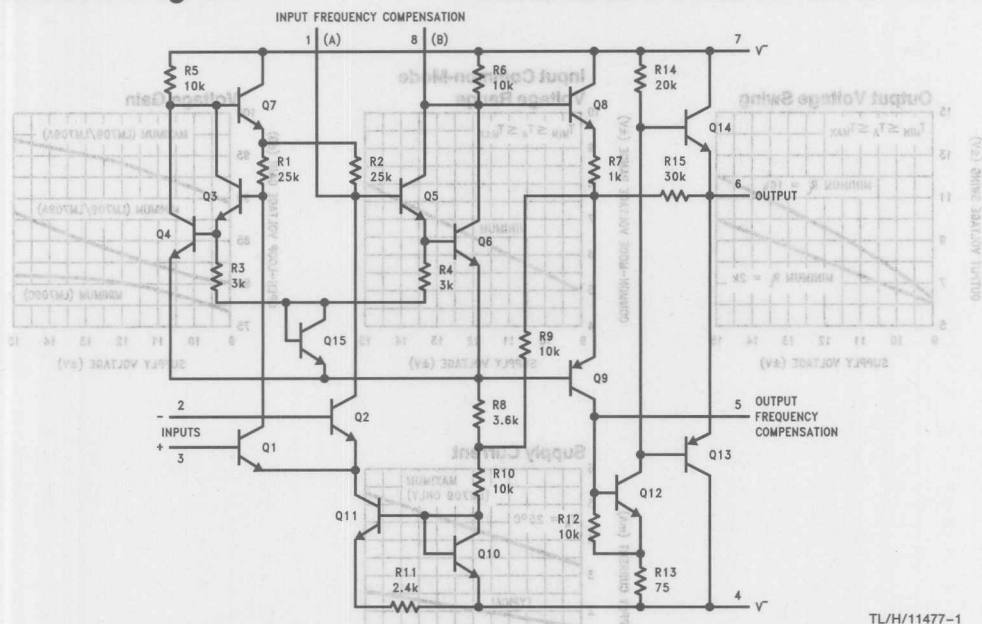
| Parameter | Conditions | LM709A | | | LM709 | | | LM709C | | | Units |
|---|--|--------------------------|----------------------|-----|------------|------------|-----|------------|------------|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | T _A = 25°C, R _S ≤ 10 kΩ | 0.6 | 2.0 | | 1.0 | 5.0 | | 2.0 | 7.5 | | mV |
| Input Bias Current | T _A = 25°C | 100 | 200 | | 200 | 500 | | 300 | 1500 | | nA |
| Input Offset Current | T _A = 25°C | 10 | 50 | | 50 | 200 | | 100 | 500 | | nA |
| Input Resistance | T _A = 25°C | 350 | 700 | | 150 | 400 | | 50 | 250 | | kΩ |
| Output Resistance | T _A = 25°C | 150 | | | 150 | | | 150 | | | Ω |
| Supply Current | T _A = 25°C, V _S = ±15V | 2.5 | 3.6 | | 2.6 | 5.5 | | 2.6 | 6.6 | | mA |
| Transient Response | V _{IN} = 20 mV, C _L ≤ 100 pF | | | | | | | | | | |
| Risetime | T _A = 25°C | | 1.5 | | 0.3 | 1.0 | | 0.3 | 1.0 | | μs |
| Overshoot | | | 30 | | 10 | 30 | | 10 | 30 | | % |
| Slew Rate | T _A = 25°C | 0.25 | | | 0.25 | | | 0.25 | | | V/μs |
| Input Offset Voltage | R _S ≤ 10 kΩ | | | 3.0 | | | 6.0 | | | 10 | mV |
| Average Temperature Coefficient of Input Offset Voltage | R _S = 50Ω T _A = 25°C to T _{MAX} T _A = 25°C to T _{MIN} R _S = 10 kΩ T _A = 25°C to T _{MAX} T _A = 25°C to T _{MIN} | 1.8 1.8 2.0 4.8 | 10 10 15 25 | | 3.0 6.0 | | | 6.0 12 | | | μV/°C |
| Large Signal Voltage Gain | V _S = ±15V, R _L ≥ 2 kΩ V _{OUT} = ±10V | 25 | | 70 | 25 | 45 | 70 | 15 | 45 | | V/mV |
| Output Voltage Swing | V _S = ±15V, R _L = 10 kΩ V _S = ±15V, R _L = 2 kΩ | ±12 ±10 | ±14 ±13 | | ±12 ±10 | ±14 ±13 | | ±12 ±10 | ±14 ±13 | | V |
| Input Voltage Range | V _S = ±15V | ±8 | | | ±8 | ±10 | | ±8 | ±10 | | V |
| Common-Mode Rejection Ratio | R _S ≤ 10 kΩ | 80 | 110 | | 70 | 90 | | 65 | 90 | | dB |
| Supply Voltage Rejection Ratio | R _S ≤ 10 kΩ | 40 | 100 | | 25 | 150 | | 25 | 200 | | μV/V |
| Input Offset Current | T _A = T _{MAX} T _A = T _{MIN} | 3.5 40 | 50 250 | | 20 100 | 200 500 | | 75 125 | 400 750 | | nA |
| Input Bias Current | T _A = T _{MIN} | 0.3 | 0.6 | | 0.5 | 1.5 | | 0.36 | 2.0 | | μA |
| Input Resistance | T _A = T _{MIN} | 85 | 170 | | 40 | 100 | | 50 | 250 | | kΩ |

Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature for LM709/LM709A and 100°C maximum for LM709C. For operating at elevated temperatures, the device must be derated based on thermal resistance θ_{JA} , $T_{J(MAX)}$ and T_A .

Note 2: These specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the LM709/LM709A and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for the LM709C with the following conditions: $\pm 9\text{V} \leq V_S \leq \pm 15\text{V}$, $C_1 = 5000\text{ pF}$, $R_1 = 1.5\text{ k}\Omega$, $C_2 = 200\text{ pF}$ and $R_2 = 51\Omega$.

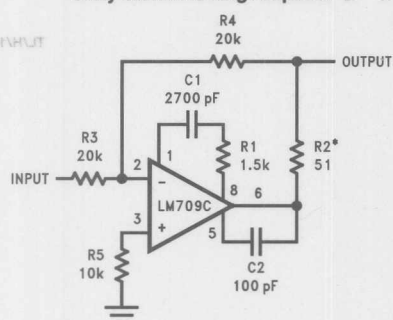
Note 3: Absolute Maximum Ratings indicate limits which if exceeded may result in damage. Operating Ratings are conditions where the device is expected to be functional but not necessarily within the guaranteed performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Schematic Diagram**

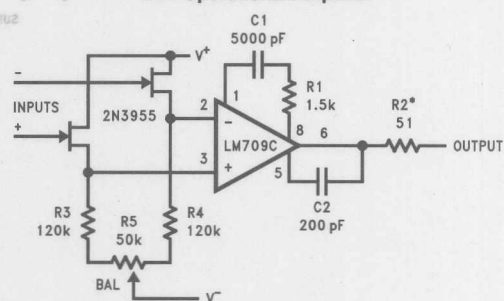


Typical Applications**

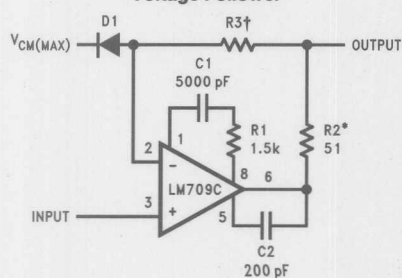
Unity Gain Inverting Amplifier



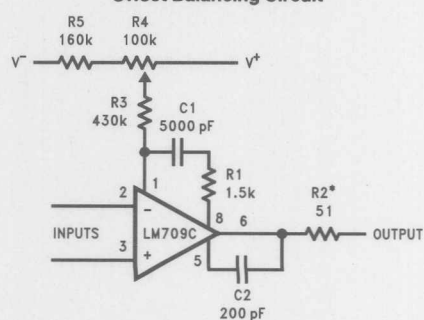
FET Operational Amplifier



Voltage Follower



Offset Balancing Circuit



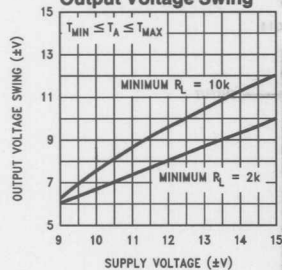
*To be used with any capacitive loading on output.

**Pin connections shown are for metal can package.

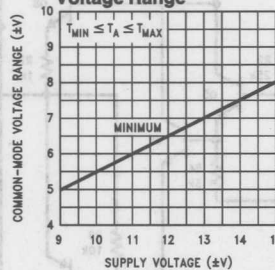
†Should be equal to DC source resistance on input.

Guaranteed Performance Characteristics

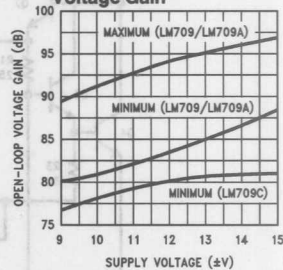
Output Voltage Swing



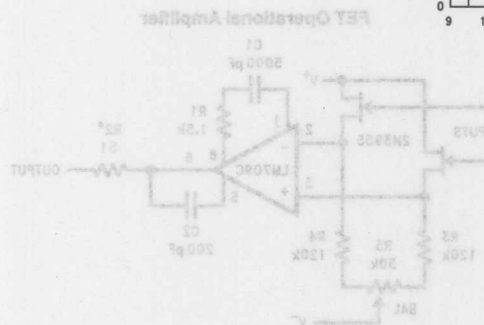
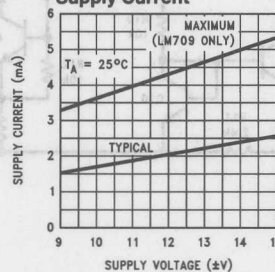
Input Common-Mode Voltage Range



Voltage Gain

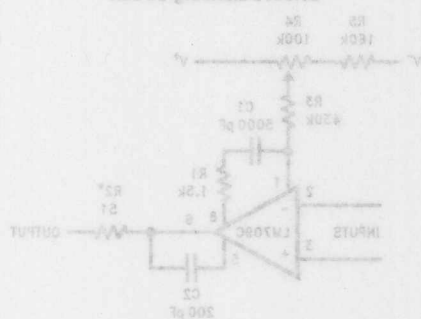


Supply Current

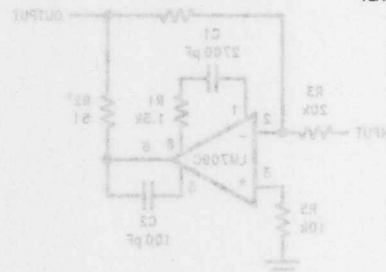


TLH/11477-9

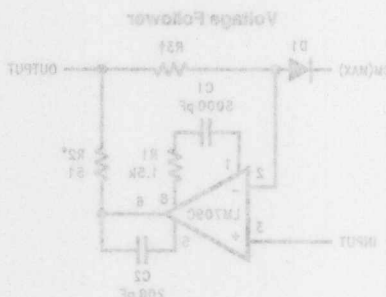
Offset Balancing Circuit



TLH/11477-9



TLH/11477-9

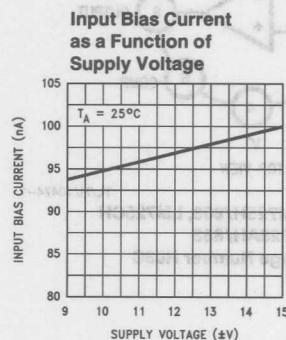
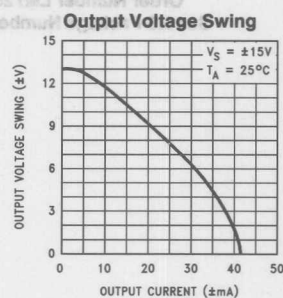
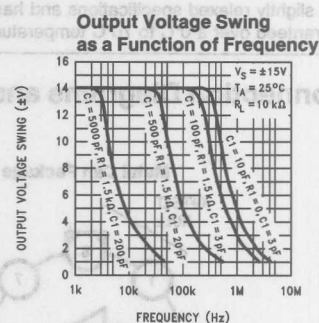
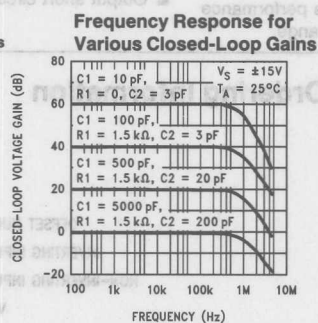
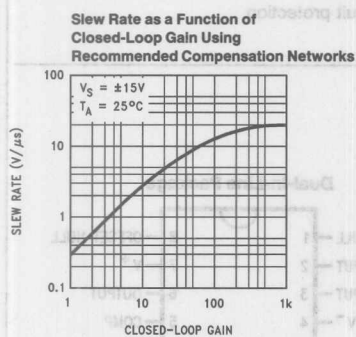
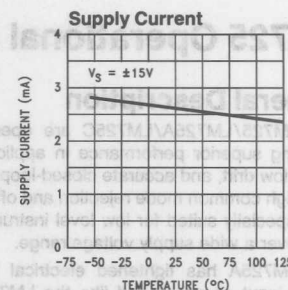
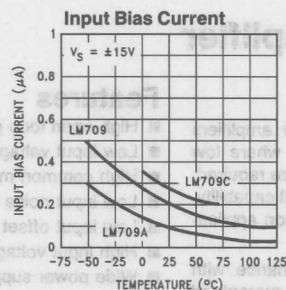
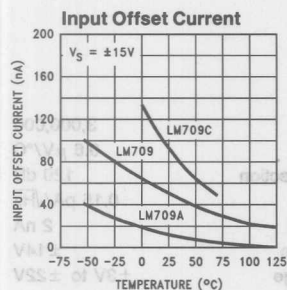


TLH/11477-9

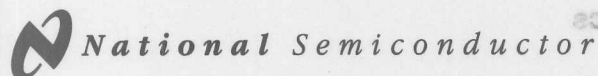
*To be used with any negative loading on output.
 **Pin connections shown are for metal can package.
 †Should be used to DC source resistance on input.

Typical Performance Characteristics

LM709



TL/H/11477-10



LM725 Operational Amplifier

General Description

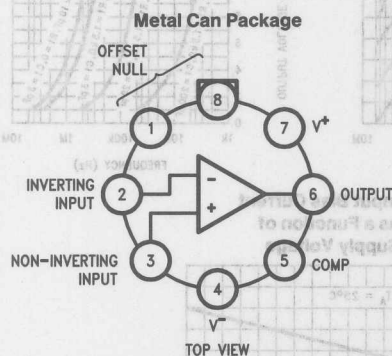
The LM725/LM725A/LM725C are operational amplifiers featuring superior performance in applications where low noise, low drift, and accurate closed-loop gain are required. With high common mode rejection and offset null capability, it is especially suited for low level instrumentation applications over a wide supply voltage range.

The LM725A has tightened electrical performance with higher input accuracy and like the LM725, is guaranteed over a -55°C to $+125^{\circ}\text{C}$ temperature range. The LM725C has slightly relaxed specifications and has its performance guaranteed over a 0°C to 70°C temperature range.

Features

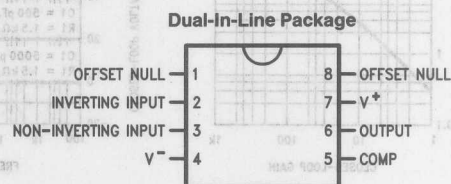
- High open loop gain 3,000,000
- Low input voltage drift $0.6 \mu\text{V}/^{\circ}\text{C}$
- High common mode rejection 120 dB
- Low input noise current $0.15 \text{ pA}/\sqrt{\text{Hz}}$
- Low input offset current 2 nA
- High input voltage range $\pm 14\text{V}$
- Wide power supply range $\pm 3\text{V}$ to $\pm 22\text{V}$
- Offset null capability
- Output short circuit protection

Connection Diagrams and Ordering Information



Order Number LM725H/883, LM725CH
or LM725AH/883
See NS Package Number H08C

TL/H/10474-1



Order Number LM725CN
See NS Package Number N08E

TL/H/10474-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-------------------------------------|--------|
| Supply Voltage | ± 22V |
| Internal Power Dissipation (Note 1) | 500 mW |
| Differential Input Voltage | ± 5V |
| Input Voltage (Note 2) | ± 22V |

| | | |
|---------------------------------------|-----------------|--------------|
| Storage Temperature Range | -65°C to +150°C | |
| Lead Temperature (Soldering, 10 Sec.) | 260°C | |
| Maximum Junction Temperature | 150°C | |
| Operating Temperature Range | $T_{A(MIN)}$ | $T_{A(MAX)}$ |
| LM725 | -55°C | to +125°C |
| LM725A | -55°C | to +125°C |
| LM725C | 0°C | to +70°C |

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM725A | | | LM725 | | | LM725C | | | Units |
|---|---|--------|--------|------|--------|--------|-----|--------|--------|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (Without External Trim) | $T_A = 25^\circ\text{C}$, $R_S \leq 10\text{ k}\Omega$ | | | 0.5 | | 0.5 | 1.0 | | 0.5 | 2.5 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 2.0 | 5.0 | | 2.0 | 20 | | 2.0 | 35 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 42 | 80 | | 42 | 100 | | 42 | 125 | nA |
| Input Noise Voltage | $T_A = 25^\circ\text{C}$ | | | | | | | | | | |
| | $f_o = 10\text{ Hz}$ | | 15 | | | 15 | | | 15 | | nV/ $\sqrt{\text{Hz}}$ |
| | $f_o = 100\text{ Hz}$ | | 9.0 | | | 9.0 | | | 9.0 | | nV/ $\sqrt{\text{Hz}}$ |
| | $f_o = 1\text{ kHz}$ | | 8.0 | | | 8.0 | | | 8.0 | | nV/ $\sqrt{\text{Hz}}$ |
| Input Noise Current | $T_A = 25^\circ\text{C}$ | | | | | | | | | | |
| | $f_o = 10\text{ Hz}$ | | 1.0 | | | 1.0 | | | 1.0 | | pA/ $\sqrt{\text{Hz}}$ |
| | $f_o = 100\text{ Hz}$ | | 0.3 | | | 0.3 | | | 0.3 | | pA/ $\sqrt{\text{Hz}}$ |
| | $f_o = 1\text{ kHz}$ | | 0.15 | | | 0.15 | | | 0.15 | | pA/ $\sqrt{\text{Hz}}$ |
| Input Resistance | $T_A = 25^\circ\text{C}$ | | 1.5 | | | 1.5 | | | 1.5 | | M Ω |
| Input Voltage Range | $T_A = 25^\circ\text{C}$ | ± 13.5 | ± 14 | | ± 13.5 | ± 14 | | ± 13.5 | ± 14 | | V |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}$, $R_L \geq 2\text{ k}\Omega$, $V_{OUT} = \pm 10\text{V}$ | 1000 | 3000 | | 1000 | 3000 | | 250 | 3000 | | V/mV |
| Common-Mode Rejection Ratio | $T_A = 25^\circ\text{C}$, $R_S \leq 10\text{ k}\Omega$ | 120 | | | 110 | 120 | | 94 | 120 | | dB |
| Power Supply Rejection Ratio | $T_A = 25^\circ\text{C}$, $R_S \leq 10\text{ k}\Omega$ | | 2.0 | 5.0 | | 2.0 | 10 | | 2.0 | 35 | $\mu\text{V/V}$ |
| Output Voltage Swing | $T_A = 25^\circ\text{C}$, $R_L \geq 10\text{ k}\Omega$ | ± 12.5 | ± 13.5 | | ± 12 | ± 13.5 | | ± 12 | ± 13.5 | | V |
| | $R_L \geq 2\text{ k}\Omega$ | ± 12.0 | ± 13.5 | | ± 10 | ± 13.5 | | ± 10 | ± 13.5 | | V |
| Power Consumption | $T_A = 25^\circ\text{C}$ | | 80 | 105 | | 80 | 105 | | 80 | 150 | mW |
| Input Offset Voltage (Without External Trim) | $R_S \leq 10\text{ k}\Omega$ | | | 0.7 | | | 1.5 | | | 3.5 | mV |
| Average Input Offset Voltage Drift (Without External Trim) | $R_S = 50\Omega$ | | | 2.0 | | 2.0 | 5.0 | | 2.0 | | $\mu\text{V}/^\circ\text{C}$ |
| Average Input Offset Voltage Drift (With External Trim) | $R_S = 50\Omega$ | | 0.6 | 1.0 | | 0.6 | | | 0.6 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current | $T_A = T_{MAX}$ | | 1.2 | 4.0 | | 1.2 | 20 | | 1.2 | 35 | nA |
| | $T_A = T_{MIN}$ | | 7.5 | 18.0 | | 7.5 | 40 | | 4.0 | 50 | nA |
| Average Input Offset Current Drift | | | 35 | 90 | | 35 | 150 | | 10 | | pA/ $^\circ\text{C}$ |
| Input Bias Current | $T_A = T_{MAX}$ | | 20 | 70 | | 20 | 100 | | | 125 | nA |
| | $T_A = T_{MIN}$ | | 80 | 180 | | 80 | 200 | | | 250 | nA |

Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM725A | | | LM725 | | | LM725C | | | Units |
|------------------------------|--|-----------|-----|-----|-----------|-----|-----|----------|-----|-----|-----------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Large Signal Voltage Gain | $R_L \geq 2\text{ k}\Omega$ | | | | | | | | | | V/V |
| | $T_A = T_{MAX}$ | 1,000,000 | | | 1,000,000 | | | 125,000 | | | V/V |
| | $R_L \geq 2\text{ k}\Omega$ $T_A = T_{MIN}$ | 500,000 | | | 250,000 | | | 125,000 | | | V/V |
| Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 110 | | | 100 | | | 115 | | | dB |
| Power Supply Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | | | 8.0 | | | 20 | | | 20 | $\mu\text{V/V}$ |
| Output Voltage Swing | $R_L \geq 2\text{ k}\Omega$ | ± 12 | | | ± 10 | | | ± 10 | | | V |

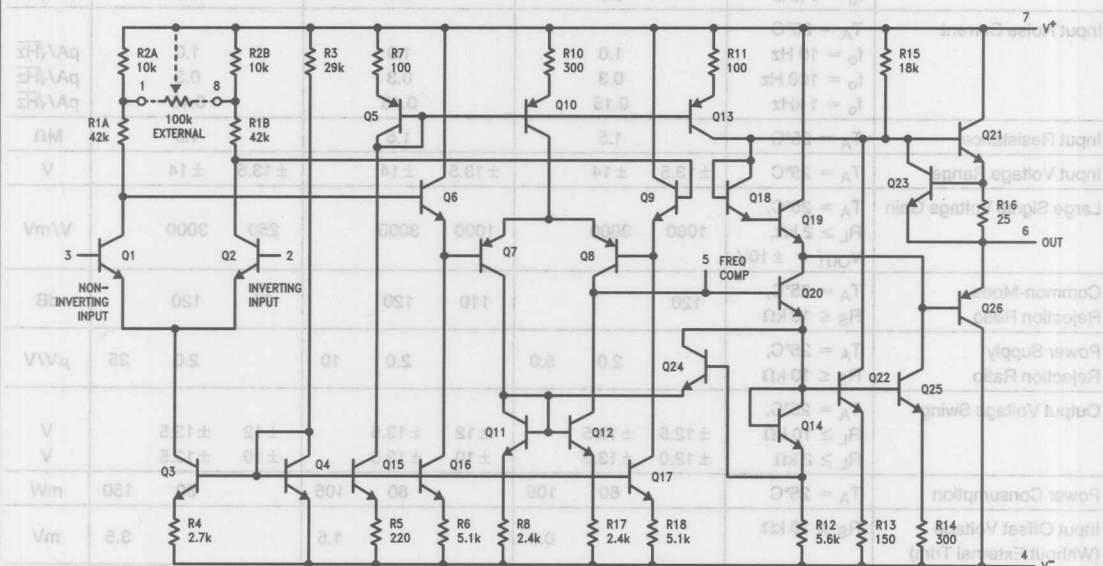
Note 1: Derate at 150°C/W for operation at ambient temperatures above 75°C .

Note 2: For supply voltages less than $\pm 22\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

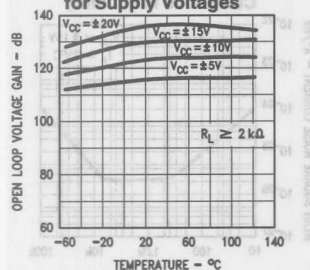
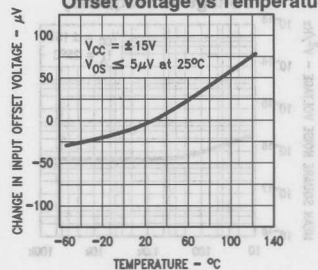
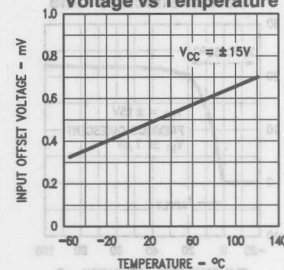
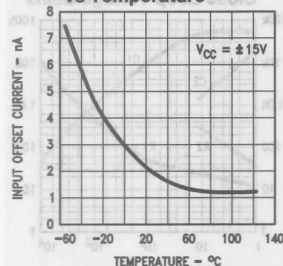
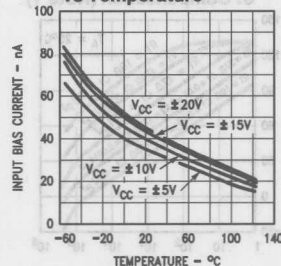
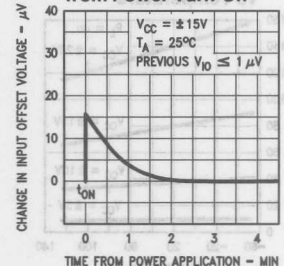
Note 3: These specifications apply for $V_S = \pm 15\text{V}$ unless otherwise specified.

Note 4: For Military electrical specifications RETS725AX are available for LM725AH and RETS725X are available for LM725H.

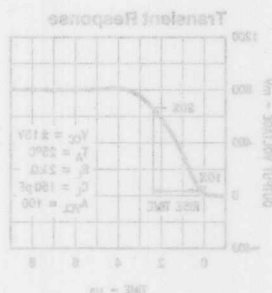
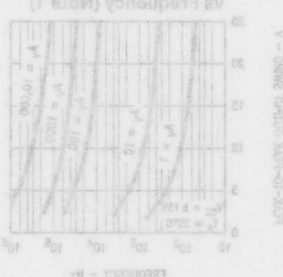
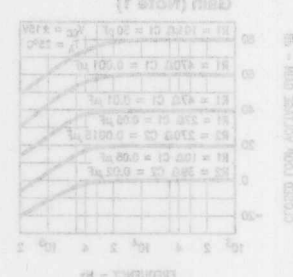
Schematic Diagram



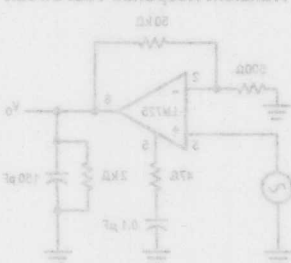
Typical Performance Characteristics

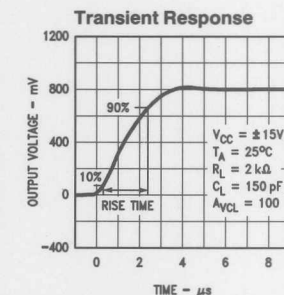
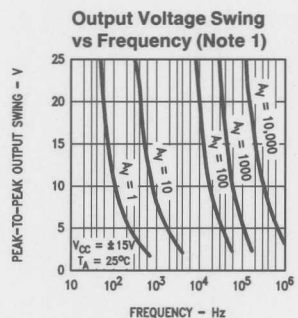
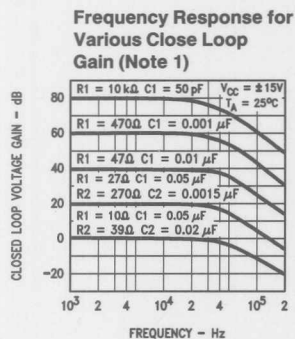
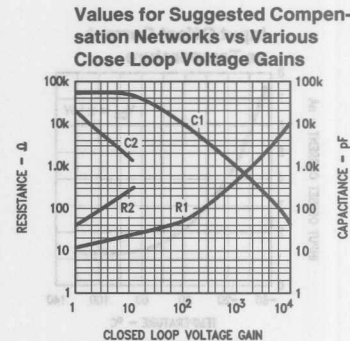
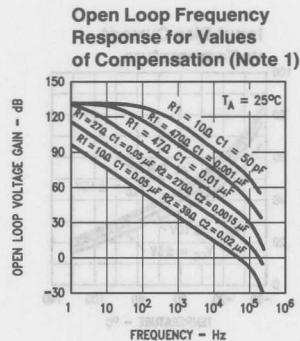
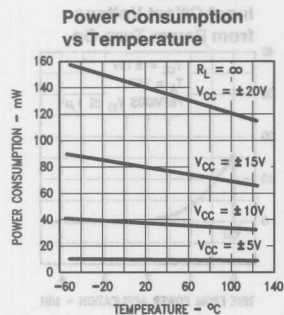
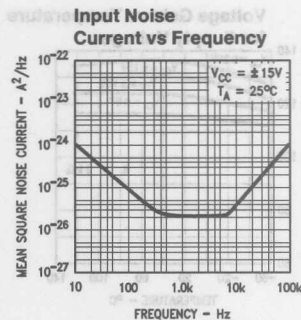
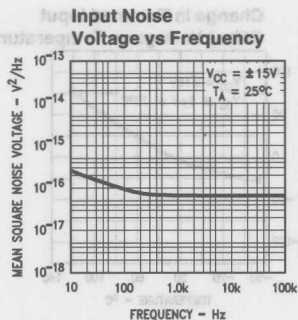
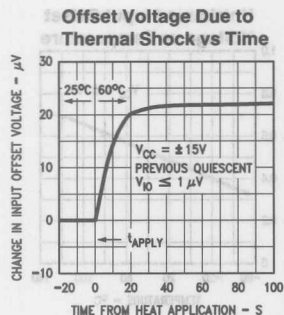
Voltage Gain vs Temperature
for Supply VoltagesChange in Trimmed Input
Offset Voltage vs TemperatureUntrimmed Input Offset
Voltage vs TemperatureInput Offset Current
vs TemperatureInput Bias Current
vs TemperatureStabilization Time of
Input Offset Voltage
from Power Turn-On

TL/H/10474-6

Output Voltage Swing
vs Frequency (Note 1)Frequency Response for
Various Closed Loop
Gain (Note 1)

Transient Response Test Circuit

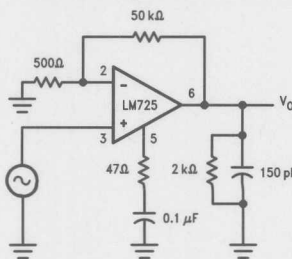




Note 1: Performance is shown using recommended compensation networks.

TL/H/10474-7

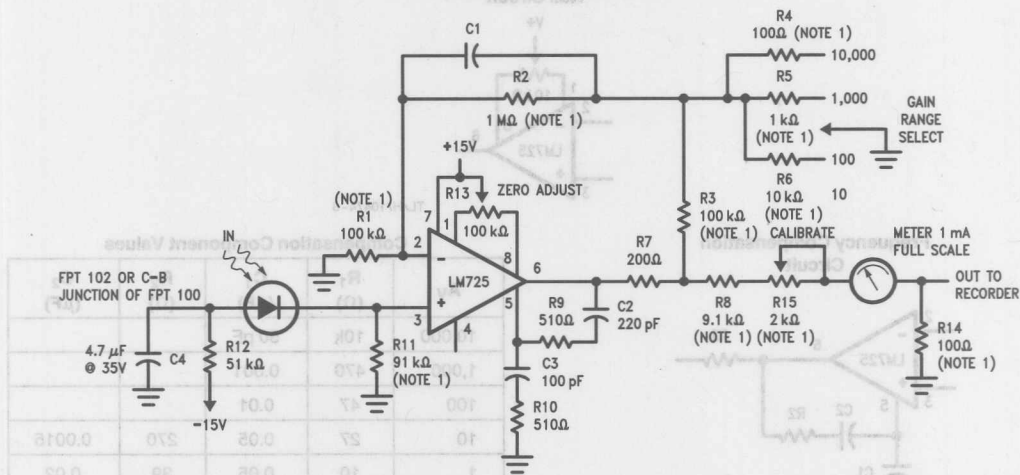
Transient Response Test Circuit



TL/H/10474-8

Typical Applications

Photodiode Amplifier

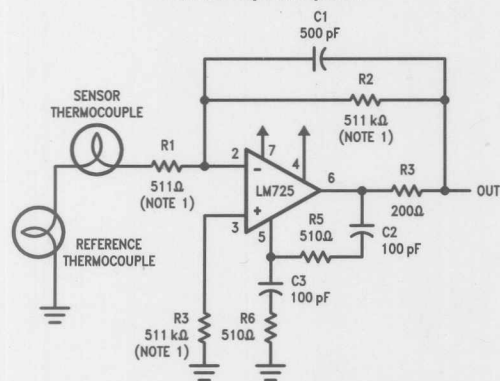


DC Gains = 10,000; 1,000; 100; and 10

Bandwidth = Determined by value of C1

TL/H/10474-9

Thermocouple Amplifier



TL/H/10474-10

$$\frac{R2}{R5} = \frac{R6}{R7} \text{ for best CMR}$$

$$R1 = R4$$

$$R2 = R5$$

$$\text{Gain} = \frac{R6}{R2} + \left(\frac{2R1}{R3} \right)$$

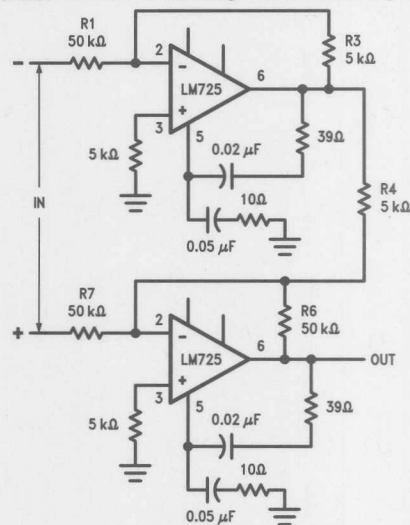
DC Gain = 1000

Bandwidth = DC to 540 Hz

Equivalent Input Noise = 0.24 μV_{rms}

Note 1: Indicates ±1% metal film resistors recommended for temperature stability.

±100V Common Mode Range Differential Amplifier

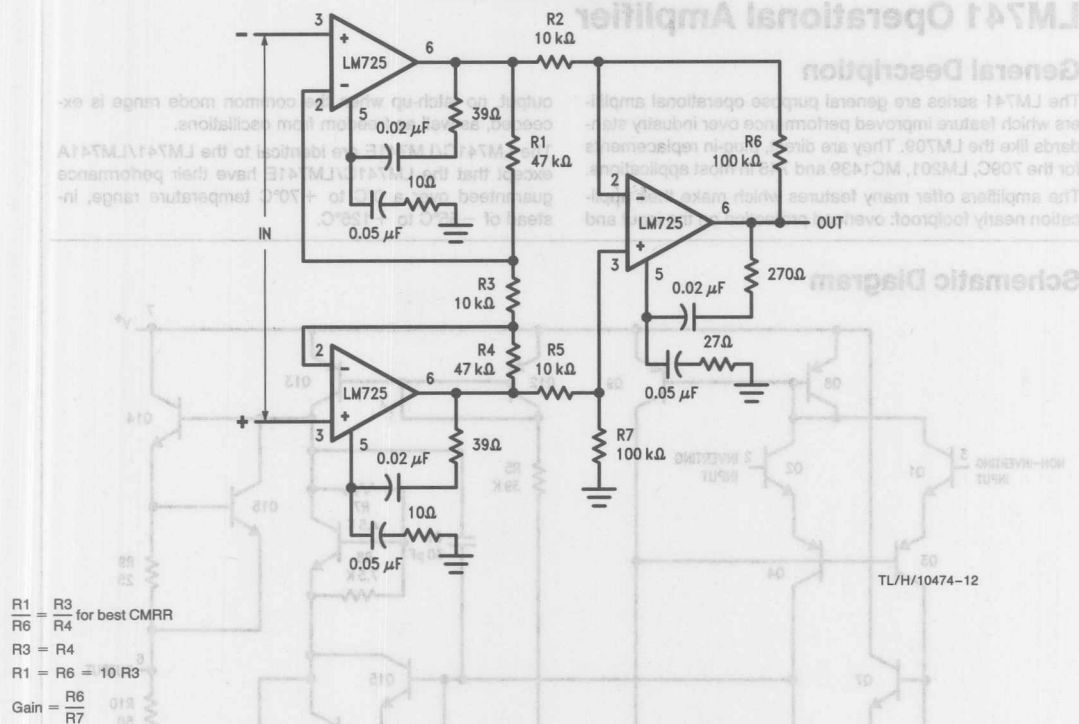


TL/H/10474-11

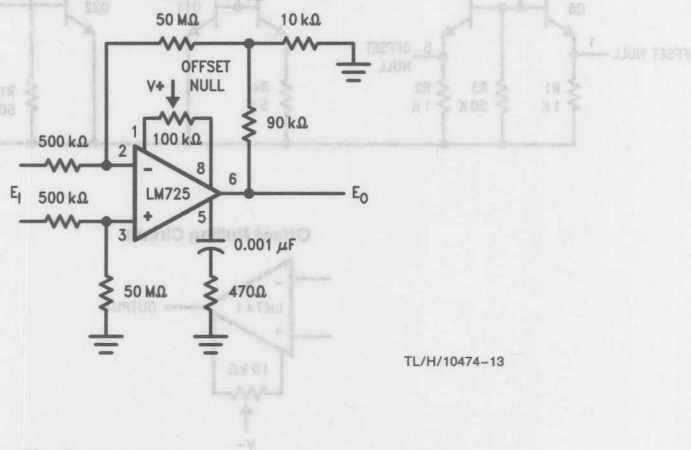
Typical Applications (Continued)

LM725

Instrumentation Amplifier with High Common Mode Rejection



Precision Amplifier $A_{VCL} = 1000$





LM741 Operational Amplifier

General Description

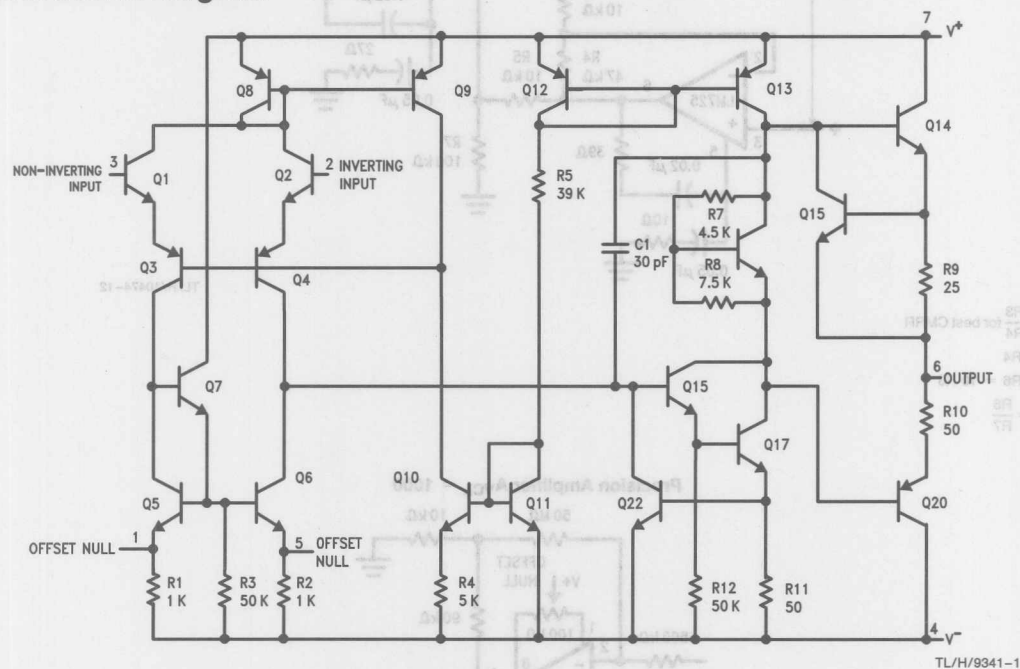
The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and

output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to $+70^{\circ}\text{C}$ temperature range, instead of -55°C to $+125^{\circ}\text{C}$.

Schematic Diagram



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/
Distributors for availability and specifications.

(Note 5)

| | LM741A | LM741E | LM741 | LM741C |
|-------------------------------|-----------------|-----------------|-----------------|-----------------|
| Supply Voltage | ±22V | ±22V | ±22V | ±18V |
| Power Dissipation (Note 1) | 500 mW | 500 mW | 500 mW | 500 mW |
| Differential Input Voltage | ±30V | ±30V | ±30V | ±30V |
| Input Voltage (Note 2) | ±15V | ±15V | ±15V | ±15V |
| Output Short Circuit Duration | Continuous | Continuous | Continuous | Continuous |
| Operating Temperature Range | -55°C to +125°C | 0°C to +70°C | -55°C to +125°C | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C | -65°C to +150°C | -65°C to +150°C | -65°C to +150°C |
| Junction Temperature | 150°C | 100°C | 150°C | 100°C |
| Soldering Information | | | | |
| N-Package (10 seconds) | 260°C | 260°C | 260°C | 260°C |
| J- or H-Package (10 seconds) | 300°C | 300°C | 300°C | 300°C |
| M-Package | | | | |
| Vapor Phase (60 seconds) | 215°C | 215°C | 215°C | 215°C |
| Infrared (15 seconds) | 215°C | 215°C | 215°C | 215°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | | | | |
|------------------------|------|------|------|------|
| ESD Tolerance (Note 6) | 400V | 400V | 400V | 400V |
|------------------------|------|------|------|------|

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM741A/LM741E | | | LM741 | | | LM741C | | | Units |
|---------------------------------------|--|---------------|-----|-------|-------|-----|-----|--------|-----|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$ | | | | | | | | | | |
| | $R_S \leq 10\text{ k}\Omega$ | | 0.8 | 3.0 | | 1.0 | 5.0 | | 2.0 | 6.0 | mV |
| | $R_S \leq 50\Omega$ | | | | | | | | | | mV |
| Average Input Offset Voltage Drift | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | 4.0 | | | | | | | mV |
| | $R_S \leq 50\Omega$ | | | | | | | | | | mV |
| | $R_S \leq 10\text{ k}\Omega$ | | | | | | 6.0 | | | 7.5 | mV |
| Average Input Offset Current Drift | | | | 15 | | | | | | | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Voltage Adjustment Range | $T_A = 25^\circ\text{C}, V_S = \pm 20\text{V}$ | ±10 | | | ±15 | | | ±15 | | | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 3.0 | 30 | | 20 | 200 | | 20 | 200 | nA |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | 70 | | 85 | 500 | | | 300 | nA |
| Average Input Offset Current Drift | | | | 0.5 | | | | | | | $\text{nA}/^\circ\text{C}$ |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 30 | 80 | | 80 | 500 | | 80 | 500 | nA |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | 0.210 | | | 1.5 | | | 0.8 | μA |
| Input Resistance | $T_A = 25^\circ\text{C}, V_S = \pm 20\text{V}$ | 1.0 | 6.0 | | 0.3 | 2.0 | | 0.3 | 2.0 | | M Ω |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}, V_S = \pm 20\text{V}$ | | 0.5 | | | | | | | | M Ω |
| Input Voltage Range | $T_A = 25^\circ\text{C}$ | | | | | | | ±12 | ±13 | | V |
| | $T_{AMIN} \leq T_A \leq T_{AMAX}$ | | | | ±12 | ±13 | | | | | V |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}, R_L \geq 2\text{ k}\Omega$ | | | | | | | | | | |
| | $V_S = \pm 20\text{V}, V_O = \pm 15\text{V}$ | 50 | | | 50 | 200 | | 20 | 200 | | V/mV |
| | $V_S = \pm 15\text{V}, V_O = \pm 10\text{V}$ | | | | | | | | | | V/mV |
| | $V_S = \pm 5\text{V}, V_O = \pm 2\text{V}$ | | | | | | | | | | V/mV |
| Large Signal Voltage Gain | $T_{AMIN} \leq T_A \leq T_{AMAX}, R_L \geq 2\text{ k}\Omega$ | | | | | | | | | | |
| | $V_S = \pm 20\text{V}, V_O = \pm 15\text{V}$ | 32 | | | 25 | | | 15 | | | V/mV |
| | $V_S = \pm 15\text{V}, V_O = \pm 10\text{V}$ | | | | | | | | | | V/mV |
| | $V_S = \pm 5\text{V}, V_O = \pm 2\text{V}$ | 10 | | | | | | | | | V/mV |

| Parameter | Conditions | LM741A/LM741E | | | LM741 | | | LM741C | | | Units |
|--|---|----------------------|-------------|------------|----------------------|----------------------|-----------|----------------------|----------------------|-----|--------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Voltage Swing | $V_S = \pm 20V$ $R_L \geq 10\text{ k}\Omega$ $R_L \geq 2\text{ k}\Omega$ | ± 16 ± 15 | | | | | | | | | V V |
| | $V_S = \pm 15V$ $R_L \geq 10\text{ k}\Omega$ $R_L \geq 2\text{ k}\Omega$ | | | | ± 12 ± 10 | ± 14 ± 13 | | ± 12 ± 10 | ± 14 ± 13 | | V V |
| Output Short Circuit Current | $T_A = 25^\circ\text{C}$ $T_{AMIN} \leq T_A \leq T_{AMAX}$ | 10 10 | 25 | 35 40 | | 25 | | | 25 | | mA mA |
| Common-Mode Rejection Ratio | $T_{AMIN} \leq T_A \leq T_{AMAX}$ $R_S \leq 10\text{ k}\Omega$, $V_{CM} = \pm 12V$ | | | | 70 | 90 | | 70 | 90 | | dB |
| | $R_S \leq 50\Omega$, $V_{CM} = \pm 12V$ | 80 | 95 | | | | | | | | dB |
| Supply Voltage Rejection Ratio | $T_{AMIN} \leq T_A \leq T_{AMAX}$ $V_S = \pm 20V$ to $V_S = \pm 5V$ $R_S \leq 50\Omega$ $R_S \leq 10\text{ k}\Omega$ | | | | | | | | | | dB |
| | | 86 | 96 | | 77 | 96 | | 77 | 96 | | dB |
| Transient Response Rise Time Overshoot | $T_A = 25^\circ\text{C}$, Unity Gain | | 0.25 6.0 | 0.8 20 | | 0.3 5 | | | 0.3 5 | | μs % |
| | | | | | | | | | | | |
| Bandwidth (Note 4) | $T_A = 25^\circ\text{C}$ | 0.437 | 1.5 | | | | | | | | MHz |
| Slew Rate | $T_A = 25^\circ\text{C}$, Unity Gain | 0.3 | 0.7 | | | 0.5 | | | 0.5 | | V/ μs |
| Supply Current | $T_A = 25^\circ\text{C}$ | | | | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| Power Consumption | $T_A = 25^\circ\text{C}$ $V_S = \pm 20V$ $V_S = \pm 15V$ | | 80 | 150 | | | | | | | mW mW |
| | | | | | | 50 | 85 | | 50 | 85 | mW |
| LM741A | $V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$ | | | 165 135 | | | | | | | mW mW |
| | | | | | | | | | | | |
| LM741E | $V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$ | | | 150 150 | | | | | | | mW mW |
| | | | | | | | | | | | |
| LM741 | $V_S = \pm 15V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$ | | | | | 60 45 | 100 75 | | | | mW mW |
| | | | | | | | | | | | |

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_J max. (listed under "Absolute Maximum Ratings"). $T_J = T_A + (\theta_{JA} P_D)$.

| Thermal Resistance | Cerdip (J) | DIP (N) | HO8 (H) | SO-8 (M) |
|-------------------------------------|------------|---------|---------|----------|
| θ_{JA} (Junction to Ambient) | 100°C/W | 100°C/W | 170°C/W | 195°C/W |
| θ_{JC} (Junction to Case) | N/A | N/A | 25°C/W | N/A |

Note 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

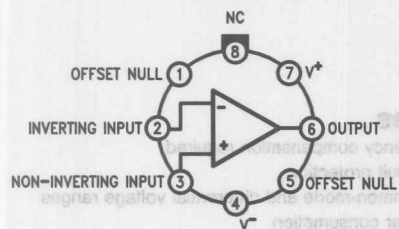
Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 k Ω in series with 100 pF.

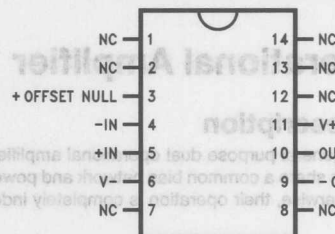
Metal Can Package



TL/H/9341-2

Order Number LM741H, LM741H/883*,
LM741AH/883 or LM741CH
See NS Package Number H08C

Ceramic Dual-In-Line Package



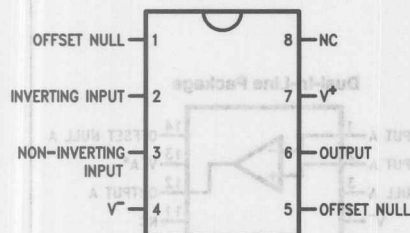
TL/H/9341-5

Order Number LM741J-14/883*, LM741AJ-14/883**
See NS Package Number J14A

*also available per JM38510/10101

**also available per JM38510/10102

Dual-In-Line or S.O. Package



TL/H/9341-3

Order Number LM741J, LM741J/883,
LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

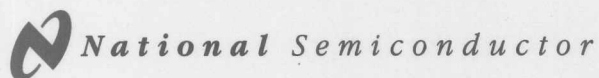
Ceramic Flatpak



TL/H/9341-6

Order Number LM741W/883
See NS Package Number W10A

*LM741H is available per JM38510/10101



LM747 Dual Operational Amplifier

General Description

The LM747 is a general purpose dual operational amplifier. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

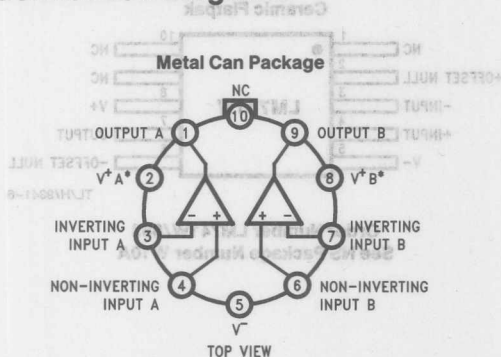
Additional features of the LM747 are: no latch-up when input common mode range is exceeded, freedom from oscillations, and package flexibility.

The LM747C/LM747E is identical to the LM747/LM747A except that the LM747C/LM747E has its specifications guaranteed over the temperature range from 0°C to +70°C* instead of -55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low power consumption
- No latch-up
- Balanced offset null

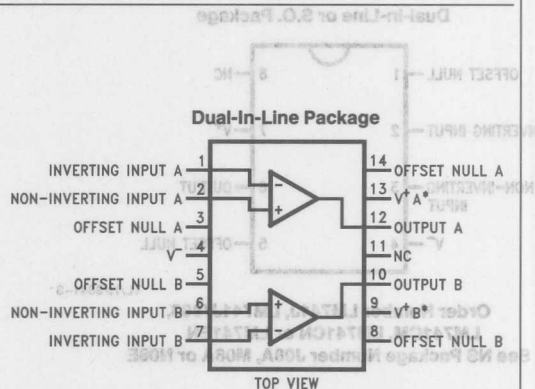
Connection Diagrams



Order Number LM747H
See NS Package Number H10C

*V+ A and V+ B are internally connected.

TL/H/11479-4



Order Number LM747CN or LM747EN
See NS Package Number N14A

TL/H/11479-5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage
LM747/LM747A
LM747C/LM747E

±22V

±18V

Power Dissipation (Note 1)
Differential Input Voltage

800 mW

±30V

Input Voltage (Note 2)

±15V

Output Short-Circuit Duration

Indefinite

Operating Temperature Range

-55°C to +125°C

LM747/LM747A

LM747C/LM747E

0°C to +70°C

Storage Temperature Range

-65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

300°C

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM747A/LM747E | | | LM747 | | | LM747C | | | Units |
|---------------------------------------|--|---------------|-----|-------|-------|-----|-----|--------|-----|-----|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$ | | | | | | | | | | |
| | $R_S \leq 10\text{ k}\Omega$ | | | | 1.0 | | 5.0 | 2.0 | | 6.0 | mV |
| | $R_S \leq 50\Omega$ | | 0.8 | 3.0 | | | | | | | |
| | $R_S \leq 50\Omega$ | | | 4.0 | | | | | | 7.5 | mV |
| | $R_S \leq 10\text{ k}\Omega$ | | | | | | 6.0 | | | | |
| Average Input Offset Voltage Drift | | | | 15 | | | | | | | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Voltage Adjustment Range | $T_A = 25^\circ\text{C}, V_S = \pm 20\text{V}$ | ±10 | | | ±15 | | | ±15 | | | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 3.0 | 30 | | 20 | 200 | | 20 | 200 | nA |
| | | | | 70 | | 85 | 500 | | | 300 | |
| Average Input Offset Current Drift | | | | 0.5 | | | | | | | $\text{nA}/^\circ\text{C}$ |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 30 | 80 | | 80 | 500 | | 80 | 500 | nA |
| | $T_{\text{AMIN}} \leq T_A \leq T_{\text{AMAX}}$ | | | 0.210 | | | 1.5 | | | 0.8 | μA |
| Input Resistance | $T_A = 25^\circ\text{C}, V_S = \pm 20\text{V}$ | 1.0 | 6.0 | | 0.3 | 2.0 | | 0.3 | 2.0 | | $\text{M}\Omega$ |
| | $V_S = \pm 20\text{V}$ | | 0.5 | | | | | | | | |
| Input Voltage Range | $T_A = 25^\circ\text{C}$ | | | | | | | ±12 | ±13 | | V |
| | | ±12 | ±13 | | ±12 | ±13 | | | | | |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}, R_L \geq 2\text{ k}\Omega$ | | | | | | | | | | |
| | $V_S = \pm 20\text{V}, V_O = \pm 15\text{V}$ | 50 | | | | | | | | | V/mV |
| | $V_S = \pm 15\text{V}, V_O = \pm 10\text{V}$ | | | | 50 | 200 | | 20 | 200 | | V/mV |
| | $R_L \geq 2\text{ k}\Omega$ | | | | | | | | | | |
| | $V_S = \pm 20\text{V}, V_O = \pm 15\text{V}$ | 32 | | | | | | | | | V/mV |
| | $V_S = \pm 15\text{V}, V_O = \pm 10\text{V}$ | | | | 25 | | | 15 | | | V/mV |
| | $V_S = \pm 5\text{V}, V_O = \pm 2\text{V}$ | 10 | | | | | | | | | V/mV |
| Output Voltage Swing | $V_S = \pm 20\text{V}$ | | | | | | | | | | |
| | $R_L \geq 10\text{ k}\Omega$ | ±16 | | | | | | | | | V |
| | $R_L \geq 2\text{ k}\Omega$ | ±15 | | | | | | | | | |
| | $V_S = \pm 15\text{V}$ | | | | ±12 | ±14 | | ±12 | ±14 | | V |
| | $R_L \geq 10\text{ k}\Omega$ | | | | ±10 | ±13 | | ±10 | ±13 | | |
| | $R_L \geq 2\text{ k}\Omega$ | | | | | | | | | | |
| | | | | | | | | | | | |
| Output Short Circuit Current | $T_A = 25^\circ\text{C}$ | 10 | 25 | 35 | | 25 | | | 25 | | mA |
| | | 10 | | 40 | | | | | | | |
| Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega, V_{\text{CM}} = \pm 12\text{V}$ | | | | 70 | 90 | | 70 | 90 | | dB |
| | $R_S \leq 50\text{ k}\Omega, V_{\text{CM}} = \pm 12\text{V}$ | 80 | 95 | | | | | | | | |

| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Unit |
|--------------------------------|---|-------|------|-----|-----|-----|-----|-----|-----|-----|------------|
| Supply Voltage Rejection Ratio | $V_S = \pm 20V$ to $V_S = \pm 5V$ $R_S \leq 50\Omega$ $R_S \leq 10 k\Omega$ | 86 | 96 | | 77 | 96 | | 77 | 96 | | dB |
| Transient Response | $T_A = 25^\circ C$, Unity Gain | | | | | | | | | | |
| Rise Time | | | 0.25 | 0.8 | | 0.3 | | | 0.3 | | μs |
| Overshoot | | | 6.0 | 20 | | 5 | | | 5 | | % |
| Bandwidth (Note 4) | $T_A = 25^\circ C$ | 0.437 | 1.5 | | | | | | | | MHz |
| Slew Rate | $T_A = 25^\circ C$, Unity Gain | 0.3 | 0.7 | | | 0.5 | | | 0.5 | | V/ μs |
| Supply Current/Amp | $T_A = 25^\circ C$ | | | 2.5 | | 1.7 | 2.8 | | 1.7 | 2.8 | mA |
| Power Consumption/Amp | $T_A = 25^\circ C$ $V_S = \pm 20V$ $V_S = \pm 15V$ | | 80 | 150 | | 50 | 85 | | 50 | 85 | mW |
| LM747A | $V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$ | | | 165 | | | | | | | mW |
| LM747E | $V_S = \pm 20V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$ | | | 150 | | | | | | | mW |
| LM747 | $V_S = \pm 15V$ $T_A = T_{AMIN}$ $T_A = T_{AMAX}$ | | | 150 | | 60 | 100 | | 45 | 75 | mW |

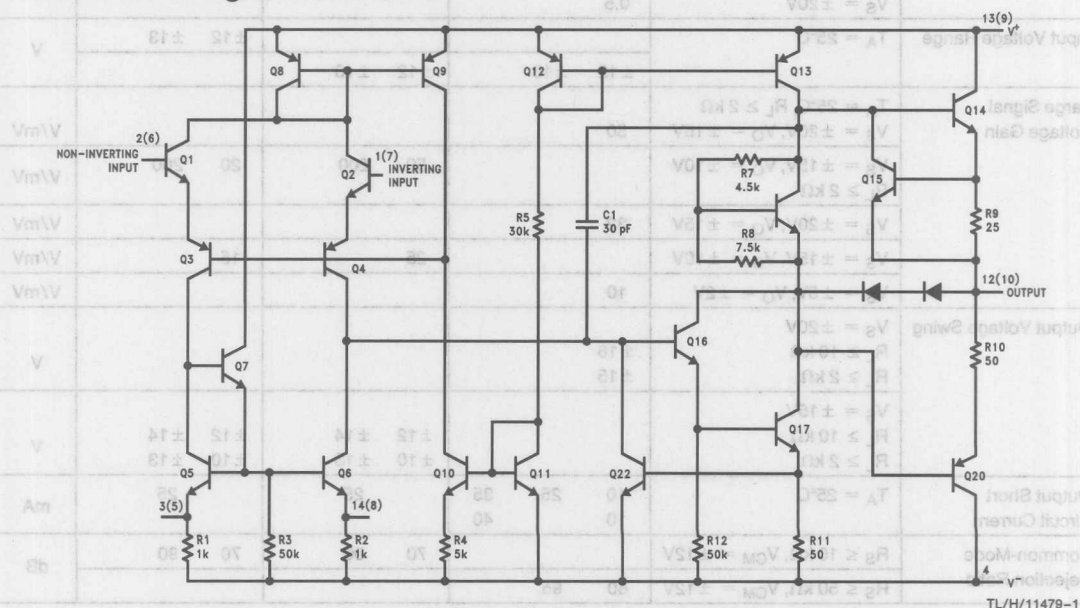
Note 1: The maximum junction temperature of the LM747C/LM747E is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $\pm 5V \leq V_S \leq \pm 20V$ and $-55^\circ C \leq T_A \leq 125^\circ C$ for the LM747A and $0^\circ C \leq T_A \leq 70^\circ C$ for the LM747E unless otherwise specified. The LM747 and LM747C are specified for $V_S = \pm 15V$ and $-55^\circ C \leq T_A \leq 125^\circ C$ and $0^\circ C \leq T_A \leq 70^\circ C$, respectively, unless otherwise specified.

Note 4: Calculated value from: $0.35/\text{Rise Time}$ (μs).

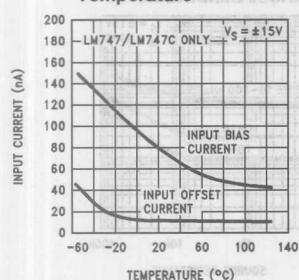
Schematic Diagram (Each Amplifier)



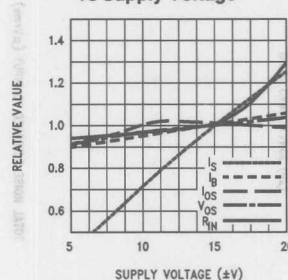
Note: Numbers in parentheses are pin numbers for amplifier B. DIP only.

Typical Performance Characteristics

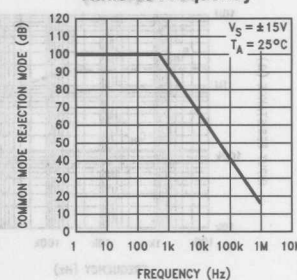
Input Bias and Offset Currents vs Ambient Temperature



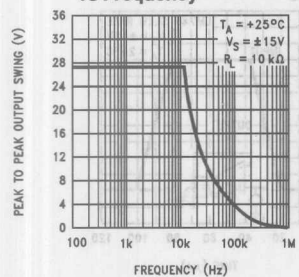
DC Parameters vs Supply Voltage



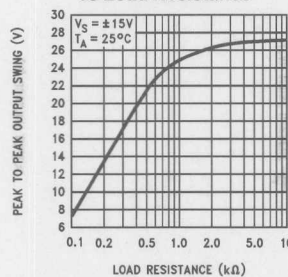
Common Mode Rejection Ratio vs Frequency



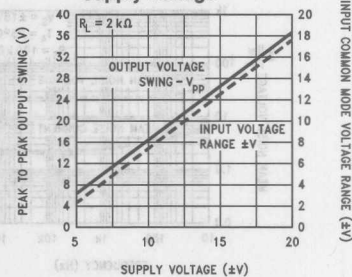
Output Voltage Swing vs Frequency



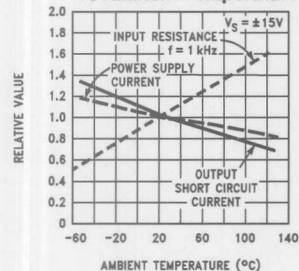
Output Voltage Swing vs Load Resistance



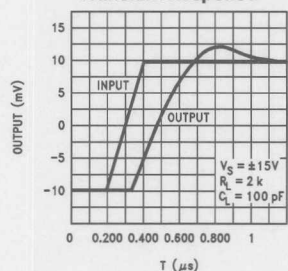
Output Swing and Input Range vs Supply Voltage



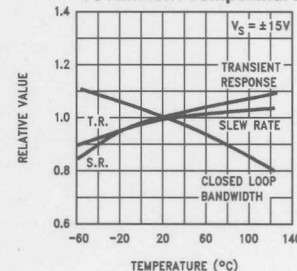
Normalized DC Parameters vs Ambient Temperature



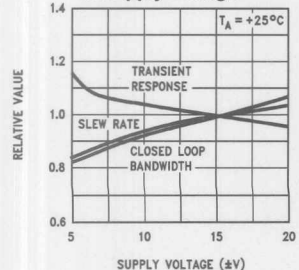
Transient Response



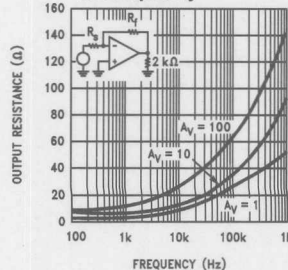
Frequency Characteristics vs Ambient Temperature



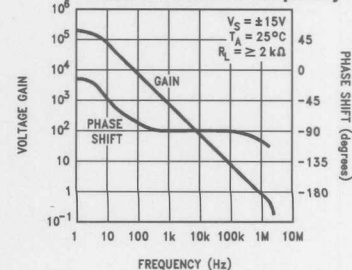
Frequency Characteristics vs Supply Voltage



Output Resistance vs Frequency



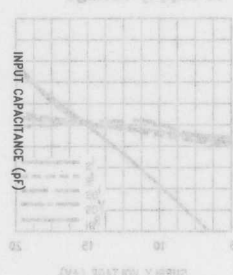
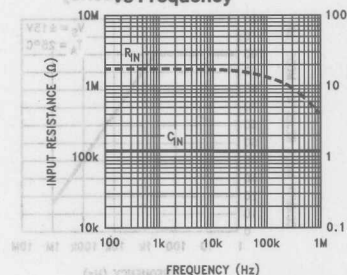
Open Loop Transfer Characteristics vs Frequency



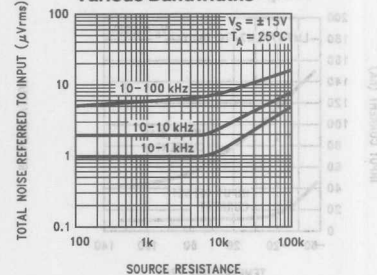
TL/H/11479-2

Typical Performance Characteristics (Continued)

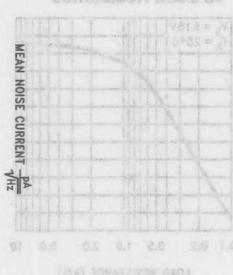
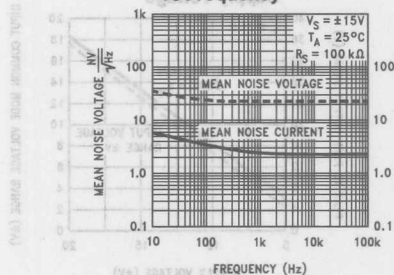
Input Resistance and Input Capacitance vs Frequency



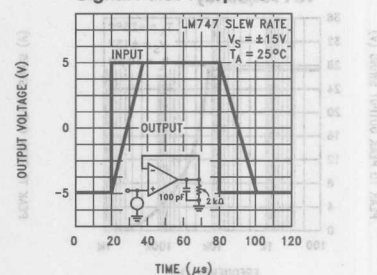
Broadband Noise for Various Bandwidths



Input Noise Voltage and Current vs Frequency

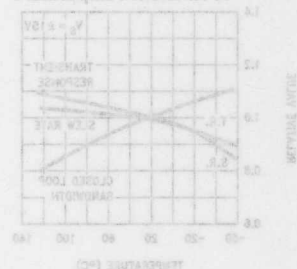


Voltage Follower Large Signal Pulse Response

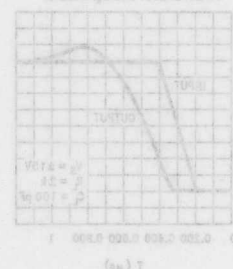


TL/H/11479-3

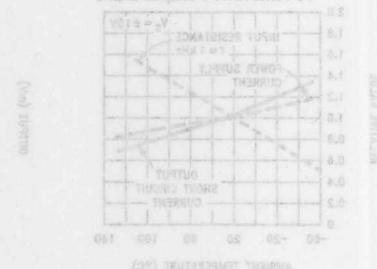
Frequency Characteristics vs Ambient Temperature



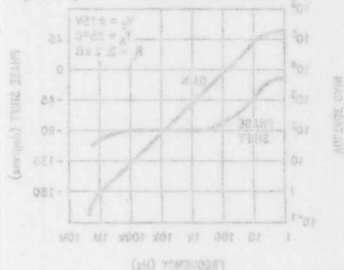
Transient Response



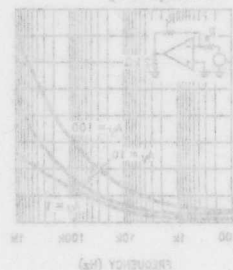
Normalized DC Parameters vs Ambient Temperature



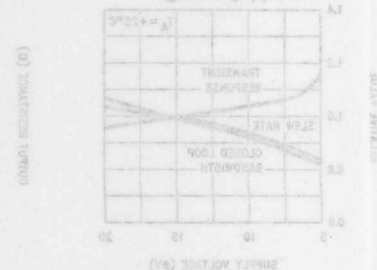
Open Loop Transfer Characteristics vs Frequency



Output Resistance vs Frequency



Frequency Characteristics vs Supply Voltage





LM748 Operational Amplifier

General Description

The LM748 is a general purpose operational amplifier with external frequency compensation.

The unity-gain compensation specified makes the circuit stable for all feedback configurations, even with capacitive loads. It is possible to optimize compensation for best high frequency performance at any gain. As a comparator, the output can be clamped at any desired level to make it compatible with logic circuits.

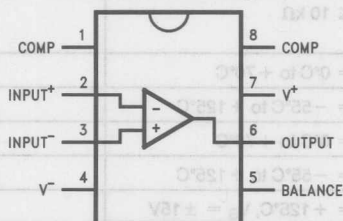
The LM748C is specified for operation over the 0°C to +70°C temperature range.

Features

- Frequency compensation with a single 30 pF capacitor
- Operation from $\pm 5\text{V}$ to $\pm 20\text{V}$
- Continuous short-circuit protection
- Operation as a comparator with differential inputs as high as $\pm 30\text{V}$
- No latch-up when common mode range is exceeded
- Same pin configuration as the LM101

Connection Diagram

Dual-In-Line Package



Top View

Order Number LM748CN
See NS Package Number N08B

TL/H/11478-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|----------------------------|--------|
| Supply Voltage | ±22V |
| Power Dissipation (Note 1) | 500 mW |
| Differential Input Voltage | ±30V |

| | |
|--|-----------------|
| Input Voltage (Note 2) | ±15V |
| Output Short-Circuit Duration (Note 3) | |
| Operating Temperature Range: | |
| LM748C | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | +300°C |

Electrical Characteristics (Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|-----|-----|------|------------------------------|
| Input Offset Voltage | $T_A = 25^\circ\text{C}$, $R_S \leq 10\text{ k}\Omega$ | | 1.0 | 5.0 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 40 | 200 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 120 | 500 | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 300 | 800 | | k Ω |
| Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ | | 1.8 | 2.8 | mA |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{ k}\Omega$ | 50 | 160 | | V/mV |
| Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | | 6.0 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $R_S \leq 50\Omega$ | | 3.0 | | $\mu\text{V}/^\circ\text{C}$ |
| | $R_S \leq 10\text{ k}\Omega$ | | 6.0 | | $\mu\text{V}/^\circ\text{C}$ |
| Input Offset Current | $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | | | 300 | nA |
| | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 500 | nA |
| Input Bias Current | $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | | | 0.8 | μA |
| | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | | | 1.5 | μA |
| Supply Current | $T_A = +125^\circ\text{C}$, $V_S = \pm 15\text{V}$ | | 1.2 | 2.25 | mA |
| | $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ | | 1.9 | 3.3 | mA |
| Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{ k}\Omega$ | 25 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{ k}\Omega$ | ±12 | ±14 | | V |
| | $V_S = \pm 15\text{V}$, $R_L = 2\text{ k}\Omega$ | ±10 | ±13 | | V |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | ±12 | | | V |
| Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 77 | 90 | | dB |

Note 1: For operating at elevated temperatures, the device must be derated based on a maximum junction to case thermal resistance of 45°C per watt, or 150°C per watt junction to ambient. (See Curves).

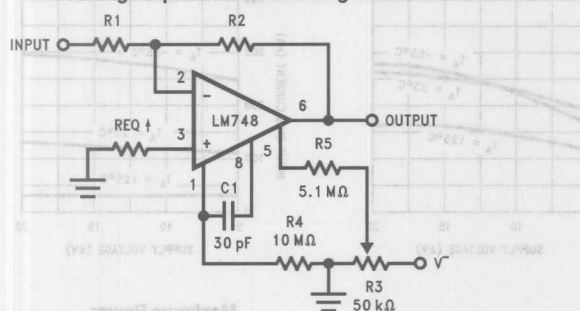
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to +125°C and ambient temperatures to +70°C.

Note 4: These specifications apply for $\pm 5\text{V} \leq V_S \leq +15\text{V}$ and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, unless otherwise specified.

Typical Applications

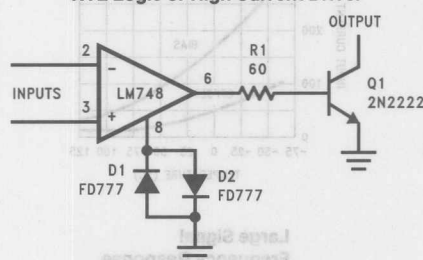
Inverting Amplifier with Balancing Circuit



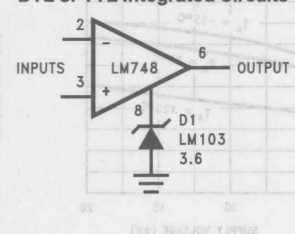
†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

TL/H/11478-3

Voltage Comparator for Driving RTL Logic or High Current Driver

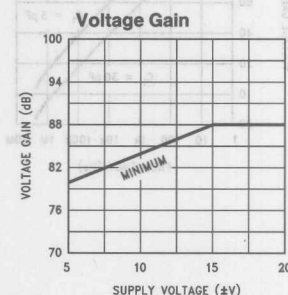
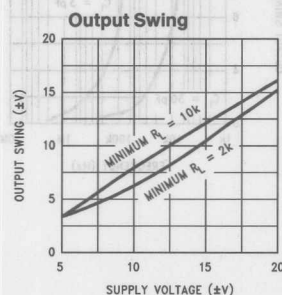
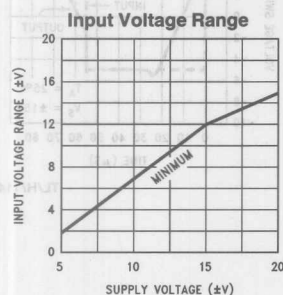


Voltage Comparator for Driving DTL or TTL Integrated Circuits



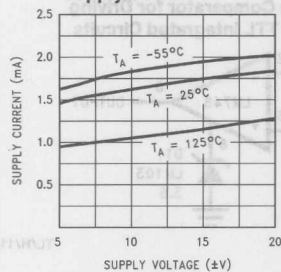
TL/H/11478-4

Guaranteed Performance Characteristics (Note 4)

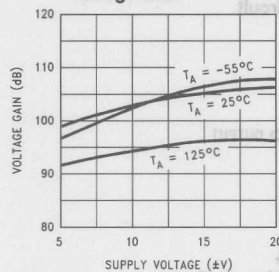


TL/H/11478-6

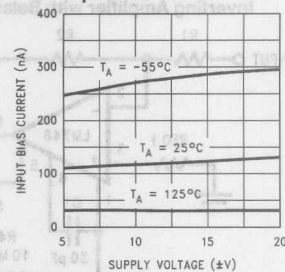
Supply Current



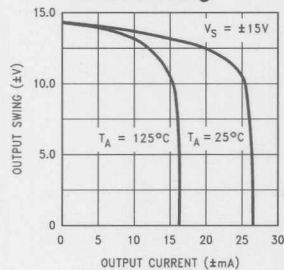
Voltage Gain



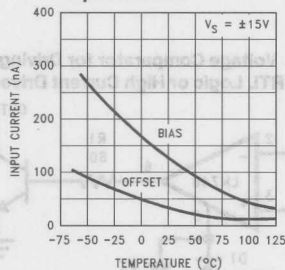
Input Bias Current



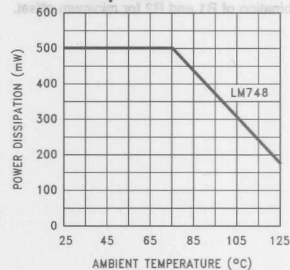
Current Limiting



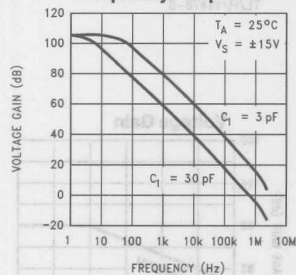
Input Current



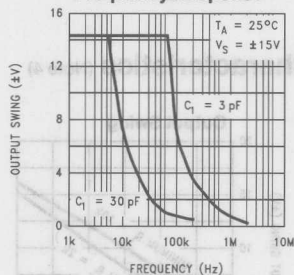
Maximum Power Dissipation



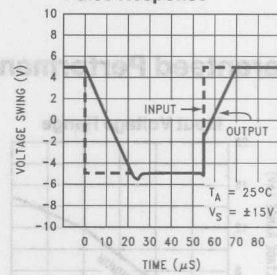
Open Loop Frequency Response



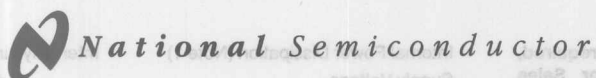
Large Signal Frequency Response



Voltage Follower Pulse Response



TL/H/11478-7



LM759/LM77000 Power Operational Amplifiers

General Description

The LM759 and LM77000 are high performance operational amplifiers that feature high output current capability. The LM759 is capable of providing 325 mA and the LM77000 providing 250 mA. Both amplifiers feature small signal characteristics that are better than the LM741. The amplifiers are designed to operate from a single or dual power supply with an input common mode range that includes the negative supply. The high gain and high output power provide superior performance. Internal current limiting, thermal shut-down, and safe area compensation are employed making the LM759 and LM77000 essentially indestructible.

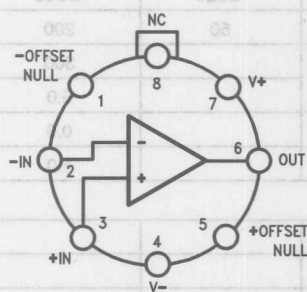
Features

- Output current
LM759—325 mA minimum
LM77000—250 mA minimum
- Internal short circuit current limiting
- Internal thermal overload protection
- Internal output transistors safe-area protection
- Input common mode voltage range includes ground or negative supply

Applications

- Voltage regulators
- Audio amplifiers
- Servo amplifiers
- Power drivers

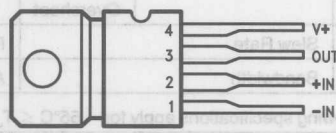
Connection Diagrams and Ordering Information



Lead 4 connected to case.

Top View

Order Number LM759MH, LM759CH or LM759H/883
See NS Package Number H08C



Top View

Order Number LM759CP or LM77000CP
See NS Package Number P04A

LM759/LM77000

1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------|-----------------|
| Storage Temperature Range | |
| Metal Can | -65°C to +175°C |
| Plastic Package | -65°C to +150°C |

| | |
|--------------------------------------|-----------------|
| Operating Junction Temperature Range | |
| Military (LM759M) | -55°C to +150°C |
| Commercial (LM759C, LM77000C) | 0°C to +125°C |

| | |
|-------------------------------------|-------|
| Lead Temperature | |
| Metal Can (soldering, 60 sec) | 300°C |
| Plastic Package (soldering, 10 sec) | 265°C |

| | |
|-------------------------------------|--------------------|
| Internal Power Dissipation (Note 1) | Internally Limited |
| Supply Voltage | ±18V |
| Differential Input Voltage | 30V |
| Input Voltage (note 2) | ±15V |

LM759

Electrical Characteristics $T_J = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------|------------------------------|---|---------------------------|---------------------------|-----|------------------|
| V_{IO} | Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | 1.0 | 3.0 | mV |
| I_{IO} | Input Offset Current | | | 5.0 | 30 | nA |
| I_{IB} | Input Bias Current | | | 50 | 150 | nA |
| Z_i | Input Impedance | | 0.25 | 1.5 | | M Ω |
| I_{CC} | Supply Current | | | 12 | 18 | mA |
| V_{IR} | Input Voltage Range | | $V^+ - 2\text{V to } V^-$ | $V^+ - 2\text{V to } V^-$ | | V |
| I_{OS} | Output Short Circuit Current | $ V_{CC} - V_O = 30\text{V}$ | | ±200 | | mA |
| $I_{O\text{ PEAK}}$ | Peak Output Current | $3.0\text{V} \leq V_{CC} - V_O \leq 10\text{V}$ | ±325 | ±500 | | mA |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 50\Omega$, $V_O = \pm 10\text{V}$ | 50 | 200 | | V/mV |
| TR | Transient Response | $R_L = 50\Omega$, $A_V = 1.0$ | | 300 | | ns |
| | | | | 5.0 | | % |
| SR | Slew Rate | $R_L = 50\Omega$, $A_V = 1.0$ | | 0.6 | | V/ μs |
| BW | Bandwidth | $A_V = 1.0$ | | 1.0 | | MHz |

The following specifications apply for $-55^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$

| | | | | | | |
|----------|------------------------------|--|-----|-------|-----|------|
| V_{IO} | Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | | 4.5 | mV |
| I_{IO} | Input Offset Current | | | | 60 | nA |
| I_{IB} | Input Bias Current | | | | 300 | nA |
| CMRR | Common Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 80 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 80 | 100 | | dB |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 50\Omega$, $V_O = \pm 10\text{V}$ | 25 | 200 | | V/mV |
| V_{OP} | Output Voltage Swing | $R_L = 50\Omega$ | ±10 | ±12.5 | | V |

LM759C

Electrical Characteristics $T_J = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---------------------|------------------------------|---|---------------------------|---------------------------|-----|------------------|
| V_{IO} | Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | 1.0 | 6.0 | mV |
| I_{IO} | Input Offset Current | | | 5.0 | 50 | nA |
| I_{IB} | Input Bias Current | | | 50 | 250 | nA |
| Z_I | Input Impedance | | 0.25 | 1.5 | | M Ω |
| I_{CC} | Supply Current | | | 12 | 18 | mA |
| V_{IR} | Input Voltage Range | | $V^+ - 2\text{V to } V^-$ | $V^+ - 2\text{V to } V^-$ | | V |
| I_{OS} | Output Short Circuit Current | $ V_{CC} - V_O = 30\text{V}$ | | ± 200 | | mA |
| $I_{O\text{ PEAK}}$ | Peak Output Current | $3.0\text{V} \leq V_{CC} - V_O \leq 10\text{V}$ | ± 325 | ± 500 | | mA |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 50\Omega$, $V_O = \pm 10\text{V}$ | 25 | 200 | | V/mV |
| TR | Transient Response | $R_L = 50\Omega$, $A_V = 1.0$ | Rise Time | 300 | | ns |
| | | | Overshoot | 10 | | % |
| SR | Slew Rate | $R_L = 50\Omega$, $A_V = 1.0$ | | 0.5 | | V/ μs |
| BW | Bandwidth | $A_V = 1.0$ | | 1.0 | | MHz |

The following specifications apply for $0^\circ \leq T_J \leq +125^\circ\text{C}$

| | | | | | | |
|----------|------------------------------|--|----------|------------|-----|------|
| V_{IO} | Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | | 7.5 | mV |
| I_{IO} | Input Offset Current | | | | 100 | nA |
| I_{IB} | Input Bias Current | | | | 400 | nA |
| CMRR | Common Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 70 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 80 | 100 | | dB |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 50\Omega$, $V_O = \pm 10\text{V}$ | 25 | 200 | | V/mV |
| V_{OP} | Output Voltage Swing | $R_L = 50\Omega$ | ± 10 | ± 12.5 | | V |

Note 1: Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values which follow the EIA-659 standard.

Note 2: For a supply voltage less than 30V between V^+ and V^- , the absolute maximum input voltage is equal to the supply voltage.

Note 3: For military electrical specifications RET590X are available for LM759C.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|------------------------------|---|-----------------------|-----------------------|-----|------------------|
| V_{IO} | Input Offset Voltage | $R_S \leq 10 \text{ k}\Omega$ | | 1.0 | 8.0 | mV |
| I_{IO} | Input Offset Current | | | 5.0 | 50 | nA |
| I_{IB} | Input Bias Current | | | 50 | 250 | nA |
| Z_I | Input Impedance | | 0.25 | 1.5 | | M Ω |
| I_{CC} | Supply Current | | | 12 | 18 | mA |
| V_{IR} | Input Voltage Range | | +13 to V ⁻ | +13 to V ⁻ | | V |
| I_{OS} | Output Short Circuit Current | $ V_{CC} - V_O = 30\text{V}$ | | ± 200 | | mA |
| $I_{O \text{ PEAK}}$ | Peak Output Current | $3.0\text{V} \leq V_{CC} - V_O \leq 10\text{V}$ | ± 250 | ± 400 | | mA |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 50\Omega, V_O = \pm 10\text{V}$ | 25 | 200 | | V/mV |
| TR | Transient Response | $R_L = 50\Omega, A_V = 1.0$ | | 300 | | ns |
| | | | | 10 | | % |
| SR | Slew Rate | $R_L = 50\Omega, A_V = 1.0$ | | 0.5 | | V/ μs |
| BW | Bandwidth | $A_V = 1.0$ | | 1.0 | | MHz |

The following specifications apply for $0^\circ \leq T_J \leq +125^\circ\text{C}$

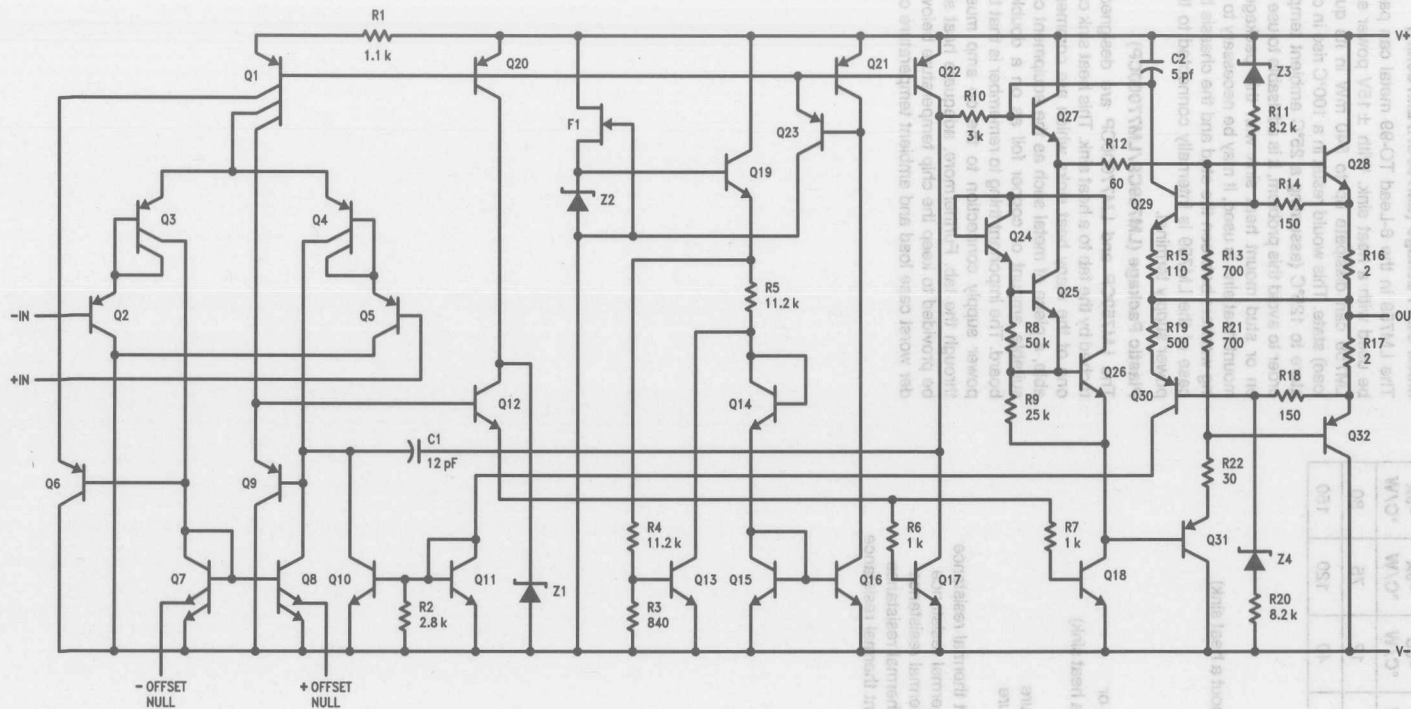
| | | | | | | |
|----------|------------------------------|---|----------|------------|-----|------|
| V_{IO} | Input Offset Voltage | $R_S \leq 10 \text{ k}\Omega$ | | | 10 | mV |
| I_{IO} | Input Offset Current | | | | 100 | nA |
| I_{IB} | Input Bias Current | | | | 400 | nA |
| CMR | Common Mode Rejection | $R_S \leq 10 \text{ k}\Omega$ | 70 | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$ | 80 | 100 | | dB |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 50\Omega, V_O = \pm 10\text{V}$ | 25 | 200 | | V/mV |
| V_{OP} | Output Voltage Swing | $R_L = 50\Omega$ | ± 10 | ± 12.5 | | V |

Note 1: Although the internal power dissipation is limited, the junction temperature must be kept below the maximum specified temperature in order to meet data sheet specifications. To calculate the maximum junction temperature or heat sink required, use the thermal resistance values which follow the Equivalent Circuit Schematic.

Note 2: For a supply voltage less than 30V between V⁺ and V⁻, the absolute maximum input voltage is equal to the supply voltage.

Note 3: For military electrical specifications RETS759X are available for LM759H.

Equivalent Circuit



Note: All resistor values in ohms.

TL/H/10075-3

| Symbol | Value | Unit |
|----------|-------|------|
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |
| A_{OL} | 100 | dB |

LM759/LM7700

| Package | Typ θ_{JC} °C/W | Max θ_{JC} °C/W | Typ θ_{JA} °C/W | Max θ_{JA} °C/W |
|---------------------|------------------------------|------------------------------|------------------------------|------------------------------|
| Plastic Package (P) | 8.0 | 12 | 75 | 80 |
| Metal Can (H) | 30 | 40 | 120 | 150 |

$$P_{D \text{ Max}} = \frac{T_{J \text{ Max}} - T_A}{\theta_{JC} + \theta_{CA}} \text{ or}$$

$$= \frac{T_{J \text{ Max}} - T_A}{\theta_{JA}} \text{ (without a heat sink)}$$

$$\theta_{CA} = \theta_{CS} + \theta_{SA}$$

Solving T_J :

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}) \text{ or}$$

$$= T_A + P_D \theta_{JA} \text{ (without a heat sink)}$$

Where:

- T_J = Junction Temperature
- T_A = Ambient Temperature
- P_D = Power Dissipation
- θ_{JA} = Junction to ambient thermal resistance
- θ_{JC} = Junction to case thermal resistance
- θ_{CA} = Case to ambient thermal resistance
- θ_{CS} = Case to heat sink thermal resistance
- θ_{SA} = Heat sink to ambient thermal resistance

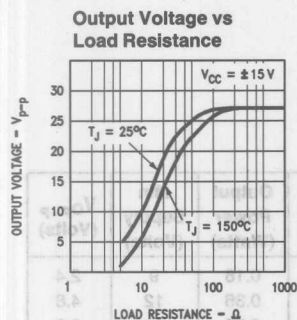
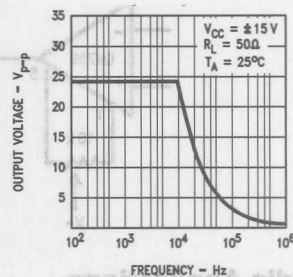
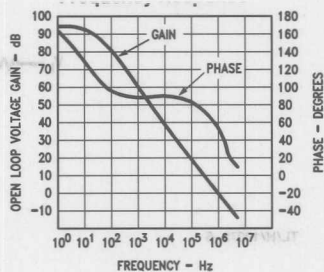
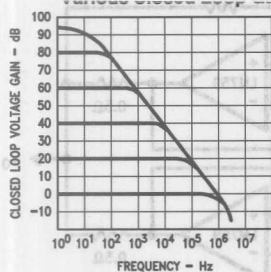
Mounting Hints

Metal Can Package (LM759CH/LM759MH)

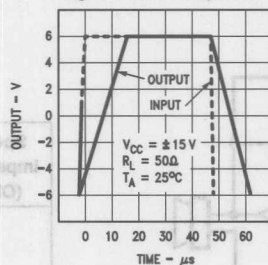
The LM759 in the 8-Lead TO-99 metal can package must be used with a heat sink. With $\pm 15V$ power supplies, the LM759 can dissipate up to 540 mW in its quiescent (no load) state. This would result in a 100°C rise in chip temperature to 125°C (assuming a 25°C ambient temperature). In order to avoid this problem, it is advisable to use either a slip on or stud mount heat sink with this package. If a stud mount heat sink is used, it may be necessary to use insulating washers between the stud and the chassis because the case of the LM759 is internally connected to the negative power supply terminal.

Plastic Package (LM759CP/LM77000CP)

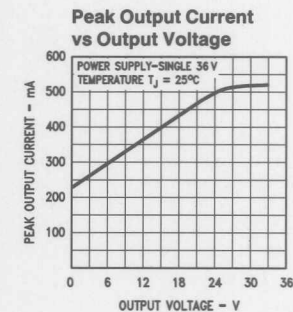
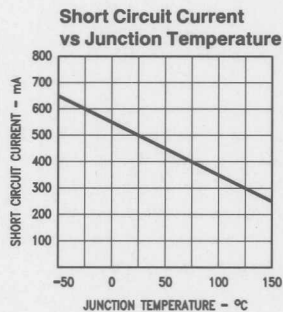
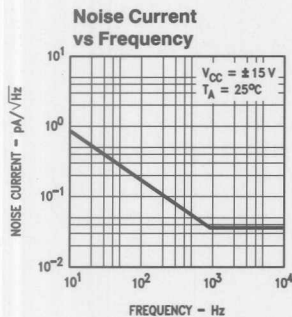
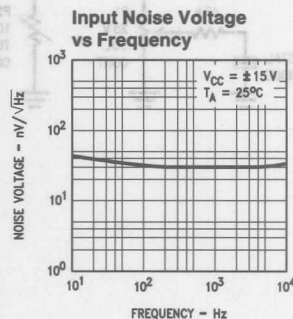
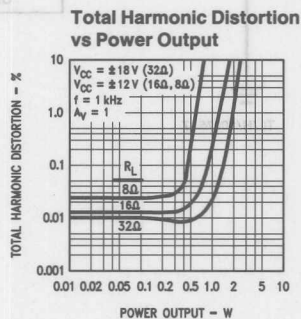
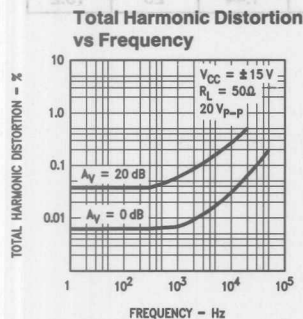
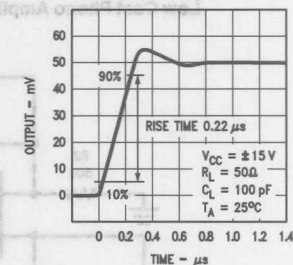
The LM759CP and LM77000CP are designed to be attached by the tab to a heat sink. This heat sink can be either one of the many heat sinks which are commercially available, a piece of metal such as the equipment chassis, or a suitable amount of copper foil as on a double sided PC board. The important thing to remember is that the negative power supply connection to the op amp must be made through the tab. Furthermore, adequate heat sinking must be provided to keep the chip temperature below 125°C under worst case load and ambient temperature conditions.



Voltage Follower Large Signal Pulse Response

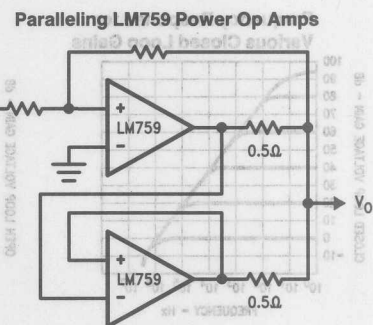
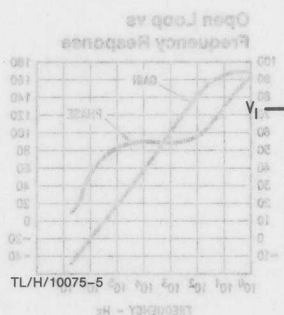
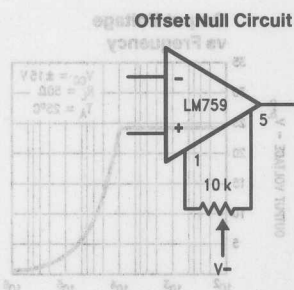


Voltage Follower Transient Response



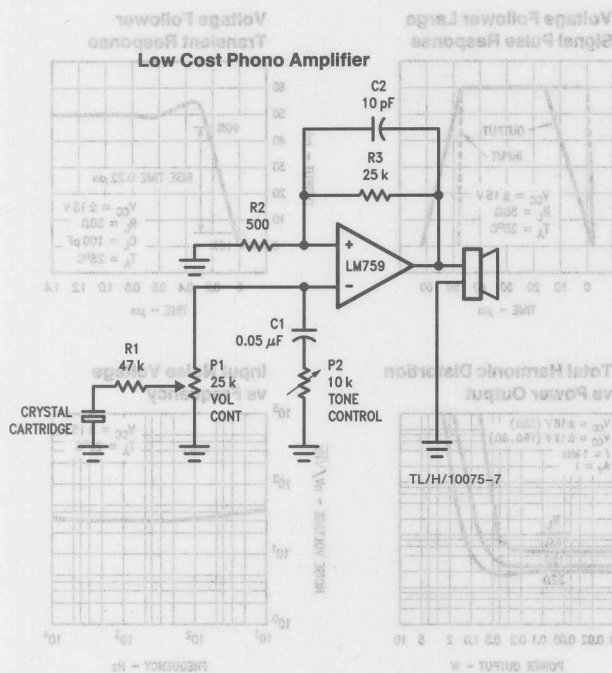
TL/H/10075-4

Applications

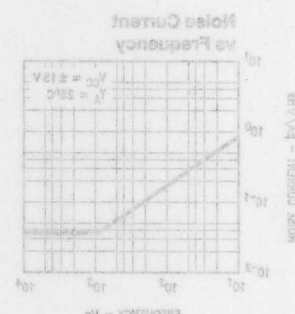
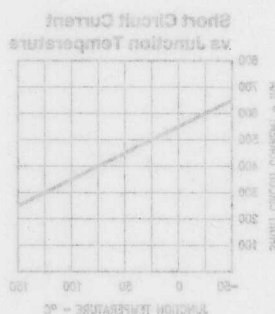
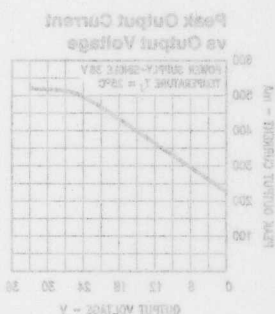


TL/H/10075-6

Audio Applications

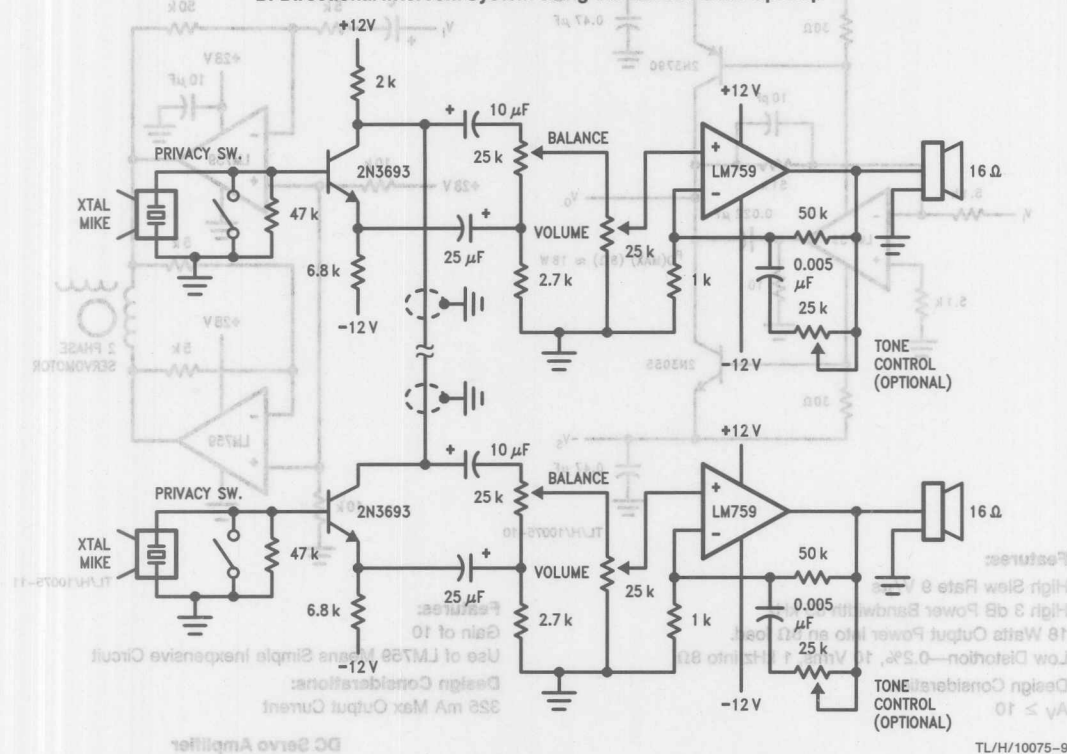


| Speaker Impedance (Ohms) | Output Power (Watts) | Min Supply (Volts) | V _{OP-P} (Volts) |
|--------------------------|----------------------|--------------------|---------------------------|
| 4 | 0.18 | 9 | 2.4 |
| 8 | 0.36 | 12 | 4.8 |
| 16 | 0.72 | 15 | 9.6 |
| 32 | 1.44 | 25 | 19.2 |



Applications (Continued)

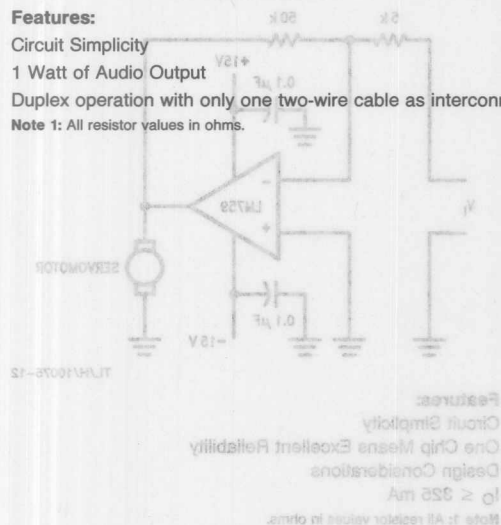
Bi-Directional Intercom System Using the LM759 Power Op Amp



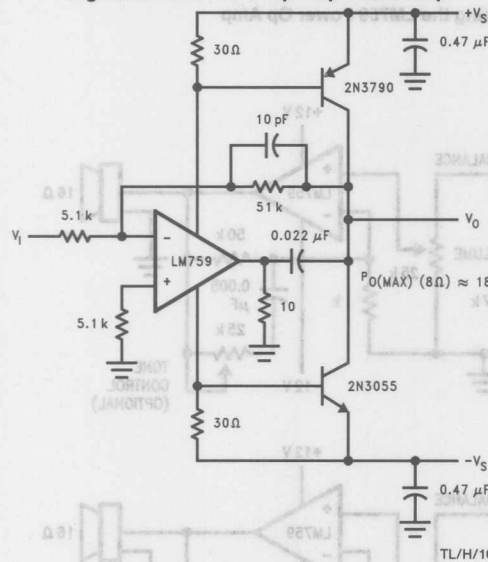
Features:

- Circuit Simplicity
- 1 Watt of Audio Output
- Duplex operation with only one two-wire cable as interconnect.

Note 1: All resistor values in ohms.



High Slew Rate Power Op Amp/Audio Amp

**Features:**

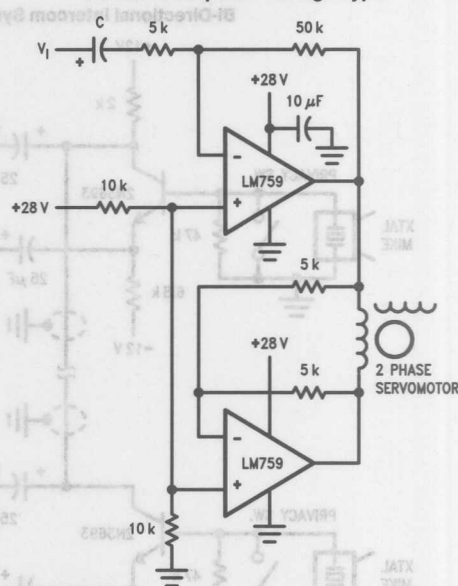
High Slew Rate $9 \text{ V}/\mu\text{s}$
 High 3 dB Power Bandwidth 85 kHz
 18 Watts Output Power into an 8Ω load.
 Low Distortion—0.2%, 10 Vrms, 1 kHz into 8Ω

Design Consideration

$A_V \geq 10$

TL/H/10075-10

AG Servo Amplifier—Bridge Type



TL/H/10075-11

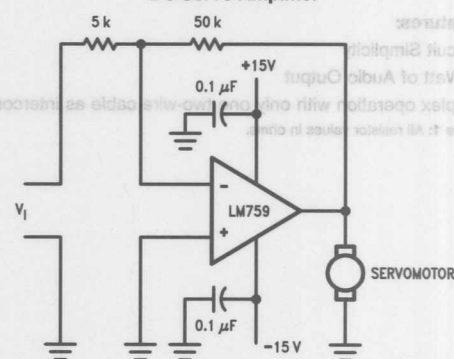
Features:

Gain of 10
 Use of LM759 Means Simple Inexpensive Circuit

Design Considerations:

325 mA Max Output Current

DC Servo Amplifier



TL/H/10075-12

Features:

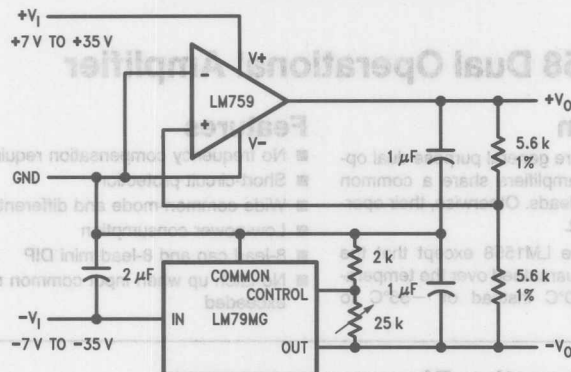
Circuit Simplicity
 One Chip Means Excellent Reliability
 Design Considerations

$I_O \leq 325 \text{ mA}$

Note 1: All resistor values in ohms.

Regulator Applications

Adjustable Dual Tracking Regulator



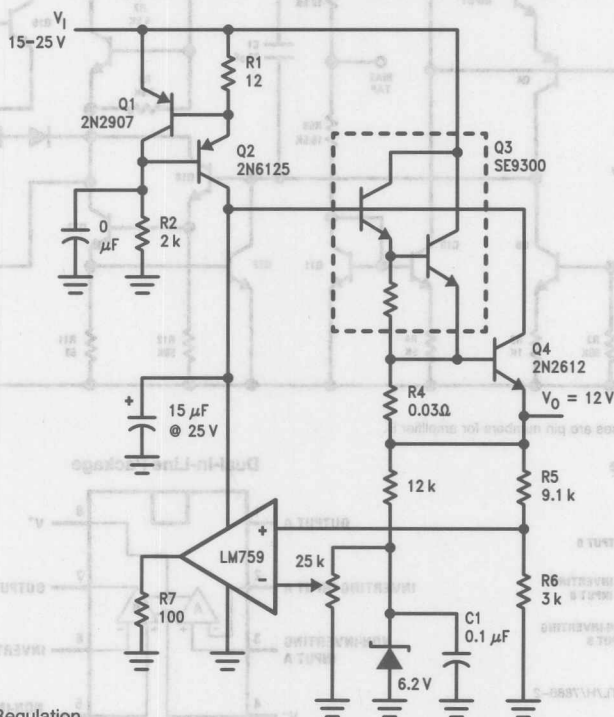
TL/H/10075-13

Features:

Wide Output Voltage Range ($\pm 2.2\text{V}$ to $\pm 30\text{V}$)Excellent Load Regulation $\Delta V_O < \pm 5\text{ mV}$ for $\Delta I_O = \pm 0.2\text{ A}$ Excellent Line Regulation $\Delta V_O < \pm 2\text{ mV}$ for $\Delta V_I = 10\text{V}$

Note 1: All resistor values in ohms.

10 Amp — 12 Volt Regulator



TL/H/10075-14

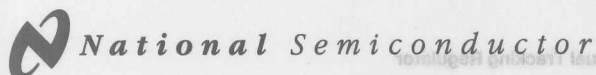
Features:

Excellent Load and Line Regulation

Excellent Temperature Coefficient-Depends

Largely on Tempco of the Reference Zener

Note 1: All resistor values in ohms.



LM1558/LM1458 Dual Operational Amplifier

General Description

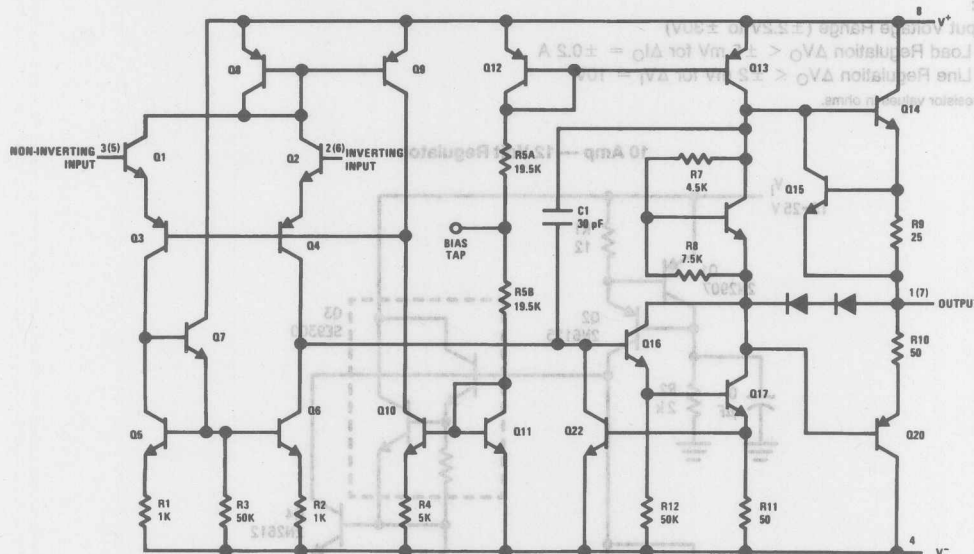
The LM1558 and the LM1458 are general purpose dual operational amplifiers. The two amplifiers share a common bias network and power supply leads. Otherwise, their operation is completely independent.

The LM1458 is identical to the LM1558 except that the LM1458 has its specifications guaranteed over the temperature range from 0°C to +70°C instead of -55°C to +125°C.

Features

- No frequency compensation required
- Short-circuit protection
- Wide common-mode and differential voltage ranges
- Low-power consumption
- 8-lead can and 8-lead mini DIP
- No latch up when input common mode range is exceeded

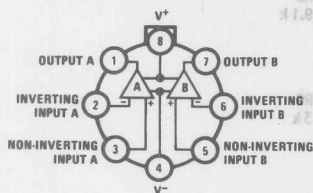
Schematic and Connection Diagrams



Note: Numbers in parentheses are pin numbers for amplifier B.

TL/H/7886-1

Metal Can Package

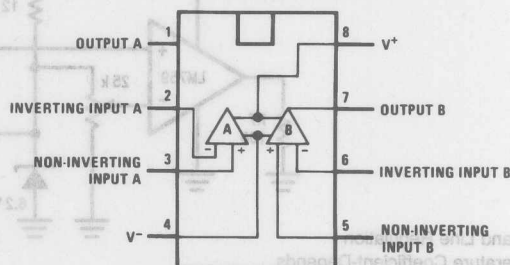


TL/H/7886-2

Top View

Order Number LM1558H,
LM1558H/883 or LM1458H
See NS Package Number H08C

Dual-In-Line Package



TL/H/7886-3

Top View

Order Number LM1558J, LM1558J/883, LM1458J, LM1458M or LM1458N
See NS Package Number J08A, M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

Supply Voltage

LM1558

±22V

LM1458

±18V

Power Dissipation (Note 1)

LM1558H/LM1458H

500 mW

LM1458N

400 mW

Differential Input Voltage

±30V

Input Voltage (Note 2)

±15V

Output Short-Circuit Duration

Continuous

Operating Temperature Range

LM1558

−55°C to +125°C

LM1458

0°C to +70°C

Storage Temperature Range

−65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

260°C

Soldering Information

Dual-In-Line Package

Soldering (10 seconds)

260°C

Small Outline Package

Vapor Phase (60 seconds)

215°C

Infrared (15 seconds)

220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD tolerance (Note 5)

300V

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM1558 | | | LM1458 | | | Units |
|--------------------------------|---|--------|-----|-----|--------|-----|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^\circ\text{C}$, $R_S \leq 10\text{ k}\Omega$ | | 1.0 | 5.0 | | 1.0 | 6.0 | mV |
| Input Offset Current | $T_A = 25^\circ\text{C}$ | | 80 | 200 | | 80 | 200 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 200 | 500 | | 200 | 500 | nA |
| Input Resistance | $T_A = 25^\circ\text{C}$ | 0.3 | 1.0 | | 0.3 | 1.0 | | M Ω |
| Supply Current Both Amplifiers | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ | | 3.0 | 5.0 | | 3.0 | 5.6 | mA |
| Large Signal Voltage Gain | $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$ $V_{OUT} = \pm 10\text{V}$, $R_L \geq 2\text{ k}\Omega$ | 50 | 160 | | 20 | 160 | | V/mV |
| Input Offset Voltage | $R_S \leq 10\text{ k}\Omega$ | | | 6.0 | | | 7.5 | mV |
| Input Offset Current | | | | 500 | | | 300 | nA |
| Input Bias Current | | | | 1.5 | | | 0.8 | μA |
| Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$ $R_L \geq \text{k}\Omega$ | 25 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{ k}\Omega$ $R_L = 2\text{ k}\Omega$ | ±12 | ±14 | | ±12 | ±14 | | V |
| | | ±10 | ±13 | | ±10 | ±13 | | V |
| Input Voltage Range | $V_S = \pm 15\text{V}$ | ±12 | | | ±12 | | | V |
| Common Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 70 | 90 | | 70 | 90 | | dB |
| Supply Voltage Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 77 | 96 | | 77 | 96 | | dB |

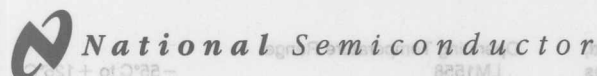
Note 1: The maximum junction temperature of the LM1558 is 150°C, while that of the LM1458 is 100°C. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 20°C/W, junction to case. For the DIP the device must be derated based on a thermal resistance of 187°C/W, junction to ambient.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: These specifications apply for $V_S = \pm 15\text{V}$ and $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$, unless otherwise specified. With the LM1458, however, all specifications are limited to $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ and $V_S = \pm 15\text{V}$.

Note 4: Refer to RETS 1558V for LM1558J and LM1558H military specifications.

Note 5: Human body model, 1.5 k Ω in series with 100 pF.



LM1875 20W Audio Power Amplifier

General Description

The LM1875 is a monolithic power amplifier offering very low distortion and high quality performance for consumer audio applications.

The LM1875 delivers 20 watts into a 4Ω or 8Ω load on $\pm 25V$ supplies. Using an 8Ω load and $\pm 30V$ supplies, over 30 watts of power may be delivered. The amplifier is designed to operate with a minimum of external components. Device overload protection consists of both internal current limit and thermal shutdown.

The LM1875 design takes advantage of advanced circuit techniques and processing to achieve extremely low distortion levels even at high output power levels. Other outstanding features include high gain, fast slew rate and a wide power bandwidth, large output voltage swing, high current capability, and a very wide supply range. The amplifier is internally compensated and stable for gains of 10 or greater.

Connection Diagram

| Am | 8.8 | 9.0 | 9.0 | 9.0 | 9.0 |
|-----|-----|-----|-----|-----|-----|
| VmV | | 180 | 20 | 180 | 50 |
| Vm | 7.5 | | | | |
| Am | 300 | | | | |
| Au | 0.8 | | | | |
| VmV | | | | | |
| V | | | | | |
| V | | | | | |
| V | | | | | |
| dB | 90 | 70 | 90 | 70 | 90 |
| dB | 98 | 77 | 98 | 77 | 98 |



Front View

Order Number LM1875T
See NS Package Number T05B

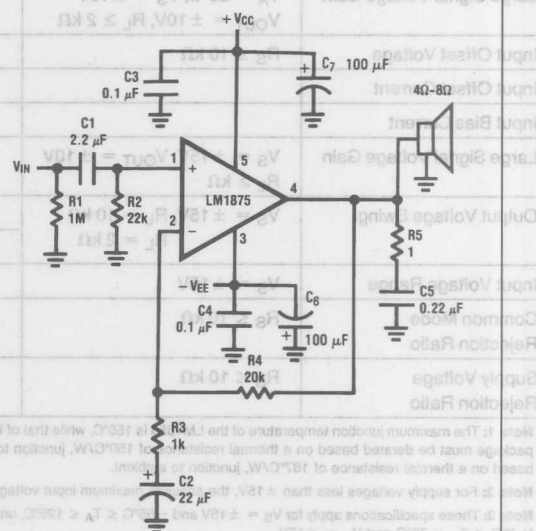
Features

- Up to 30 watts output power
- A_{VO} typically 90 dB
- Low distortion: 0.015%, 1 kHz, 20 W
- Wide power bandwidth: 70 kHz
- Protection for AC and DC short circuits to ground
- Thermal protection with parol circuit
- High current capability: 4A
- Wide supply range 16V-60V
- Internal output protection diodes
- 94 dB ripple rejection
- Plastic power package TO-220

Applications

- High performance audio systems
- Bridge amplifiers
- Stereo phonographs
- Servo amplifiers
- Instrument systems

Typical Applications



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage

60V

Input Voltage

$-V_{EE}$ to V_{CC}

Storage Temperature

-65°C to $+150^{\circ}\text{C}$

Junction Temperature

150°C

Lead Temperature (Soldering, 10 seconds)

260°C

θ_{JC}

3°C

θ_{JA}

73°C

Electrical Characteristics

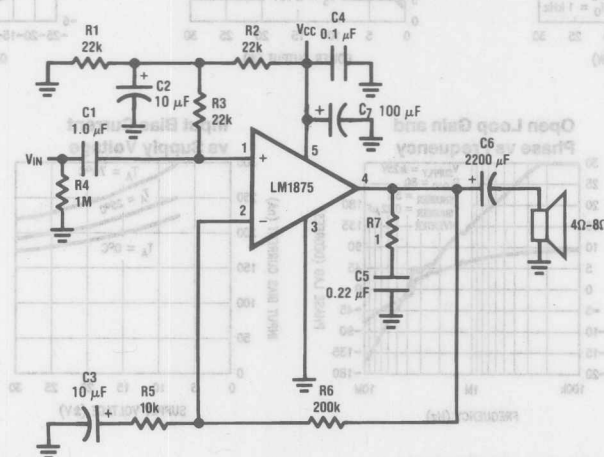
$V_{CC} = +25\text{V}$, $-V_{EE} = -25\text{V}$, $T_{\text{AMBIENT}} = 25^{\circ}\text{C}$, $R_L = 8\Omega$, $A_V = 20$ (26 dB), $f_o = 1\text{ kHz}$, unless otherwise specified.

| Parameter | Conditions | Typical | Tested Limits | Units |
|--------------------------------|---|-----------|---------------|------------------|
| Supply Current | $P_{\text{OUT}} = 0\text{W}$ | 70 | 100 | mA |
| Output Power (Note 1) | THD = 1% | 25 | | W |
| THD (Note 1) | $P_{\text{OUT}} = 20\text{W}$, $f_o = 1\text{ kHz}$ | 0.015 | | % |
| | $P_{\text{OUT}} = 20\text{W}$, $f_o = 20\text{ kHz}$ | 0.05 | 0.4 | % |
| | $P_{\text{OUT}} = 20\text{W}$, $R_L = 4\Omega$, $f_o = 1\text{ kHz}$ | 0.022 | | % |
| | $P_{\text{OUT}} = 20\text{W}$, $R_L = 4\Omega$, $f_o = 20\text{ kHz}$ | 0.07 | 0.6 | % |
| Offset Voltage | | ± 1 | ± 15 | mV |
| Input Bias Current | | ± 0.2 | ± 2 | μA |
| Input Offset Current | | 0 | ± 0.5 | μA |
| Gain-Bandwidth Product | $f_o = 20\text{ kHz}$ | 5.5 | | MHz |
| Open Loop Gain | DC | 90 | | dB |
| PSRR | V_{CC} , 1 kHz, 1 Vrms | 95 | 52 | dB |
| | V_{EE} , 1 kHz, 1 Vrms | 83 | 52 | dB |
| Max Slew Rate | 20W, 8 Ω , 70 kHz BW | 8 | | V/ μs |
| Current Limit | $V_{\text{OUT}} = V_{\text{SUPPLY}} - 10\text{V}$ | 4 | 3 | A |
| Equivalent Input Noise Voltage | $R_S = 600\Omega$, CCIR | 3 | | μVrms |

Note 1: Assumes the use of a heat sink having a thermal resistance of 1°C/W and no insulator with an ambient temperature of 25°C . Because the output limiting circuitry has a negative temperature coefficient, the maximum output power delivered to a 4Ω load may be slightly reduced when the tab temperature exceeds 55°C .

Typical Applications (Continued)

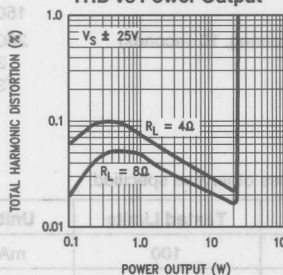
Typical Single Supply Operation



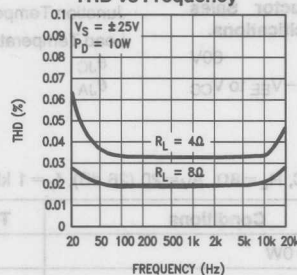
TL/H/5030-3

Typical Performance Characteristics

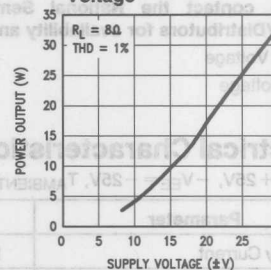
THD vs Power Output



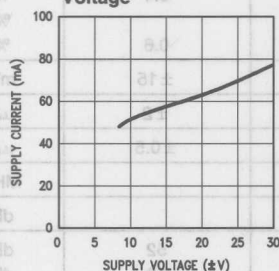
THD vs Frequency



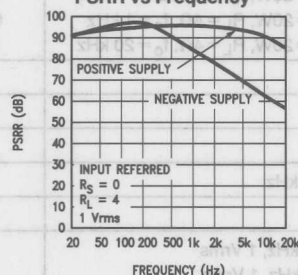
Power Output vs Supply Voltage



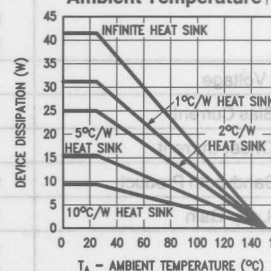
Supply Current vs Supply Voltage



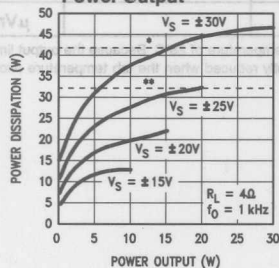
PSRR vs Frequency



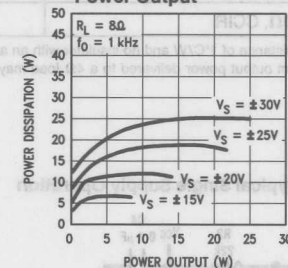
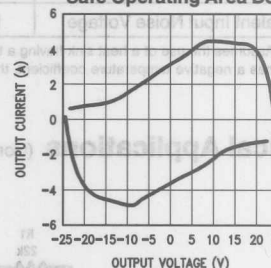
Device Dissipation vs Ambient Temperature†



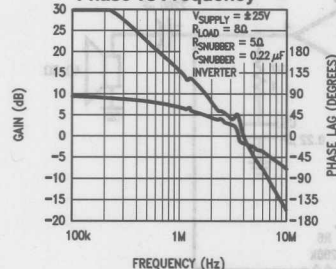
Power Dissipation vs Power Output



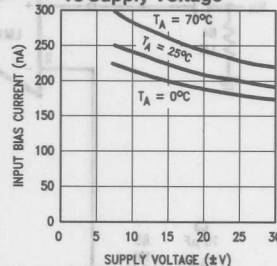
Power Dissipation vs Power Output

I_{OUT} vs V_{OUT}-Current Limit/ Safe Operating Area Boundary

Open Loop Gain and Phase vs Frequency



Input Bias Current vs Supply Voltage



*Thermal shutdown with infinite heat sink

**Thermal shutdown with $1^{\circ}C/W$ heat sink

TL/H/5030-4

Application Hints

STABILITY

The LM1875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but, as with any other high-current amplifier, the LM1875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

Proper layout of the printed circuit board is very important. While the LM1875 will be stable when installed in a board similar to the ones shown in this data sheet, it is sometimes necessary to modify the layout somewhat to suit the physical requirements of a particular application. When designing a different layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μF supply decoupling capacitors as close as possible to the LM1875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths for these components should be as short as possible.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input leads are long. The problem can be eliminated by placing a small capacitor (on the order of 50 pF to 500 pF) across the circuit input.

Most power amplifiers do not drive highly capacitive loads well, and the LM1875 is no exception. If the output of the LM1875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about 0.1 μF . The amplifier can typically drive load capacitances up to 2 μF or so without oscillating, but this is not recommended. If highly capacitive loads are expected, a resistor (at least 1 Ω) should be placed in series with the output of the LM1875. A method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10 Ω resistor in parallel with a 5 μH inductor.

DISTORTION

The preceding suggestions regarding circuit board grounding techniques will also help to prevent excessive distortion levels in audio applications. For low THD, it is also necessary to keep the power supply traces and wires separated from the traces and wires connected to the inputs of the LM1875. This prevents the power supply currents, which are large and nonlinear, from inductively coupling to the LM1875 inputs. Power supply wires should be twisted together and separated from the circuit board. Where these wires are soldered to the board, they should be perpendicular to the plane of the board at least to a distance of a couple of inches. With a proper physical layout, THD levels at 20 kHz with 10W output to an 8 Ω load should be less than 0.05%, and less than 0.02% at 1 kHz.

CURRENT LIMIT AND SAFE OPERATING AREA (SOA) PROTECTION

A power amplifier's output transistors can be damaged by excessive applied voltage, current flow, or power dissipation. The voltage applied to the amplifier is limited by the design of the external power supply, while the maximum current passed by the output devices is usually limited by internal circuitry to some fixed value. Short-term power dissipation is usually not limited in monolithic audio power amplifiers, and this can be a problem when driving reactive loads, which may draw large currents while high voltages appear on the output transistors. The LM1875 not only limits current to around 4A, but also reduces the value of the limit current when an output transistor has a high voltage across it.

When driving nonlinear reactive loads such as motors or loudspeakers with built-in protection relays, there is a possibility that an amplifier output will be connected to a load whose terminal voltage may attempt to swing beyond the power supply voltages applied to the amplifier. This can cause degradation of the output transistors or catastrophic failure of the whole circuit. The standard protection for this type of failure mechanism is a pair of diodes connected between the output of the amplifier and the supply rails. These are part of the internal circuitry of the LM1875, and needn't be added externally when standard reactive loads are driven.

THERMAL PROTECTION

The LM1875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 170°C, the LM1875 shuts down. It starts operating again when the die temperature drops to about 145°C, but if the temperature again begins to rise, shutdown will occur at only 150°C. Therefore, the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will limit the maximum die temperature to a lower value. This greatly reduces the stresses imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen for thermal resistance low enough that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

POWER DISSIPATION AND HEAT SINKING

The LM1875 must always be operated with a heat sink, even when it is not required to drive a load. The maximum idling current of the device is 100 mA, so that on a 60V power supply an unloaded LM1875 must dissipate 6W of power. The 54°C/W junction-to-ambient thermal resistance of a TO-220 package would cause the die temperature to rise 324°C above ambient, so the thermal protection circuitry will shut the amplifier down if operation without a heat sink is attempted.

Application Hints (Continued)

In order to determine the appropriate heat sink for a given application, the power dissipation of the LM1875 in that application must be known. When the load is resistive, the maximum average power that the IC will be required to dissipate is approximately:

$$P_{D(MAX)} \approx \frac{V_S^2}{2\pi^2 R_L} + P_Q$$

where V_S is the total power supply voltage across the LM1875, R_L is the load resistance, and P_Q is the quiescent power dissipation of the amplifier. The above equation is only an approximation which assumes an "ideal" class B output stage and constant power dissipation in all other parts of the circuit. The curves of "Power Dissipation vs Power Output" give a better representation of the behavior of the LM1875 with various power supply voltages and resistive loads. As an example, if the LM1875 is operated on a 50V power supply with a resistive load of 8Ω, it can develop up to 19W of internal power dissipation. If the die temperature is to remain below 150°C for ambient temperatures up to 70°C, the total junction-to-ambient thermal resistance must be less than

$$\frac{150^\circ\text{C} - 70^\circ\text{C}}{19\text{W}} = 4.2^\circ\text{C/W.}$$

Using $\theta_{JC} = 2^\circ\text{C/W}$, the sum of the case-to-heat-sink interface thermal resistance and the heat-sink-to-ambient thermal resistance must be less than 2.2°C/W. The case-to-heat-sink thermal resistance of the TO-220 package varies with the mounting method used. A metal-to-metal interface will be about 1°C/W if lubricated, and about 1.2°C/W if dry.

If a mica insulator is used, the thermal resistance will be about 1.6°C/W lubricated and 3.4°C/W dry. For this example, we assume a lubricated mica insulator between the LM1875 and the heat sink. The heat sink thermal resistance must then be less than

$$4.2^\circ\text{C/W} - 2^\circ\text{C/W} - 1.6^\circ\text{C/W} = 0.6^\circ\text{C/W.}$$

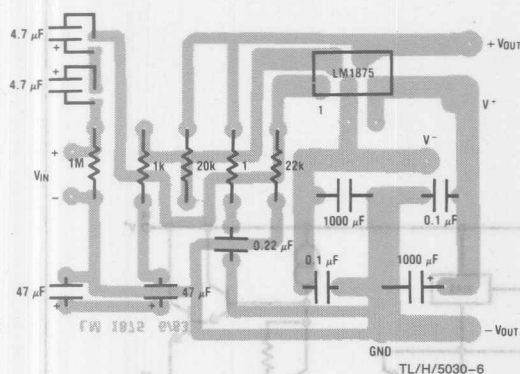
This is a rather large heat sink and may not be practical in some applications. If a smaller heat sink is required for reasons of size or cost, there are two alternatives. The maximum ambient operating temperature can be reduced to 50°C (122°F), resulting in a 1.6°C/W heat sink, or the heat sink can be isolated from the chassis so the mica washer is not needed. This will change the required heat sink to a 1.2°C/W unit if the case-to-heat-sink interface is lubricated.

Note: When using a single supply, maximum transfer of heat away from the LM1875 can be achieved by mounting the device directly to the heat sink (tab is at ground potential); this avoids the use of a mica or other type insulator.

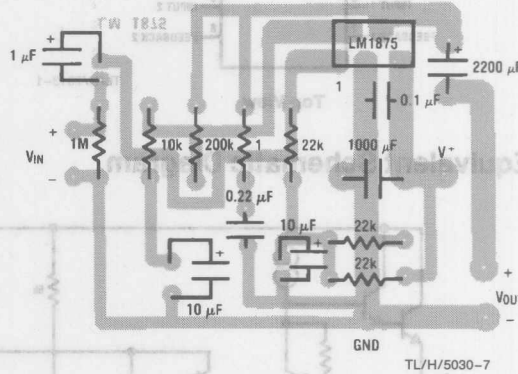
The thermal requirements can become more difficult when an amplifier is driving a reactive load. For a given magnitude of load impedance, a higher degree of reactance will cause a higher level of power dissipation within the amplifier. As a general rule, the power dissipation of an amplifier driving a 60° reactive load (usually considered to be a worst-case loudspeaker load) will be roughly that of the same amplifier driving the resistive part of that load. For example, a loudspeaker may at some frequency have an impedance with a magnitude of 8Ω and a phase angle of 60°. The real part of this load will then be 4Ω, and the amplifier power dissipation will roughly follow the curve of power dissipation with a 4Ω load.

Component Layouts

Split Supply



Single Supply



LM1877 Dual Audio Power Amplifier

General Description

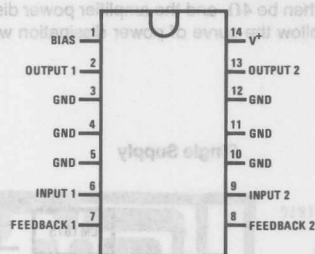
The LM1877 is a monolithic dual power amplifier designed to deliver 12W/channel continuous into 8Ω loads. The LM1877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection, and output Q point centering. The LM1877 is internally compensated for all gains greater than 10.

Features

- 2W/channel
- -65 dB ripple rejection, output referred
- -65 dB channel separation, output referred

Connection Diagram

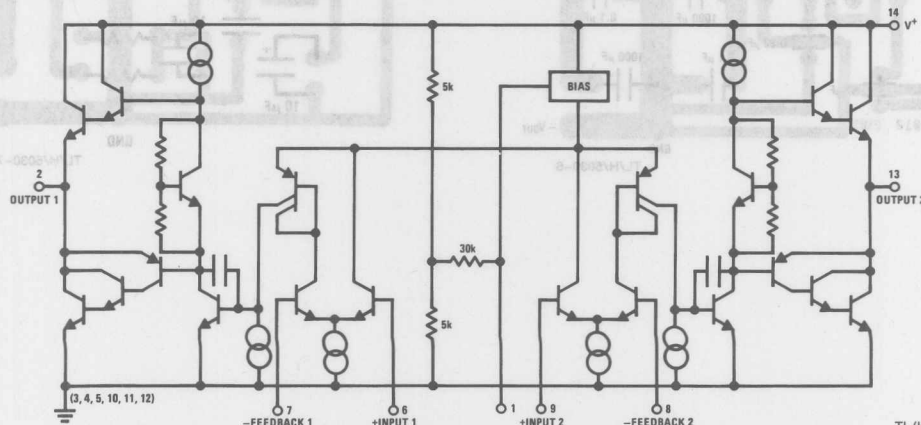
Dual-In-Line Package
or Surface Mount Package



Top View

TL/H/7913-1

Equivalent Schematic Diagram



TL/H/7913-2

- Wide supply range, 6V-24V
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------|-----------------|
| Supply Voltage | 26V |
| Input Voltage | $\pm 0.7V$ |
| Operating Temperature | 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |
| Junction Temperature | 150°C |

Lead Temperature

| | |
|---------------------------------|-------|
| N-Package Soldering (10 sec.) | 260°C |
| M-Package Infrared (15 sec.) | 220°C |
| M-Package Vapor Phase (60 sec.) | 215°C |

Thermal Resistance

| | |
|---------------------------|---------|
| θ_{JC} (N-Package) | 30°C/W |
| θ_{JA} (N-Package) | 79°C/W |
| θ_{JC} (M-Package) | 27°C/W |
| θ_{JA} (M-Package) | 114°C/W |

Electrical Characteristics

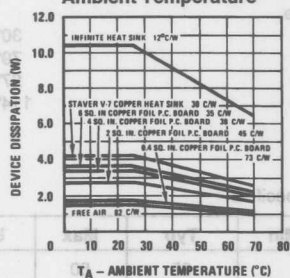
$V_S = 20V$, $T_A = 25^\circ C$, (See Note 1) $R_L = 8\Omega$, $A_v = 50$ (34 dB) unless otherwise specified

| Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------|---|-----|-----------|-----|------------|
| Total Supply Current | $P_O = 0W$ | | 25 | 50 | mA |
| Output Power | THD = 10% | | | | |
| LM1877 | $V_S = 20V$, $R_L = 8\Omega$ | 2.0 | | | W/Ch |
| | $V_S = 12V$, $R_L = 8\Omega$ | | 1.3 | | W/Ch |
| Total Harmonic Distortion | $f = 1\text{ kHz}$, $V_S = 14V$ | | | | |
| LM1877 | $P_O = 50\text{ mW/Channel}$ | | 0.075 | | % |
| | $P_O = 500\text{ mW/Channel}$ | | 0.045 | | % |
| | $P_O = 1\text{ W/Channel}$ | | 0.055 | | % |
| Output Swing | $R_L = 8\Omega$ | | $V_S - 6$ | | Vp-p |
| Channel Separation | $C_F = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$, $f = 1\text{ kHz}$, Output Referred | | | | |
| | $V_S = 20V$, $V_O = 4\text{ Vrms}$ | -50 | -70 | | dB |
| | $V_S = 7V$, $V_O = 0.5\text{ Vrms}$ | | -60 | | dB |
| PSRR Power Supply | $C_F = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$, Rejection Ratio $f = 120\text{ Hz}$, Output Referred | | | | |
| | $V_S = 20V$, $V_{RIPPLE} = 1\text{ Vrms}$ | -50 | -65 | | dB |
| | $V_S = 7V$, $V_{RIPPLE} = 0.5\text{ Vrms}$ | | -40 | | dB |
| Noise | Equivalent Input Noise | | | | |
| | $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$, $BW = 20\text{ Hz} - 20\text{ kHz}$, Output Noise Wideband | | 2.5 | | μV |
| | $R_S = 0$, $C_N = 0.1\text{ }\mu F$, $A_v 200$ | | 0.80 | | mV |
| Open Loop Gain | $R_S = 0$, $f = 100\text{ kHz}$, $R_L = 8\Omega$ | | 70 | | dB |
| Input Offset Voltage | | | 15 | | mV |
| Input Bias Current | | | 50 | | nA |
| Input Impedance | Open Loop | | 4 | | M Ω |
| DC Output Level | $V_S = 20V$ | 9 | 10 | 11 | V |
| Slew Rate | | | 2.0 | | V/ μs |
| Power Bandwidth | | | 65 | | kHz |
| Current Limit | | | 1.0 | | A |

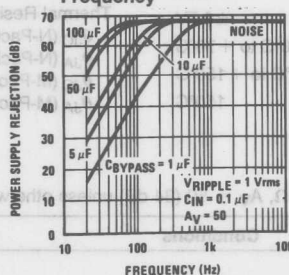
Note 1: For operation at ambient temperature greater than 25°C, the LM1877 must be derated based on a maximum 150°C junction temperature.

Typical Performance Characteristics

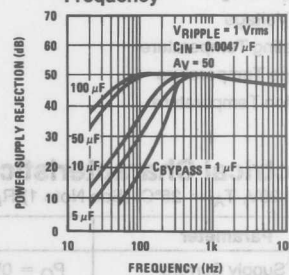
Device Dissipation vs Ambient Temperature



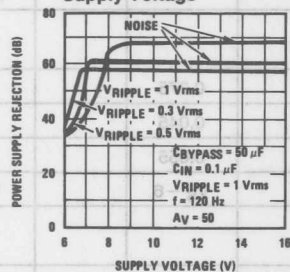
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



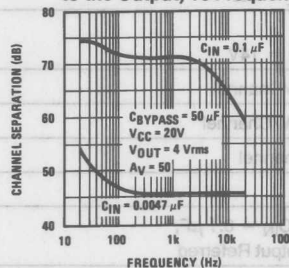
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



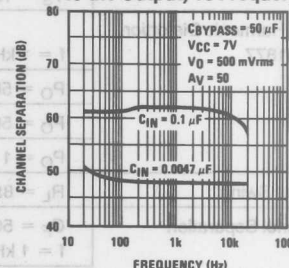
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



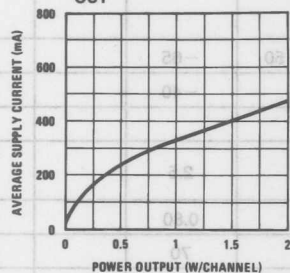
Channel Separation (Referred to the Output) vs Frequency



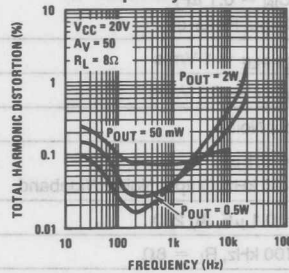
Channel Separation (Referred to the Output) vs Frequency



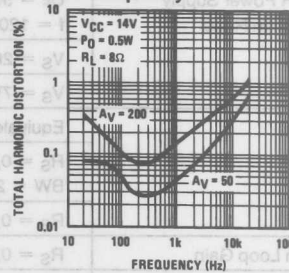
Average Supply Current vs P_{OUT}



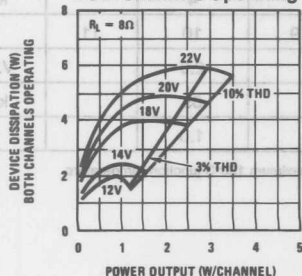
Total Harmonic Distortion vs Frequency



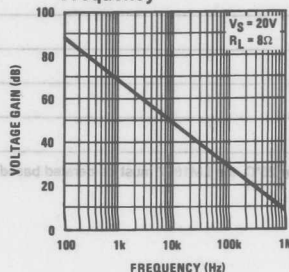
Total Harmonic Distortion vs Frequency



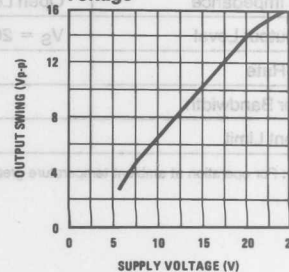
Power Dissipation (W) Both Channels Operating



Open Loop Gain vs Frequency

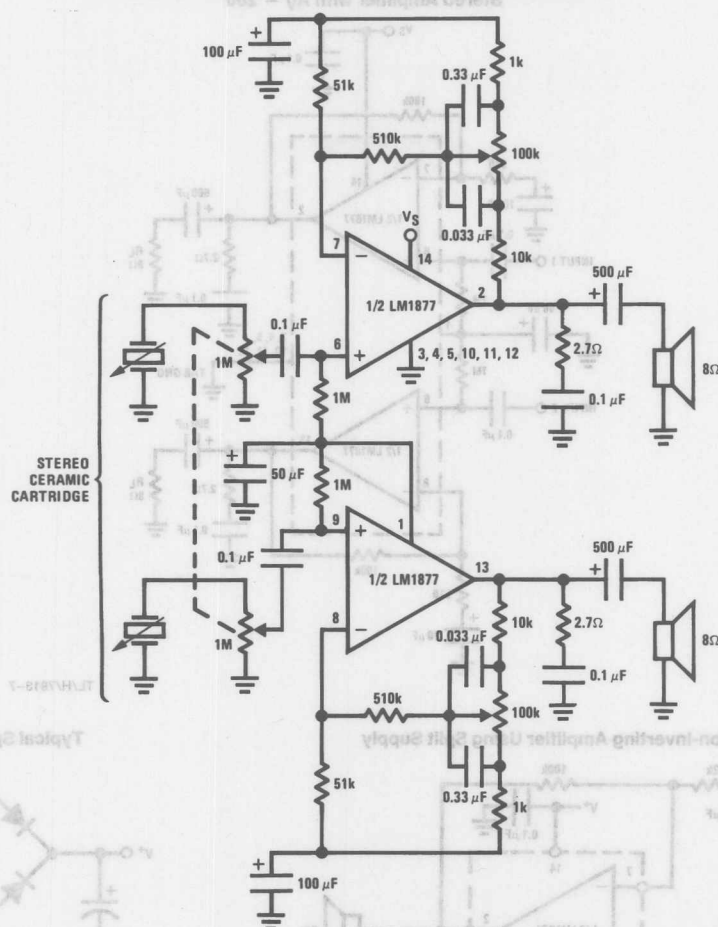


Output Swing vs Supply Voltage



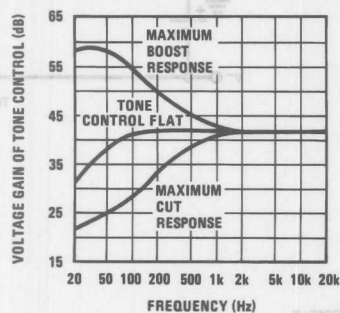
Typical Applications

Stereo Phonograph Amplifier with Bass Tone Control



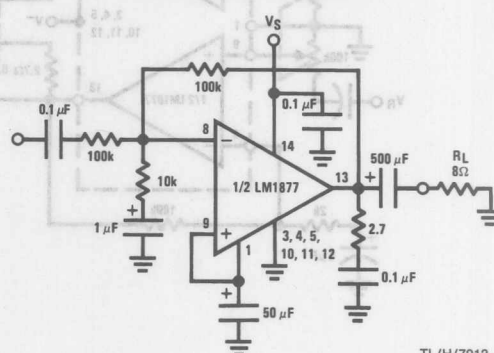
TL/H/7913-4

Frequency Response of Bass Tone Control



TL/H/7913-5

Inverting Unity Gain Amplifier

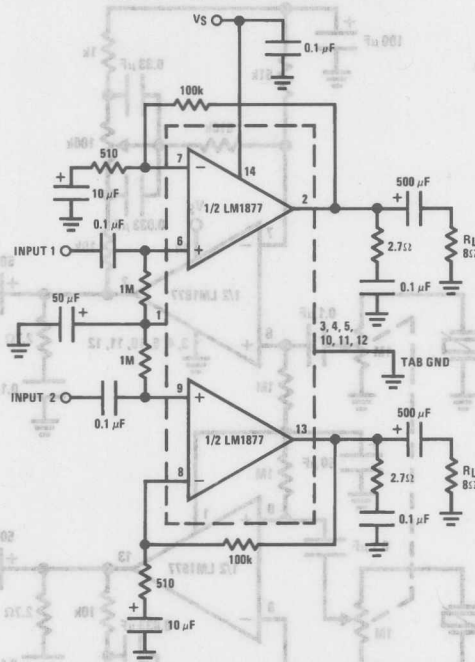


TL/H/7913-6

LM1877

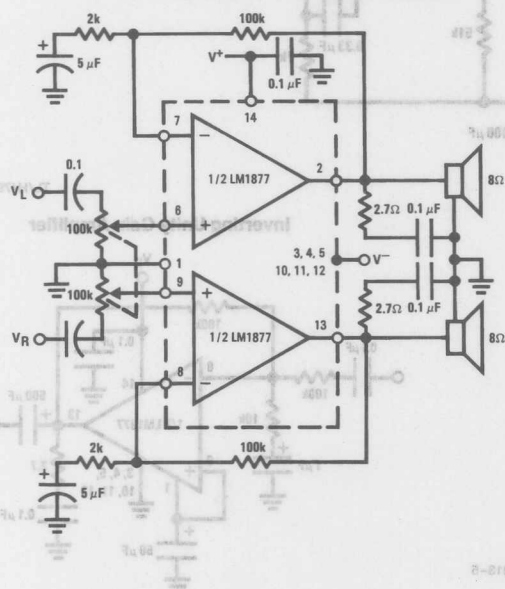
1

Typical Applications (Continued)

Stereo Amplifier with $A_v = 200$ 

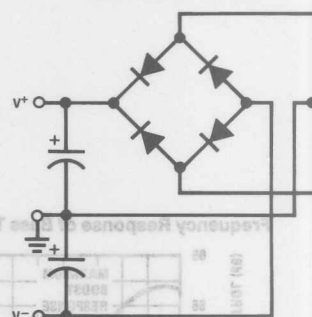
TL/H/7913-7

Non-Inverting Amplifier Using Split Supply

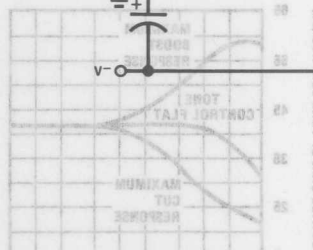


TL/H/7913-8

Typical Split Supply



TL/H/7913-9



LM1896/LM2896 Dual Audio Power Amplifier

General Description

The LM1896 is a high performance 6V stereo power amplifier designed to deliver 1 watt/channel into 4Ω or 2 watts bridged monaural into 8Ω. Utilizing a unique patented compensation scheme, the LM1896 is ideal for sensitive AM radio applications. This new circuit technique exhibits lower wideband noise, lower distortion, and less AM radiation than conventional designs. The amplifier's wide supply range (3V–9V) is ideal for battery operation. For higher supplies ($V_S > 9V$) the LM2896 is available in an 11-lead single-in-line package. The LM2896 package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

Features

- Low AM radiation
- Low noise
- 3V, 4Ω, stereo $P_O = 250$ mW
- Wide supply operation 3V–15V (LM2896)
- Low distortion
- No turn on "pop"
- Adjustable voltage gain and bandwidth
- Smooth waveform clipping
- $P_O = 9W$ bridged, LM2896

Applications

- Compact AM-FM radios
- Stereo tape recorders and players
- High power portable stereos

Typical Applications

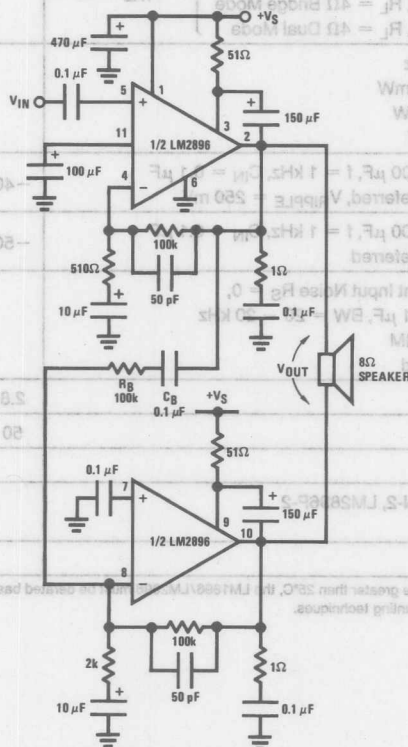


FIGURE 1. LM2896 in Bridge Configuration ($A_V = 400$, $BW = 20$ kHz)
Order Number LM1896N Order Number LM2896P
See NS Package Number N14A See NS Package Number P11A

Office/Distributors for availability and specifications.**Supply Voltage**

LM1896

LM2896

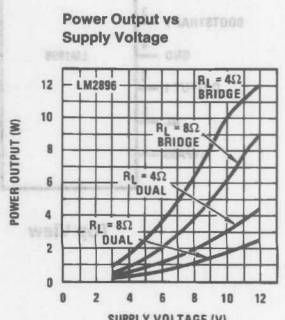
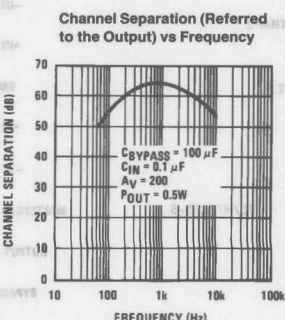
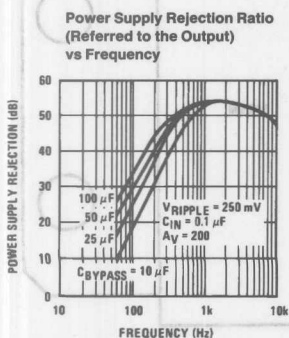
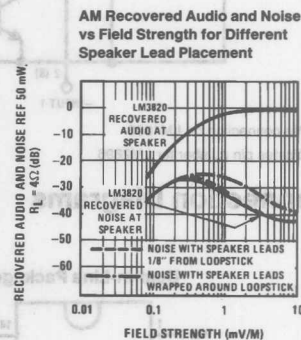
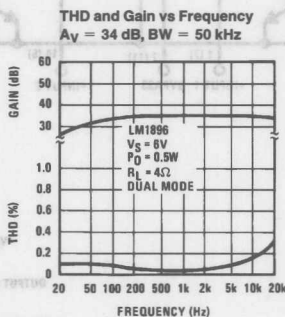
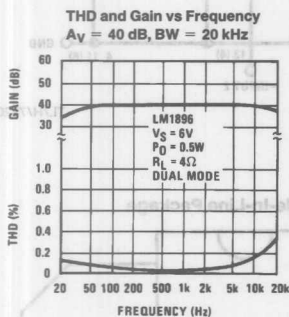
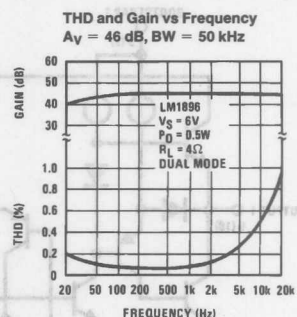
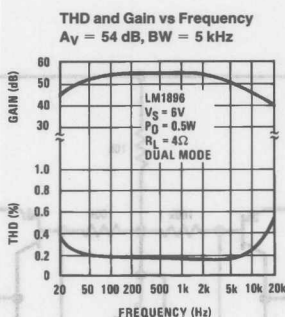
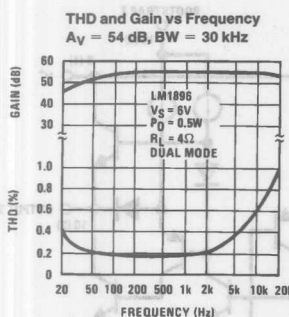
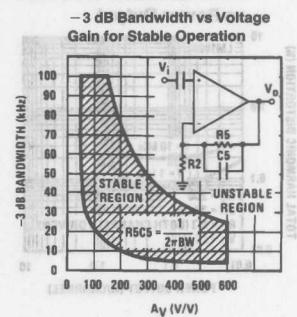
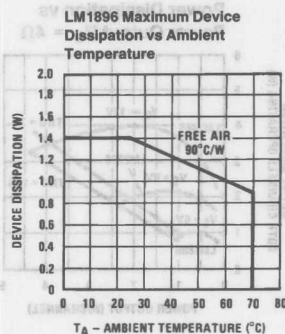
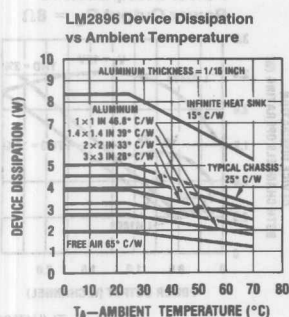
 $V_S = 12V$ $V_S = 18V$ **Operating Temperature (Note 1)** $0^\circ\text{C to } +70^\circ\text{C}$ **Storage Temperature** $-65^\circ\text{C to } +150^\circ\text{C}$ **Thermal Resistance** θ_{JC} (DIP) θ_{JA} (DIP) θ_{JC} (SIP) θ_{JA} (SIP) 30°C/W 137°C/W 10°C/W 55°C/W **Electrical Characteristics**

Unless otherwise specified, $T_A = 25^\circ\text{C}$, $A_V = 200$ (46 dB). For the LM1896; $V_S = 6V$ and $R_L = 4\Omega$. For LM2896, $T_{AB} = 25^\circ\text{C}$, $V_S = 12V$ and $R_L = 8\Omega$. Test circuit shown in Figure 2.

| Parameter | Conditions | LM1896 | | | LM2896 | | | Units |
|-------------------------------------|---|--------|------|-----|--------|------|-----|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Supply Current | $P_O = 0W$, Dual Mode | | 15 | 25 | | 25 | 40 | mA |
| Operating Supply Voltage | | 3 | | 10 | 3 | | 15 | V |
| Output Power | THD = 10%, $f = 1\text{ kHz}$ | | | | | | | |
| LM1896N-1 | $V_S = 6V$, $R_L = 4\Omega$ Dual Mode | 0.9 | 1.1 | | | | | W/ch |
| LM1896N-2 | $V_S = 6V$, $R_L = 8\Omega$ Bridge Mode | | 1.8 | 2.1 | | | | W |
| | $V_S = 9V$, $R_L = 8\Omega$ Dual Mode | | 1.3 | | | | | W/ch |
| LM2896P-1 | $V_S = 12V$, $R_L = 8\Omega$ Dual Mode | | | | 2.0 | 2.5 | | W/ch |
| LM2896P-2 | $V_S = 12V$, $R_L = 8\Omega$ Bridge Mode | | | | 7.2 | 9.0 | | W |
| | $V_S = 9V$, $R_L = 4\Omega$ Bridge Mode | | | | | 7.8 | | W |
| | $V_S = 9V$, $R_L = 4\Omega$ Dual Mode | | | | | 2.5 | | W/ch |
| Distortion | $f = 1\text{ kHz}$ | | | | | | | |
| | $P_O = 50\text{ mW}$ | | 0.09 | | | 0.09 | | % |
| | $P_O = 0.5W$ | | 0.11 | | | 0.11 | | % |
| | $P_O = 1W$ | | | | | 0.14 | | % |
| Power Supply Rejection Ratio (PSRR) | $C_{BY} = 100\text{ }\mu\text{F}$, $f = 1\text{ kHz}$, $C_{IN} = 0.1\text{ }\mu\text{F}$ Output Referred, $V_{RIPPLE} = 250\text{ mV}$ | -40 | -54 | | -40 | -54 | | dB |
| Channel Separation | $C_{BY} = 100\text{ }\mu\text{F}$, $f = 1\text{ kHz}$, $C_{IN} = 0.1\text{ }\mu\text{F}$ Output Referred | -50 | -64 | | -50 | -64 | | dB |
| Noise | Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\text{ }\mu\text{F}$, $BW = 20 - 20\text{ kHz}$ CCIR/ARM Wideband | | 1.4 | | | 1.4 | | μV |
| | | | 1.4 | | | 1.4 | | μV |
| | | | 2.0 | | | 2.0 | | μV |
| DC Output Level | | 2.8 | 3 | 3.2 | 5.6 | 6 | 6.4 | V |
| Input Impedance | | 50 | 100 | 350 | 50 | 100 | 350 | k Ω |
| Input Offset Voltage | | | 5 | | | 5 | | mV |
| Voltage Difference between Outputs | LM1896N-2, LM2896P-2 | | 10 | 20 | | 10 | 20 | mV |
| Input Bias Current | | | 120 | | | 120 | | nA |

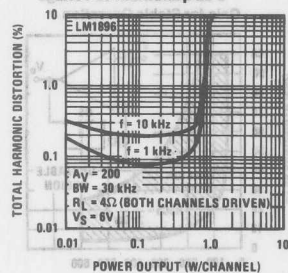
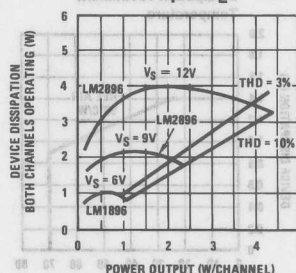
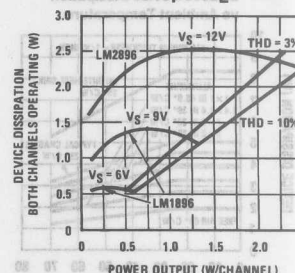
Note 1: For operation at ambient temperature greater than 25°C , the LM1896/LM2896 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon mounting techniques.

Typical Performance Curves



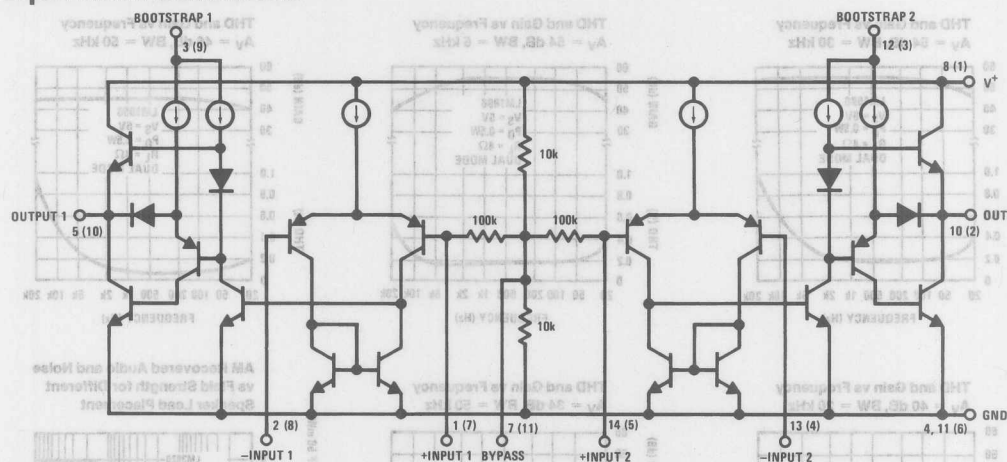
Typical Performance Curves (Continued)

Total Harmonic Distortion vs Power Output

Power Dissipation vs Power Output $R_L = 4\Omega$ Power Dissipation vs Power Output $R_L = 8\Omega$ 

TL/H/7920-3

Equivalent Schematic

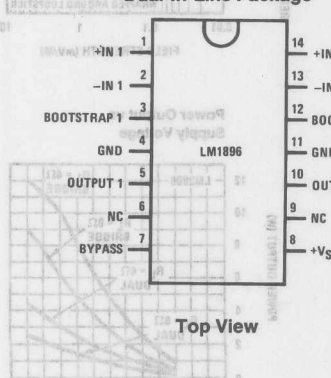


6, 9 No connection on LM1896
() indicates pin number for LM2896

TL/H/7920-4

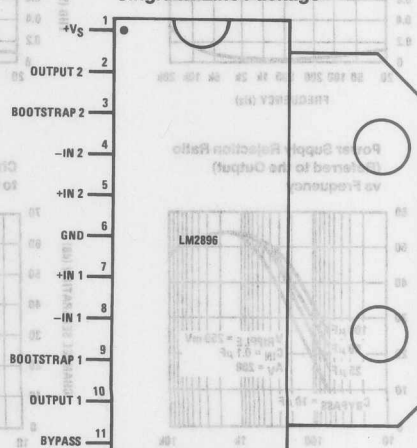
Connection Diagrams

Dual-In-Line Package



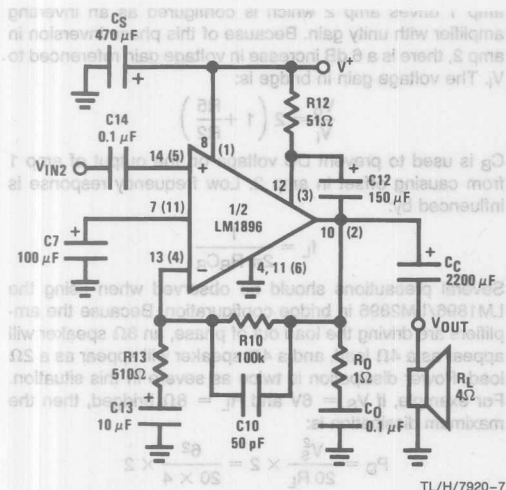
Top View

Single-In-Line Package



Top View

TL/H/7920-6



TL/H/7920-7

6, 9 No connection on LM1896
() Indicates pin number for LM2896

FIGURE 2. Stereo Amplifier with $A_V = 200$, $BW = 30$ kHz

External Components (Figure 2)

Components

1. R2, R5, R10, R13

2. R3, R12

3. R0

4. C1, C14

5. C2, C13

6. C3, C12

7. C5, C10

8. C7

9. Cc

10. C0

11. Cs

Sets voltage gain, $A_V = 1 + R5/R2$ for one channel and $A_V = 1 + R10/R13$ for the other channel.

Bootstrap resistor sets drive current for output stage and allows pins 3 and 12 to go above V_S .

Works with C_0 to stabilize output stage.

Input coupling capacitor. Pins 1 and 14 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R_{IN} C1}$$

Feedback capacitors. Ensure unity gain at DC. Also a low frequency pole at:

$$f_L = \frac{1}{2\pi R2 C2}$$

Bootstrap capacitors, used to increase drive to output stage. A low frequency pole is set by:

$$f_L = \frac{1}{2\pi R3 C3}$$

Compensation capacitor. These stabilize the amplifiers and adjust their bandwidth. See curve of bandwidth vs allowable gain.

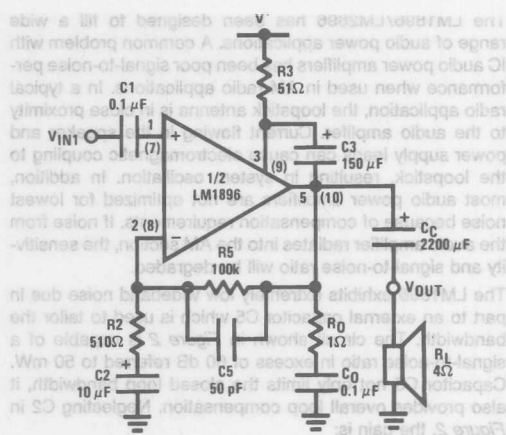
Improves power supply rejection (See Typical Performance Curves). Increasing C7 increases turn-on delay.

Output coupling capacitor. Isolates pins 5 and 10 from the load. Low frequency pole set by:

$$f_L = \frac{1}{2\pi Cc R_L}$$

Works with R_0 to stabilize output stage.

Provides power supply filtering.



TL/H/7920-8

Comments

A curve of -3 dB BW (ω_c) vs A_V is shown in Figure 3. The power amplifier is an LM1896. The receiver section in this example is a simple audio amplifier. The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The bridge outputs are shown in Figure 4.

Application Hints

AM Radios

The LM1896/LM2896 has been designed to fill a wide range of audio power applications. A common problem with IC audio power amplifiers has been poor signal-to-noise performance when used in AM radio applications. In a typical radio application, the loopstick antenna is in close proximity to the audio amplifier. Current flowing in the speaker and power supply leads can cause electromagnetic coupling to the loopstick, resulting in system oscillation. In addition, most audio power amplifiers are not optimized for lowest noise because of compensation requirements. If noise from the audio amplifier radiates into the AM section, the sensitivity and signal-to-noise ratio will be degraded.

The LM1896 exhibits extremely low wideband noise due in part to an external capacitor C5 which is used to tailor the bandwidth. The circuit shown in Figure 2 is capable of a signal-to-noise ratio in excess of 60 dB referred to 50 mW. Capacitor C5 not only limits the closed loop bandwidth, it also provides overall loop compensation. Neglecting C2 in Figure 2, the gain is:

$$A_V(S) = \frac{S + A_V \omega_o}{S + \omega_o}$$

$$\text{where } A_V = \frac{R_2 + R_5}{R_2}, \quad \omega_o = \frac{1}{R_5 C_5}$$

A curve of -3 dB BW (ω_o) vs A_V is shown in the Typical Performance Curves.

Figure 3 shows a plot of recovered audio as a function of field strength in $\mu\text{V}/\text{M}$. The receiver section in this example is an LM3820. The power amplifier is located about two inches from the loopstick antenna. Speaker leads run parallel to the loopstick and are $1/8$ inch from it. Referenced to a 20 dB S/N ratio, the improvement in noise performance over conventional designs is about 10 dB. This corresponds to an increase in usable sensitivity of about 8.5 dB.

Bridge Amplifiers

The LM1896/LM2896 can be used in the bridge mode as a monaural power amplifier. In addition to much higher power output, the bridge configuration does not require output coupling capacitors. The load is connected directly between the amplifier outputs as shown in Figure 4.

Amp 1 has a voltage gain set by $1 + R_5/R_2$. The output of amp 1 drives amp 2 which is configured as an inverting amplifier with unity gain. Because of this phase inversion in amp 2, there is a 6 dB increase in voltage gain referred to V_i . The voltage gain in bridge is:

$$\frac{V_o}{V_i} = 2 \left(1 + \frac{R_5}{R_2} \right)$$

C_B is used to prevent DC voltage on the output of amp 1 from causing offset in amp 2. Low frequency response is influenced by:

$$f_L = \frac{1}{2\pi R_B C_B}$$

Several precautions should be observed when using the LM1896/LM2896 in bridge configuration. Because the amplifiers are driving the load out of phase, an 8Ω speaker will appear as a 4Ω load, and a 4Ω speaker will appear as a 2Ω load. Power dissipation is twice as severe in this situation. For example, if $V_S = 6\text{V}$ and $R_L = 8\Omega$ bridged, then the maximum dissipation is:

$$P_D = \frac{V_S^2}{20 R_L} \times 2 = \frac{6^2}{20 \times 4} \times 2$$

$$P_D = 0.9 \text{ Watts}$$

This amount of dissipation is equivalent to driving two 4Ω loads in the stereo configuration.

When adjusting the frequency response in the bridge configuration, R_5C_5 and $R_{10}C_{10}$ form a 2 pole cascade and the -3 dB bandwidth is actually shifted to a lower frequency:

$$BW = \frac{0.707}{2\pi RC}$$

where R = feedback resistor

C = feedback capacitor

To measure the output voltage, a floating or differential meter should be used because a prolonged output short will over dissipate the package. Figure 1 shows the complete bridge amplifier.

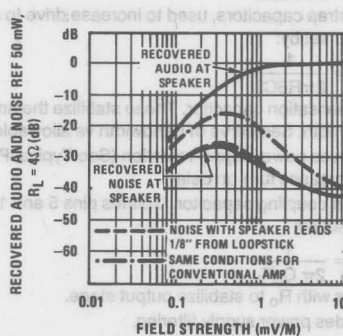


FIGURE 3. Improved AM Sensitivity over Conventional Design

Application Hints (Continued)

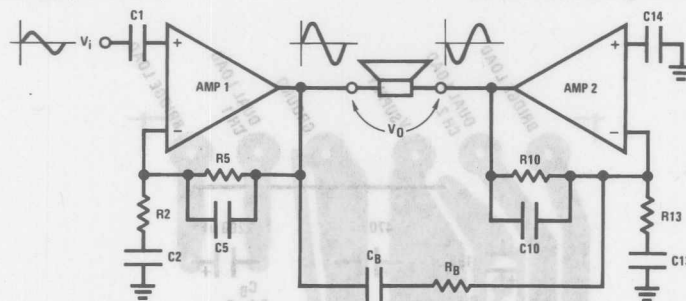


Figure 4. Bridge Amplifier Connection

TL/H/7920-10

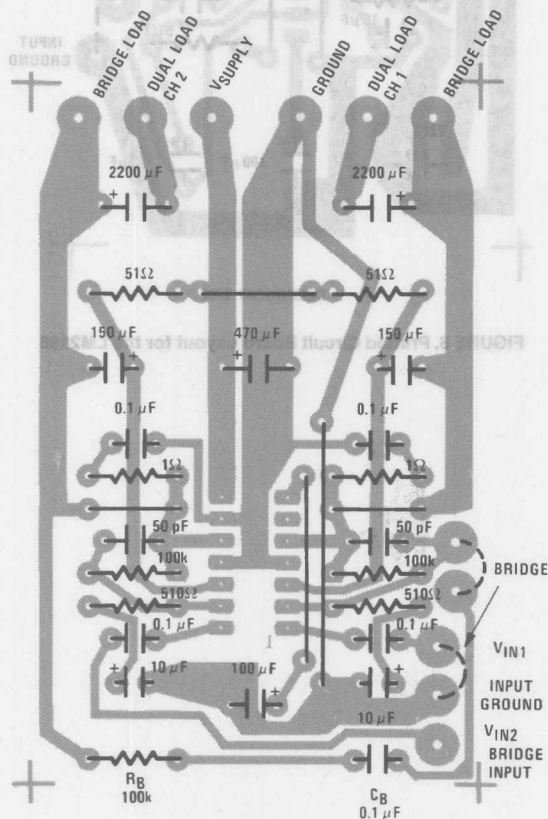
Printed Circuit Layout

Printed Circuit Board Layout

Figure 5 and Figure 6 show printed circuit board layouts for the LM1896 and LM2896. The circuits are wired as stereo amplifiers. The signal source ground should return to the input ground shown on the boards. Returning the loads to power supply ground through a separate wire will keep the THD at its lowest value. The inputs should be terminated in

less than 50 k Ω to prevent an input-output oscillation. This oscillation is dependent on the gain and the proximity of the bridge elements R_B and C_B to the (+) input. If the bridge mode is not used, do not insert R_B , C_B into the PCB.

To wire the amplifier into the bridge configuration, short the capacitor on pin 7 (pin 1 of the LM1896) to ground. Connect together the nodes labeled BRIDGE and drive the capacitor connected to pin 5 (pin 14 of the LM1896).



COMPONENT SIDE

FIGURE 5. Printed Circuit Board Layout for the LM1896

TL/H/7920-11

LM2877 Dual 4W Audio Power Amplifier

General Description

The LM2877 is a monolithic dual power amplifier designed to deliver 4W/channel continuous into 8Ω loads. The LM2877 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders and AM-FM stereo receivers, etc. Each power amplifier is biased from a common internal regulator to provide high power supply rejection and output Q point centering. The LM2877 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package.

Features

- 4W/channel
- -68 dB ripple rejection, output referred
- -70 dB channel separation, output referred

- Wide supply range, 6-24V

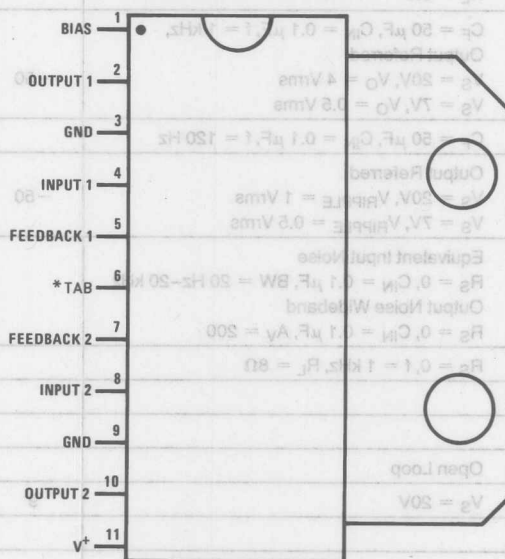
- Very low cross-over distortion
- Low audio band noise
- AC short circuit protected
- Internal thermal shutdown

Applications

- Multi-channel audio systems
- Stereo phonographs
- Tape recorders and players
- AM-FM radio receivers
- Servo amplifiers
- Intercom systems
- Automotive products

Connection Diagram

(Single-In-Line Package)



Top View

Order Number LM2877P
See NS Package Number P11A

*Pin 6 must be connected to GND.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------|--------------|
| Supply Voltage | 26V |
| Input Voltage | $\pm 0.7V$ |
| Operating Temperature | 0°C to +70°C |

| | |
|---------------------------------------|-----------------|
| Storage Temperature | -65°C to +150°C |
| Junction Temperature | 150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Thermal Resistance | |
| θ_{JC} | 10°C/W |
| θ_{JA} | 55°C/W |

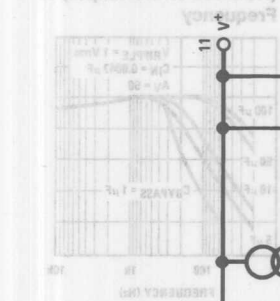
Electrical Characteristics $V_S = 20V$, $T_{TAB} = 25^\circ C$, $R_L = 8\Omega$, $A_v = 50$ (34 dB) unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------|--|------------|---|-----|----------------------------|
| Total Supply Current | $P_O = 0W$ | | 25 | 50 | mA |
| Operating Supply Voltage | | 6 | | 24 | V |
| Output Power/Channel | $f = 1\text{ kHz}$, $THD = 10\%$, $T_{TAB} = 25^\circ C$ $V_S = 20V$ $V_S = 18V$ $V_S = 12V$, $R_L = 4\Omega$ $V_S = 12V$, $R_L = 8\Omega$ | 4.0 1.5 | 4.5 1.9 1.0 | | W W W W |
| Distortion, THD | $f = 1\text{ kHz}$, $V_S = 20V$ $P_O = 50\text{ mW/Channel}$ $P_O = 1W\text{/Channel}$ $P_O = 2W\text{/Channel}$ $f = 1\text{ kHz}$, $V_S = 12V$, $R_L = 4\Omega$ $P_O = 50\text{ mW/Channel}$ $P_O = 500\text{ mW/Channel}$ $P_O = 1W\text{/Channel}$ | | 0.1 0.07 0.07 0.25 0.20 0.15 | | % % % % % % |
| Output Swing | $R_L = 8\Omega$ | | $V_S - 4$ | | V_{p-p} |
| Channel Separation | $C_F = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$, $f = 1\text{ kHz}$, Output Referred $V_S = 20V$, $V_O = 4\text{ Vrms}$ $V_S = 7V$, $V_O = 0.5\text{ Vrms}$ | -50 | -70 -60 | | dB dB |
| PSRR Power Supply | $C_F = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$, $f = 120\text{ Hz}$ | | | | |
| Rejection Ratio | Output Referred $V_S = 20V$, $V_{RIPPLE} = 1\text{ Vrms}$ $V_S = 7V$, $V_{RIPPLE} = 0.5\text{ Vrms}$ | -50 | -68 -40 | | dB dB |
| Noise | Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$, $BW = 20\text{ Hz} - 20\text{ kHz}$ Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$, $A_v = 200$ | | 2.5 0.80 | | μV mV |
| Open Loop Gain | $R_S = 0$, $f = 1\text{ kHz}$, $R_L = 8\Omega$ | | 70 | | dB |
| Input Offset Voltage | | | 15 | | mV |
| Input Bias Current | | | 50 | | nA |
| Input Impedance | Open Loop | | 4 | | M Ω |
| DC Output Level | $V_S = 20V$ | 9 | 10 | 11 | V |
| Slew Rate | | | 2.0 | | V/ μs |
| Power Bandwidth | | | 65 | | kHz |
| Current Limit | | | 1.0 | | A |

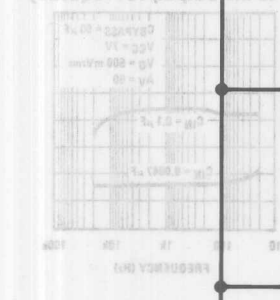
Note 1: For operation at ambient temperature greater than 25°C, the LM2877 must be derated based on a maximum 150°C junction temperature using a thermal resistance which depends upon device mounting techniques.

Equivalent Schematic Diagram

Power Supply Rejection Ratio
(Referenced to the Output) vs
Frequency



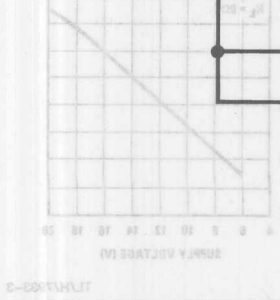
Channel Separation (Referenced
to the Output) vs Frequency



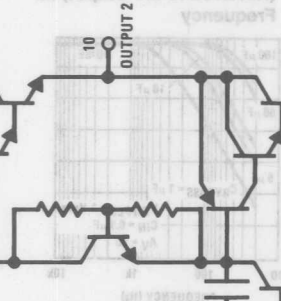
Total Harmonic Distortion
vs Frequency



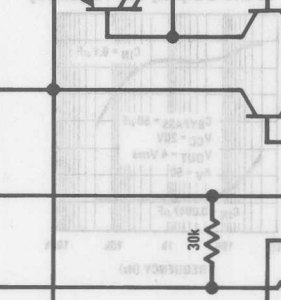
Output Swing vs Supply
Voltage



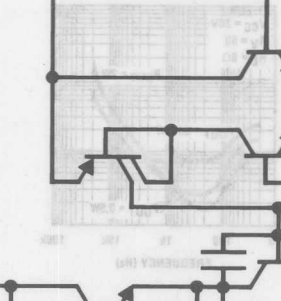
Power Supply Rejection Ratio
(Referenced to the Output) vs
Frequency



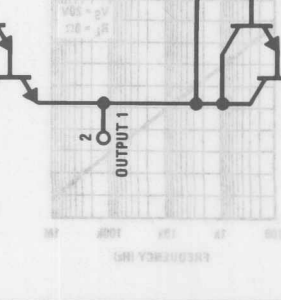
Channel Separation (Referenced
to the Output) vs Frequency



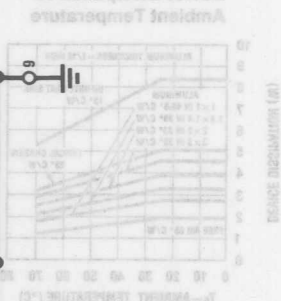
Total Harmonic Distortion
vs Frequency



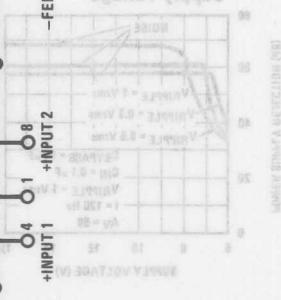
Power Output
vs Frequency



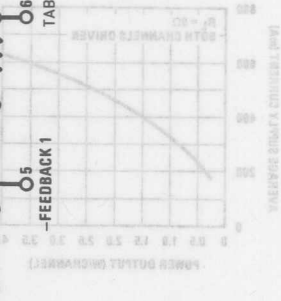
Power Output
vs Frequency



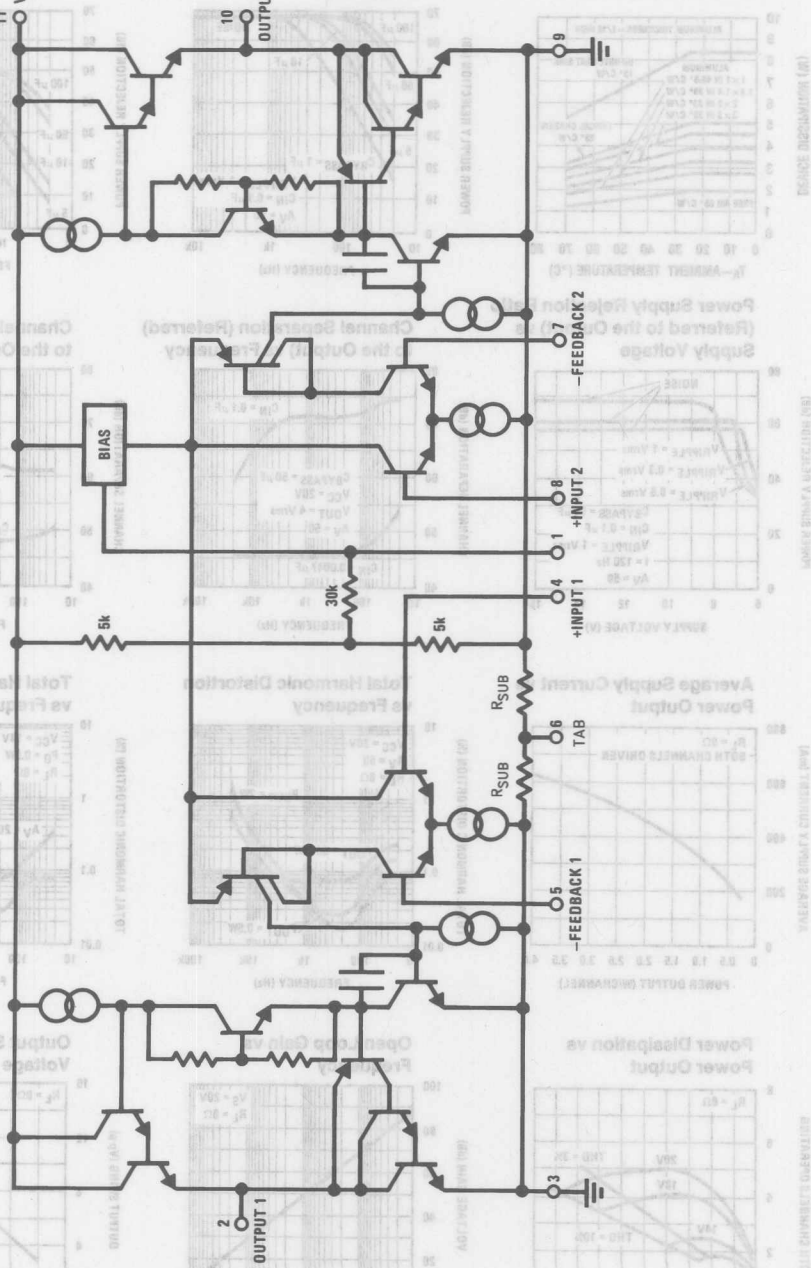
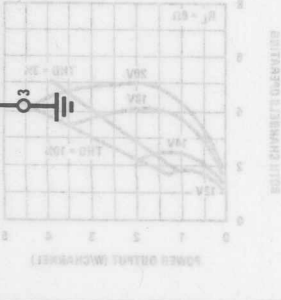
Power Supply Rejection Ratio
(Referenced to the Output) vs
Frequency



Channel Separation (Referenced
to the Output) vs Frequency

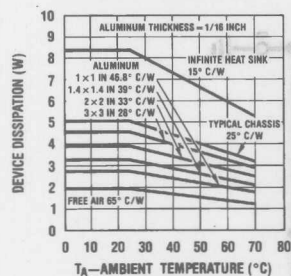


Power Output
vs Frequency

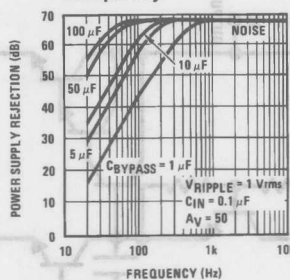


Typical Performance Characteristics

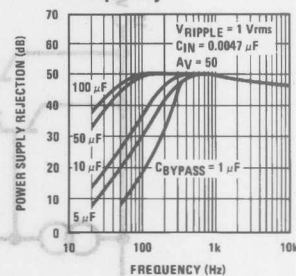
Device Dissipation vs Ambient Temperature



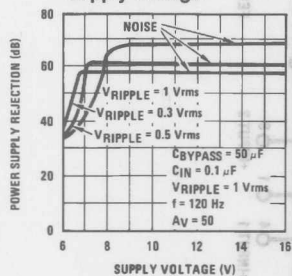
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



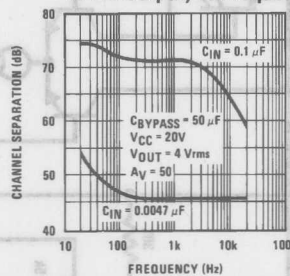
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



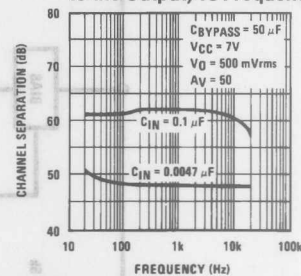
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



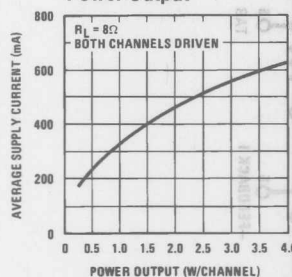
Channel Separation (Referred to the Output) vs Frequency



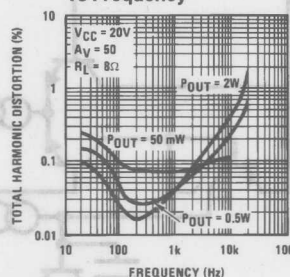
Channel Separation (Referred to the Output) vs Frequency



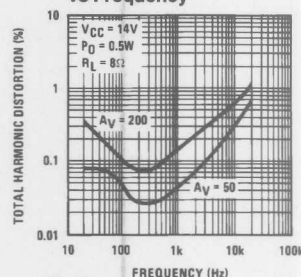
Average Supply Current vs Power Output



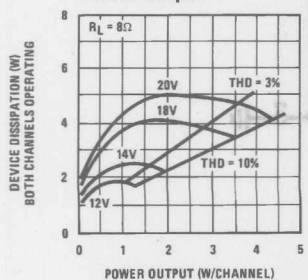
Total Harmonic Distortion vs Frequency



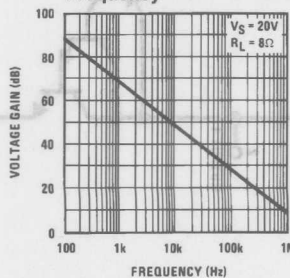
Total Harmonic Distortion vs Frequency



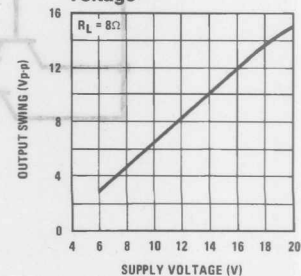
Power Dissipation vs Power Output



Open Loop Gain vs Frequency



Output Swing vs Supply Voltage

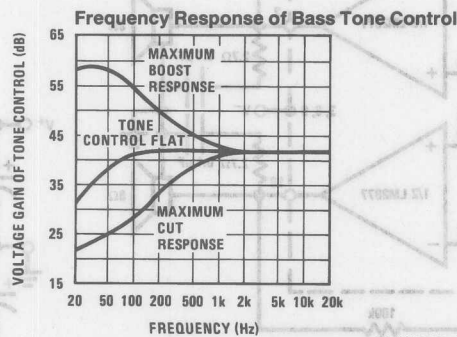
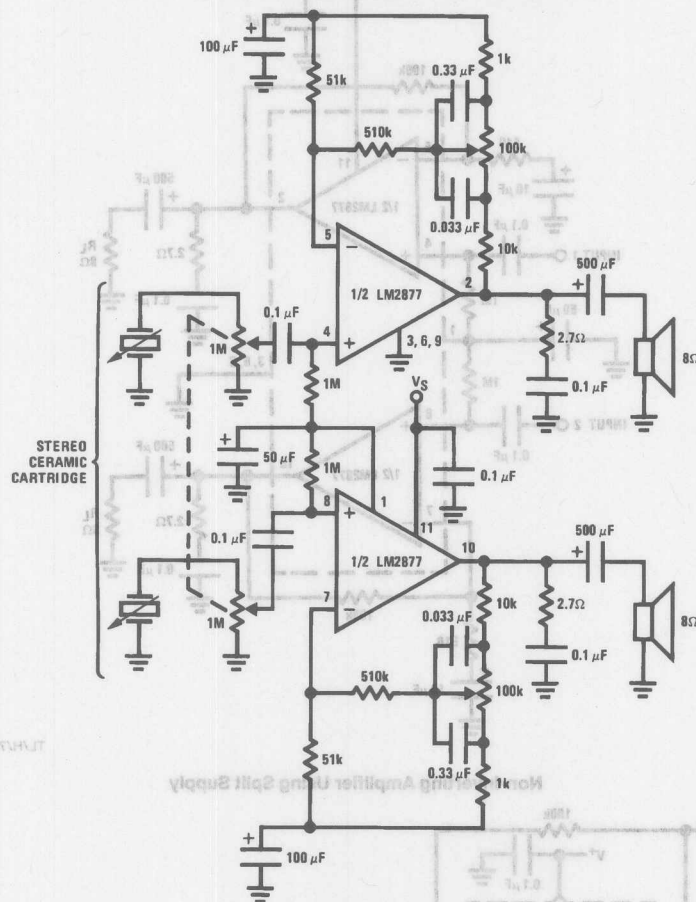


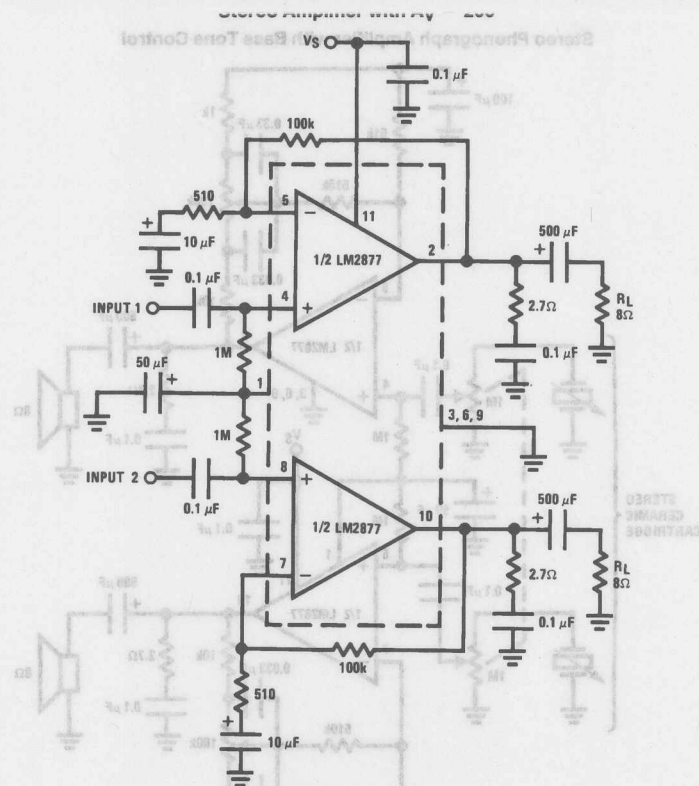
Typical Applications

(Continued) Typical Applications

LM2877

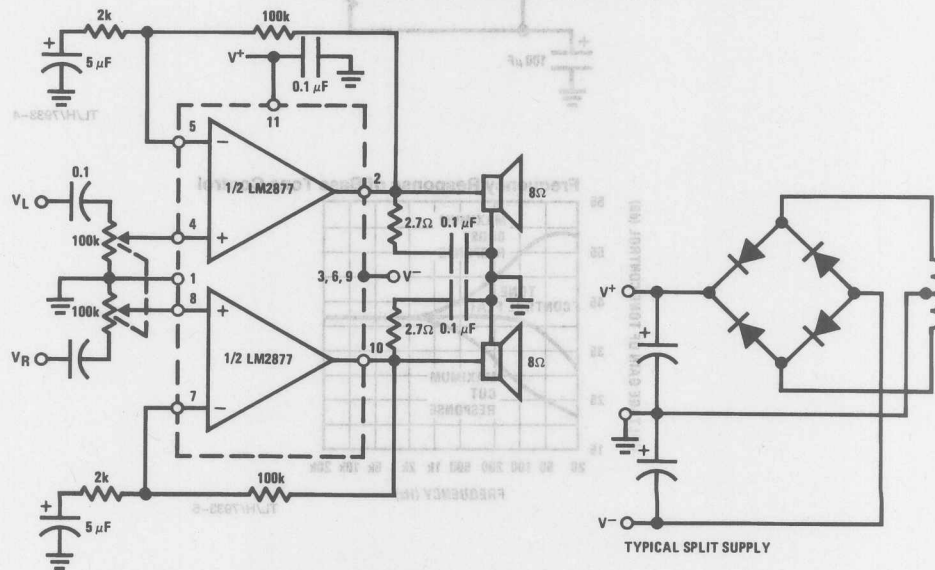
Stereo Phonograph Amplifier with Bass Tone Control





TL/H/7933-6

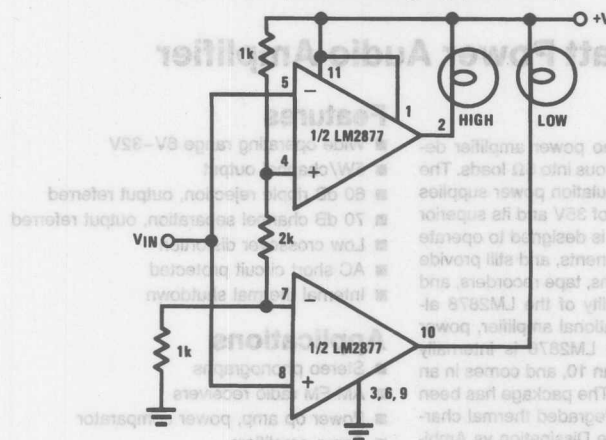
Non-Inverting Amplifier Using Split Supply



TL/H/7933-7

Typical Applications (Continued)

Window Comparator Driving High, Low Lamps



TL/H/7933-8

Truth Table

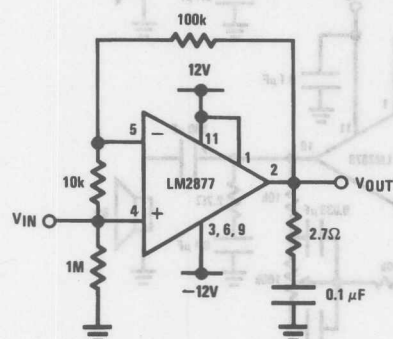
| V_{IN} | High | Low |
|---|------|-----|
| $< \frac{1}{4} V^+$ | Off | On |
| $\frac{1}{4} V^+ \text{ to } \frac{3}{4} V^+$ | Off | Off |
| $> \frac{3}{4} V^+$ | On | Off |

Application Hints

The LM2877 is an improved LM377 in typical audio applications. In the LM2877, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within $\pm 0.7V$ of this pin 1 voltage. Nevertheless, the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2877 is to limit the maximum input differential voltage to $\pm 7V$. If this differential voltage is exceeded, the input characteristics may change.

Figure 1 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 M Ω resistor.



TL/H/7933-9

FIGURE 1

LM2878 Dual 5 Watt Power Audio Amplifier

General Description

The LM2878 is a high voltage stereo power amplifier designed to deliver 5W/channel continuous into 8Ω loads. The amplifier is ideal for use with low regulation power supplies due to the absolute maximum rating of 35V and its superior power supply rejection. The LM2878 is designed to operate with a low number of external components, and still provide flexibility for use in stereo phonographs, tape recorders, and AM-FM stereo receivers. The flexibility of the LM2878 allows it to be used as a power operational amplifier, power comparator or servo amplifier. The LM2878 is internally compensated for all gains greater than 10, and comes in an 11-lead single-in-line package (SIP). The package has been redesigned, resulting in the slightly degraded thermal characteristics shown in the figure Device Dissipation vs Ambient Temperature.

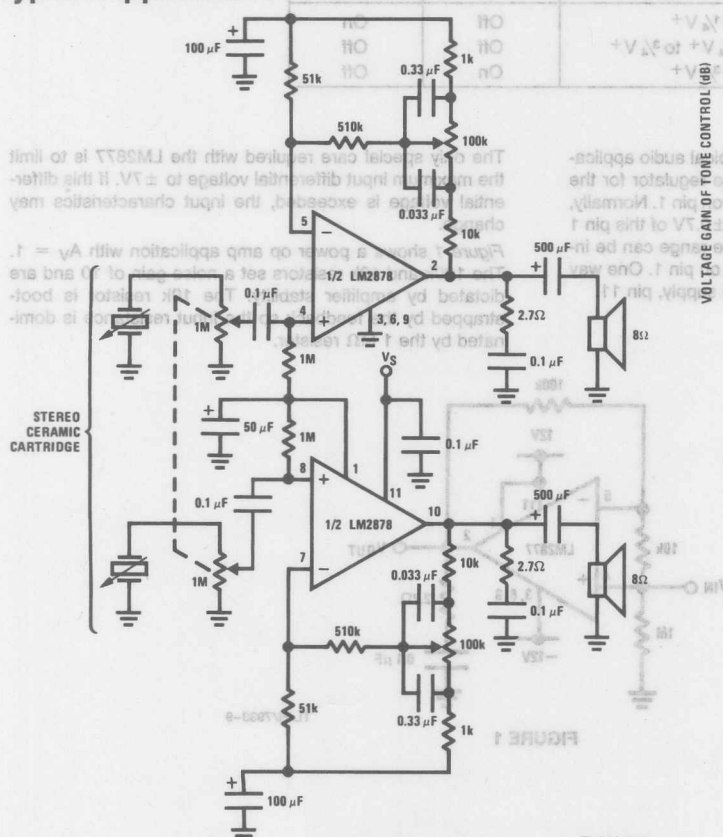
Features

- Wide operating range 6V–32V
- 5W/channel output
- 60 dB ripple rejection, output referred
- 70 dB channel separation, output referred
- Low crossover distortion
- AC short circuit protected
- Internal thermal shutdown

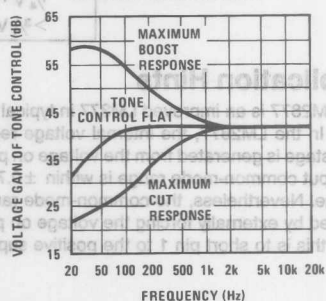
Applications

- Stereo phonographs
- AM-FM radio receivers
- Power op amp, power comparator
- Servo amplifiers

Typical Applications



Frequency Response of Bass Tone Control



TL/H/7934-2

TL/H/7934-1

FIGURE 1. Stereo Phonograph Amplifier with Bass Tone Control

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------|--------------------------------|
| Supply Voltage | 35V |
| Input Voltage (Note 1) | $\pm 0.7V$ |
| Operating Temperature (Note 2) | $0^{\circ}C$ to $+70^{\circ}C$ |

| | |
|---------------------------------------|------------------------------------|
| Storage Temperature | $-65^{\circ}C$ to $+150^{\circ}C$ |
| Junction Temperature | $+150^{\circ}C$ |
| Lead Temperature (Soldering, 10 sec.) | $+260^{\circ}C$ |
| Thermal Resistance | $10^{\circ}C/W$ $55^{\circ}C/W$ |
| θ_{JC} | |
| θ_{JA} | |

Electrical Characteristics $V_S = 22V$, $T_{TAB} = 25^{\circ}C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB) unless otherwise specified.

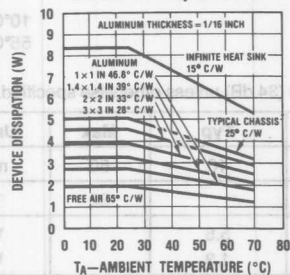
| Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------------|---|-----|------------|-----|------------|
| Total Supply Current | $P_O = 0W$ | | 10 | 50 | mA |
| Operating Supply Voltage | | 6 | | 32 | V |
| Output Power/Channel | $f = 1\text{ kHz}$, THD = 10%, $T_{TAB} = 25^{\circ}C$ $f = 1\text{ kHz}$, THD = 10%, $V_S = 12V$ | 5 | 5.5 1.3 | | W W |
| Distortion | $f = 1\text{ kHz}$, $R_L = 8\Omega$ $P_O = 50\text{ mW}$ | | 0.20 | | % |
| | $P_O = 0.5W$ | | 0.15 | | % |
| | $P_O = 2W$ | | 0.14 | | % |
| Output Swing | $R_L = 8\Omega$ | | $V_S - 6V$ | | Vp-p |
| Channel Separation | $C_{BYPASS} = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$ $f = 1\text{ kHz}$, Output Referred $V_O = 4\text{ Vrms}$ | -50 | -70 | | dB |
| PSRR Power Supply Rejection Ratio | $C_{BYPASS} = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$ $f = 120\text{ Hz}$, Output Referred $V_{ripple} = 1\text{ Vrms}$ | -50 | -60 | | dB |
| PSRR Negative Supply | Measured at DC, Input Referred | | -60 | | dB |
| Common-Mode Range | Split Supplies $\pm 15V$, Pin 1 Tied to Pin 11 | | ± 13.5 | | V |
| Input Offset Voltage | | | 10 | | mV |
| Noise | Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$ $BW = 20 - 20\text{ kHz}$ | | 2.5 | | μV |
| | CCIR*ARM | | 3.0 | | μV |
| | Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$, $A_V = 200$ | | 0.8 | | mV |
| Open Loop Gain | $R_S = 51\Omega$, $f = 1\text{ kHz}$, $R_L = 8\Omega$ | | 70 | | dB |
| Input Bias Current | | | 100 | | nA |
| Input Impedance | Open Loop | | 4 | | M Ω |
| DC Output Voltage | $V_S = 22V$ | 10 | 11 | 12 | V |
| Slew Rate | | | 2 | | V/ μS |
| Power Bandwidth | 3 dB Bandwidth at 2.5W | | 65 | | kHz |
| Current Limit | | | 1.5 | | A |

Note 1: $\pm 0.7V$ applies to audio applications; for extended range, see Application Hints.

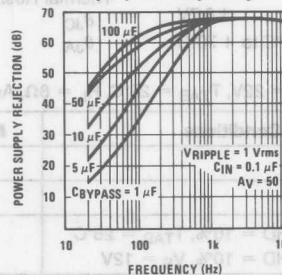
Note 2: For operation at ambient temperature greater than $25^{\circ}C$, the LM2878 must be derated based on a maximum $150^{\circ}C$ junction temperature using a thermal resistance which depends upon device mounting techniques.

Typical Performance Characteristics

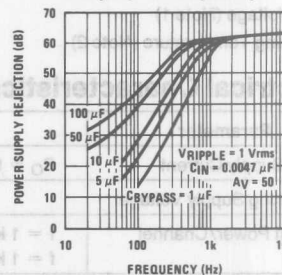
Device Dissipation vs Ambient Temperature



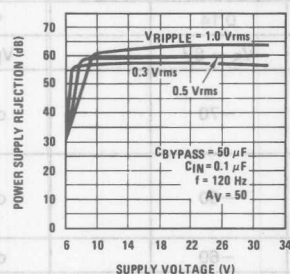
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



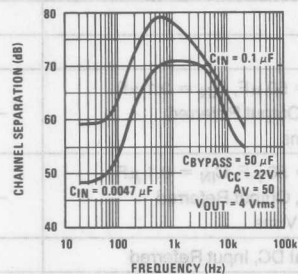
Power Supply Rejection Ratio (Referred to the Output) vs Frequency



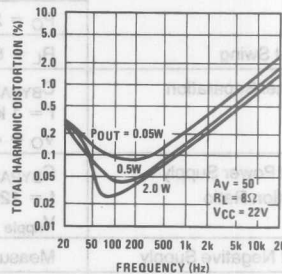
Power Supply Rejection Ratio (Referred to the Output) vs Supply Voltage



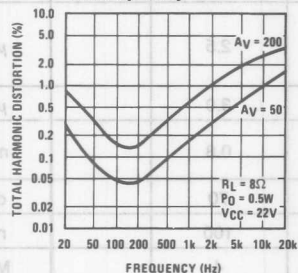
Channel Separation (Referred to the Output) vs Frequency



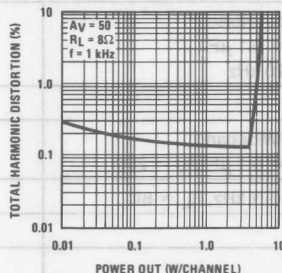
Total Harmonic Distortion vs Frequency



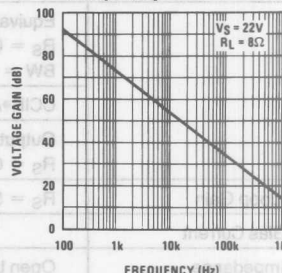
Total Harmonic Distortion vs Frequency



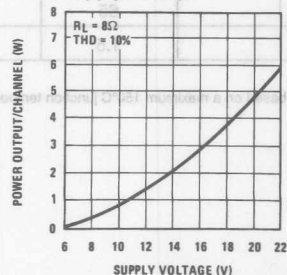
Total Harmonic Distortion vs Power Out



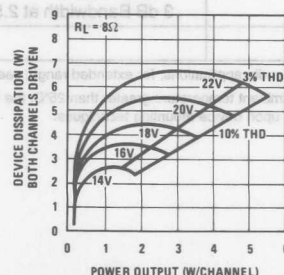
Open Loop Gain vs Frequency



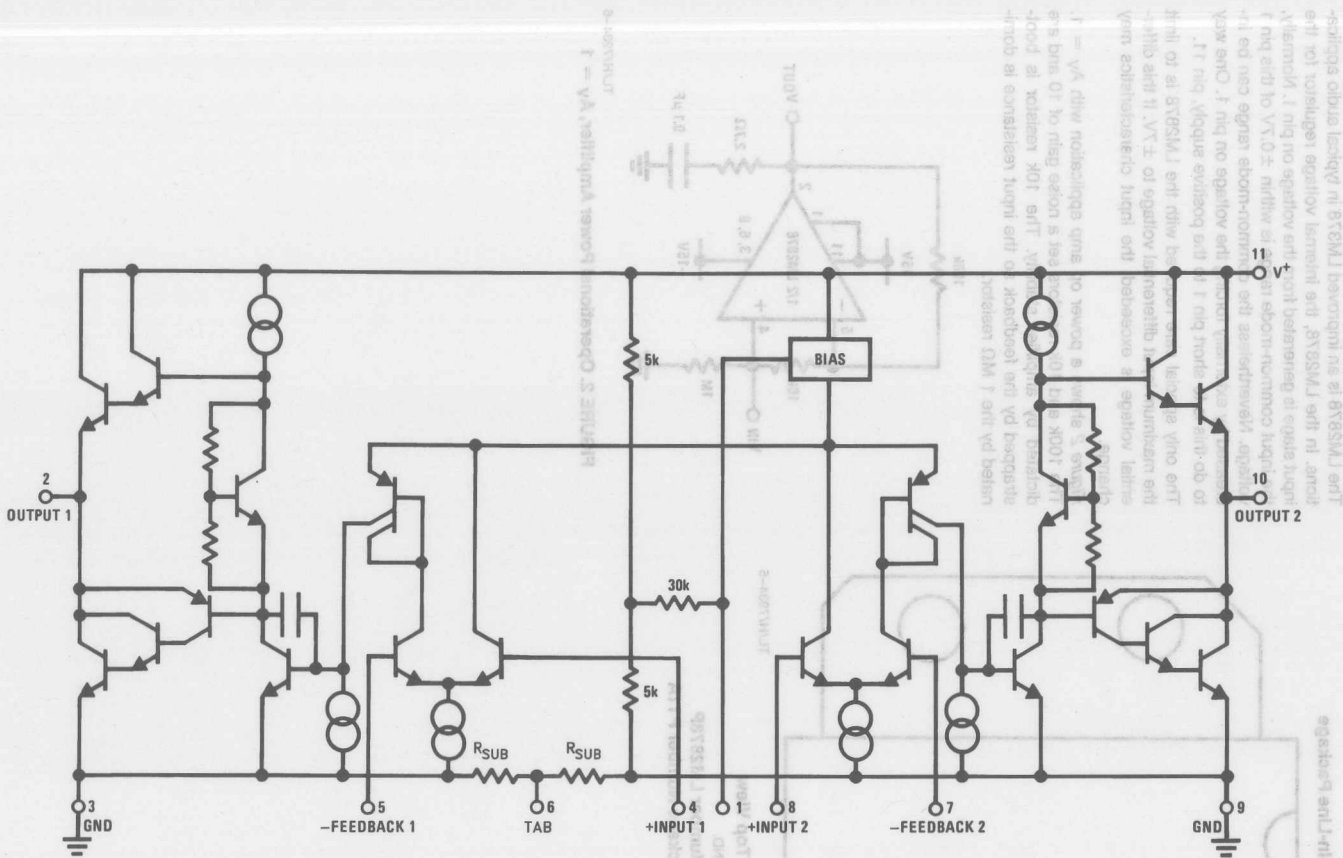
Power Output/Channel vs Supply Voltage



Power Dissipation vs Power Out



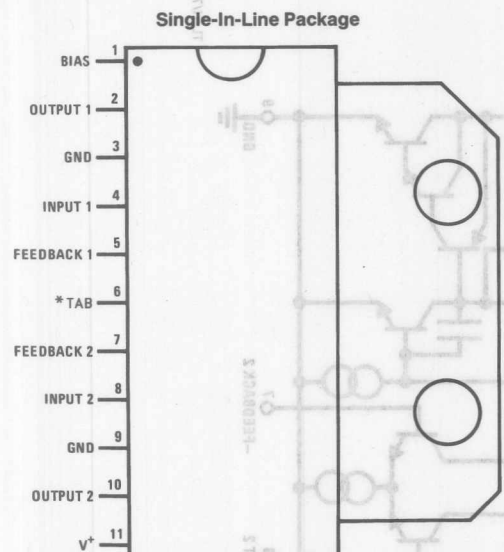
Equivalent Schematic Diagram



TL/H/7934-4

LM2878

Connection Diagram



Top View

*Pin 6 must be connected to GND.

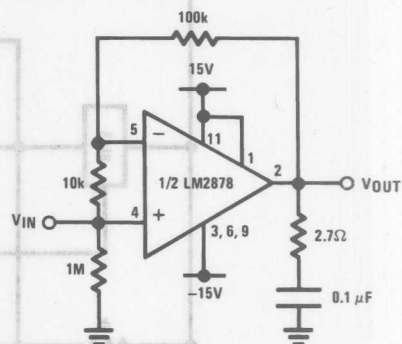
Order Number LM2878P
See NS Package Number P11A

Application Hints

The LM2878 is an improved LM378 in typical audio applications. In the LM2878, the internal voltage regulator for the input stage is generated from the voltage on pin 1. Normally, the input common-mode range is within $\pm 0.7V$ of this pin 1 voltage. Nevertheless the common-mode range can be increased by externally forcing the voltage on pin 1. One way to do this is to short pin 1 to the positive supply, pin 11.

The only special care required with the LM2878 is to limit the maximum input differential voltage to $\pm 7V$. If this differential voltage is exceeded, the input characteristics may change.

Figure 2 shows a power op amp application with $A_V = 1$. The 100k and 10k resistors set a noise gain of 10 and are dictated by amplifier stability. The 10k resistor is bootstrapped by the feedback so the input resistance is dominated by the 1 M Ω resistor.



TL/H/7934-6

FIGURE 2. Operational Power Amplifier, $A_V = 1$

External Components (Figure 3)

1. R2, R5, R7, R10 Sets voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R10/R7$ for the other channel.
2. R4, R8 Resistors set input impedance and supply bias current for the positive input.
3. R_O Works with C_O to stabilize output stage.
4. C1 Improves power supply rejection (see Typical Performance Characteristics).
5. C11 Stabilizes amplifier, may need to be larger depending on power supply filtering.

Typical Applications (Continued)

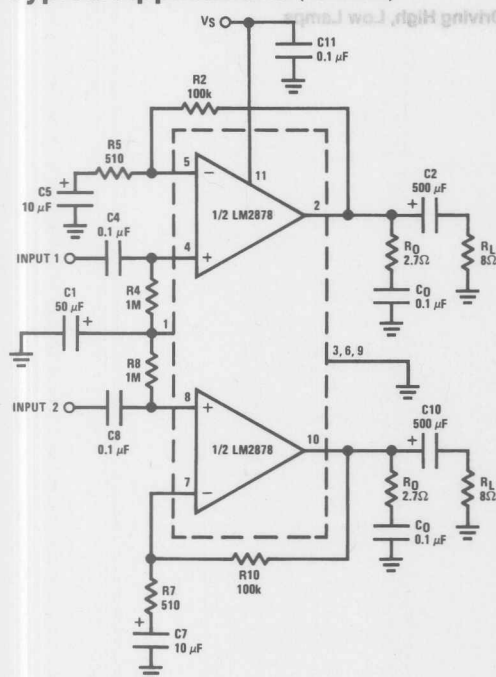


FIGURE 3. Stereo Amplifier with $A_V = 200$

TL/H/7934-7

6. C4, C8 Input coupling capacitor. Pins 4 and 8 are at a DC potential of $V_S/2$. Low frequency pole set by:

$$f_L = \frac{1}{2\pi R4C4}$$
7. C5, C7 Feedback capacitors. Ensure unity gain at DC. Also low frequency pole at:

$$f_L = \frac{1}{2\pi R5C5}$$
8. C_O Works with R_O to stabilize output stage.
9. C2, C10 Output coupling capacitor. Low frequency pole given by:

$$f_L = \frac{1}{R\pi RLC2}$$

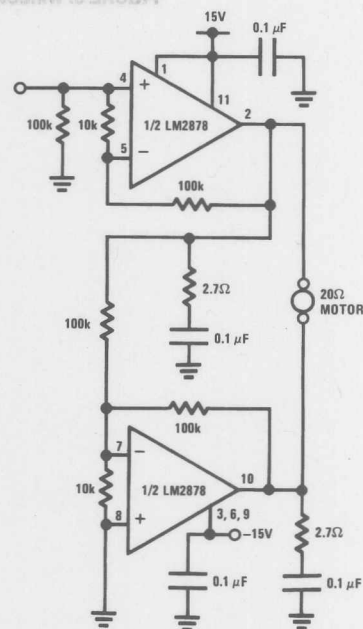
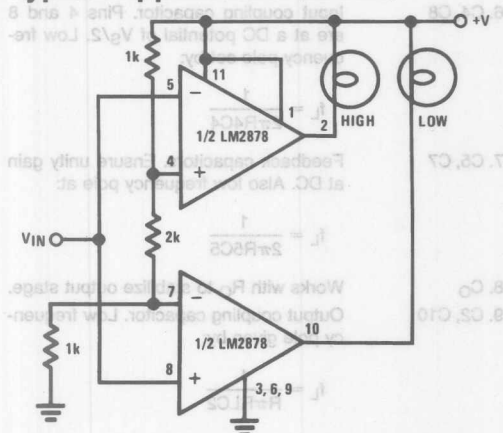


FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

TL/H/7934-8

Typical Applications (Continued)



TL/H/7934-9

FIGURE 5. Window Comparator Driving High, Low Lamps

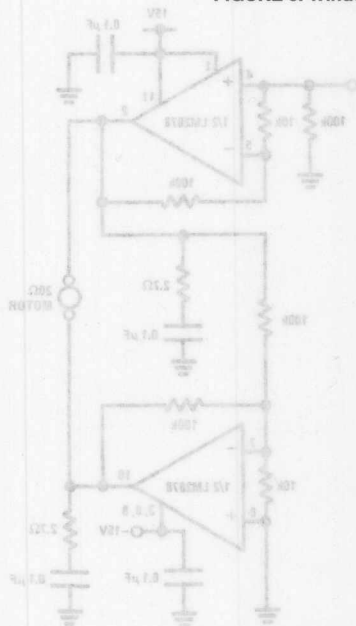
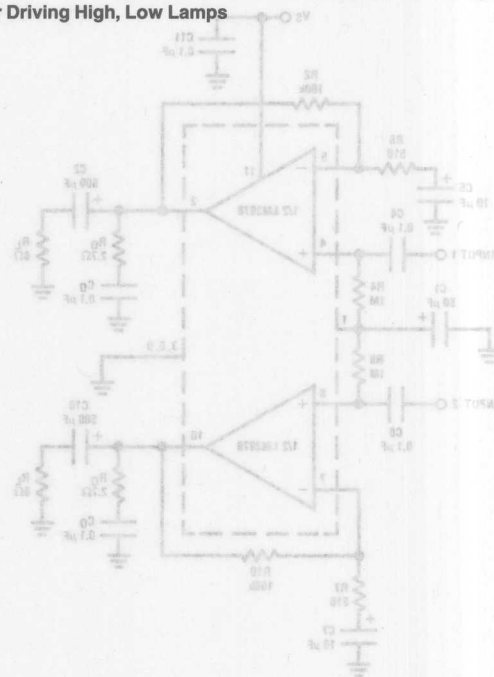


FIGURE 4. LM2878 Servo Amplifier in Bridge Configuration

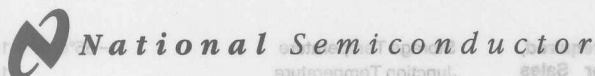
FIGURE 3. Stereo Amplifier with $A_V = 200$

External Components (Figure 3)

1. R2, R5, R7, R10 Set voltage gain $A_V = 1 + R2/R5$ for one channel and $A_V = 1 + R7/R10$ for the other channel.
 2. R4, R6 Set input impedance and supply current for the input stage.
 3. R3, R9 Set input impedance for the output stage.
 4. C1, C2 Input coupling capacitors (see typical performance characteristics).
 5. C11 Stabilizes amplifier, may need to be large depending on power supply filtering.

Truth Table

| V_{IN} | High | Low |
|--------------------------------------|------|-----|
| $V_{IN} < \frac{1}{4}V_+$ | Off | On |
| $\frac{1}{4}V_+$ to $\frac{3}{4}V_+$ | Off | Off |
| $V_{IN} > \frac{3}{4}V_+$ | On | Off |



LM2879

LM2879 Dual 8W Audio Amplifier

General Description

The LM2879 is a monolithic dual power amplifier which offers high quality performance for stereo phonographs, tape players, recorders, AM-FM stereo receivers, etc.

The LM2879 will deliver 8W/channel to an 8Ω load. The amplifier is designed to operate with a minimum of external components and contains an internal bias regulator to bias each amplifier. Device overload protection consists of both internal current limit and thermal shutdown.

Features

- A_{VO} typical 90 dB
- 9W per channel (typical)
- 60 dB ripple rejection
- 70 dB channel separation

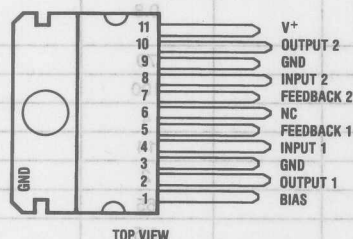
- Self-centering biasing
- 4 MΩ input impedance
- Internal current limiting
- Internal thermal protection

Applications

- Multi-channel audio systems
- Tape recorders and players
- Movie projectors
- Automotive systems
- Stereo phonographs
- Bridge output stages
- AM-FM radio receivers
- Intercoms
- Servo amplifiers
- Instrument systems

Connection Diagram and Typical Application

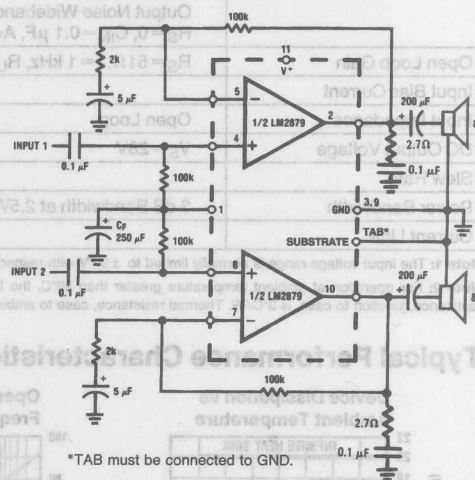
Plastic Package



TOP VIEW

Order Number LM2879T
See NS Package Number TA11B

Stereo Amplifier



*TAB must be connected to GND.

FIGURE 1

TL/H/5291-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------|--------------------------------|
| Supply Voltage | 35V |
| Input Voltage (Note 1) | $\pm 0.7V$ |
| Operating Temperature (Note 2) | $0^{\circ}C$ to $+70^{\circ}C$ |

| | |
|------------------------------------|-----------------------------------|
| Storage Temperature | $-65^{\circ}C$ to $+150^{\circ}C$ |
| Junction Temperature | $150^{\circ}C$ |
| Lead Temp. (Soldering, 10 seconds) | $260^{\circ}C$ |
| ESD rating to be determined. | |
| Thermal Resistance | |
| θ_{JC} | $1^{\circ}C/W$ |
| θ_{JA} | $43^{\circ}C/W$ |

Electrical Characteristics

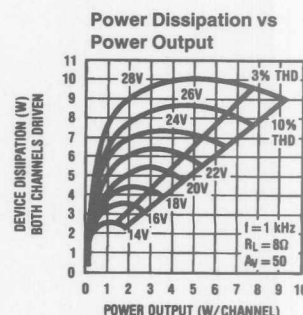
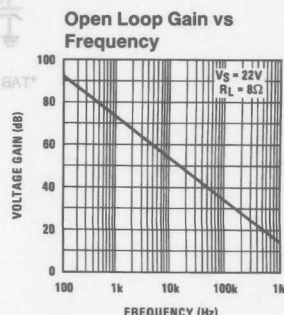
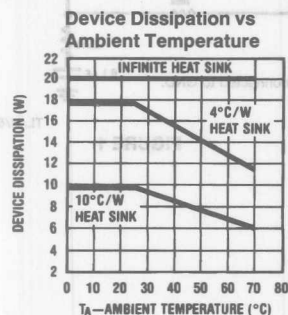
$V_S = 28V$, $T_{TAB} = 25^{\circ}C$, $R_L = 8\Omega$, $A_V = 50$ (34 dB), unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------|---|-----|-------------------|-----|--------------------------|
| Total Supply Current | $P_O = 0W$ | | 12 | 65 | mA |
| Operating Supply Voltage | | 6 | | 32 | V |
| Output Power/Channel | $f = 1\text{ kHz}$, THD = 10%, $T_{TAB} = 25^{\circ}C$ | 6 | 8 | | W |
| Distortion | $f = 1\text{ kHz}$, $R_L = 8\Omega$ $P_O = 1\text{ W/Channel}$ | | 0.05 | 1 | % |
| Output Swing | $R_L = 8\Omega$ | | $V_S - 6V$ | | Vp-p |
| Channel Separation | $C_{BYPASS} = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$ $f = 1\text{ kHz}$, Output Referred $V_O = 4\text{ Vrms}$ | -50 | -70 | | dB |
| PSRR Positive Supply | $C_{BYPASS} = 50\text{ }\mu F$, $C_{IN} = 0.1\text{ }\mu F$ $f = 120\text{ Hz}$, Output Referred $V_{ripple} = 1\text{ Vrms}$ | -50 | -60 | | dB |
| PSRR Negative Supply | Measured at DC, Input Referred | | -60 | | dB |
| Common-Mode Range | Split Supplies $\pm 15V$, Pin 1 Tied to Pin 11 | | ± 13.5 | | V |
| Input Offset Voltage | | | 10 | | mV |
| Noise | Equivalent Input Noise $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$ BW = 20 – 20 kHz CCIR•ARM Output Noise Wideband $R_S = 0$, $C_{IN} = 0.1\text{ }\mu F$, $A_V = 200$ | | 2.5 3.0 0.8 | | μV μV mV |
| Open Loop Gain | $R_S = 51\Omega$, $f = 1\text{ kHz}$, $R_L = 8\Omega$ | | 70 | | dB |
| Input Bias Current | | | 100 | | nA |
| Input Impedance | Open Loop | | 4 | | M Ω |
| DC Output Voltage | $V_S = 28V$ | | 14 | | V |
| Slew Rate | | | 2 | | V/ μs |
| Power Bandwidth | 3 dB Bandwidth at 2.5W | | 65 | | kHz |
| Current Limit | | | 1.5 | | A |

Note 1: The input voltage range is normally limited to $\pm 0.7V$ with respect to pin 1. This range may be extended by shorting pin 1 to the positive supply.

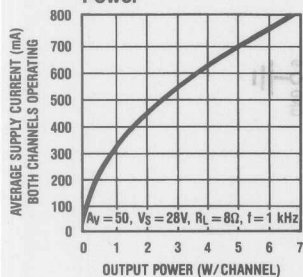
Note 2: For operation at ambient temperature greater than $25^{\circ}C$, the LM2879 must be derated based on a maximum $150^{\circ}C$ junction temperature. Thermal resistance, junction to case, is $3^{\circ}C/W$. Thermal resistance, case to ambient, is $40^{\circ}C/W$.

Typical Performance Characteristics

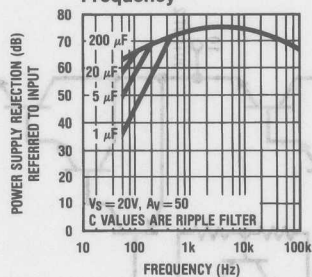


Typical Performance Characteristics (Continued)

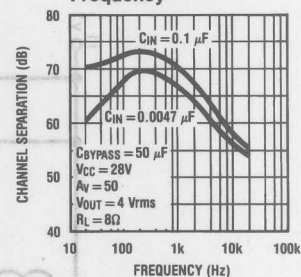
Supply Current vs Output Power



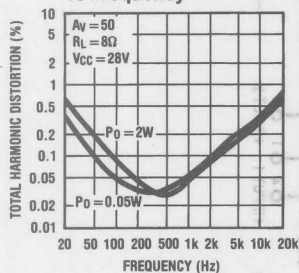
Supply Rejection vs Frequency



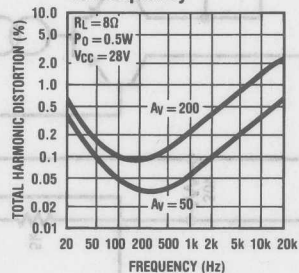
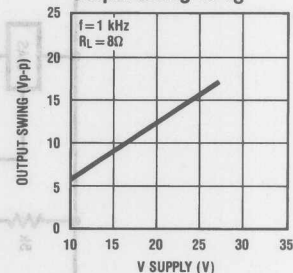
Channel Separation (Referred to the Output) vs Frequency



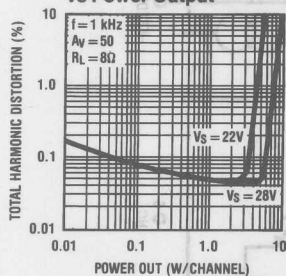
Total Harmonic Distortion vs Frequency



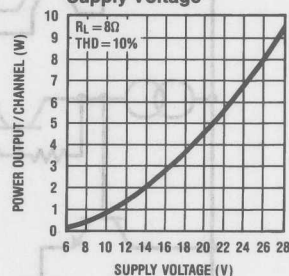
Total Harmonic Distortion vs Frequency

Output Swing vs V_S 

Total Harmonic Distortion vs Power Output

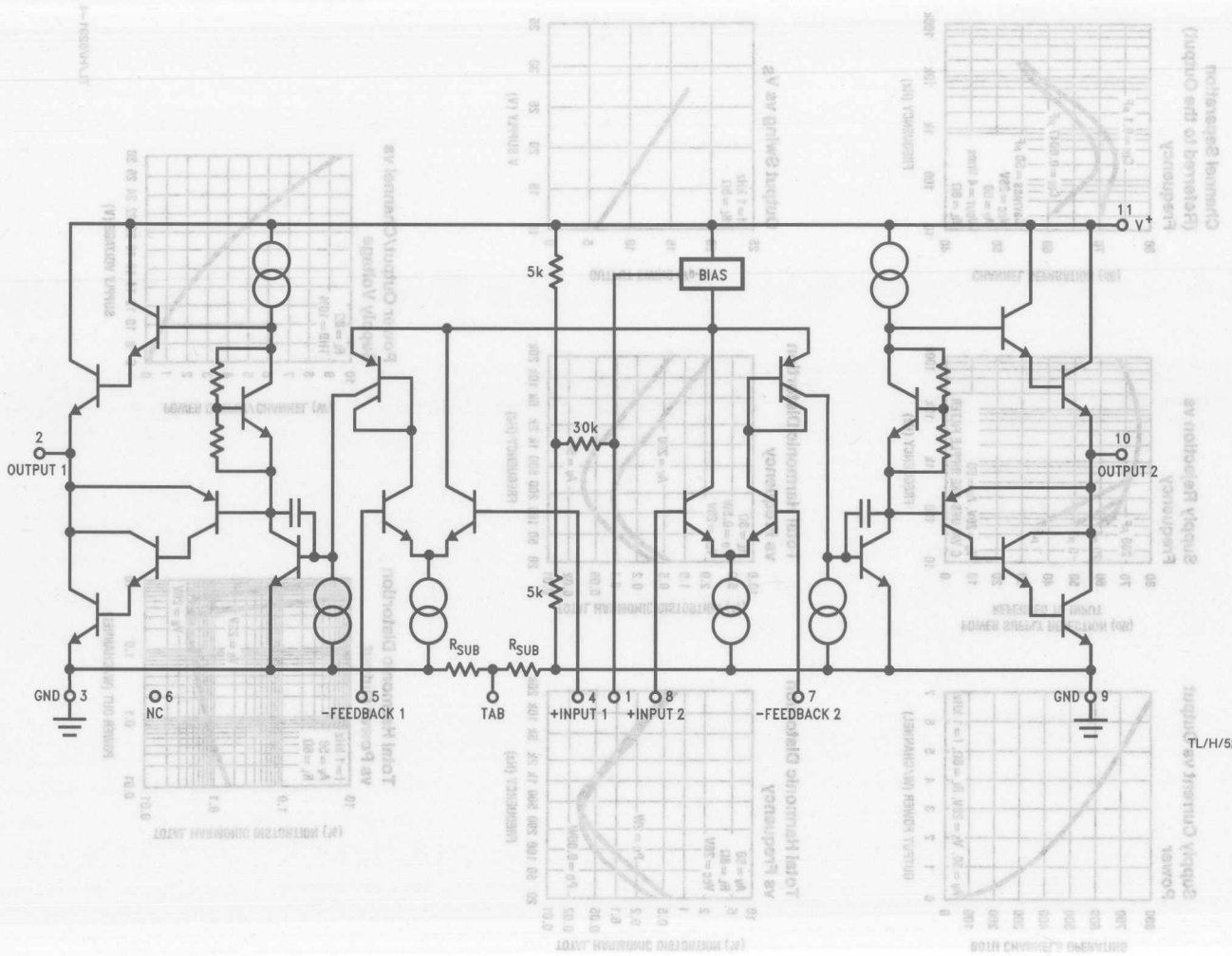


Power Output/Channel vs Supply Voltage



TL/H/5291-4

Equivalent Schematic Diagram

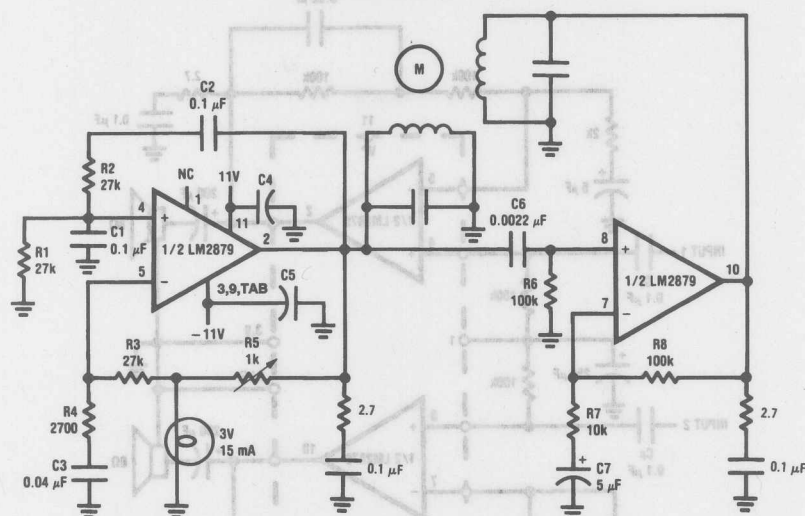


TL/H/5291-5

Typical Applications

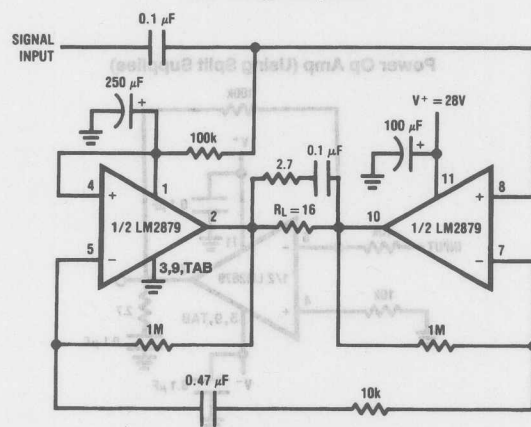
Typical Applications (Continued)

Two-Phase Motor Drive



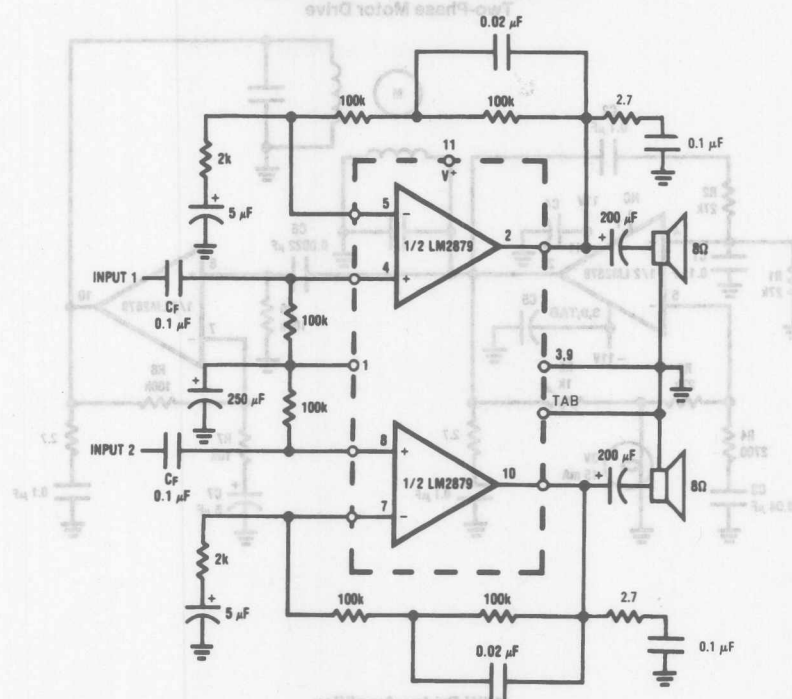
TL/H/5291-6

12W Bridge Amplifier



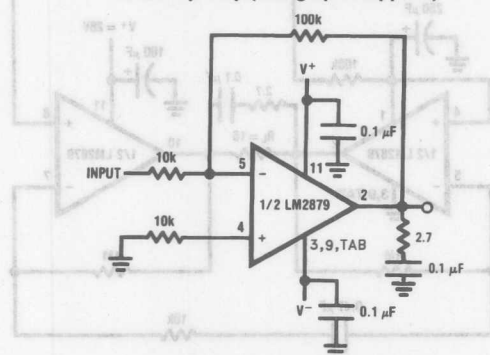
TL/H/5291-7

Simple Stereo Amplifier with Bass Boost

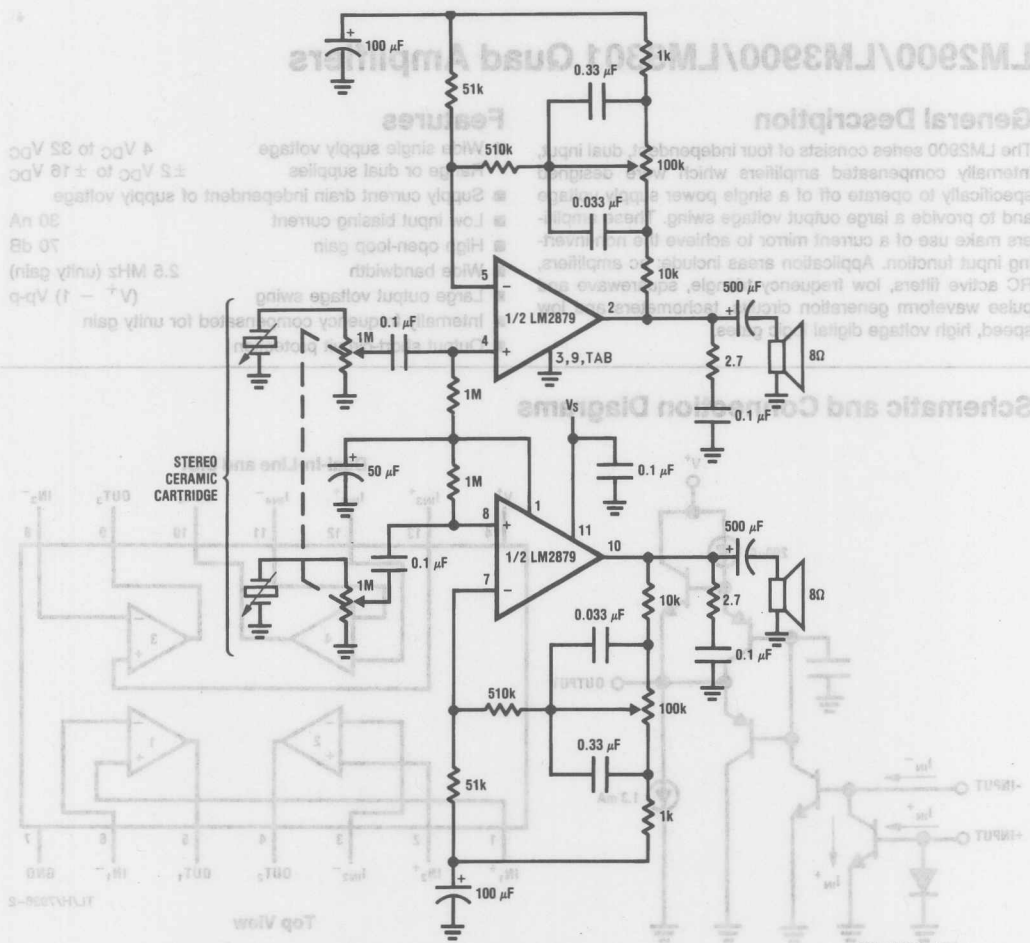


TL/H/5291-8

Power Op Amp (Using Split Supplies)

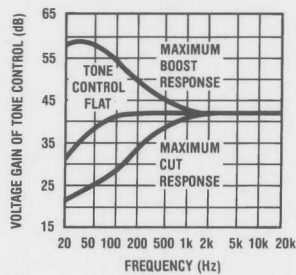


TL/H/5291-9



TL/H/5291-10

Frequency Response of Bass Tone Control



TL/H/5291-11

LM2900/LM3900/LM3301 Quad Amplifiers

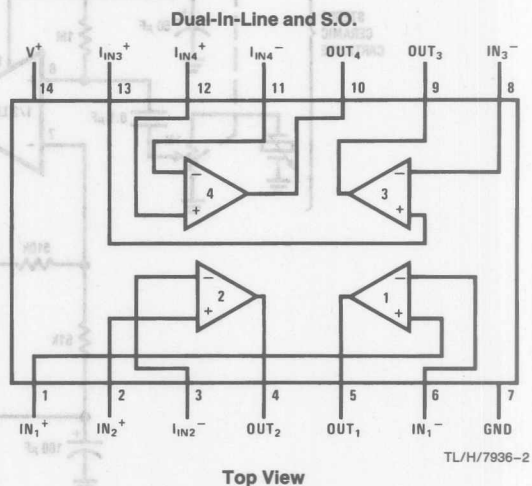
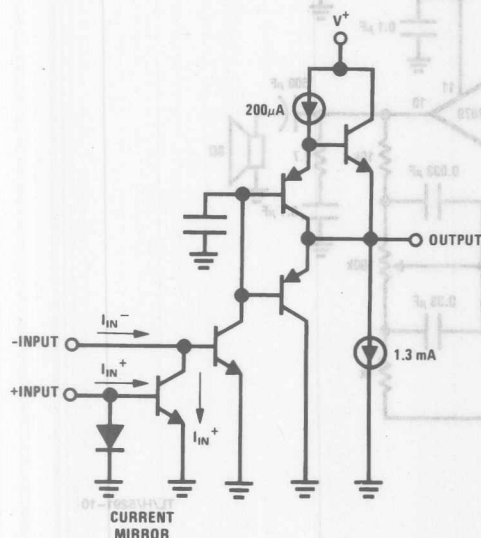
General Description

The LM2900 series consists of four independent, dual input, internally compensated amplifiers which were designed specifically to operate off of a single power supply voltage and to provide a large output voltage swing. These amplifiers make use of a current mirror to achieve the non-inverting input function. Application areas include: ac amplifiers, RC active filters, low frequency triangle, squarewave and pulse waveform generation circuits, tachometers and low speed, high voltage digital logic gates.

Features

- Wide single supply voltage 4 V_{DC} to 32 V_{DC}
- Range or dual supplies ±2 V_{DC} to ±16 V_{DC}
- Supply current drain independent of supply voltage
- Low input biasing current 30 nA
- High open-loop gain 70 dB
- Wide bandwidth 2.5 MHz (unity gain)
- Large output voltage swing ($V^+ - 1$) V_{p-p}
- Internally frequency compensated for unity gain
- Output short-circuit protection

Schematic and Connection Diagrams



Order Number LM2900N, LM3900M, LM3900N or LM3301N
See NS Package Number M14A or N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | | LM2900/LM3900 | | | LM3301 | | |
|---|--|---|--|--|---|--|--|
| Supply Voltage | | 32 V _{DC} ±16 V _{DC} | | | 28 V _{DC} ±14 V _{DC} | | |
| Power Dissipation (T _A = 25°C) (Note 1) | | 1080 mW | | | 1080 mW | | |
| Molded DIP | | | | | | | |
| S.O. Package | | 765 mW | | | | | |
| Input Currents, I _{IN} ⁺ or I _{IN} ⁻ | | 20 mA _{DC} | | | 20 mA _{DC} | | |
| Output Short-Circuit Duration—One Amplifier | | Continuous | | | Continuous | | |
| T _A = 25°C (See Application Hints) | | | | | | | |
| Operating Temperature Range | | -40°C to +85°C | | | -40°C to +85°C | | |
| LM2900 | | | | | | | |
| LM3900 | | 0°C to +70°C | | | | | |
| Storage Temperature Range | | -65°C to +150°C | | | -65°C to +150°C | | |
| Lead Temperature (Soldering, 10 sec.) | | 260°C | | | 260°C | | |
| Soldering Information | | | | | | | |
| Dual-In-Line Package | | | | | | | |
| Soldering (10 sec.) | | 260°C | | | 260°C | | |
| Small Outline Package | | | | | | | |
| Vapor Phase (60 sec.) | | 215°C | | | 215°C | | |
| Infrared (15 sec.) | | 220°C | | | 220°C | | |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | | | | | |
| ESD tolerance (Note 7) | | 2000V | | | 2000V | | |

Electrical Characteristics T_A = 25°C, V⁺ = 15 V_{DC}, unless otherwise stated

| Parameter | | Conditions | | LM2900 | | | LM3900 | | | LM3301 | | | Units |
|---------------------------|-----------------------|---|--|--------|-----|-----|--------|-----|-----|--------|-----|-----|------------------|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Open Loop | Voltage Gain | Over Temp. | | | | | | | | | | | V/mV |
| | Voltage Gain | ΔV _O = 10 V _{DC} | | 1.2 | 2.8 | | 1.2 | 2.8 | | 1.2 | 2.8 | | |
| | Input Resistance | Inverting Input | | 1 | | | 1 | | | 1 | | | MΩ |
| | Output Resistance | | | 8 | | | 8 | | | 9 | | | kΩ |
| Unity Gain Bandwidth | | Inverting Input | | 2.5 | | | 2.5 | | | 2.5 | | | MHz |
| Input Bias Current | | Inverting Input, V ⁺ = 5 V _{DC} | | 30 | 200 | | 30 | 200 | | 30 | 300 | | nA |
| Slew Rate | | Positive Output Swing | | 0.5 | | | 0.5 | | | 0.5 | | | V/μs |
| | | Negative Output Swing | | 20 | | | 20 | | | 20 | | | |
| Supply Current | | R _L = ∞ On All Amplifiers | | 6.2 | 10 | | 6.2 | 10 | | 6.2 | 10 | | mA _{DC} |
| Output Voltage Swing | V _{OUT} High | R _L = 2k, I _{IN} ⁻ = 0, V ⁺ = 15.0 V _{DC} | | 13.5 | | | 13.5 | | | 13.5 | | | V _{DC} |
| | V _{OUT} Low | I _{IN} ⁻ = 10 μA, I _{IN} ⁺ = 0 | | 0.09 | 0.2 | | 0.09 | 0.2 | | 0.09 | 0.2 | | |
| | V _{OUT} High | V ⁺ = Absolute Maximum Ratings, I _{IN} ⁻ = 0, I _{IN} ⁺ = 0, R _L = ∞ | | 29.5 | | | 29.5 | | | 26.0 | | | |
| Output Current Capability | Source | | | 6 | 18 | | 6 | 10 | | 5 | 18 | | mA _{DC} |
| | Sink | (Note 2) | | 0.5 | 1.3 | | 0.5 | 1.3 | | 0.5 | 1.3 | | |
| | I _{SINK} | V _{OL} = 1V, I _{IN} ⁻ = 5 μA | | 5 | | | 5 | | | 5 | | | |

Electrical Characteristics (Note 6), $V^+ = 15\text{ V}_{\text{DC}}$, unless otherwise stated (Continued)

| Parameter | Conditions | LM2900 | | | LM3900 | | | LM3301 | | | Units |
|------------------------|--|--------|-----|-----|--------|-----|-----|--------|-----|------|---------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Power Supply Rejection | $T_A = 25^\circ\text{C}$, $f = 100\text{ Hz}$ | | 70 | | | 70 | | | 70 | | dB |
| Mirror Gain | @ $20\text{ }\mu\text{A}$ (Note 3) | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | 0.90 | 1 | 1.10 | $\mu\text{A}/\mu\text{A}$ |
| | @ $200\text{ }\mu\text{A}$ (Note 3) | 0.90 | 1.0 | 1.1 | 0.90 | 1.0 | 1.1 | 0.90 | 1 | 1.10 | |
| Δ Mirror Gain | @ $20\text{ }\mu\text{A}$ to $200\text{ }\mu\text{A}$ (Note 3) | | 2 | 5 | | 2 | 5 | | 2 | 5 | % |
| Mirror Current | (Note 4) | | 10 | 500 | | 10 | 500 | | 10 | 500 | μA_{DC} |
| Negative Input Current | $T_A = 25^\circ\text{C}$ (Note 5) | | 1.0 | | | 1.0 | | | 1.0 | | mA_{DC} |
| Input Bias Current | Inverting Input | | 300 | | | 300 | | | | | nA |

Note 1: For operating at high temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of $92^\circ\text{C}/\text{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. Thermal resistance for the S.O. package is $131^\circ\text{C}/\text{W}$.

Note 2: The output current sink capability can be increased for large signal conditions by overdriving the inverting input. This is shown in the section on Typical Characteristics.

Note 3: This spec indicates the current gain of the current mirror which is used as the non-inverting input.

Note 4: Input V_{BE} match between the non-inverting and the inverting inputs occurs for a mirror current (non-inverting input current) of approximately $10\text{ }\mu\text{A}$. This is therefore a typical design center for many of the application circuits.

Note 5: Clamp transistors are included on the IC to prevent the input voltages from swinging below ground more than approximately $-0.3\text{ V}_{\text{DC}}$. The negative input currents which may result from large signal overdrive with capacitance input coupling need to be externally limited to values of approximately 1 mA . Negative input currents in excess of 4 mA will cause the output voltage to drop to a low voltage. This maximum current applies to any one of the input terminals. If more than one of the input terminals are simultaneously driven negative smaller maximum currents are allowed. Common-mode current biasing can be used to prevent negative input voltages; see for example, the "Differentiator Circuit" in the applications section.

Note 6: These specs apply for $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, unless otherwise stated.

Note 7: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Application Hints

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak input current. Currents as large as 20 mA will not damage the device, but the current mirror on the non-inverting input will saturate and cause a loss of mirror gain at mA current levels—especially at high operating temperatures.

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

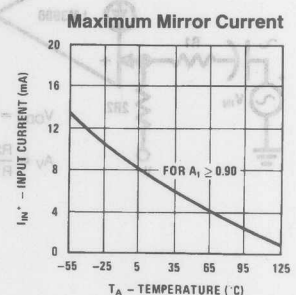
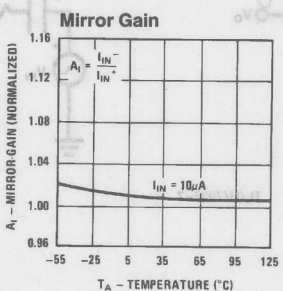
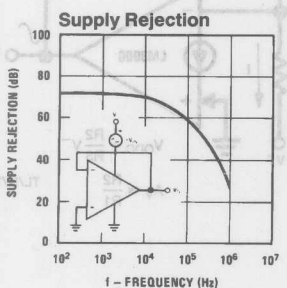
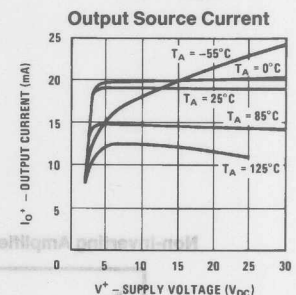
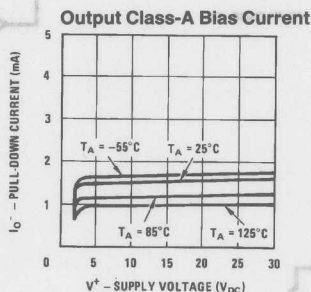
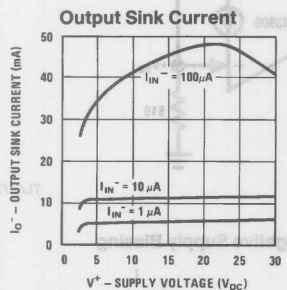
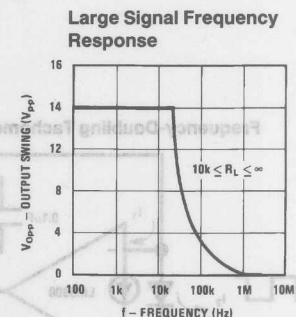
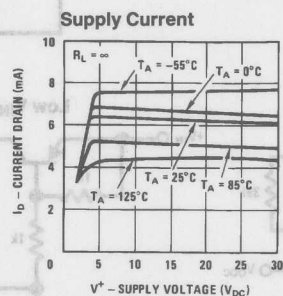
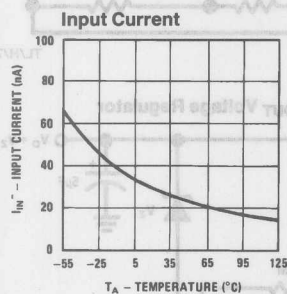
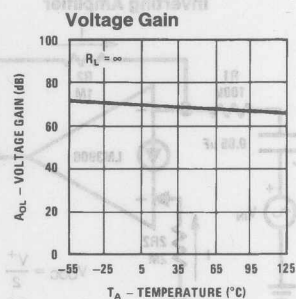
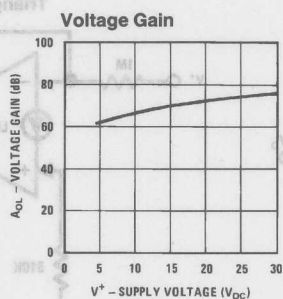
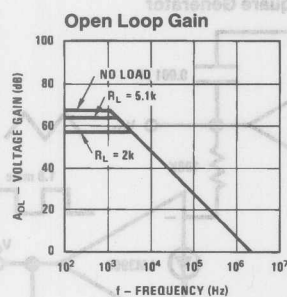
Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. For example, when operating from a well-regulated $+5\text{ V}_{\text{DC}}$ power supply at $T_A = 25^\circ\text{C}$ with a $100\text{ k}\Omega$ shunt-feedback resistor (from the output to the inverting input) a short directly to the power supply will not cause catastrophic failure but the current magnitude will be approximately 50 mA and the junction temperature will be above T_J max. Larger feedback resistors will reduce the current, $11\text{ M}\Omega$ provides approximately 30 mA , an open circuit provides 1.3 mA , and a direct connection from the output to the non-inverting input will result in catastrophic failure when the output is shorted to V^+ as this then places the base-emitter junction of the input transistor directly across the power supply. Short-circuits to ground will have magnitudes of approximately 30 mA and will not cause catastrophic failure at $T_A = 25^\circ\text{C}$.

Unintentional signal coupling from the output to the non-inverting input can cause oscillations. This is likely only in breadboard hook-ups with long component leads and can be prevented by a more careful lead dress or by locating the non-inverting input biasing resistor close to the IC. A quick check of this condition is to bypass the non-inverting input to ground with a capacitor. High impedance biasing resistors used in the non-inverting input circuit make this input lead highly susceptible to unintentional AC signal pickup.

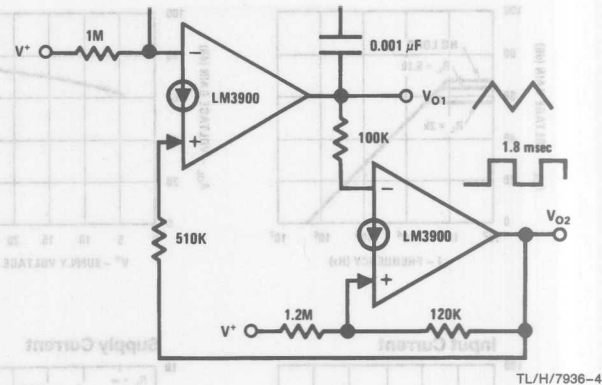
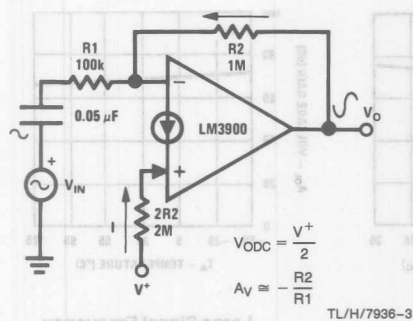
Operation of this amplifier can be best understood by noticing that input currents are differenced at the inverting-input terminal and this difference current then flows through the external feedback resistor to produce the output voltage. Common-mode current biasing is generally useful to allow operating with signal levels near ground or even negative as this maintains the inputs biased at $+V_{\text{BE}}$. Internal clamp transistors (see note 5) catch-negative input voltages at approximately $-0.3\text{ V}_{\text{DC}}$ but the magnitude of current flow has to be limited by the external input network. For operation at high temperature, this limit should be approximately $100\text{ }\mu\text{A}$.

This new "Norton" current-differencing amplifier can be used in most of the applications of a standard IC op amp. Performance as a DC amplifier using only a single supply is not as precise as a standard IC op amp operating with split supplies but is adequate in many less critical applications. New functions are made possible with this amplifier which are useful in single power supply systems. For example, biasing can be designed separately from the AC gain as was shown in the "inverting amplifier," the "difference integrator" allows controlling the charging and the discharging of the integrating capacitor with positive voltages, and the "frequency doubling tachometer" provides a simple circuit which reduces the ripple voltage on a tachometer output DC voltage.

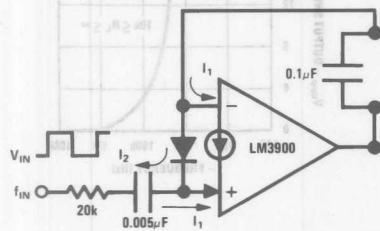
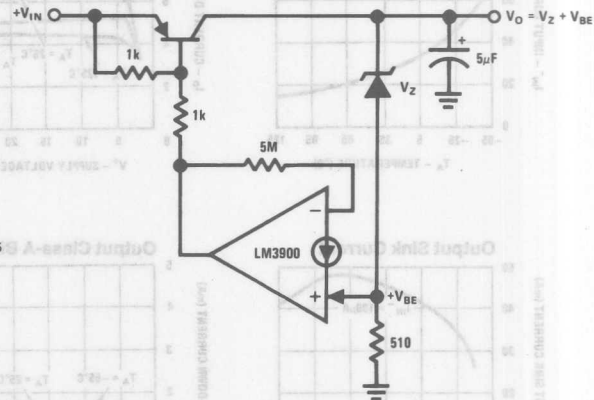
Typical Performance Characteristics



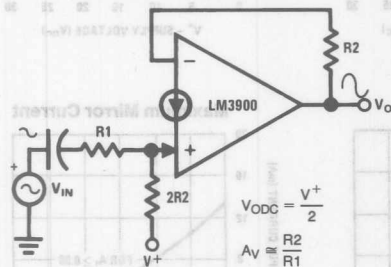
TL/H/7936-9



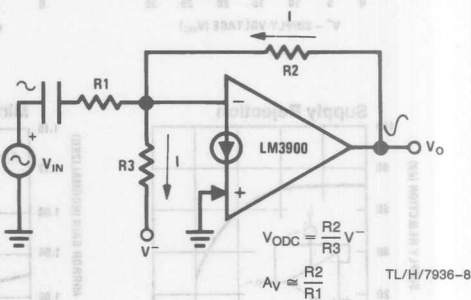
Frequency-Doubling Tachometer

Low $V_{IN} - V_{OUT}$ Voltage Regulator

Non-Inverting Amplifier

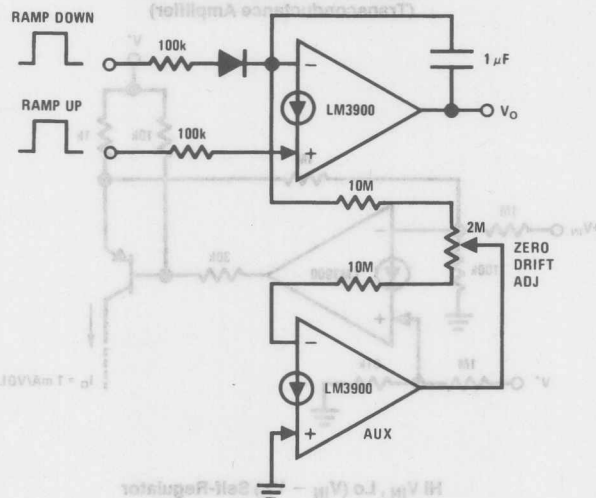


Negative Supply Biasing



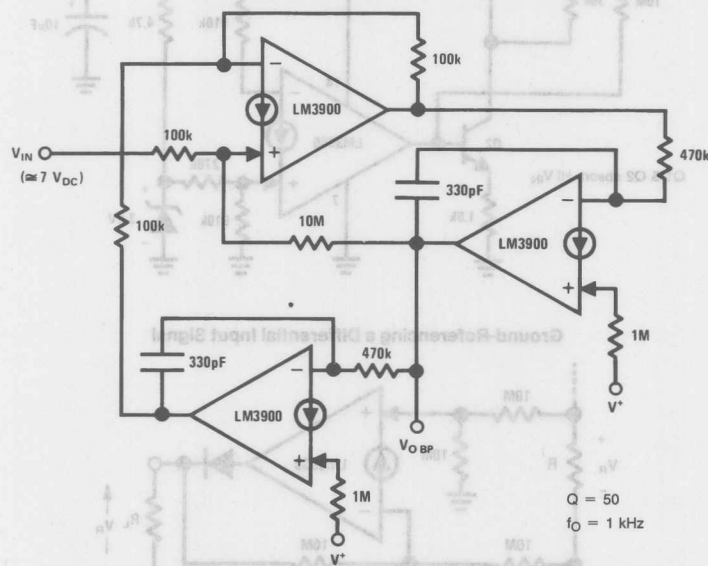
Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

Low-Drift Ramp and Hold Circuit



TL/H/7936-10

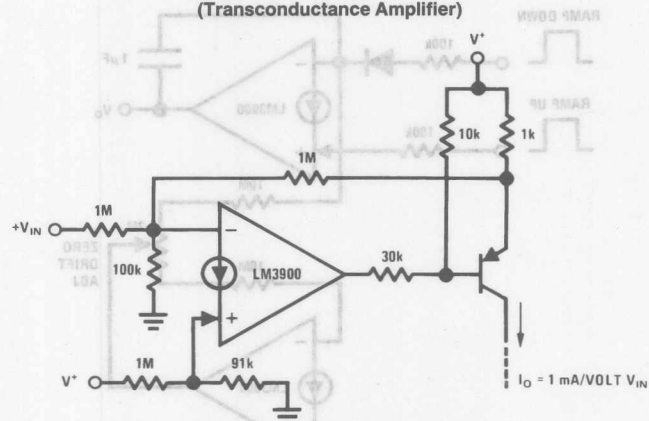
Bi-Quad Active Filter (2nd Degree State-Variable Network)


 $Q = 50$
 $f_0 = 1\text{ kHz}$

TL/H/7936-11

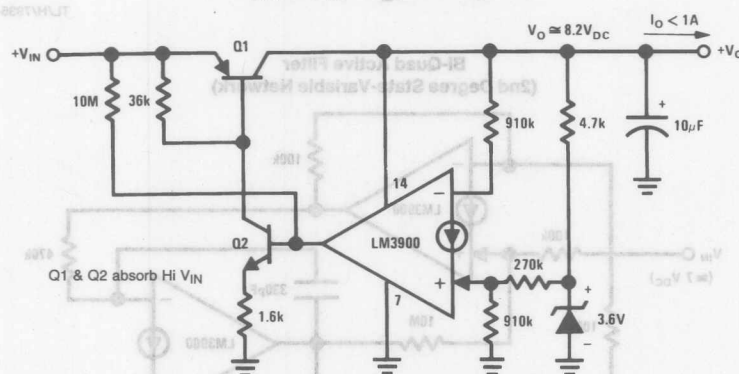
Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

Voltage-Controlled Current Source (Transconductance Amplifier)



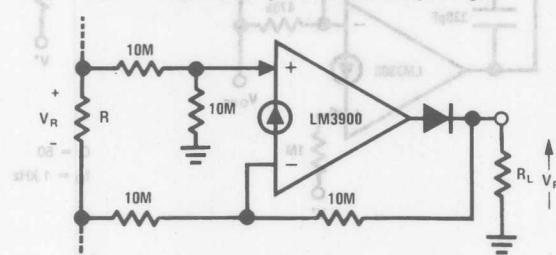
TL/H/7936-12

Hi V_{IN} , Lo ($V_{\text{IN}} - V_O$) Self-Regulator



TL/H/7936-13

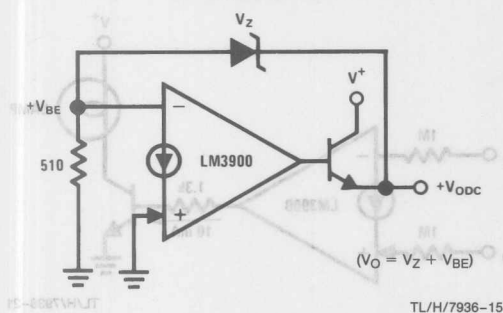
Ground-Referencing a Differential Input Signal



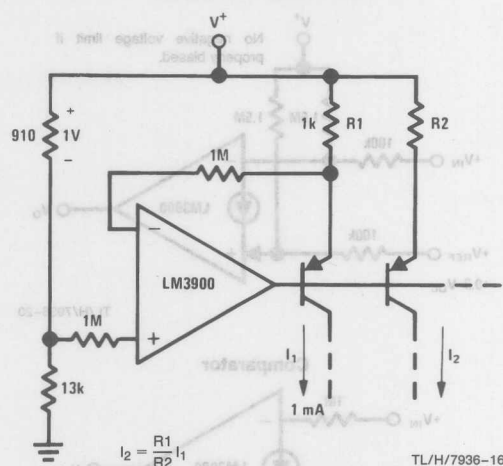
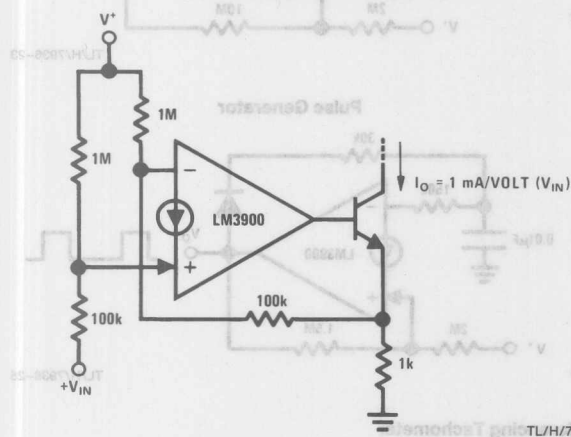
TL/H/7936-14

Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

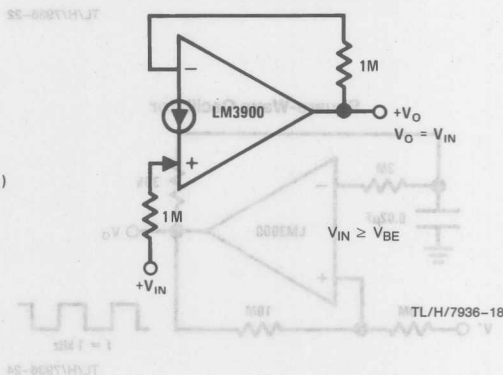
Voltage Regulator



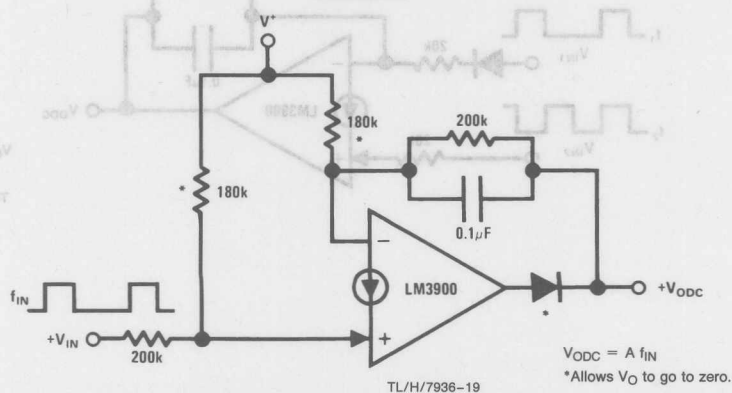
Fixed Current Sources

Voltage-Controlled Current Sink
(Transconductance Amplifier)

Buffer Amplifier



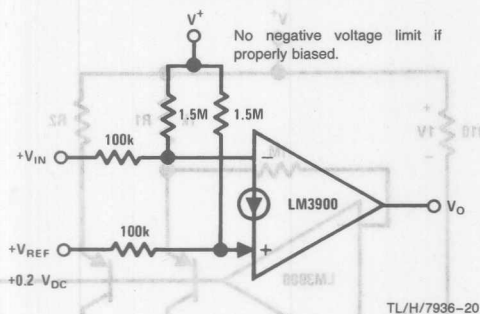
Tachometer



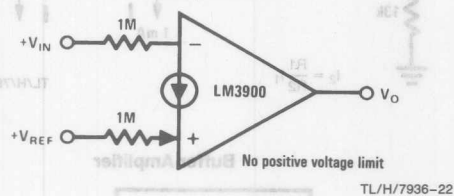
$V_{\text{ODC}} = A f_{\text{IN}}$
 *Allows V_{O} to go to zero.

Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

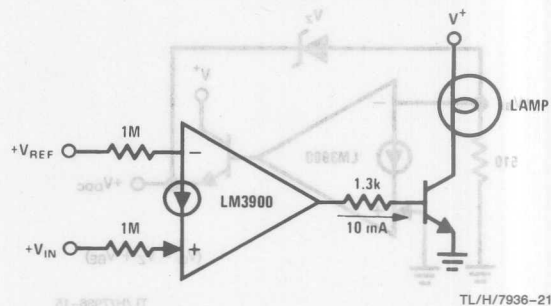
Low-Voltage Comparator



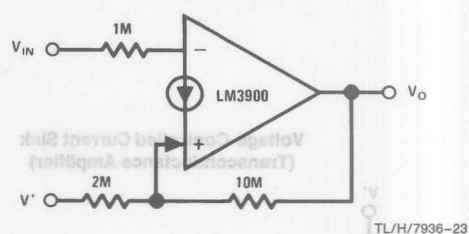
Comparator



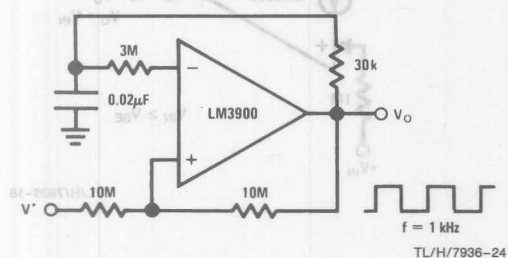
Power Comparator



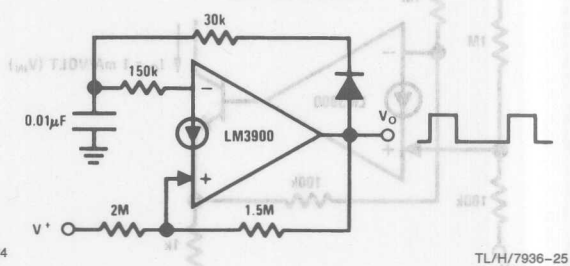
Schmitt-Trigger



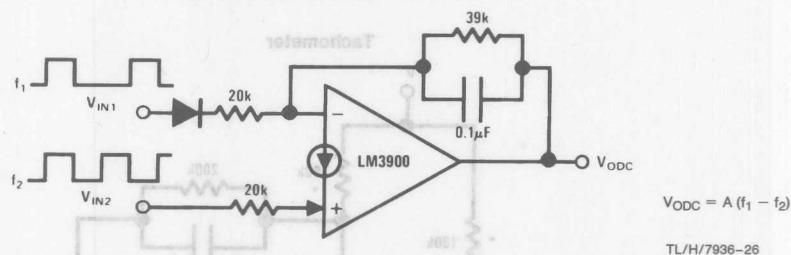
Square-Wave Oscillator



Pulse Generator

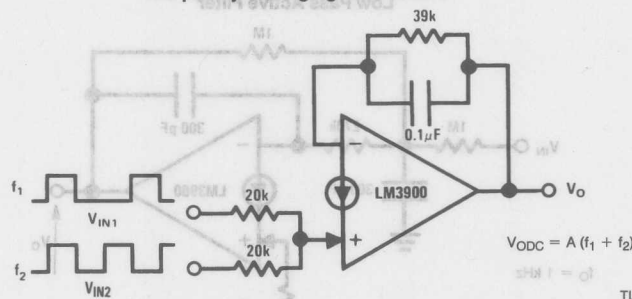


Frequency Differencing Tachometer

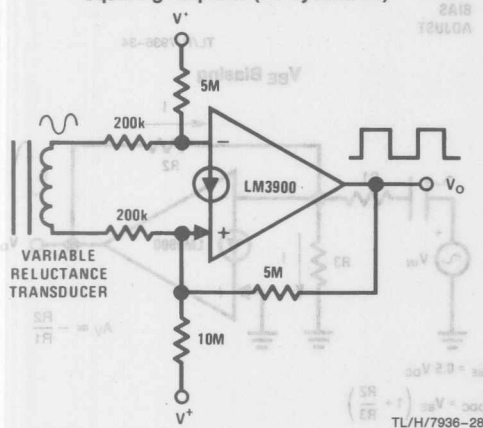


Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

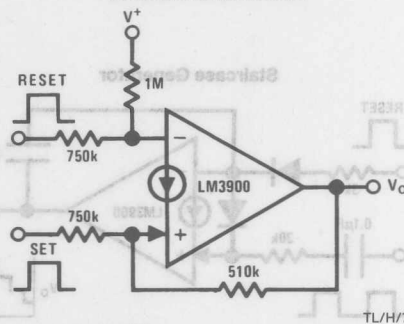
Frequency Averaging Tachometer



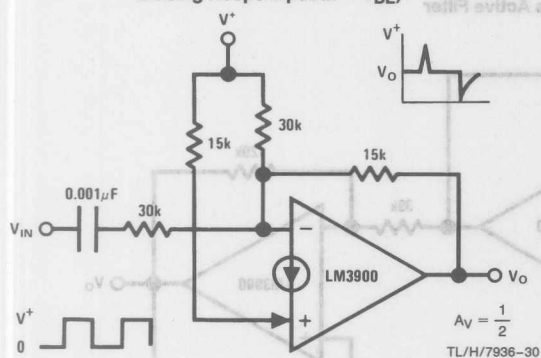
Squaring Amplifier (W/Hysteresis)



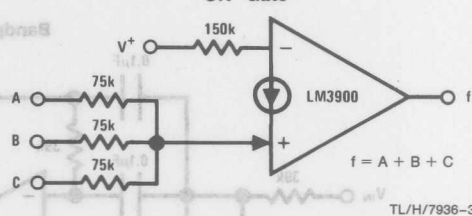
Bi-Stable Multivibrator



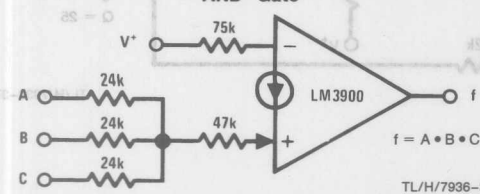
Differentiator (Common-Mode Biasing Keeps Input at V_{BE})



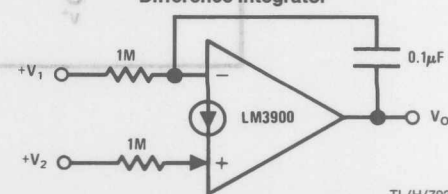
"OR" Gate



"AND" Gate

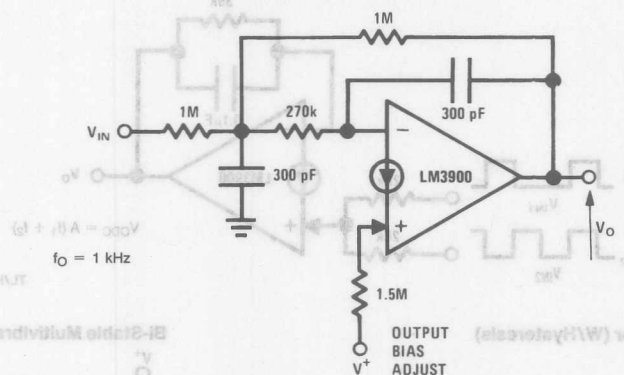


Difference Integrator



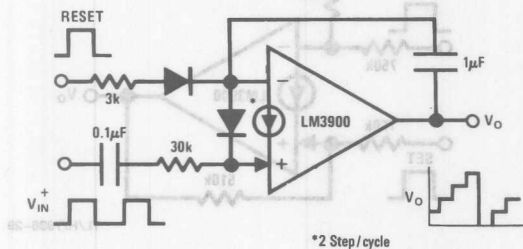
Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

Low Pass Active Filter



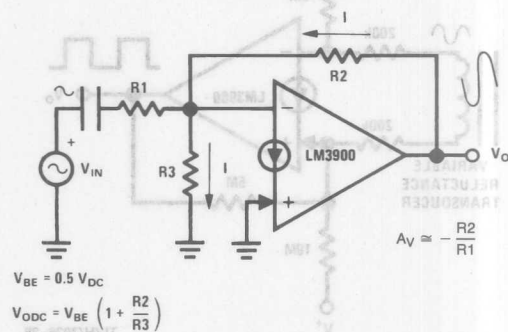
TL/H/7936-34

Staircase Generator



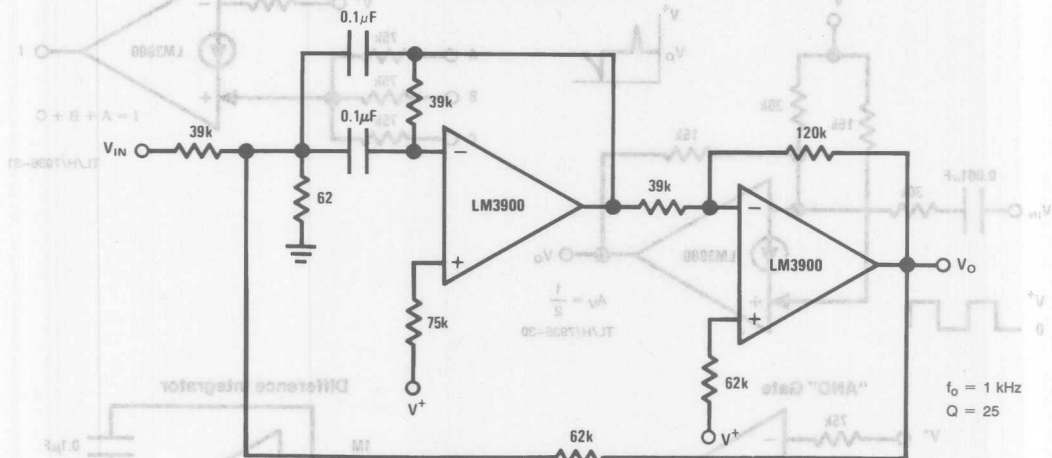
TL/H/7936-35

V_{BE} Biasing



TL/H/7936-36

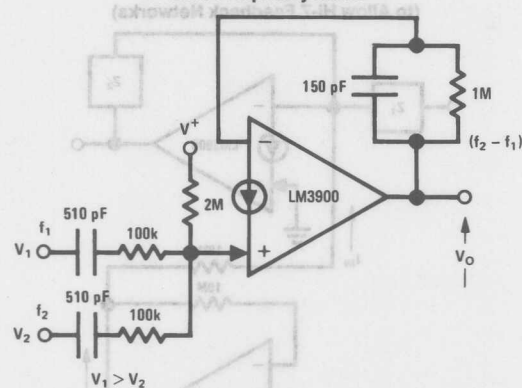
Bandpass Active Filter



TL/H/7936-37

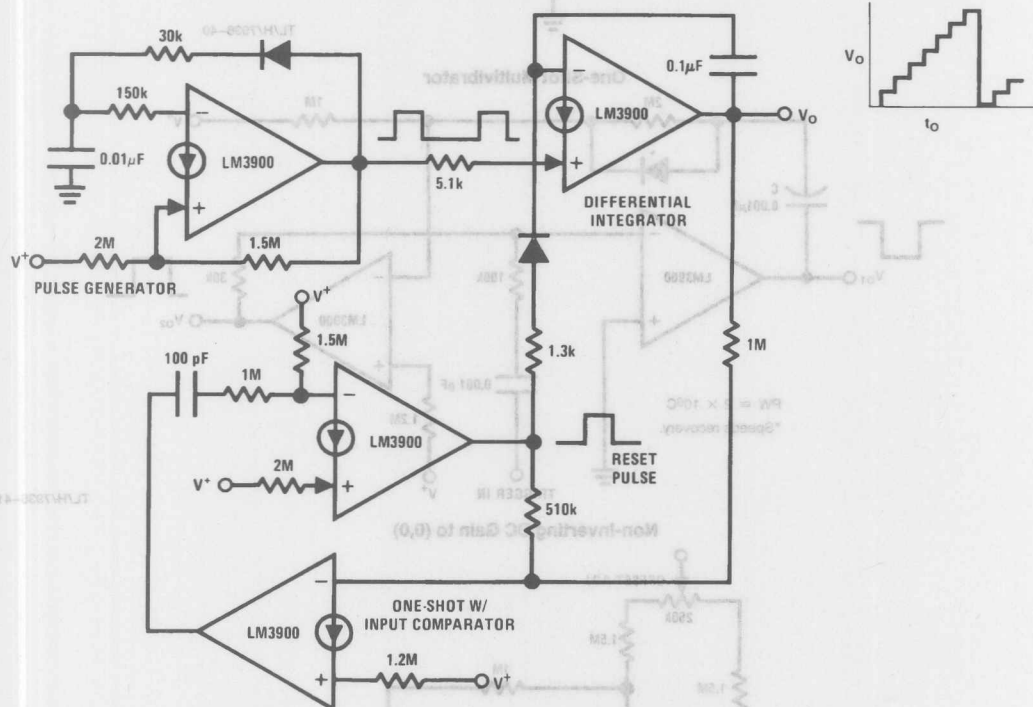
Typical Applications (V⁺ = 15 V_{DC}) (Continued)

Low-Frequency Mixer



TL/H/7936-38

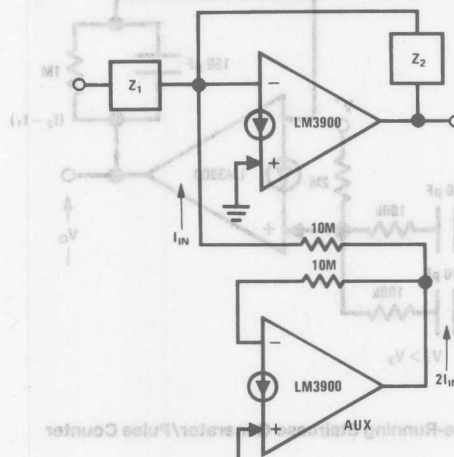
Free-Running Staircase Generator/Pulse Counter



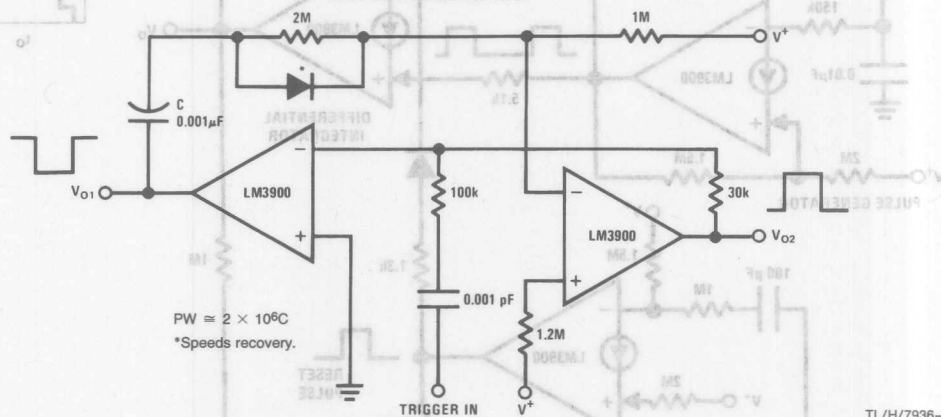
TL/H/7936-39

Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

Supplying I_{IN} with Aux. Amp (to Allow Hi-Z Feedback Networks)

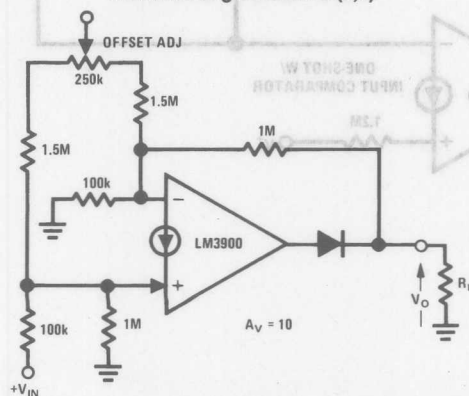


One-Shot Multivibrator



$PW \approx 2 \times 10^6 C$
*Speeds recovery.

Non-Inverting DC Gain to (0,0)

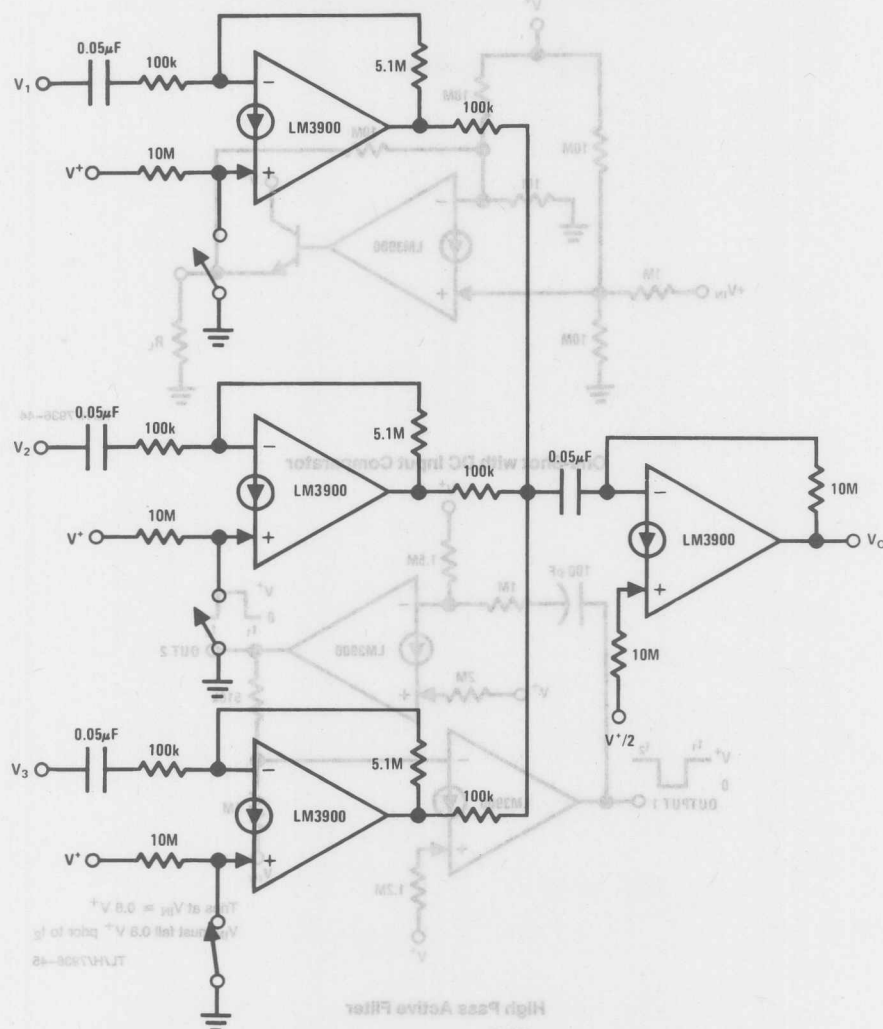


TL/H/7936-41

TL/H/7936-42

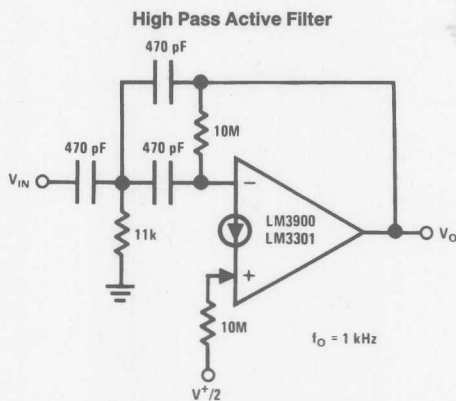
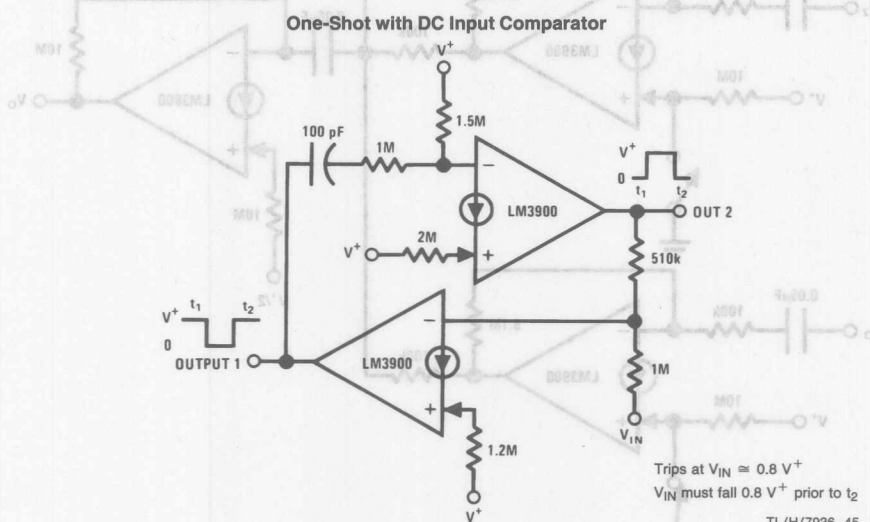
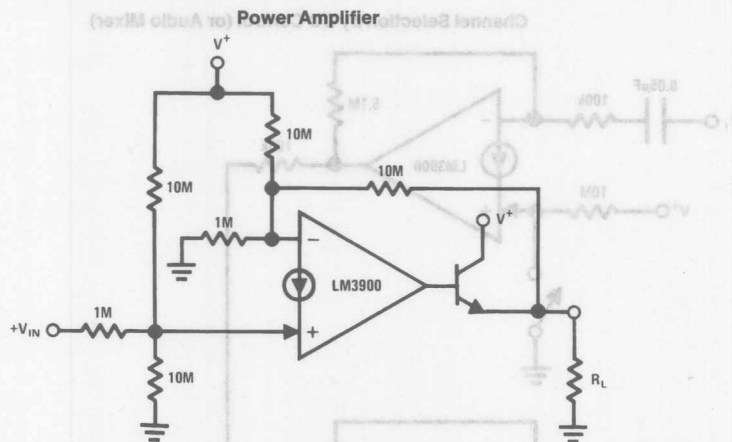
Typical Applications (V⁺ = 15 V_{DC}) (Continued)

Channel Selection by DC Control (or Audio Mixer)



TL/H/7936-43

Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)



Sample-Hold and Compare with New + V_{IN}



The diagram shows an LM3900 configured as a monostable multivibrator. The RESET input is connected to a 3k resistor, which is in series with a diode. The other end of the diode is connected to the inverting input of the LM3900. A 100k resistor connects the non-inverting input to the positive supply voltage V^+ . The output of the LM3900 is connected to a 1μF capacitor, which is also connected to the output V_O . The output waveform is shown as a single pulse. The input waveform is a square wave labeled RESET.

TL/H/7936-48

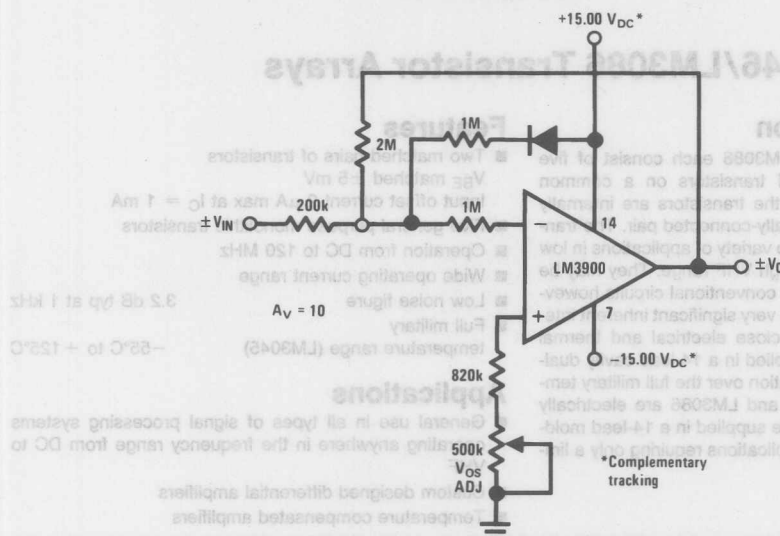
Phase-Locked Loop



$V^+ (15V_{DC})$

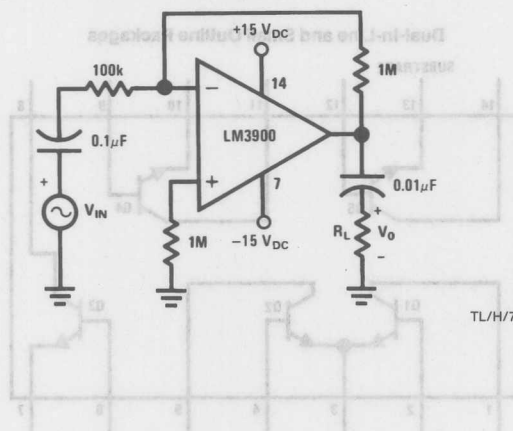


Non-Inverting DC Gain



TL/H/7936-51

AC Amplifier



TL/H/7936-52



LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

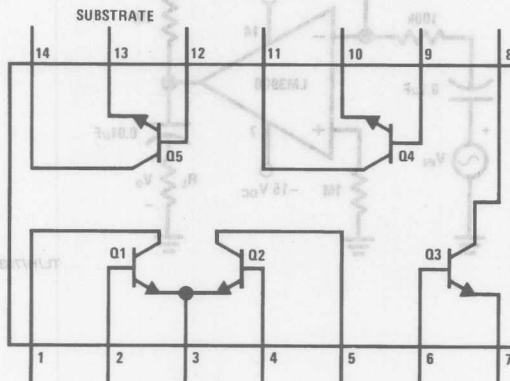
- Two matched pairs of transistors
 V_{BE} matched ± 5 mV
 Input offset current $2 \mu\text{A}$ max at $I_C = 1 \text{ mA}$
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz
- Full military temperature range (LM3045) -55°C to $+125^\circ\text{C}$

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram

Dual-In-Line and Small Outline Packages



Top View

Order Number LM3045J, LM3046M, LM3046N or LM3086N
 See NS Package Number J14A, M14A or N14A

TL/H/7950-1

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/
Distributors for availability and specifications.

| | LM3045 | | LM3046/LM3086 | | Units |
|--|--|---------------|---|---------------|----------------------|
| | Each Transistor | Total Package | Each Transistor | Total Package | |
| Power Dissipation: | | | | | |
| $T_A = 25^\circ\text{C}$ | 300 | 750 | 300 | 750 | mW |
| $T_A = 25^\circ\text{C to } 55^\circ\text{C}$ | | | 300 | 750 | mW |
| $T_A > 55^\circ\text{C}$ | | | Derate at 6.67 | | mW/ $^\circ\text{C}$ |
| $T_A = 25^\circ\text{C to } 75^\circ\text{C}$ | 300 | 750 | | | mW |
| $T_A > 75^\circ\text{C}$ | Derate at 8 | | | | mW/ $^\circ\text{C}$ |
| Collector to Emitter Voltage, V_{CEO} | 15 | | 15 | | V |
| Collector to Base Voltage, V_{CBO} | 20 | | 20 | | V |
| Collector to Substrate Voltage, V_{CIO} (Note 1) | 20 | | 20 | | V |
| Emitter to Base Voltage, V_{EBO} | 5 | | 5 | | V |
| Collector Current, I_C | 50 | | 50 | | mA |
| Operating Temperature Range | $-55^\circ\text{C to } +125^\circ\text{C}$ | | $-40^\circ\text{C to } +85^\circ\text{C}$ | | |
| Storage Temperature Range | $-65^\circ\text{C to } +150^\circ\text{C}$ | | $-65^\circ\text{C to } +85^\circ\text{C}$ | | |
| Soldering Information | | | | | |
| Dual-In-Line Package Soldering (10 Sec.) | 260 $^\circ\text{C}$ | | 260 $^\circ\text{C}$ | | |
| Small Outline Package | | | | | |
| Vapor Phase (60 Seconds) | | | 215 $^\circ\text{C}$ | | |
| Infrared (15 Seconds) | | | 220 $^\circ\text{C}$ | | |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Conditions | Limits | | | Limits | | | Units |
|--|--|----------------|-------|-----|--------|-------|-----|--------------------------------|
| | | LM3045, LM3046 | | | LM3086 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Collector to Base Breakdown Voltage ($V_{(BR)CBO}$) | $I_C = 10\text{ }\mu\text{A}, I_E = 0$ | 20 | 60 | | 20 | 60 | | V |
| Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$) | $I_C = 1\text{ mA}, I_B = 0$ | 15 | 24 | | 15 | 24 | | V |
| Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$) | $I_C = 10\text{ }\mu\text{A}, I_{CI} = 0$ | 20 | 60 | | 20 | 60 | | V |
| Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$) | $I_E 10\text{ }\mu\text{A}, I_C = 0$ | 5 | 7 | | 5 | 7 | | V |
| Collector Cutoff Current (I_{CBO}) | $V_{CB} = 10\text{V}, I_E = 0$ | | 0.002 | 40 | | 0.002 | 100 | nA |
| Collector Cutoff Current (I_{CEO}) | $V_{CE} = 10\text{V}, I_B = 0$ | | | 0.5 | | | 5 | μA |
| Static Forward Current Transfer Ratio (Static Beta) (h_{FE}) | $V_{CE} = 3\text{V}$ $\begin{cases} I_C = 10\text{ mA} \\ I_C = 1\text{ mA} \\ I_C = 10\text{ }\mu\text{A} \end{cases}$ | | 100 | | | 100 | | |
| | | 40 | 100 | | 40 | 100 | | |
| | | | 54 | | | 54 | | |
| Input Offset Current for Matched Pair Q_1 and Q_2 $ I_{O1} - I_{O2} $ | $V_{CE} = 3\text{V}, I_C = 1\text{ mA}$ | | 0.3 | 2 | | | | μA |
| Base to Emitter Voltage (V_{BE}) | $V_{CE} = 3\text{V}$ $\begin{cases} I_E = 1\text{ mA} \\ I_E = 10\text{ mA} \end{cases}$ | | 0.715 | | | 0.715 | | V |
| | | | 0.800 | | | 0.800 | | |
| Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $ | $V_{CE} = 3\text{V}, I_C = 1\text{ mA}$ | 0.45 | 5 | | | | | mV |
| Magnitude of Input Offset Voltage for Isolated Transistors $ V_{BE3} - V_{BE4} , V_{BE4} - V_{BE5} , V_{BE5} - V_{BE3} $ | $V_{CE} = 3\text{V}, I_C = 1\text{ mA}$ | 0.45 | 5 | | | | | mV |
| Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$ | $V_{CE} = 3\text{V}, I_C = 1\text{ mA}$ | | -1.9 | | | -1.9 | | mV/ $^{\circ}\text{C}$ |
| Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$) | $I_B = 1\text{ mA}, I_C = 10\text{ mA}$ | | 0.23 | | | 0.23 | | V |
| Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{IO}}{\Delta T}\right)$ | $V_{CE} = 3\text{V}, I_C = 1\text{ mA}$ | | 1.1 | | | | | $\mu\text{V}/^{\circ}\text{C}$ |

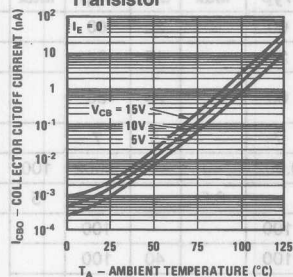
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

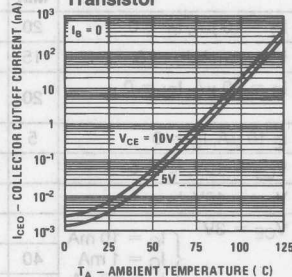
| Parameter | Conditions | Min | Typ | Max | Units |
|---|--|-----|----------------------------------|-----|------------------|
| Low Frequency Noise Figure (NF) | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V},$ $I_C = 100 \mu\text{A}, R_S = 1 \text{ k}\Omega$ | | 3.25 | | dB |
| LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS | | | | | |
| Forward Current Transfer Ratio (h_{fe}) | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V},$ $I_C = 1 \text{ mA}$ | | 110 (LM3045, LM3046) (LM3086) | | |
| Short Circuit Input Impedance (h_{ie}) | | | 3.5 | | $\text{k}\Omega$ |
| Open Circuit Output Impedance (h_{oe}) | | | 15.6 | | μmho |
| Open Circuit Reverse Voltage Transfer Ratio (h_{re}) | | | 1.8×10^{-4} | | |
| ADMITTANCE CHARACTERISTICS | | | | | |
| Forward Transfer Admittance (Y_{fe}) | $f = 1 \text{ MHz}, V_{CE} = 3 \text{ V},$ $I_C = 1 \text{ mA}$ | | $31 - j 1.5$ | | |
| Input Admittance (Y_{ie}) | | | $0.3 + j 0.04$ | | |
| Output Admittance (Y_{oe}) | | | $0.001 + j 0.03$ | | |
| Reverse Transfer Admittance (Y_{re}) | | | See Curve | | |
| Gain Bandwidth Product (f_T) | $V_{CE} = 3 \text{ V}, I_C = 3 \text{ mA}$ | 300 | 550 | | |
| Emitter to Base Capacitance (C_{EB}) | $V_{EB} = 3 \text{ V}, I_E = 0$ | | 0.6 | | pF |
| Collector to Base Capacitance (C_{CB}) | $V_{CB} = 3 \text{ V}, I_C = 0$ | | 0.58 | | pF |
| Collector to Substrate Capacitance (C_{Ci}) | $V_{CS} = 3 \text{ V}, I_C = 0$ | | 2.8 | | pF |

Typical Performance Characteristics

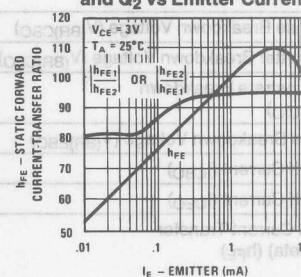
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor

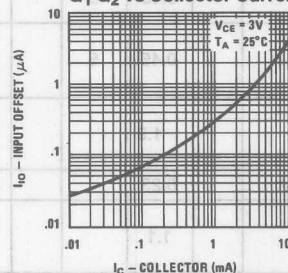


Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q₁ and Q₂ vs Emitter Current

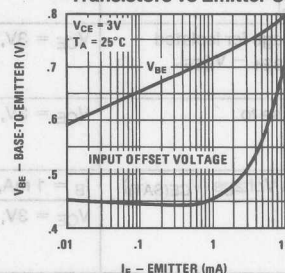


TL/H/7950-2

Typical Input Offset Current for Matched Transistor Pair Q₁ Q₂ vs Collector Current



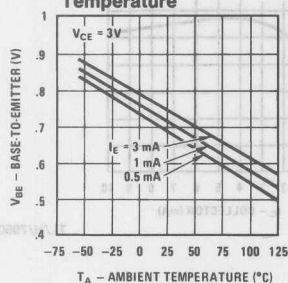
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



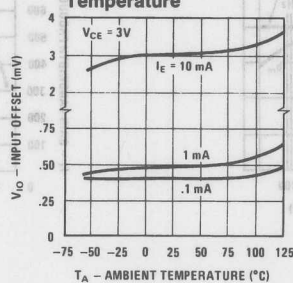
TL/H/7950-3

Typical Performance Characteristics (Continued)

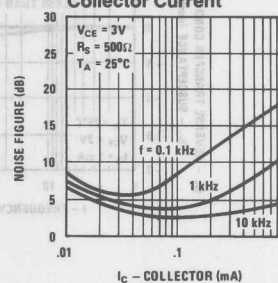
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

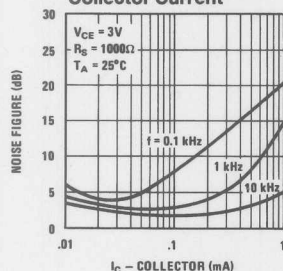


Typical Noise Figure vs Collector Current

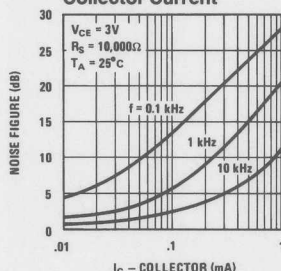


TL/H/7950-4

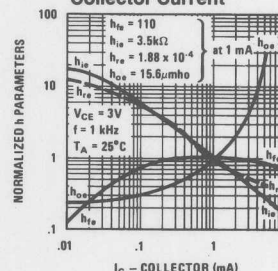
Typical Noise Figure vs Collector Current



Typical Noise Figure vs Collector Current

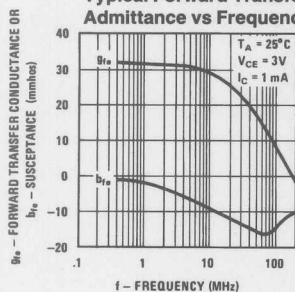


Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

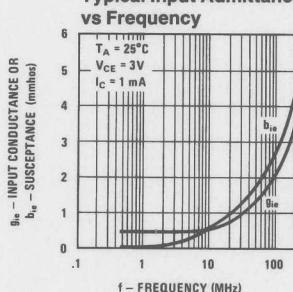


TL/H/7950-5

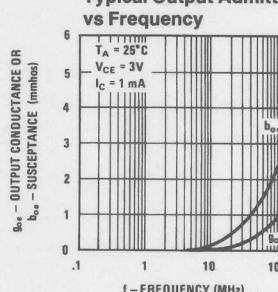
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency



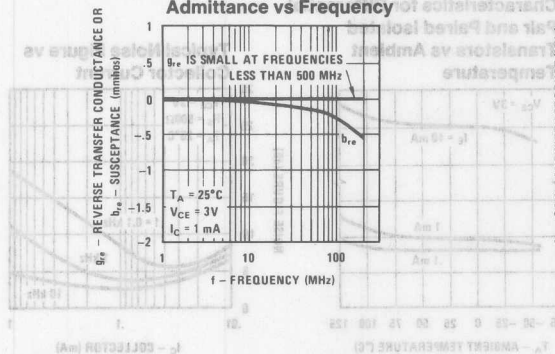
Typical Output Admittance vs Frequency



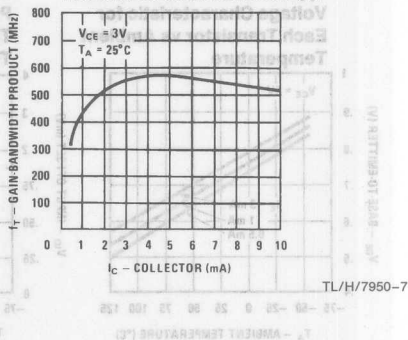
TL/H/7950-6

Typical Performance Characteristics (Continued)

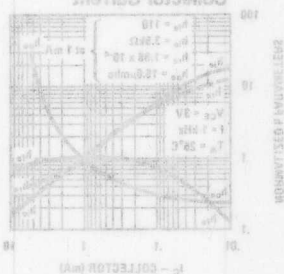
Typical Reverse Transfer Admittance vs Frequency



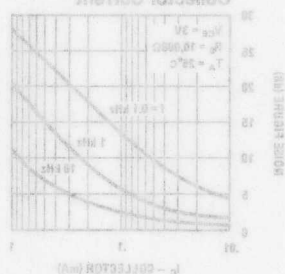
Typical Gain-Bandwidth Product vs Collector Current



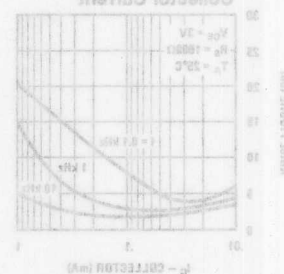
Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



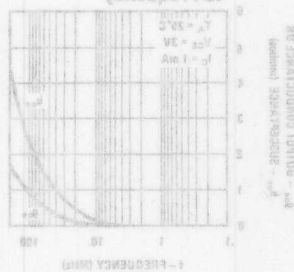
Typical Noise Figure vs Collector Current



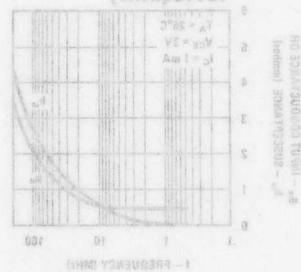
Typical Noise Figure vs Collector Current



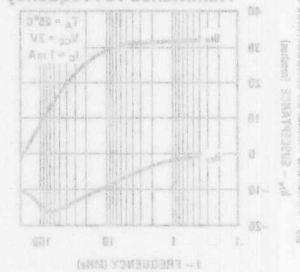
Typical Output Admittance vs Frequency



Typical Input Admittance vs Frequency



Typical Forward Transfer Admittance vs Frequency



LM3080

Operational Transconductance Amplifier

General Description

The LM3080 is a programmable transconductance block intended to fulfill a wide variety of variable gain applications. The LM3080 has differential inputs and high impedance push-pull outputs. The device has high input impedance and its transconductance (g_m) is directly proportional to the amplifier bias current (I_{ABC}).

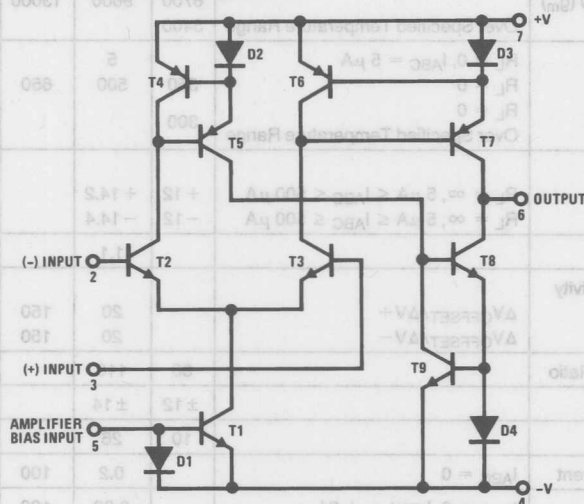
High slew rate together with programmable gain make the LM3080 an ideal choice for variable gain applications such as sample and hold, multiplexing, filtering, and multiplying.

The LM3080N and LM3080AN are guaranteed from 0°C to +70°C.

Features

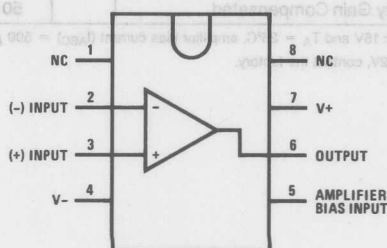
- Slew rate (unity gain compensated): 50 V/ μ s
- Fully adjustable gain: 0 to $g_m \cdot R_L$ limit
- Extended g_m linearity: 3 decades
- Flexible supply voltage range: $\pm 2V$ to $\pm 18V$
- Adjustable power consumption

Schematic and Connection Diagrams



TL/H/7148-1

Dual-In-Line Package



Top View

TL/H/7148-2

Order Number LM3080AN, LM3080M or LM3080N
See NS Package Number M08A or N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 2)

LM3080

LM3080A

Power Dissipation

Differential Input Voltage

 $\pm 18\text{V}$ $\pm 22\text{V}$

250 mW

 $\pm 5V$ Amplifier Bias Current (I_{ABC})

2 mA

DC Input Voltage

 $+V_S$ to $-V_S$

Output Short Circuit Duration

Indefinite

Operating Temperature Range

LM3080N or LM3080AN

0°C to +70°C

Storage Temperature Range

—65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

260°C

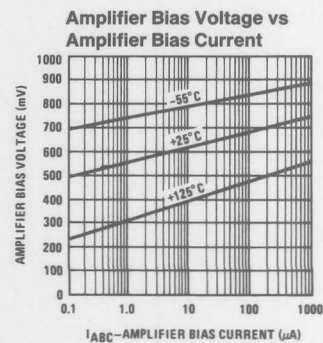
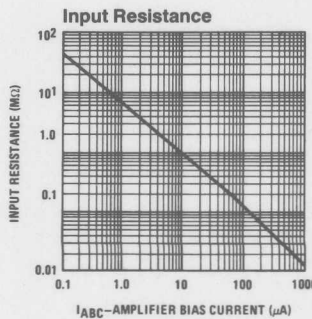
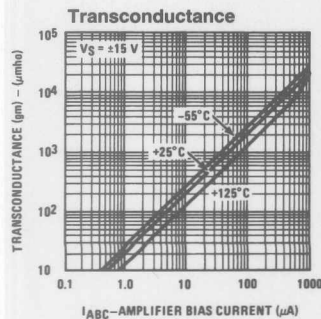
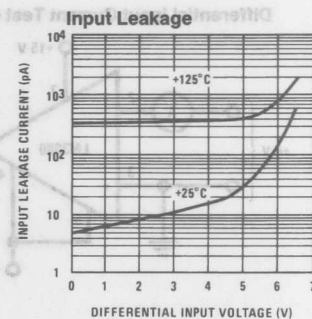
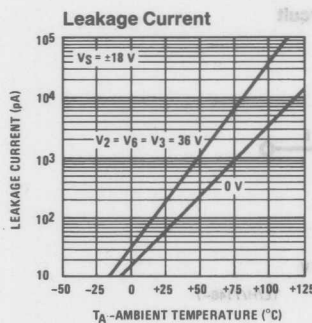
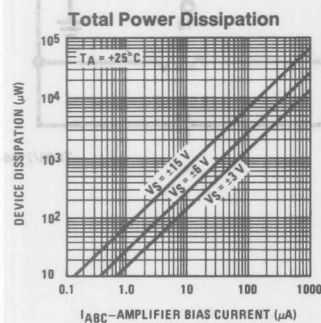
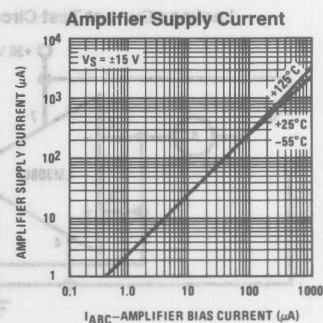
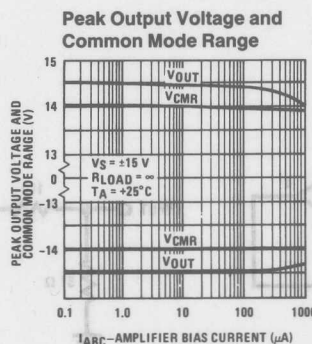
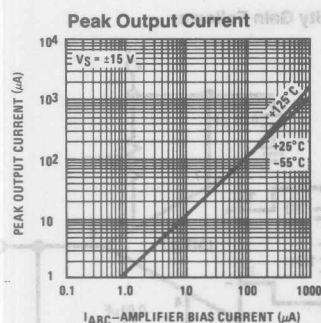
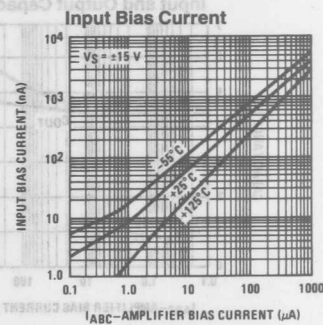
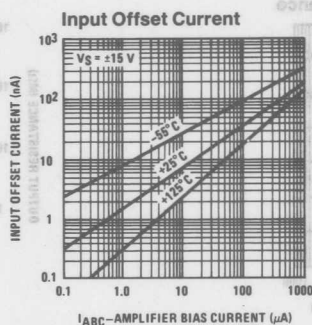
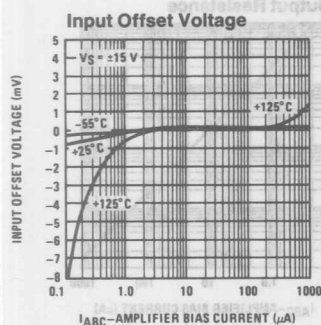
Electrical Characteristics (Note 1)

| Parameter | Conditions | LM3080 | | | LM3080A | | | Units |
|------------------------------------|--|----------|----------|-------|----------|----------|-------|------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | Over Specified Temperature Range $I_{ABC} = 5 \mu A$ | | 0.4 | 5 | 0.4 | 2 | 5 | mV |
| | | | | 6 | | 5 | | mV |
| | | | 0.3 | | 0.3 | 2 | | mV |
| Input Offset Voltage Change | $5 \mu A \leq I_{ABC} \leq 500 \mu A$ | | 0.1 | | 0.1 | 3 | | mV |
| Input Offset Current | | | 0.1 | 0.6 | 0.1 | 0.6 | | μA |
| Input Bias Current | Over Specified Temperature Range | | 0.4 | 5 | 0.4 | 5 | | μA |
| | | | 1 | 7 | 1 | 8 | | μA |
| Forward Transconductance (g_m) | Over Specified Temperature Range | 6700 | 9600 | 13000 | 7700 | 9600 | 12000 | μmho |
| | | 5400 | | | 4000 | | | μmho |
| Peak Output Current | $R_L = 0, I_{ABC} = 5 \mu A$ | | 5 | | 3 | 5 | 7 | μA |
| | $R_L = 0$ | 350 | 500 | 650 | 350 | 500 | 650 | μA |
| | $R_L = 0$ | 300 | | | 300 | | | μA |
| | Over Specified Temperature Range | | | | | | | μA |
| Peak Output Voltage | $R_L = \infty, 5 \mu A \leq I_{ABC} \leq 500 \mu A$ $R_L = \infty, 5 \mu A \leq I_{ABC} \leq 500 \mu A$ | +12 | +14.2 | | +12 | +14.2 | | V |
| | | -12 | -14.4 | | -12 | -14.4 | | V |
| Amplifier Supply Current | | | 1.1 | | 1.1 | | | mA |
| Input Offset Voltage Sensitivity | $\Delta V_{OFFSET} / \Delta V +$ $\Delta V_{OFFSET} / \Delta V -$ | | 20 | 150 | 20 | 150 | | $\mu V/V$ |
| | | | 20 | 150 | 20 | 150 | | $\mu V/V$ |
| Common Mode Rejection Ratio | | 80 | 110 | | 80 | 110 | | dB |
| Common Mode Range | | ± 12 | ± 14 | | ± 12 | ± 14 | | V |
| Input Resistance | | 10 | 26 | | 10 | 26 | | k Ω |
| Magnitude of Leakage Current | $I_{ABC} = 0$ | | 0.2 | 100 | 0.2 | 5 | | nA |
| Differential Input Current | $I_{ABC} = 0, Input = \pm 4V$ | | 0.02 | 100 | 0.02 | 5 | | nA |
| Open Loop Bandwidth | | | 2 | | 2 | | | MHz |
| Slew Rate | Unity Gain Compensated | | 50 | | 50 | | | V/ μs |

Note 1: These specifications apply for $V_S = \pm 15V$ and $T_A = 25^\circ C$, amplifier bias current (I_{ABC}) = 500 μA , unless otherwise specified.

Note 2: Selection to supply voltage above $\pm 22V$, contact the factory.

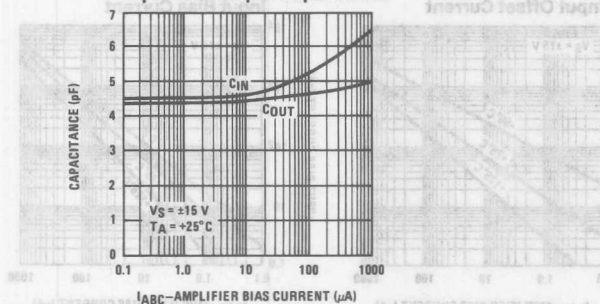
Typical Performance Characteristics



TL/H/7148-3

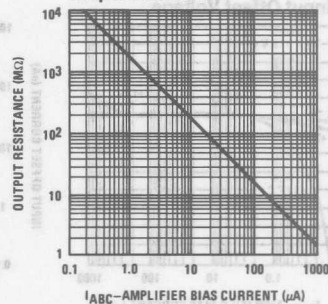
Typical Performance Characteristics (Continued)

Input and Output Capacitance



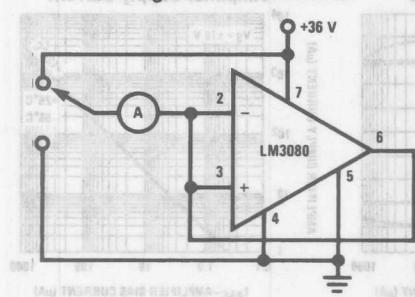
TL/H/7148-4

Output Resistance



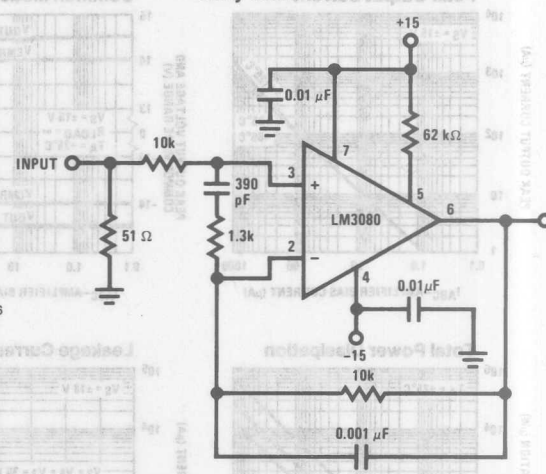
TL/H/7148-5

Leakage Current Test Circuit



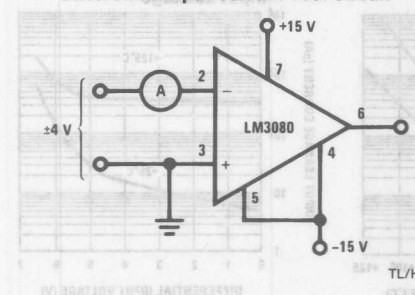
TL/H/7148-6

Unity Gain Follower



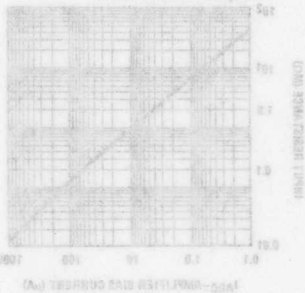
TL/H/7148-8

Differential Input Current Test Circuit



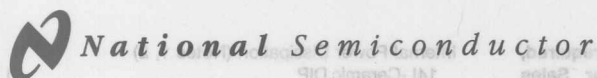
TL/H/7148-7

Input Resistance



Transconductance





LM3303/LM3403 Quad Operational Amplifiers

General Description

The LM3303 and LM3403 are monolithic quad operational amplifiers consisting of four independent high gain, internally frequency compensated, operational amplifiers designed to operate from a single power supply or dual power supplies over a wide range of voltages. The common mode input range includes the negative supply, thereby eliminating the necessity for external biasing components in many applications.

Features

- Input common mode voltage range includes ground or negative supply
- Output voltage can swing to ground or negative supply

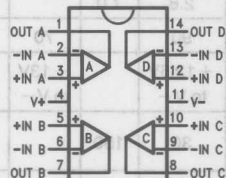
- Four internally compensated operational amplifiers in a single package
- Wide power supply range: single supply of 3.0V to 36V, dual supply of $\pm 1.5V$ to $\pm 18V$
- Class AB output stage for minimal crossover distortion
- Short circuit protected outputs
- High open loop gain 200k
- LM741 operational amplifier type performance

Applications

- Filters
- Voltage controlled oscillators

Connection Diagram

14-Lead DIP and SO-14 Package



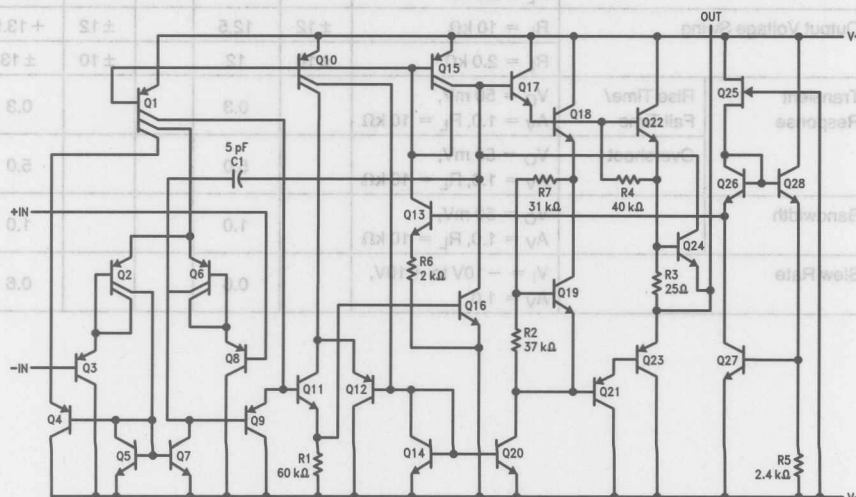
Top View

TL/H/10064-1

Order Information

| Device Code | Package Code | Package Description |
|-------------|--------------|----------------------|
| LM3303J | J14A | Ceramic DIP |
| LM3303N | N14A | Molded DIP |
| LM3303M | M14A | Molded Surface Mount |
| LM3403J | J14A | Ceramic DIP |
| LM3403N | N14A | Molded DIP |
| LM3403M | M14A | Molded Surface Mount |

Equivalent Circuit (1/4 of Circuit)



TL/H/10064-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature Range

| | |
|----------------------|-----------------|
| Ceramic DIP | -65°C to +175°C |
| Molded DIP and SO-14 | -65°C to +150°C |

Operating Temperature Range

| | |
|---------------------|----------------|
| Industrial (LM3303) | -40°C to +85°C |
| Commercial (LM3403) | 0°C to +70°C |

Lead Temperature

| | |
|---|-------|
| Ceramic DIP (Soldering, 60 sec.) | 300°C |
| Molded DIP and SO-14 (Soldering, 10 sec.) | 265°C |

Internal Power Dissipation (Notes 1, 2)

| | |
|-----------------|-------|
| 14L-Ceramic DIP | 1.36W |
| 14L-Molded DIP | 1.04W |
| SO-14 | 0.93W |

Supply Voltage between V+ and V- 36V

Differential Input Voltage (Note 3) ±30V

Input Voltage (V-) - 0.3V to V+

ESD Tolerance (To Be Determined)

LM3303 and LM3403

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise specified

| Symbol | Parameter | Conditions | LM3303 | | | LM3403 | | | Units |
|----------|---|--|------------|--------------|-----|------------|--------------|-----|------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{IO} | Input Offset Voltage | | | 2.0 | 8.0 | | 2.0 | 8.0 | mV |
| I_{IO} | Input Offset Current | | | 30 | 75 | | 30 | 50 | nA |
| I_{IB} | Input Bias Current | | | 200 | 500 | | 200 | 500 | nA |
| Z_i | Input Impedance | | 0.3 | 1.0 | | 0.3 | 1.0 | | M Ω |
| I_{CC} | Supply Current | $V_O = 0\text{V}$, $R_L = \infty$ | | 2.8 | 7.0 | | 2.8 | 7.0 | mA |
| CMR | Common Mode Rejection | $R_S \leq 10\text{ k}\Omega$ | 70 | 90 | | 70 | 90 | | dB |
| V_{IR} | Input Voltage Range | | +12V to V- | +12.5V to V- | | +13V to V- | +13.5V to V- | | V |
| PSRR | Power Supply Rejection Ratio | | | 30 | 150 | | 30 | 150 | $\mu\text{V/V}$ |
| I_{OS} | Output Short Circuit Current (Per Amplifier) (Note 4) | | ±10 | ±30 | ±45 | ±10 | ±30 | ±45 | mA |
| A_{VS} | Large Signal Voltage Gain | $V_O = \pm 10\text{V}$, $R_L \geq 2.0\text{ k}\Omega$ | 20 | 200 | | 20 | 200 | | V/mV |
| V_{OP} | Output Voltage Swing | $R_L = 10\text{ k}\Omega$ | ±12 | 12.5 | | ±12 | +13.5 | | V |
| | | $R_L = 2.0\text{ k}\Omega$ | ±10 | 12 | | ±10 | ±13 | | |
| TR | Transient Response | Rise Time/ Fall Time $V_O = 50\text{ mV}$, $A_V = 1.0$, $R_L = 10\text{ k}\Omega$ | | 0.3 | | | 0.3 | | μs |
| | | Overshoot $V_O = 50\text{ mV}$, $A_V = 1.0$, $R_L = 10\text{ k}\Omega$ | | 5.0 | | | 5.0 | | % |
| BW | Bandwidth | $V_O = 50\text{ mV}$, $A_V = 1.0$, $R_L = 10\text{ k}\Omega$ | | 1.0 | | | 1.0 | | MHz |
| SR | Slew Rate | $V_I = -10\text{V}$ to $+10\text{V}$, $A_V = 1.0$ | | 0.6 | | | 0.6 | | V/ μs |

LM3303 and LM3403 (Continued)Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 15\text{V}$, unless otherwise specifiedThe following specifications apply for $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for the LM3303, and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for the LM3403

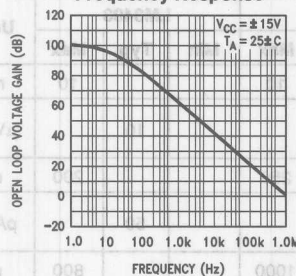
| Symbol | Parameter | Conditions | LM3303 | | | LM3403 | | | Units |
|--------------------------|--|---|----------|-----|------|----------|-----|-----|------------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{IO} | Input Offset Voltage | | | | 10 | | | 10 | mV |
| $\Delta V_{IO}/\Delta T$ | Input Offset Voltage Temperature Sensitivity | | | 10 | | | 10 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{IO} | Input Offset Current | | | | 250 | | | 200 | nA |
| $\Delta I_{IO}/\Delta T$ | Input Offset Current Temperature Sensitivity | | | 50 | | | 50 | | $\text{pA}/^\circ\text{C}$ |
| I_{IB} | Input Bias Current | | | | 1000 | | | 800 | nA |
| A_{VS} | Large Signal Voltage Gain | $V_O = \pm 10\text{V}$, $R_L \geq 2.0\text{ k}\Omega$ | 15 | | | 15 | | | V/mV |
| V_{OP} | Output Voltage Swing | $R_L = 2.0\text{ k}\Omega$ | ± 10 | | | ± 10 | | | V |

LM3303 and LM3403Electrical Characteristics $T_A = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$, $V^- = \text{GND}$, unless otherwise specified

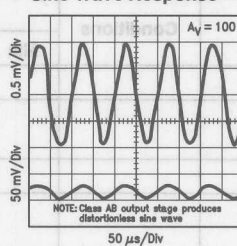
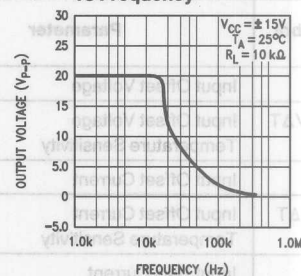
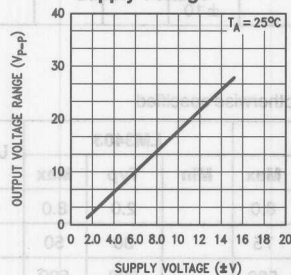
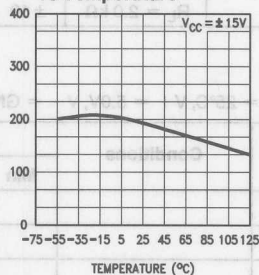
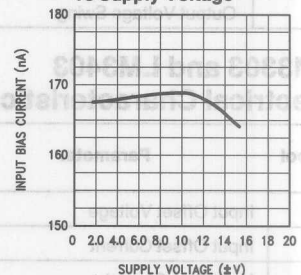
| Symbol | Parameter | Conditions | LM3303 | | | LM3403 | | | Units |
|----------|-------------------------------|---|--------------|------|-----|--------------|------|-----|------------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{IO} | Input Offset Voltage | | | | 8.0 | | 2.0 | 8.0 | mV |
| I_{IO} | Input Offset Current | | | | 75 | | 30 | 50 | nA |
| I_{IB} | Input Bias Current | | | | 500 | | 200 | 500 | nA |
| I_{CC} | Supply Current | | | 2.5 | 7.0 | | 2.5 | 7.0 | mA |
| PSRR | Power Supply Rejection Ratio | | | | 150 | | | 150 | $\mu\text{V}/\text{V}$ |
| A_{VS} | Large Signal Voltage Gain | $R_L \geq 2.0\text{ k}\Omega$ | 20 | 200 | | 20 | 200 | | V/mV |
| V_{OP} | Output Voltage Swing (Note 5) | $R_L = 10\text{ k}\Omega$ | 3.3 | | | 3.3 | | | V |
| | | $5.0\text{V} \leq V^+ \leq 30\text{V}$, $R_L = 10\text{ k}\Omega$ | (V+) -2.0 | | | (V+) -2.0 | | | |
| CS | Channel Separation | $1.0\text{ Hz} \leq f \leq 20\text{ kHz}$ (Input Referenced) | | -120 | | | -120 | | dB |

Note 1: $T_{J\text{ Max}} = 150^\circ\text{C}$ for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.**Note 2:** Ratings apply to ambient temperature at 25°C . Above this temperature, derate the 14L-Ceramic DIP at $9.1\text{ mW}/^\circ\text{C}$, the 14L-Molded DIP at $8.3\text{ mW}/^\circ\text{C}$, and the SO-14 at $7.5\text{ mW}/^\circ\text{C}$.**Note 3:** For supply voltage less than 30V between V^+ and V^- , the absolute maximum input voltage is equal to the supply voltage.**Note 4:** Not to exceed maximum package power dissipation.**Note 5:** Output will swing to ground.

Typical Performance Characteristics

Open Loop
Frequency Response

Sine Wave Response

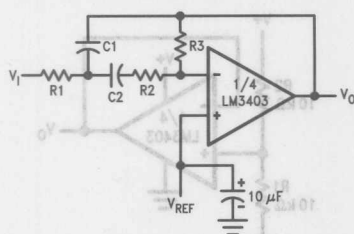
Output Voltage
vs FrequencyOutput Swing vs
Supply VoltageInput Bias Current
vs TemperatureInput Bias Current
vs Supply Voltage

TL/H/10064-3

Note 1: $T_{J, Max} = 150^\circ C$ for the Molded DIP and SO-14, and $175^\circ C$ for the Ceramic DIP.
 Note 2: Ratings apply to ambient temperature at $25^\circ C$. Above this temperature, derate the LM3303/LM3403 at 0.5 mW/ $^\circ C$ and the LM3303/LM3403 at 0.5 mW/ $^\circ C$.
 Note 3: For supply voltage less than 30V between V_+ and V_- , the absolute maximum input voltage is equal to the supply voltage.
 Note 4: Not to exceed maximum package power dissipation.
 Note 5: Output will swing to ground.

Typical Applications

Multiple Feedback Bandpass Filter



TL/H/10064-4

 f_o = center frequency

BW = Bandwidth

R in kΩ

C in μF

$$Q = \frac{f_o}{BW} < 10$$

$$C1 = C2 = \frac{Q}{3}$$

 $R1 = R2 = 1 R3 = 9Q^2 - 1$ Using scaling factors in these expressions.

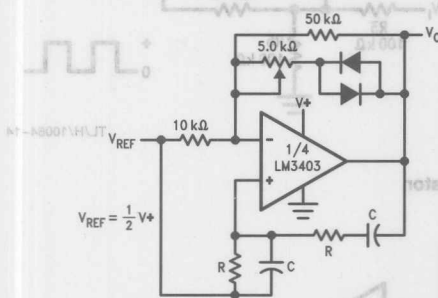
If source impedance is high or varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Design example:

given: $Q = 5$, $f_o = 1$ kHzLet $R1 = R2 = 10$ kΩthen $R3 = 9(5)^2 - 10$ $R3 = 215$ kΩ

$$C = \frac{5}{3} = 1.6 \text{ nF}$$

Wein Bridge Oscillator

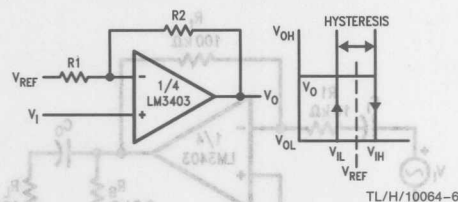


TL/H/10064-5

$$f_o = \frac{1}{2\pi RC} \text{ for } f_o = 1 \text{ kHz}$$

 $R = 16$ kΩ $C = 0.01$ μF

Comparator with Hysteresis



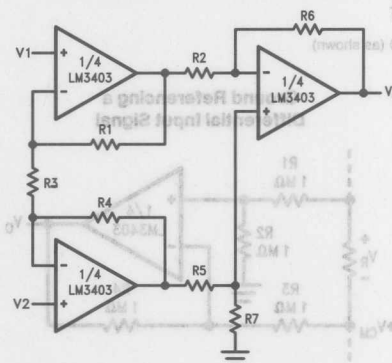
TL/H/10064-6

$$V_{IL} = \frac{R1}{R1 + R2} (V_{OL} - V_{REF}) + V_{REF}$$

$$V_{IH} = \frac{R1}{R1 + R2} (V_{OH} - V_{REF}) + V_{REF}$$

$$H = \frac{R1}{R1 + R2} (V_{OH} - V_{OL})$$

High Impedance Differential Amplifier



TL/H/10064-7

$$V_{OUT} = C(1 + a + b)(V2 - V1)$$

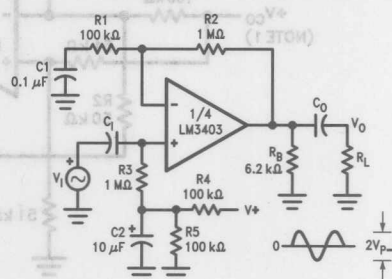
$$\frac{R2}{R5} = \frac{R6}{R7} \text{ for best CMRR}$$

$$R1 = R4$$

$$R2 = R5$$

$$\text{Gain} = \frac{R6}{R5} \left(1 + \frac{2R1}{R3} \right) = C(1 + a + b)$$

AC Coupled Non-Inverting Amplifier



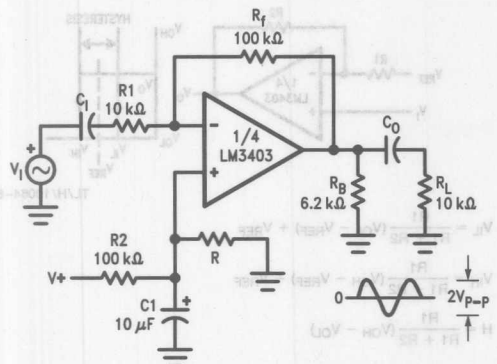
TL/H/10064-9

$$A_v = 1 + \frac{R2}{R1}$$

$$A_v = 11 \text{ (as shown)}$$

Typical Applications (Continued)

AC Coupled Inverting Amplifier

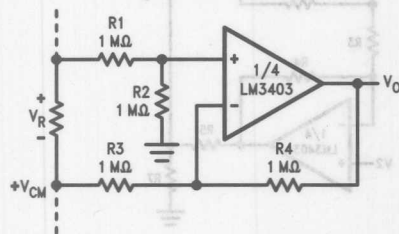


TL/H/10064-8

$$A_v = \frac{R_f}{R_1}$$

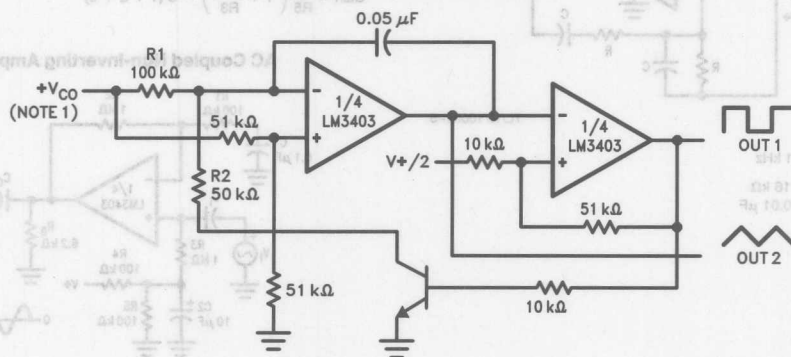
$A_v = 10$ (as shown)

Ground Referencing a Differential Input Signal



TL/H/10064-11

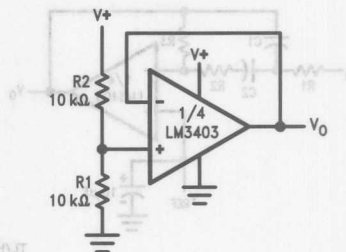
Voltage Controlled Oscillator



Note 1: Wide Control Voltage Range:
 $0V \leq V_{CO} \leq 2(V \pm 1.5V)$

TL/H/10064-12

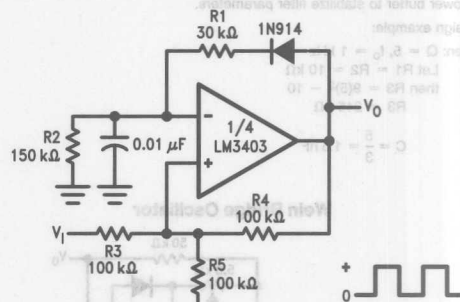
Voltage Reference



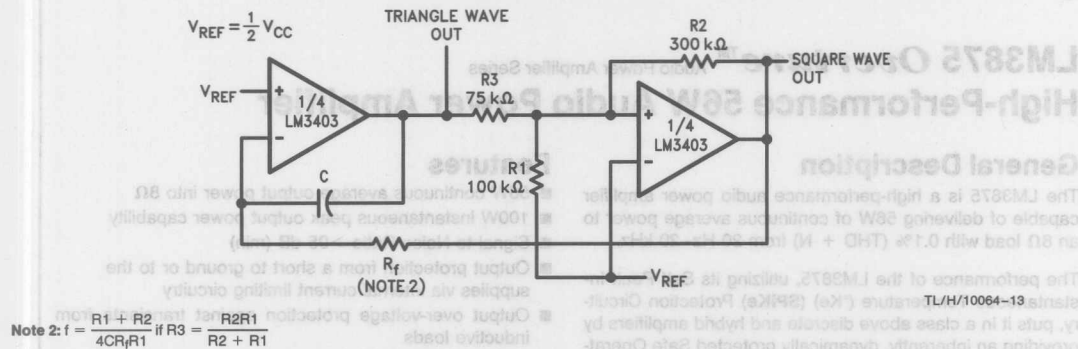
$$V_O = \frac{R_1}{R_1 + R_2} \left(= \frac{V+}{2} \text{ as shown} \right)$$

$$V_O = \frac{1}{2} V+$$

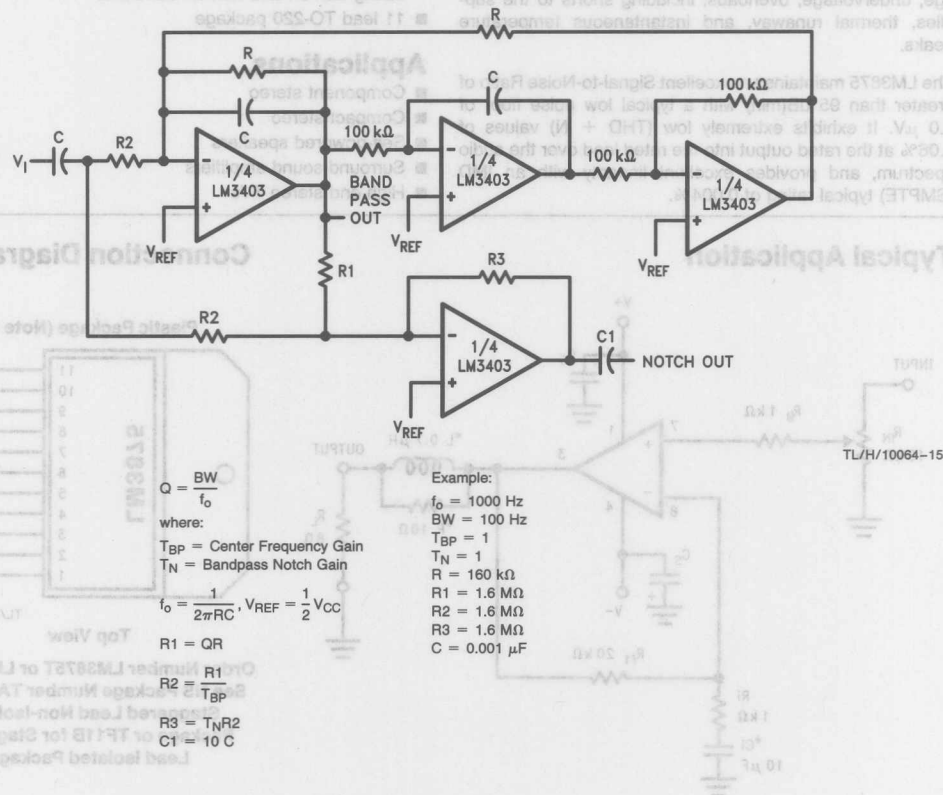
Pulse Generator



TL/H/10064-14



Bi-Quad Filter





LM3875 Overture™ Audio Power Amplifier Series

High-Performance 56W Audio Power Amplifier

General Description

The LM3875 is a high-performance audio power amplifier capable of delivering 56W of continuous average power to an 8Ω load with 0.1% (THD + N) from 20 Hz–20 kHz.

The performance of the LM3875, utilizing its Self Peak Instantaneous Temperature (°Ke) (SPIKe) Protection Circuitry, puts it in a class above discrete and hybrid amplifiers by providing an inherently, dynamically protected Safe Operating Area (SOA). SPIKe Protection means that these parts are completely safeguarded at the output against overvoltage, undervoltage, overloads, including shorts to the supplies, thermal runaway, and instantaneous temperature peaks.

The LM3875 maintains an excellent Signal-to-Noise Ratio of greater than 95 dB(min) with a typical low noise floor of 2.0 μV. It exhibits extremely low (THD + N) values of 0.06% at the rated output into the rated load over the audio spectrum, and provides excellent linearity with an IMD (SMPTE) typical rating of 0.004%.

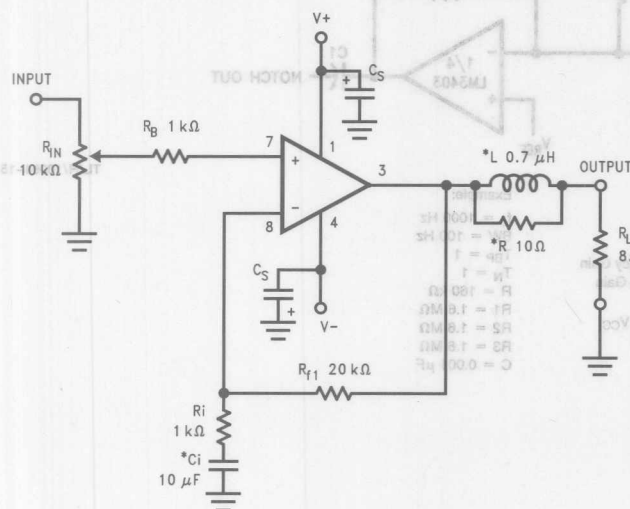
Features

- 56W continuous average output power into 8Ω
- 100W instantaneous peak output power capability
- Signal-to-Noise Ratio >95 dB (min)
- Output protection from a short to ground or to the supplies via internal current limiting circuitry
- Output over-voltage protection against transients from inductive loads
- Supply under-voltage protection, not allowing internal biasing to occur when $|V_{EE}| + |V_{CC}| \leq 12V$, thus eliminating turn-on and turn-off transients
- 11 lead TO-220 package

Applications

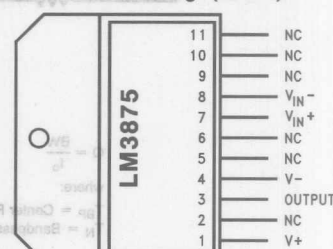
- Component stereo
- Compact stereo
- Self-powered speakers
- Surround-sound amplifiers
- High-end stereo TVs

Typical Application



Connection Diagram

Plastic Package (Note 8)



TL/H/11449-2

Top View

Order Number LM3875T or LM3875TF
See NS Package Number TA11B for
Staggered Lead Non-Isolated
Package or TF11B for Staggered
Lead Isolated Package

FIGURE 1. Typical Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $|V^+| + |V^-|$ (No Signal) 94V

Supply Voltage $|V^+| + |V^-|$ (Input Signal) 84V

Common Mode Input Voltage $(V^+ \text{ or } V^-)$ and $|V^+| + |V^-| \leq 80V$

Differential Input Voltage 60V

Output Current Internally Limited

Power Dissipation (Note 3) 125W

ESD Susceptibility (Note 4) 2500V

Junction Temperature (Note 5) 150°C

Soldering Information

T package (10 seconds) 260°C

Storage Temperature -40°C to +150°C

Thermal Resistance

θ_{JC} 1°C/W

θ_{JA} 43°C/W

Operating Ratings (Notes 1, 2)

Temperature Range

$T_{MIN} \leq T_A \leq T_{MAX}$ -20°C $\leq T_A \leq$ +85°C

Supply Voltage $|V^+| + |V^-|$ 20V to 84V

Note: Operation is guaranteed up to 84V, however, distortion may be introduced from the SPIKE Protection Circuitry when operating above 70V if proper thermal considerations are not taken into account. Refer to the Thermal Considerations section for more information. (See SPIKE Protection Response)

Electrical Characteristics (Notes 1, 2) The following specifications apply for $V^+ = +35V$, $V^- = -35V$ with $R_L = 8\Omega$ unless otherwise specified. Limits apply for $T_A = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 6) | Limit (Note 7) | Units (Limits) |
|---------------------|--------------------------------------|---|---------------------|-------------------|------------------------|
| $ V^+ + V^- $ | Power Supply Voltage | | | 20 84 | V (Min) V (Max) |
| **P _O | Output Power (Continuous Average) | THD + N = 0.1% (Max) $f = 1 \text{ kHz}$, $f = 20 \text{ kHz}$ | 56 | 40 | W (Min) |
| Peak P _O | Instantaneous Peak Output Power | | 100 | | W |
| THD + N | Total Harmonic Distortion Plus Noise | 40W, $20 \text{ Hz} \leq f \leq 20 \text{ kHz}$ $A_V = 26 \text{ dB}$ | 0.06 | | % |
| **SR | Slew Rate (Note 9) | $V_{IN} = 1.414 \text{ Vrms}$, $f = 10 \text{ kHz}$ Square-wave, $R_L = 2 \text{ k}\Omega$ | 11 | 5 | V/ μs (Min) |
| *I ₊ | Total Quiescent Power Supply Current | $V_{CM} = 0V$, $V_O = 0V$, $I_O = 0 \text{ mA}$ | 30 | 70 | mA (Max) |
| *V _{OS} | Input Offset Voltage | $V_{CM} = 0V$, $I_O = 0 \text{ mA}$ | 1 | 10 | mV (Max) |
| I _B | Input Bias Current | $V_{CM} = 0V$, $I_O = 0 \text{ mA}$ | 0.2 | 1 | μA (Max) |
| I _{OS} | Input Offset Current | $V_{CM} = 0V$, $I_O = 0 \text{ mA}$ | 0.01 | 0.2 | μA (Max) |
| I _O | Output Current Limit | $ V^+ = V^- = 10V$, $t_{on} = 10 \text{ ms}$, $V_O = 0V$ | 6 | 4 | A (Min) |
| *V _{od} | Output Dropout Voltage (Note 10) | $ V^+ - V_O $, $V^+ = 20V$, $I_O = +100 \text{ mA}$ $ V_O - V^- $, $V^- = -20V$, $I_O = -100 \text{ mA}$ | 1.6 2.7 | 5 5 | V (Max) V (Max) |
| *PSRR | Power Supply Rejection Ratio | $V^+ = 40V$ to $20V$, $V^- = -40V$, $V_{cm} = 0V$, $I_O = 0 \text{ mA}$ $V^+ = 40V$, $V^- = -40V$ to $-20V$, $V_{cm} = 0V$, $I_O = 0 \text{ mA}$ | 120 120 | 85 85 | dB (Min) |
| *CMRR | Common Mode Rejection Ratio | $V^+ = 60V$ to $20V$, $V^- = -20V$ to $-60V$, $V_{cm} = 20V$ to $-20V$, $I_O = 0 \text{ mA}$ | 120 | 80 | dB (Min) |
| *A _{VOL} | Open Loop Voltage Gain | $ V^+ = V^- = 40V$, $R_L = 2 \text{ k}\Omega$, $\Delta V_O = 60V$ | 120 | 90 | dB (Min) |
| GBWP | Gain-Bandwidth Product | $ V^+ = V^- = 40V$ $f_O = 100 \text{ kHz}$, $V_{IN} = 50 \text{ mVrms}$ | 8 | 2 | MHz (Min) |
| **e _{IN} | Input Noise | IHF - A Weighting Filter $R_{IN} = 600\Omega$ (Input Referred) | 2.0 | 8.0 | μV (Max) |

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

| Symbol | Parameter | Conditions | Typical (Note 6) | Limit (Note 7) | Units (Limits) |
|--------|---------------------------------|--|---------------------|-------------------|-------------------|
| SNR | Signal-to-Noise Ratio | $P_O = 1W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$ | 98 dB | | dB |
| | | $P_O = 40W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$ | 114 dB | | dB |
| | | $P_{pk} = 100W$, A-Weighted, Measured at 1 kHz, $R_S = 25\Omega$ | 122 dB | | dB |
| IMD | Intermodulation Distortion Test | 60 Hz, 7 kHz, 4:1 (SMPTE) | 0.004 | | % |
| | | 60 Hz, 7 kHz, 1:1 (SMPTE) | 0.006 | | % |

*DC Electrical Test; refer to Test Circuit #1.

**AC Electrical Test; refer to Test Circuit #2.

Note 1: All voltages are measured with respect to supply GND, unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Operating Ratings* indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operating at case temperatures above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of $\theta_{JC} = 1.0^\circ\text{C/W}$ (junction to case). Refer to the Thermal Resistance figure in the Application Information section under **Thermal Considerations**.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: The operating junction temperature maximum is 150°C, however, the instantaneous Safe Operating Area temperature is 250°C.

Note 6: Typicals are measured at 25°C and represent the parametric norm.

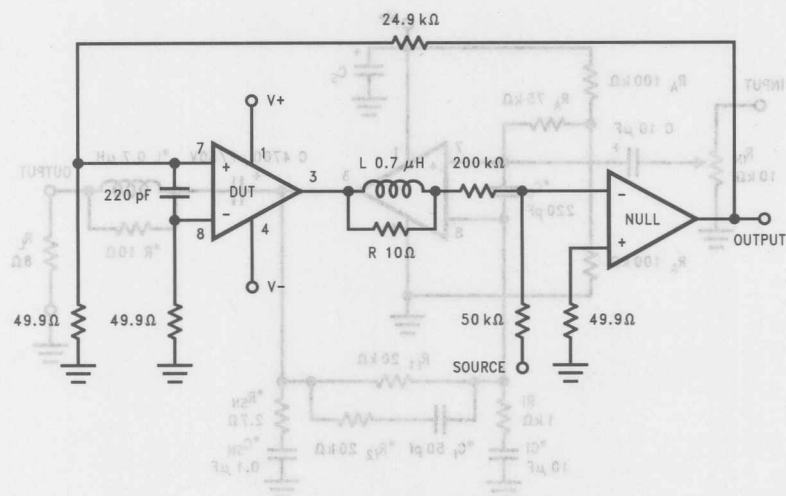
Note 7: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 8: The LM3875T package TA11B is a non-isolated package, setting the tab of the device and the heat sink at V⁻ potential when the LM3875 is directly mounted to the heat sink using only thermal compound. If a mica washer is used in addition to thermal compound, θ_{CS} (case to sink) is increased, but the heat sink will be isolated from V⁻.

Note 9: The feedback compensation network limits the bandwidth of the closed-loop response and so the slew rate will be reduced due to the high frequency roll-off. Without feedback compensation, the slew rate is typically 16V/ μs .

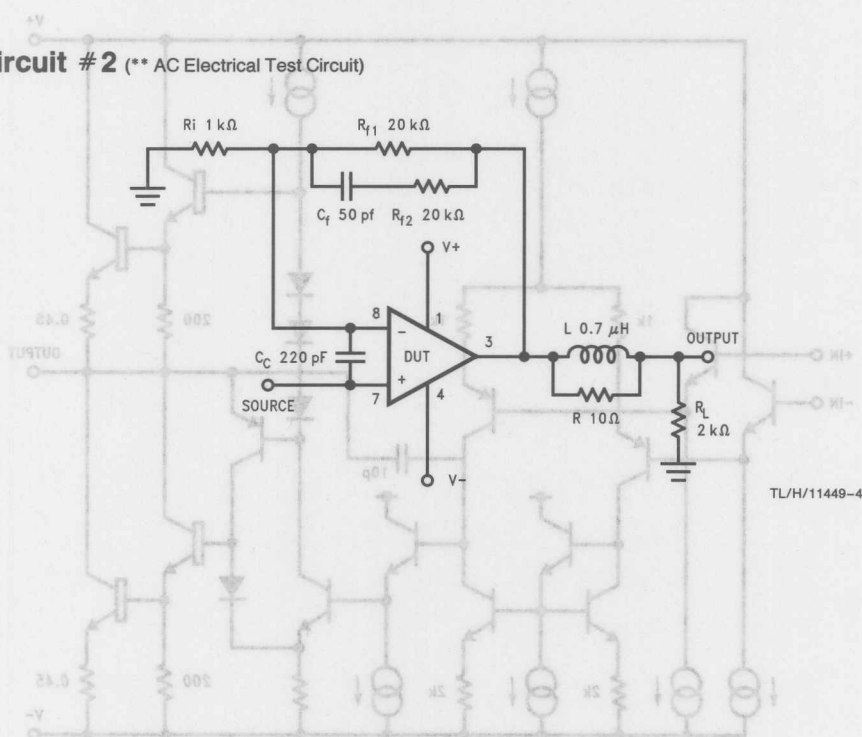
Note 10: The output dropout voltage is the supply voltage minus the clipping voltage. Refer to the Clipping Voltage vs. Supply Voltage graph in the **Typical Performance Characteristics** section.

Test Circuit # 1 *(DC Electrical Test Circuit)



TL/H/11449-3

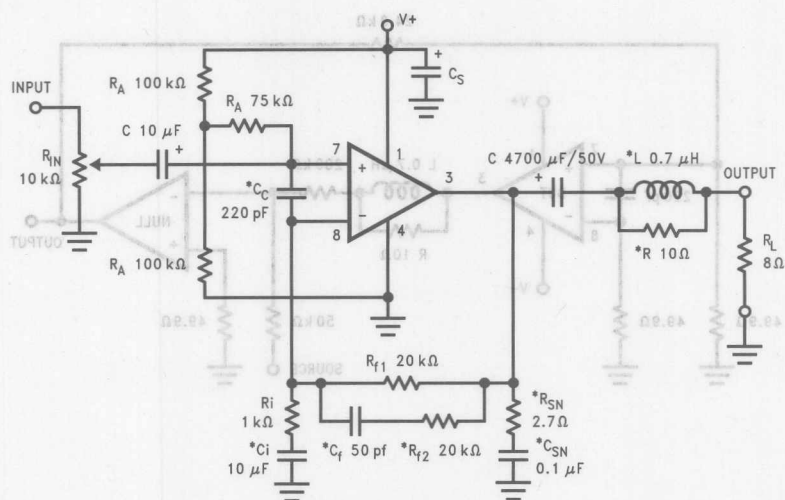
Test Circuit # 2 (** AC Electrical Test Circuit)



TL/H/11449-4

Single Supply Application Circuit

Test Circuit #1 (DC Electrical Test Circuit)

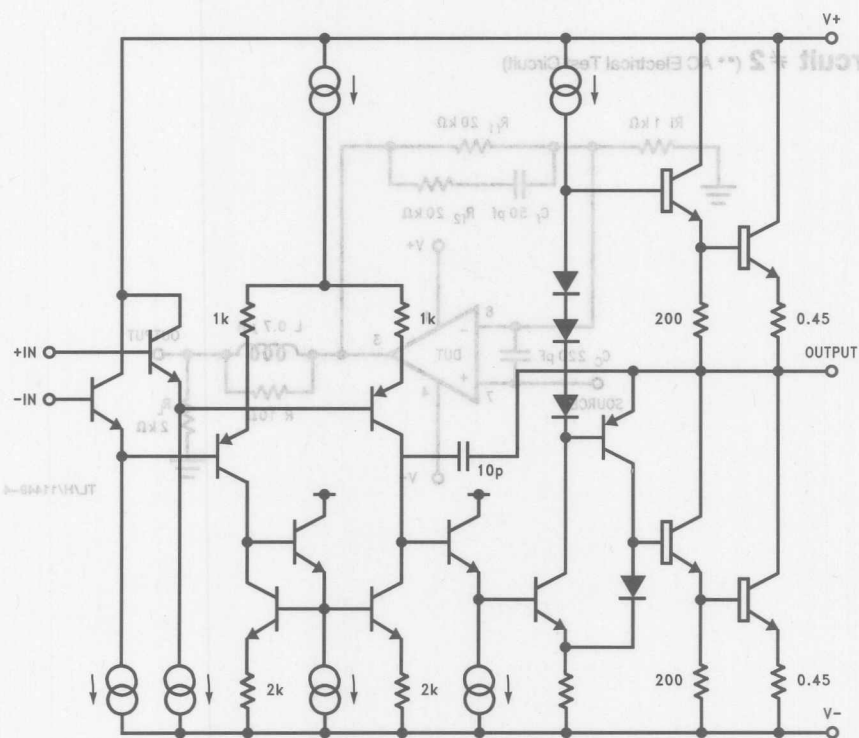


TL/H/11449-5

FIGURE 2. Typical Single Supply Audio Amplifier Application Circuit

*Optional components dependent upon specific design requirements. Refer to the External Components Description section for a component function description.

Equivalent Schematic (Excluding active protection circuitry)



TL/H/11449-6

External Components Description (Figures 1 and 2)

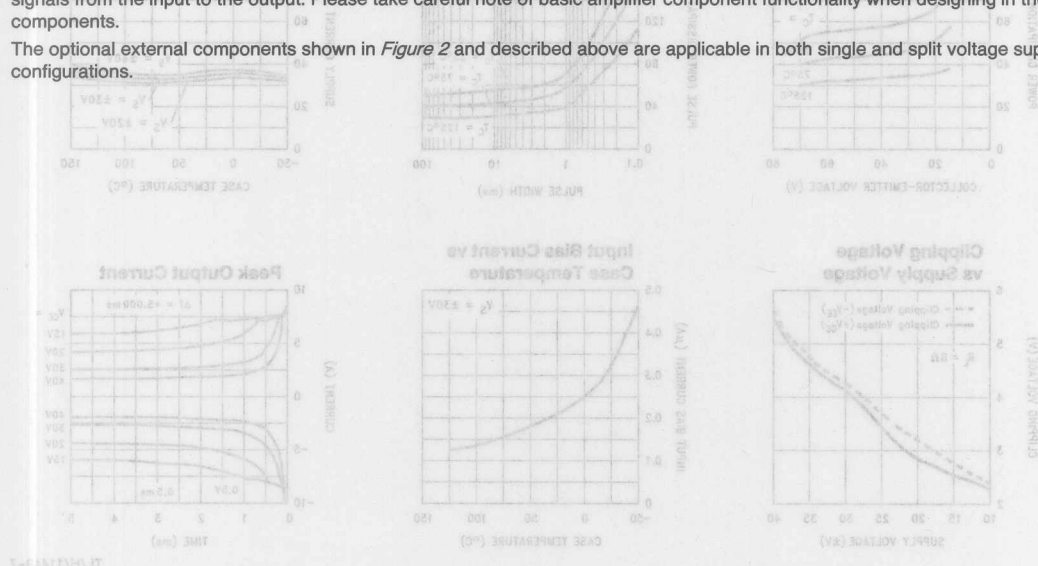
| Components | Functional Description |
|---------------|--|
| 1. R_{IN} | Acts as a volume control by setting the voltage level allowed to the amplifier's input terminals. |
| 2. R_A | Provides DC voltage biasing for the single supply operation and bias current for the positive input terminal. |
| 3. C_A | Provides bias filtering. |
| 4. C | Provides AC coupling at the input and output of the amplifier for single supply operation. |
| 5. R_B | Prevents currents from entering the amplifier's non-inverting input which may be passed through to the load upon power-down of the system due to the low input impedance of the circuitry when the under-voltage circuitry is off. This phenomenon occurs when the supply voltages are below 1.5V. |
| 6. $*C_C$ | Reduces the gain (bandwidth of the amplifier) at high frequencies to avoid quasi-saturation oscillations of the output transistor. The capacitor also suppresses external electromagnetic switching noise created from fluorescent lamps. |
| 7. R_i | Inverting input resistance to provide AC Gain in conjunction with R_{f1} . |
| 8. $*C_i$ | Feedback capacitor. Ensures unity gain at DC. Also a low frequency pole (highpass roll-off) at: $f_c = 1/(2\pi R_i C_i)$. |
| 9. R_{f1} | Feedback resistance to provide AC Gain in conjunction with R_i . |
| 10. $*R_{f2}$ | At higher frequencies feedback resistance works with C_f to provide lower AC Gain in conjunction with R_{f1} and R_i . A high frequency pole (lowpass roll-off) exists at: $f_c = [R_{f1} R_{f2}] (s + 1/R_{f2} C_f) / [(R_{f1} + R_{f2}) (s + 1/C_f (R_{f1} + R_{f2}))]$. |
| 11. $*C_f$ | Compensation capacitor that works with R_{f1} and R_{f2} to reduce the AC Gain at higher frequencies. |
| 12. $*R_{SN}$ | Works with C_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. |
| 13. $*C_{SN}$ | Works with R_{SN} to stabilize the output stage by creating a pole that eliminates high frequency oscillations. $f_c = 1/(2\pi R_{SN} C_{SN})$. |
| 14. $*L$ | Provides high impedance at high frequencies so that R may decouple a highly capacitive load and reduce the Q of the series resonant circuit due to capacitive load. Also provides a low impedance at low frequencies to short out R and pass audio signals to the load. |
| 15. $*R$ | |
| 16. C_S | Provides power supply filtering and bypassing. |

*Optional components dependent upon specific design requirements. Refer to the Application Information section for more information.

OPTIONAL EXTERNAL COMPONENT INTERACTION

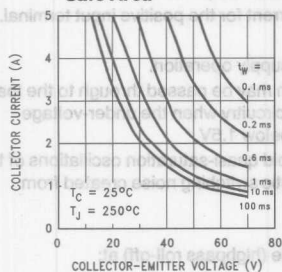
Although the optional external components have specific desired functions that are designed to reduce the bandwidth and eliminate unwanted high frequency oscillations they may cause certain undesirable effects when they interact. Interaction may occur for components whose reactances are in close proximity to one another. One example would be the coupling capacitor, C_C , and the compensation capacitor, C_f . These two components act as low impedances to certain frequencies which will couple signals from the input to the output. Please take careful note of basic amplifier component functionality when designing in these components.

The optional external components shown in Figure 2 and described above are applicable in both single and split voltage supply configurations.

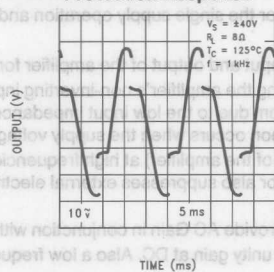


Typical Performance Characteristics

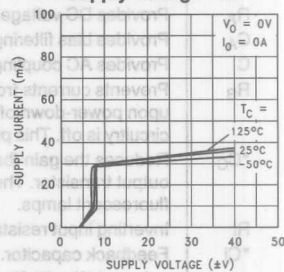
Safe Area



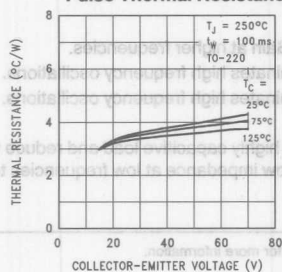
SPIKE Protection Response



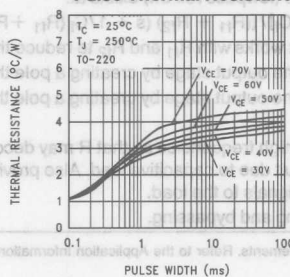
Supply Current vs Supply Voltage



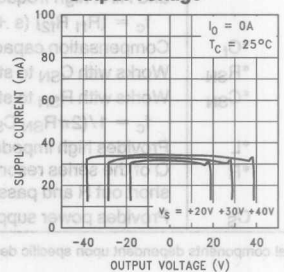
Pulse Thermal Resistance



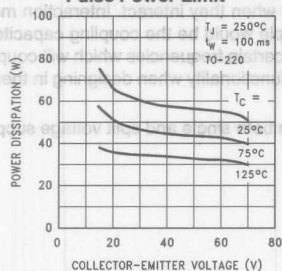
Pulse Thermal Resistance



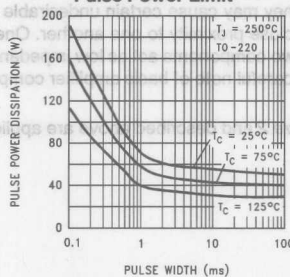
Supply Current vs Output Voltage



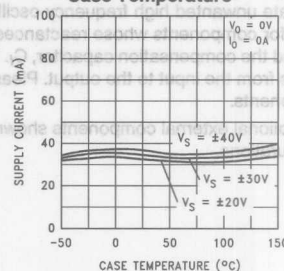
Pulse Power Limit



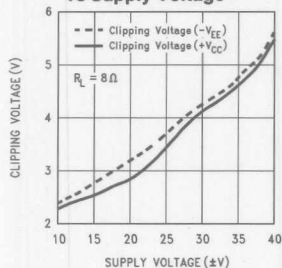
Pulse Power Limit



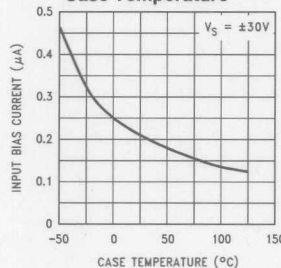
Supply Current vs Case Temperature



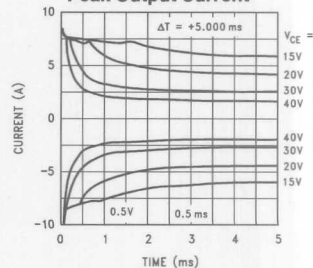
Clipping Voltage vs Supply Voltage



Input Bias Current vs Case Temperature

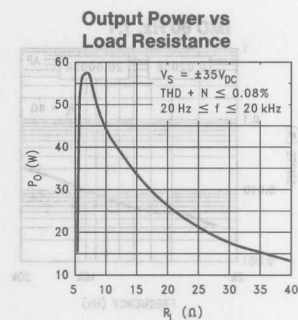
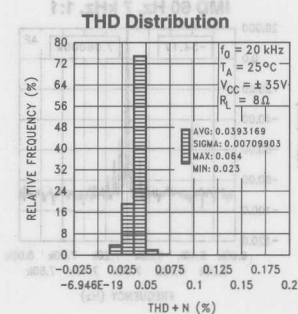
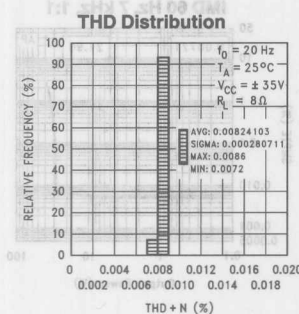
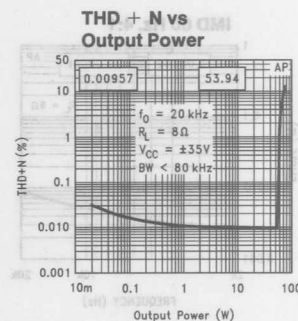
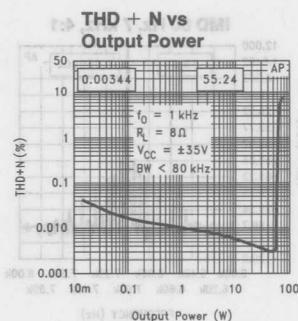
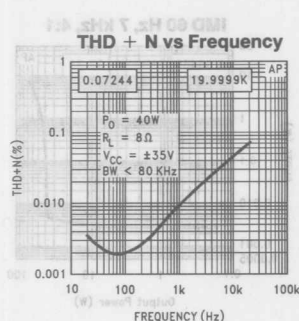


Peak Output Current



TL/H/11449-7

Typical Performance Characteristics (Continued)



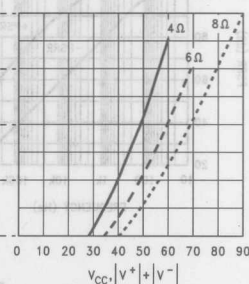
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**Max Heatsink Thermal Resistance ($^{\circ}C/W$)
at the Specified Ambient Temperature ($^{\circ}C$)**

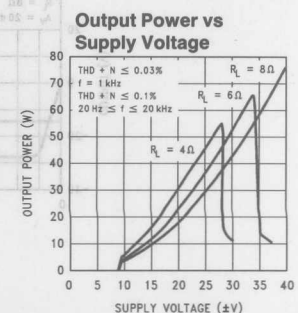
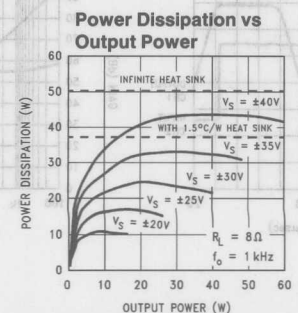
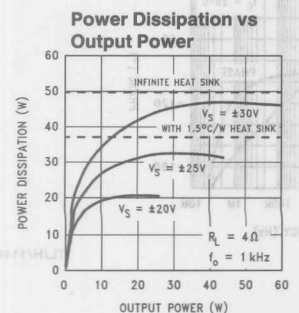
| $T_A = 25^{\circ}C$ | 40 | 50 | 60 | 70 | 80 | 90 | 100 | 110 | $T_C, ^{\circ}C$ | P_O, W |
|---------------------|-----|-----|-----|-----|-----|-----|-----|-----|------------------|----------|
| 1.3 | 1.0 | | | | | | | | 90 | 50 |
| 1.6 | 1.2 | 1.0 | | | | | | | 96 | 45 |
| 1.9 | 1.6 | 1.3 | 1.1 | | | | | | 102 | 40 |
| 2.4 | 1.9 | 1.7 | 1.4 | 1.1 | | | | | 108 | 35 |
| 3.0 | 2.5 | 2.1 | 1.8 | 1.5 | 1.1 | | | | 114 | 30 |
| 3.8 | 3.2 | 2.8 | 2.4 | 2.0 | 1.6 | 1.2 | | | 120 | 25 |
| 5.1 | 4.3 | 3.8 | 3.3 | 2.8 | 2.3 | 1.8 | 1.3 | | 126 | 20 |
| 7.1 | 6.1 | 5.5 | 4.8 | 4.1 | 3.5 | 2.8 | 2.1 | 1.5 | 132 | 15 |
| 11.3 | 9.8 | 8.8 | 7.8 | 6.8 | 5.8 | 4.8 | 3.8 | 2.8 | 138 | 10 |

Note: The maximum heat sink thermal resistance values, θ_{SA} , in the table above were calculated using a $\theta_{CS} = 0.2^{\circ}C/W$ due to thermal compound.

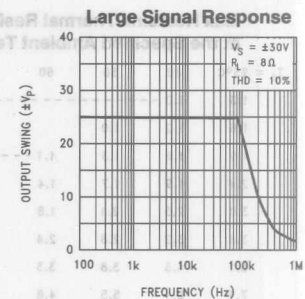
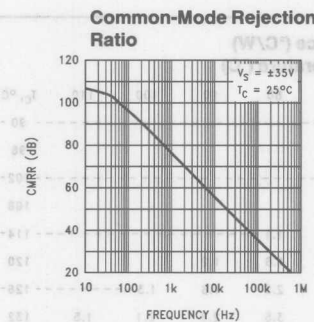
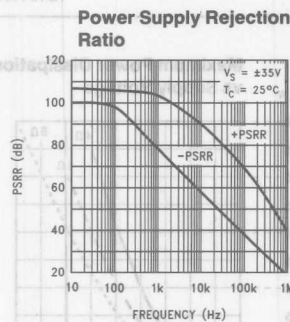
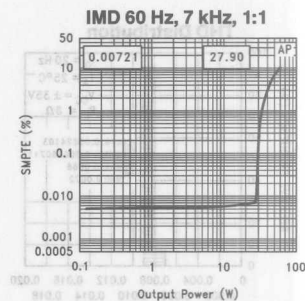
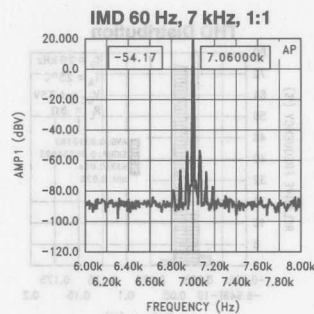
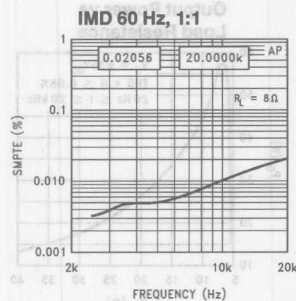
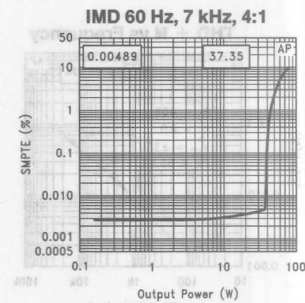
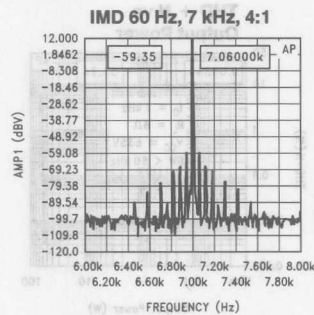
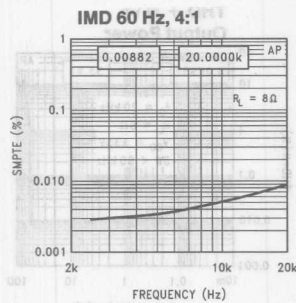
**Maximum Power Dissipation
vs Supply Voltage**



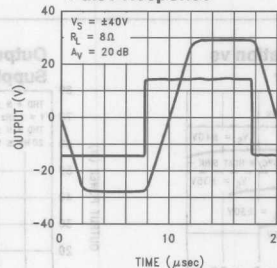
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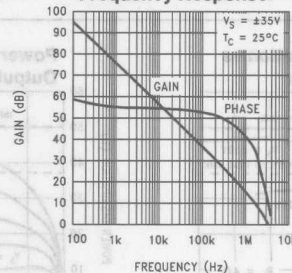


Pulse Response



Open Loop

Frequency Response



TL/H/11449-9

Application Information

GENERAL FEATURES

Under-Voltage Protection: Upon system power-up the under-voltage Protection Circuitry allows the power supplies and their corresponding caps to come up close to their full values before turning on the LM3875 such that no DC output spikes occur. Upon turn-off, the output of the LM3875 is brought to ground before the power supplies such that no transients occur at power-down.

Over-Voltage Protection: The LM3875 contains overvoltage protection circuitry that limits the output current to approximately 4A peak while also providing voltage clamping, though not through internal clamping diodes. The clamping effect is quite the same, however, the output transistors are designed to work alternately by sinking large current spikes.

SPIKe Protection: The LM3875 is protected from instantaneous peak-temperature stressing by the power transistor array. The Safe Operating Area graph in the **Typical Performance Characteristics** section shows the area of device operation where the SPIKe Protection Circuitry is not enabled. The waveform to the right of the SOA graph exemplifies how the dynamic protection will cause waveform distortion when enabled.

Thermal Protection: The LM3875 has a sophisticated thermal protection scheme to prevent long-term thermal stress to the device. When the temperature on the die reaches 165°C, the LM3875 shuts down. It starts operating again when the die temperature drops to about 155°C, but if the temperature again begins to rise, shutdown will occur again at 165°C. Therefore the device is allowed to heat up to a relatively high temperature if the fault condition is temporary, but a sustained fault will cause the device to cycle in a Schmitt Trigger fashion between the thermal shutdown temperature limits of 165°C and 155°C. This greatly reduces the stress imposed on the IC by thermal cycling, which in turn improves its reliability under sustained fault conditions.

Since the die temperature is directly dependent upon the heat sink, the heat sink should be chosen as discussed in the **Thermal Considerations** section, such that thermal shutdown will not be reached during normal operation. Using the best heat sink possible within the cost and space constraints of the system will improve the long-term reliability of any power semiconductor device.

THERMAL CONSIDERATIONS

Heat Sinking

The choice of a heat sink for a high-power audio amplifier is made entirely to keep the die temperature at a level such that the thermal protection circuitry does not operate under normal circumstances. The heat sink should be chosen to dissipate the maximum IC power for a given supply voltage and rated load.

With high-power pulses of longer duration than 100 ms, the case temperature will heat up drastically without the use of a heat sink. Therefore the case temperature, as measured at the center of the package bottom, is entirely dependent on heat sink design and the mounting of the IC to the heat sink. For the design of a heat sink for your audio amplifier application refer to the **Determining the Correct Heat Sink** section.

Since a semiconductor manufacturer has no control over which heat sink is used in a particular amplifier design, we can only inform the system designer of the parameters and the method needed in the determination of a heat sink. With this in mind, the system designer must choose his supply voltages, a rated load, a desired output power level, and know the ambient temperature surrounding the device. These parameters are in addition to knowing the maximum junction temperature and the thermal resistance of the IC, both of which are provided by National Semiconductor.

As a benefit to the system designer we have provided Maximum Power Dissipation vs Supply Voltages curves for various loads in the **Typical Performance Characteristics** section, giving an accurate figure for the maximum thermal resistance required for a particular amplifier design. This data was based on $\theta_{JC} = 1^\circ\text{C/W}$ and $\theta_{CS} = 0.2^\circ\text{C/W}$. We also provide a section regarding heat sink determination for any audio amplifier design where θ_{CS} may be a different value. It should be noted that the idea behind dissipating the maximum power within the IC is to provide the device with a low resistance to convection heat transfer such as a heat sink. Therefore, it is necessary for the system designer to be conservative in his heat sink calculations. As a rule, the lower the thermal resistance of the heat sink the higher the amount of power that may be dissipated. This is, of course, guided by the cost and size requirements of the system. Convection cooling heat sinks are available commercially, and their manufacturers should be consulted for ratings.

Proper mounting of the IC is required to minimize the thermal drop between the package and the heat sink. The heat sink must also have enough metal under the package to conduct heat from the center of the package bottom to the fins without excessive temperature drop.

A thermal grease such as Wakefield type 120 or Thermalloy Thermacote should be used when mounting the package to the heat sink. Without this compound, the thermal resistance will be no better than 0.5°C/W , and probably much worse. With the compound, thermal resistance will be 0.2°C/W or less, assuming under 0.005 inch combined flatness runout for the package and heat sink. Proper torquing of the mounting bolts is important and can be determined from heat sink manufacturer's specification sheets.

Should it be necessary to isolate V- from the heat sink, an insulating washer is required. Hard washers like beryllium oxide, anodized aluminum and mica require the use of thermal compound on both faces. Two-mil mica washers are most common, giving about 0.4°C/W interface resistance with the compound.

Silicone-rubber washers are also available. A 0.5°C/W thermal resistance is claimed without thermal compound. Experience has shown that these rubber washers deteriorate and must be replaced should the IC be dismounted.

Determining Maximum Power Dissipation

Power dissipation within the integrated circuit package is a very important parameter requiring a thorough understanding if optimum power output is to be obtained. An incorrect maximum power dissipation (P_D) calculation may result in inadequate heatsinking, causing thermal shutdown circuitry to operate and limit the output power.

Application Information (Continued)

The following equations can be used to accurately calculate the maximum and average integrated circuit power dissipation for your amplifier design, given the supply voltage, rated load, and output power. These equations can be directly applied to the Power Dissipation vs Output Power curves in the **Typical Performance Characteristics** section.

Equation (1) exemplifies the maximum power dissipation of the IC and equations (2) and (3) exemplify the average IC power dissipation expressed in different forms.

$$P_{DMAX} = V_{CC}^2 / 2\pi^2 R_L \quad (1)$$

where V_{CC} is the total supply voltage

$$P_{DAVE} = (V_{OPK}/R_L) [V_{CC}/\pi - V_{OPK}/2] \quad (2)$$

where V_{CC} is the total supply voltage and $V_{OPK} = V_{CC}/\pi$

$$P_{DAVE} = V_{CC} V_{OPK} / \pi R_L = V_{OPK}^2 / 2 R_L \quad (3)$$

where V_{CC} is the total supply voltage.

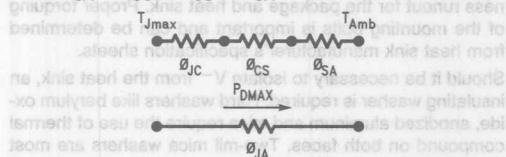
Determining the Correct Heat Sink

Once the maximum IC power dissipation is known for a given supply voltage, rated load, and the desired rated output power the maximum thermal resistance (in $^{\circ}\text{C}/\text{W}$) of a heat sink can be calculated. This calculation is made using equation (4) and is based on the fact that thermal heat flow parameters are analogous to electrical current flow properties. It is also known that typically the thermal resistance, θ_{JC} (junction to case), of the LM3875 is $1^{\circ}\text{C}/\text{W}$ and that using Thermalloy Thermacote thermal compound provides a thermal resistance, θ_{CS} (case to heat sink), of about $0.2^{\circ}\text{C}/\text{W}$ as explained in the **Heat Sinking** section.

Referring to the figure below, it is seen that the thermal resistance from the die (junction) to the outside air (ambient) is a combination of three thermal resistances, two of which are known, θ_{JC} and θ_{CS} . Since convection heat flow (power dissipation) is analogous to current flow, thermal resistance is analogous to electrical resistance, and temperature drops are analogous to voltage drops, the power dissipation out of the LM3875 is equal to the following:

$$P_{DMAX} = (T_{Jmax} - T_{Amb}) / \theta_{JA}$$

where $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$



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But since we know P_{DMAX} , θ_{JC} , and θ_{CS} for the application and we are looking for θ_{SA} , we have the following:

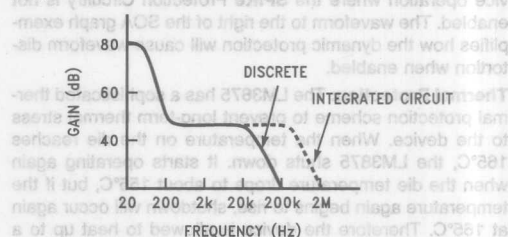
$$\theta_{SA} = [(T_{Jmax} - T_{Amb}) - P_{DMAX}(\theta_{JC} + \theta_{CS})] / P_{DMAX} \quad (4)$$

Again it must be noted that the value of θ_{SA} is dependent upon the system designer's amplifier application and its corresponding parameters as described previously. If the ambient temperature that the audio amplifier is to be working under is higher than the normal 25°C , then the thermal resistance for the heat sink, given all other things are equal, will need to be smaller.

Equations (1) and (4) are the only equations needed in the determination of the maximum heat sink thermal resistance. This is, of course, given that the system designer knows the required supply voltages to drive his rated load at a particular power output level and the parameters provided by the semiconductor manufacturer. These parameters are the junction to case thermal resistance, θ_{JC} , $T_{Jmax} = 150^{\circ}\text{C}$, and the recommended Thermalloy Thermacote thermal compound resistance, θ_{CS} .

SIGNAL-TO-NOISE RATIO

In the measurement of the signal-to-noise ratio, misinterpretations of the numbers actually measured are common. One amplifier may sound much quieter than another, but due to improper testing techniques, they appear equal in measurements. This is often the case when comparing integrated circuit designs to discrete amplifier designs. Discrete transistor amps often "run out of gain" at high frequencies and therefore have small bandwidths to noise as indicated below.



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Integrated circuits have additional open loop gain allowing additional feedback loop gain in order to lower harmonic distortion and improve frequency response. It is this 'additional bandwidth that can lead to erroneous signal-to-noise measurements' if not considered during the measurement process. In the typical example above, the difference in bandwidth appears small on a log scale but the factor of 10 in bandwidth, (200 kHz to 2 MHz) can result in a 10 dB theoretical difference in the signal-to-noise ratio (white noise is proportional to the square root of the bandwidth in a system).

In comparing audio amplifiers it is necessary to measure the magnitude of noise in the audible bandwidth by using a "weighting" filter.¹ A "weighting" filter alters the frequency response in order to compensate for the average human ear's sensitivity to the frequency spectra. The weighting filters at the same time provide the bandwidth limiting as discussed in the previous paragraph.

In addition to noise filtering, differing meter types give different noise readings. Meter responses include:

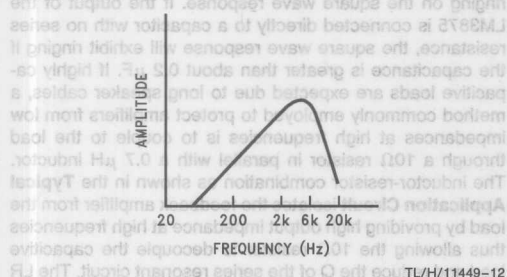
1. RMS reading,
2. average responding,
3. peak reading, and
4. quasi peak reading.

Reference 1: CCIR/ARM: A Practical Noise Measurement Method; by Ray Dolby, David Robinson and Kenneth Gundry, AES Preprint No. 1353 (F-3).

Application Information (Continued)

Although theoretical noise analysis is derived using true RMS based calculations, most actual measurements are taken with ARM (Average Responding Meter) test equipment.

Typical signal-to-noise figures are listed for an A-weighted filter which is commonly used in the measurement of noise. The shape of all weighting filters is similar, with the peak of the curve usually occurring in the 3 kHz–7 kHz region as shown below.



SUPPLY BYPASSING

The LM3875 has excellent power supply rejection and does not require a regulated supply. However, to eliminate possible oscillations all op amps and power op amps should have their supply leads bypassed with low-inductance capacitors having short leads and located close to the package terminals. Inadequate power supply bypassing will manifest itself by a low frequency oscillation known as "motorboating" or by high frequency instabilities. These instabilities can be eliminated through multiple bypassing utilizing a large tantalum or electrolytic capacitor (10 μ F or larger) which is used to absorb low frequency variations and a small ceramic capacitor (0.1 μ F) to prevent any high frequency feedback through the power supply lines.

If adequate bypassing is not provided the current in the supply leads which is a rectified component of the load current may be fed back into internal circuitry. This signal causes low distortion at high frequencies requiring that the supplies be bypassed at the package terminals with an electrolytic capacitor of 470 μ F or more.

LEAD INDUCTANCE

Power op amps are sensitive to inductance in the output lead, particularly with heavy capacitive loading. Feedback to the input should be taken directly from the output terminal, minimizing common inductance with the load.

Lead inductance can also cause voltage surges on the supplies. With long leads to the power supply, energy is stored in the lead inductance when the output is shorted. This energy can be dumped back into the supply bypass capacitors when the short is removed. The magnitude of this transient is reduced by increasing the size of the bypass capacitor near the IC. With at least a 20 μ F local bypass, these voltage surges are important only if the lead length exceeds a couple feet (> 1 μ H lead inductance). Twisting together the supply and ground leads minimizes the effect.

LAYOUT, GROUND LOOPS AND STABILITY

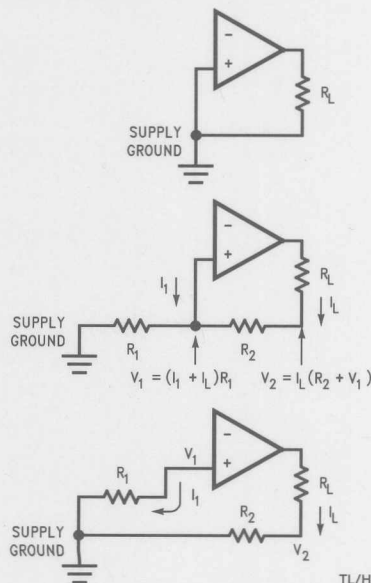
The LM3875 is designed to be stable when operated at a closed-loop gain of 10 or greater, but as with any other high-

current amplifier, the LM3875 can be made to oscillate under certain conditions. These usually involve printed circuit board layout or output/input coupling.

When designing a layout, it is important to return the load ground, the output compensation ground, and the low level (feedback and input) grounds to the circuit board common ground point through separate paths. Otherwise, large currents flowing along a ground conductor will generate voltages on the conductor which can effectively act as signals at the input, resulting in high frequency oscillation or excessive distortion. It is advisable to keep the output compensation components and the 0.1 μ F supply decoupling capacitors as close as possible to the LM3875 to reduce the effects of PCB trace resistance and inductance. For the same reason, the ground return paths should be as short as possible.

In general, with fast, high-current circuitry, all sorts of problems can arise from improper grounding which again can be avoided by returning all grounds separately to a common point. Without isolating the ground signals and returning the grounds to a common point, ground loops may occur.

"Ground Loop" is the term used to describe situations occurring in ground systems where a difference in potential exists between two ground points. Ideally a ground is a ground, but unfortunately, in order for this to be true, ground conductors with zero resistance are necessary. Since real world ground leads possess finite resistance, currents running through them will cause finite voltage drops to exist. If two ground return lines tie into the same path at different points there will be a voltage drop between them. The first figure below shows a common ground example where the positive input ground and the load ground are returned to the supply ground point via the same wire. The addition of the finite wire resistance, R_2 , results in a voltage difference between the two points as shown below.



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Application Information (Continued)

The load current I_L will be much larger than input bias current I_1 , thus V_1 will follow the output voltage directly, i.e., in phase. Therefore the voltage appearing at the non-inverting input is effectively positive feedback and the circuit may oscillate. If there were only one device to worry about then the values of R_1 and R_2 would probably be small enough to be ignored; however, several devices normally comprise a total system. Any ground return of a separate device, whose output is in phase, can feedback in a similar manner and cause instabilities. Out of phase ground loops also are troublesome, causing unexpected gain and phase errors.

The solution to most ground loop problems is to always use a single-point ground system, although this is sometimes impractical. The third figure above is an example of a single-point ground system.

The single-point ground concept should be applied rigorously to all components and all circuits when possible. Violations of single-point grounding are most common among printed circuit board designs, since the circuit is surrounded by large ground areas which invite the temptation to run a device to the closest ground spot. As a final rule, make all ground returns low resistance and low inductance by using large wire and wide traces.

Occasionally, current in the output leads (which function as antennas) can be coupled through the air to the amplifier input, resulting in high-frequency oscillation. This normally happens when the source impedance is high or the input

leads are long. The problem can be eliminated by placing a small capacitor, C_C , (on the order of 50 pF–500 pF) across the LM3875 input terminals. Refer to the **External Components Description** section relating to component interaction with C_F .

REACTIVE LOADING

It is hard for most power amplifiers to drive highly capacitive loads very effectively and normally results in oscillations or ringing on the square wave response. If the output of the LM3875 is connected directly to a capacitor with no series resistance, the square wave response will exhibit ringing if the capacitance is greater than about $0.2\ \mu\text{F}$. If highly capacitive loads are expected due to long speaker cables, a method commonly employed to protect amplifiers from low impedances at high frequencies is to couple to the load through a 10Ω resistor in parallel with a $0.7\ \mu\text{H}$ inductor. The inductor-resistor combination as shown in the **Typical Application Circuit** isolates the feedback amplifier from the load by providing high output impedance at high frequencies thus allowing the 10Ω resistor to decouple the capacitive load and reduce the Q of the series resonant circuit. The LR combination also provides low output impedance at low frequencies thus shorting out the 10Ω resistor and allowing the amplifier to drive the series RC load (large capacitive load due to long speaker cables) directly.

Application Information (Continued)

GENERALIZED AUDIO POWER AMPLIFIER DESIGN

The system designer usually knows some of the following parameters when starting an audio amplifier design:

| | |
|------------------------|----------------|
| Desired Power Output | Input Level |
| Input Impedance | Load Impedance |
| Maximum Supply Voltage | Bandwidth |

The power output and load impedance determine the power supply requirements, however, depending upon the application some system designers may be limited to certain maximum supply voltages. If the designer does have a power supply limitation, he should choose a practical load impedance which would allow the amplifier to provide the desired output power, keeping in mind the current limiting capabilities of the device. In any case, the output signal swing and current are found from (where P_O is the average output power):

$$V_{\text{peak}} = \sqrt{2 R_L P_O} \quad (1)$$

$$I_{\text{peak}} = \sqrt{(2 P_O)/R_L} \quad (2)$$

To determine the maximum supply voltage the following parameters must be considered. Add the dropout voltage (5 volts for LM3875) to the peak output swing, V_{peak} , to get the supply rail value, (i.e. $+V_{\text{peak}} + V_{\text{od}}$) at a current of I_{peak} . The regulation of the supply determines the unloaded voltage, usually about 15% higher. Supply voltage will also rise 10% during high line conditions. Therefore, the maximum supply voltage is obtained from the following equation:

$$\text{max. supplies} \approx \pm (V_{\text{peak}} + V_{\text{od}}(1 + \text{regulation}))(1.1) \quad (3)$$

The input sensitivity and the output power specs determine the minimum required gain as depicted below:

$$A_v \geq (\sqrt{P_O R_L})/(V_{\text{IN}}) = V_{\text{orms}}/V_{\text{inrms}} \quad (4)$$

Normally the gain is set between 20 and 200; for a 40W, 8 Ω audio amplifier this results in a sensitivity of 894 mV and 89 mV, respectively. Although higher gain amplifiers provide greater output power and dynamic headroom capabilities, there are certain shortcomings that go along with the so called "gain". The input referred noise floor is increased and hence the SNR is worse. With the increase in gain, there is also a reduction of the power bandwidth which results in a decrease in feedback thus not allowing the amplifier to respond as quickly to nonlinearities. This decreased ability to respond to nonlinearities increases the THD + N specification.

The desired input impedance is set by R_{IN} . Very high values can cause board layout problems and DC offsets at the output. The value for the feedback resistance, R_{f1} , should be chosen to be a relatively large value (10 k Ω –100 k Ω), and the other feedback resistance, R_{f2} , is calculated using standard op amp configuration gain equations. Most audio amplifiers are designed from the non-inverting amplifier configuration.

DESIGN A 40W/8 Ω AUDIO AMPLIFIER

Given:

| | |
|-----------------|----------------------------|
| Power Output | 40W |
| Load Impedance | 8 Ω |
| Input Level | 1V(max) |
| Input Impedance | 100 k Ω |
| Bandwidth | 20 Hz–20 kHz \pm 0.25 dB |

Equation (1) and (2) give:

$$40\text{W}/8\Omega \quad V_{\text{peak}} = 25.3\text{V} \quad I_{\text{peak}} = 3.16\text{A}$$

Therefore the supply required is: $\pm 30.3\text{V} @ 3.16\text{A}$

With 15% regulation and high line the final supply voltage is $\pm 38.3\text{V}$ using equation (3). At this point it is a good idea to check the Power Output vs Supply Voltage to ensure that the required output power is obtainable from the device while maintaining low THD + N. It is also good to check the Power Dissipation vs Supply Voltage to ensure that the device can handle the internal power dissipation. At the same time designing in a relatively practical sized heat sink with a low thermal resistance is also important. Refer to **Typical Performance Characteristics** graphs and the **Thermal Considerations** section for more information.

The minimum gain from equation (4) is: $A_v \geq 18$

We select a gain of 21 (Non-Inverting Amplifier); resulting in a sensitivity of 894 mV.

Letting R_{IN} equal 100 k Ω gives the required input impedance, however, this would eliminate the "volume control" unless an additional input impedance was placed in series with the 10 k Ω potentiometer that is depicted in *Figure 1*. Adding the additional 100 k Ω resistor would ensure the minimum required input impedance.

For low DC offsets at the output we let $R_{\text{f1}} = 100 \text{ k}\Omega$. Solving for R_{f2} (Non-Inverting Amplifier) gives the following:

$$R_{\text{f2}} = R_{\text{f1}}/(A_v - 1) = 100\text{k}/(21 - 1) = 5 \text{ k}\Omega; \text{ use } 5.1 \text{ k}\Omega$$

The bandwidth requirement must be stated as a pole, i.e., the 3 dB frequency. Five times away from a pole give 0.17 dB down, which is better than the required 0.25 dB. Therefore:

$$f_L = 20 \text{ Hz}/5 = 4 \text{ Hz}$$

$$f_H = 20 \text{ kHz} \times 5 = 100 \text{ kHz}$$

At this point, it is a good idea to ensure that the Gain Bandwidth Product for the part will provide the designed gain out to the upper 3 dB point of 100 kHz. This is why the minimum GBWP of the LM3875 is important.

$$\text{GBWP} = A_v \times f_3 \text{ dB} = 21 \times 100 \text{ kHz} = 2.1 \text{ MHz}$$

$$\text{GBWP} = 2.0 \text{ MHz (min) for LM3875}$$

Solving for the low frequency roll-off capacitor, C_i , we have:

$$C_i > 1/(2\pi R_{\text{f1}} f_L) = 7.8 \mu\text{F}; \text{ use } 10 \mu\text{F}$$

Continuous average power output in watts (or dBW) can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion. **Music Power:** A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load, specified by the part's maximum voltage swing.

two equal resistances to obtain zero output voltage and current.

Input Bias Current: The absolute value of the average of the two input currents with the output voltage and current at zero.

Input Offset Current: The absolute value of the difference in the two input currents with the output voltage and current at zero.

Input Common-Mode Voltage Range (or Input Voltage Range): The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Quiescent Supply Current: The current required from the power supply to operate the amplifier with no load and the output voltage and current at zero.

Slew Rate: The internally limited rate of change in output voltage with a large amplitude step function applied to the input.

Class B Amplifier: The most common type of audio power amplifier that consists of two output devices each of which conducts for 180° of the input cycle. The LM3875 is a Quasi-AB type amplifier.

Crossover Distortion: Distortion caused in the output stage of a class B amplifier. It can result from inadequate bias current providing a dead zone where the output does not respond to the input as the input cycle goes through its zero crossing point. Also for ICs an inadequate frequency response of the output PNP device can cause a turn-on delay giving crossover distortion on the negative going transition through zero crossing at the higher audio frequencies.

THD + N: Total Harmonic Distortion plus Noise refers to the measurement technique in which the fundamental component is removed by a bandreject (notch) filter and all remaining energy is measured including harmonics and noise.

Signal-to-Noise Ratio: The ratio of a system's output signal level to the system's output noise level obtained in the absence of a signal. The output reference signal is either specified or measured at a specified distortion level.

Continuous Average Output Power: The minimum sine wave continuous average power output in watts (or dBW) that can be delivered into the rated load, over the rated bandwidth, at the rated maximum total harmonic distortion.

Music Power: A measurement of the peak output power capability of an amplifier with either a signal duration sufficiently short that the amplifier power supply does not sag during the measurement, or when high quality external power supplies are used. This measurement (an IHF standard) assumes that with normal music program material the amplifier power supplies will sag insignificantly.

Peak Power: Most commonly referred to as the power output capability of an amplifier that can be delivered to the load; specified by the part's maximum voltage swing.

supply voltages, a rated load value, and a rated THD + N figure) and the level just before clipping distortion occurs, expressed in decibels.

Large Signal Voltage Gain: The ratio of the output voltage swing to the differential input voltage required to drive the output from zero to either swing limit. The output swing limit is the supply voltage less a specified quasi-saturation voltage. A pulse of short enough duration to minimize thermal effects is used as a measurement signal.

Output-Current Limit: The output current with a fixed output voltage and a large input overdrive. The limiting current drops with time once SPIKE protection circuitry is activated.

Output Saturation Threshold (Clipping Point): The output swing limit for a specified input drive beyond that required for zero output. It is measured with respect to the supply to which the output is swinging.

Output Resistance: The ratio of the change in output voltage to the change in output current with the output around zero.

Power Dissipation Rating: The power that can be dissipated for a specified time interval without activating the protection circuitry. For time intervals in excess of 100 ms, dissipation capability is determined by heat sinking of the IC package rather than by the IC itself.

Thermal Resistance: The peak, junction-temperature rise, per unit of internal power dissipation (units in °C/W), above the case temperature as measured at the center of the package bottom.

The DC thermal resistance applies when one output transistor is operating continuously. The AC thermal resistance applies with the output transistors conducting alternately at a high enough frequency that the peak capability of neither transistor is exceeded.

Power Bandwidth: The power bandwidth of an audio amplifier is the frequency range over which the amplifier voltage gain does not fall below 0.707 of the flat band voltage gain specified for a given load and output power.

Power bandwidth also can be measured by the frequencies at which a specified level of distortion is obtained while the amplifier delivers a power output 3 dB below the rated output. For example, an amplifier rated at 60W with ≤0.25% THD + N, would make its power bandwidth measured as the difference between the upper and lower frequencies at which 0.25% distortion was obtained while the amplifier was delivering 30W.

Gain-Bandwidth Product: The Gain-Bandwidth Product is a way of predicting the high-frequency usefulness of an op amp. The Gain-Bandwidth Product is sometimes called the unity-gain frequency or unity-gain cross frequency because the open-loop gain characteristic passes through or crosses unity gain at this frequency. Simply, we have the following relationship:

$$A_{CL1} \times f_1 = A_{CL2} \times f_2$$

Assuming that at unity-gain

$$(A_{CL1} = 1 \text{ or } 0 \text{ dB}) f_u = f_1 = \text{GBWP},$$

then we have the following:

$$\text{GBWP} = A_{CL2} \times f_2$$

then the open-loop gain can be found at any frequency. This is also an excellent equation to determine the 3 dB point of a closed-loop gain, assuming that you know the GBWP of the device. Refer to the diagram below.

Bi-amplification: The technique of splitting the audio frequency spectrum into two sections and using individual power amplifiers to drive a separate woofer and tweeter. Crossover frequencies for the amplifiers usually vary between 500 Hz and 1600 Hz. "Biamping" has the advantages of allowing smaller power amps to produce a given sound pressure level and reducing distortion effects produced by overdrive in one part of the frequency spectrum affecting the other part.

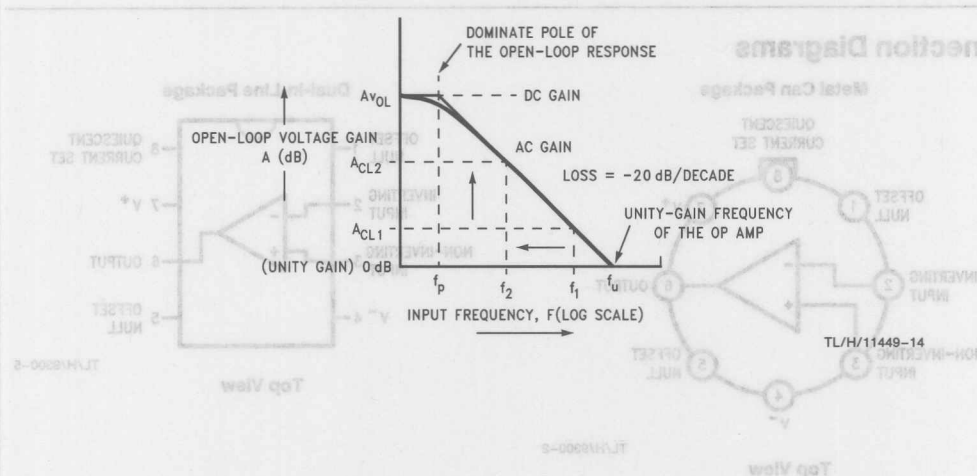
Literally: International Radio Consultative Committee
Average Responding Meter

This refers to a weighted noise measurement for a Dolby B type noise reduction system. A filter characteristic is used that gives a closer correlation of the measurement with the subjective annoyance of noise to the ear. Measurements made with this filter cannot necessarily be related to unweighted noise measurements by some fixed conversion factor since the answers obtained will depend on the spectrum of the noise source.

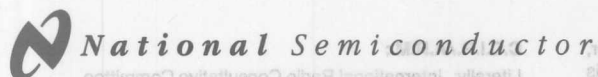
S.P.L.: Sound Pressure Level—usually measured with a microphone/meter combination calibrated to a pressure level of 0.0002 μ Bars (approximately the threshold hearing level).

$$\text{S.P.L.} = 20 \log 10 P / 0.0002 \text{ dB}$$

Where P is the R.M.S sound pressure in microbars.
(1 Bar = 1 atmosphere = 14.5 lb./in² = 194 dB S.P.L.)



| NSC Package Number | Package | Temperature Range | |
|--------------------------|------------------------|--|---|
| | | Commercial 0°C ≤ T _A ≤ +70°C | Military -55°C ≤ T _A ≤ +125°C |
| NO8E | 8-Pin Molded DIP | LM4580CH | |
| MO8A | 8-Pin Surface Mount | LM4580CM | |
| JO8E | 8-Pin Ceramic DIP | | LM4580JL LM4580JL-MIL |
| HO8C | 8-Pin Metal Can | LM4580CH | LM4580H LM4580H-MIL |



LM4250 Programmable Operational Amplifier

General Description

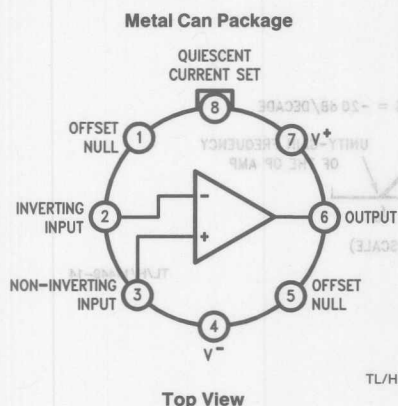
The LM4250 and LM4250C are extremely versatile programmable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product. The device is a truly general purpose operational amplifier.

The LM4250C is identical to the LM4250 except that the LM4250C has its performance guaranteed over a 0°C to $+70^{\circ}\text{C}$ temperature range instead of the -55°C to $+125^{\circ}\text{C}$ temperature range of the LM4250.

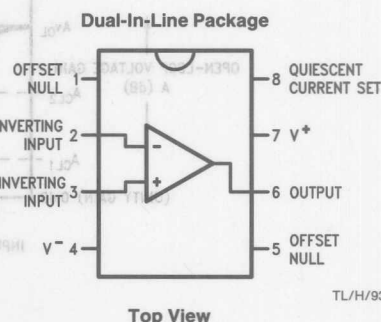
Features

- $\pm 1\text{V}$ to $\pm 18\text{V}$ power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programmable electrical characteristics
- Offset voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

Connection Diagrams



TL/H/9300-2



TL/H/9300-5

Ordering Information

| Temperature Range | | Package | NSC Package Number |
|--|---|---------------------|--------------------|
| Military $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | Commercial $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | | |
| | LM4250CN | 8-Pin Molded DIP | N08E |
| | LM4250CM | 8-Pin Surface Mount | M08A |
| LM4250J LM4250J-MIL | | 8-Pin Ceramic DIP | J08E |
| LM4250H LM4250H-MIL | LM4250CH | 8-Pin Metal Can | H08C |

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 2)

| Parameter | | LM4250 | | LM4250C | |
|---|------------------|--|--|---|--|
| Supply Voltage | $\pm 18\text{V}$ | $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ | | $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | |
| Operating Temp. Range | | $\pm 30\text{V}$ | | $\pm 30\text{V}$ | |
| Differential Input Voltage | | $\pm 15\text{V}$ | | $\pm 15\text{V}$ | |
| Input Voltage (Note 1) | | 150 nA | | 150 nA | |
| I _{SET} Current | | Continuous | | Continuous | |
| Output Short Circuit Duration | | 150°C | | 100°C | |
| T _{JMAX} | | 100°C | | 100°C | |
| H-Package | | 100°C | | 100°C | |
| N-Package | | 100°C | | 100°C | |
| J-Package | | 100°C | | 100°C | |
| M-Package | | 100°C | | 100°C | |
| Power Dissipation at T _A = 25°C | | 500 mW | | 300 mW | |
| H-Package (Still Air) | | 1200 mW | | 1200 mW | |
| (400 LF/Min Air Flow) | | 1000 mW | | 600 mW | |
| N-Package | | 350 mW | | 350 mW | |
| J-Package | | 165°C/W | | 65°C/W | |
| M-Package | | 65°C/W | | 130°C/W | |
| Thermal Resistance (Typical) θ_{JA} | | 108°C/W | | 108°C/W | |
| H-Package (Still Air) | | 190°C/W | | 190°C/W | |
| (400 LF/Min Air Flow) | | 21°C/W | | 21°C/W | |
| N-Package | | -65°C to +150°C | | -65°C to +150°C | |
| J-Package | | 260°C | | 215°C | |
| M-Package | | 215°C | | 220°C | |
| Storage Temperature Range | | 220°C | | 220°C | |
| Soldering Information | | 220°C | | 220°C | |
| Dual-In-Line Package | | 220°C | | 220°C | |
| Soldering (10 seconds) | | 220°C | | 220°C | |
| Small Outline Package | | 220°C | | 220°C | |
| Vapor Phase (60 seconds) | | 220°C | | 220°C | |
| Infrared (15 seconds) | | 220°C | | 220°C | |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | 220°C | | 220°C | |
| ESD tolerance (Note 3) | | 800V | | 800V | |

Note 1: For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

Note 2: Refer to RETS4250X for military specifications.

Note 3: Human body model, 1.5 k Ω in series with 100 pF.

Resistor Biasing

Set Current Setting Resistor to V⁻

| I _{SET} | | | | | |
|--------------------|-------------------|-------------------|-------------------|-----------------|------------------|
| V _S | 0.1 μA | 0.5 μA | 1.0 μA | 5 μA | 10 μA |
| $\pm 1.5\text{V}$ | 25.6 M Ω | 5.04 M Ω | 2.5 M Ω | 492 k Ω | 244 k Ω |
| $\pm 3.0\text{V}$ | 55.6 M Ω | 11.0 M Ω | 5.5 M Ω | 1.09 M Ω | 544 k Ω |
| $\pm 6.0\text{V}$ | 116 M Ω | 23.0 M Ω | 11.5 M Ω | 2.29 M Ω | 1.14 M Ω |
| $\pm 9.0\text{V}$ | 176 M Ω | 35.0 M Ω | 17.5 M Ω | 3.49 M Ω | 1.74 M Ω |
| $\pm 12.0\text{V}$ | 236 M Ω | 47.0 M Ω | 23.5 M Ω | 4.69 M Ω | 2.34 M Ω |
| $\pm 15.0\text{V}$ | 296 M Ω | 59.0 M Ω | 29.5 M Ω | 5.89 M Ω | 2.94 M Ω |

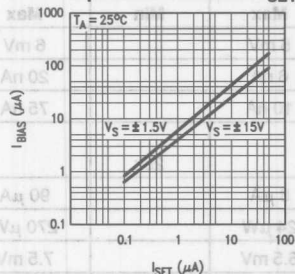
| Parameter | Conditions | $V_S = \pm 1.5V$ | | | |
|--------------------------------|---|---------------------|--------------|----------------------|----------------|
| | | $I_{SET} = 1 \mu A$ | | $I_{SET} = 10 \mu A$ | |
| | | Min | Max | Min | Max |
| V_{OS} | $R_S \leq 100 \text{ k}\Omega, T_A = 25^\circ\text{C}$ | | 3 mV | | 5 mV |
| I_{OS} | $T_A = 25^\circ\text{C}$ | | 3 nA | | 10 nA |
| I_{bias} | $T_A = 25^\circ\text{C}$ | | 7.5 nA | | 50 nA |
| Large Signal Voltage Gain | $R_L = 100 \text{ k}\Omega, T_A = 25^\circ\text{C}$ $V_O = \pm 0.6V, R_L = 10 \text{ k}\Omega$ | 40k | | 50k | |
| Supply Current | $T_A = 25^\circ\text{C}$ | | 7.5 μA | | 80 μA |
| Power Consumption | $T_A = 25^\circ\text{C}$ | | 23 μW | | 240 μW |
| V_{OS} | $R_S \leq 100 \text{ k}\Omega$ | | 4 mV | | 6 mV |
| I_{OS} | $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ | | 5 nA 3 nA | | 10 nA 10 nA |
| I_{bias} | | | 7.5 nA | | 50 nA |
| Input Voltage Range | | $\pm 0.6V$ | | $\pm 0.6V$ | |
| Large Signal Voltage Gain | $V_O = \pm 0.5V, R_L = 100 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$ | 30k | | 30k | |
| Output Voltage Swing | $R_L = 100 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$ | $\pm 0.6V$ | | $\pm 0.6V$ | |
| Common Mode Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$ | 76 dB | | 76 dB | |
| Supply Current | | | 8 μA | | 90 μA |

| Parameter | Conditions | $V_S = \pm 15V$ | | | |
|--------------------------------|--|---------------------|---------------|----------------------|----------------|
| | | $I_{SET} = 1 \mu A$ | | $I_{SET} = 10 \mu A$ | |
| | | Min | Max | Min | Max |
| V_{OS} | $R_S \leq 100 \text{ k}\Omega, T_A = 25^\circ\text{C}$ | | 3 mV | | 5 mV |
| I_{OS} | $T_A = 25^\circ\text{C}$ | | 3 nA | | 10 nA |
| I_{bias} | $T_A = 25^\circ\text{C}$ | | 7.5 nA | | 50 nA |
| Large Signal Voltage Gain | $R_L = 100 \text{ k}\Omega, T_A = 25^\circ\text{C}$ $V_O = \pm 10V, R_L = 10 \text{ k}\Omega$ | 100k | | 100k | |
| Supply Current | $T_A = 25^\circ\text{C}$ | | 10 μA | | 90 μA |
| Power Consumption | $T_A = 25^\circ\text{C}$ | | 300 μW | | 2.7 mW |
| V_{OS} | $R_S \leq 100 \text{ k}\Omega$ | | 4 mV | | 6 mV |
| I_{OS} | $T_A = +125^\circ\text{C}$ $T_A = -55^\circ\text{C}$ | | 25 nA 3 nA | | 25 nA 10 nA |
| I_{bias} | | | 7.5 nA | | 50 nA |
| Input Voltage Range | | $\pm 13.5V$ | | $\pm 13.5V$ | |
| Large Signal Voltage Gain | $V_O = \pm 10V, R_L = 100 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$ | 50k | | 50k | |
| Output Voltage Swing | $R_L = 100 \text{ k}\Omega$ $R_L = 10 \text{ k}\Omega$ | $\pm 12V$ | | $\pm 12V$ | |
| Common Mode Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | $R_S \leq 10 \text{ k}\Omega$ | 76 dB | | 76 dB | |
| Supply Current | | | 11 μA | | 100 μA |
| Power Consumption | | | 330 μW | | 3 mW |

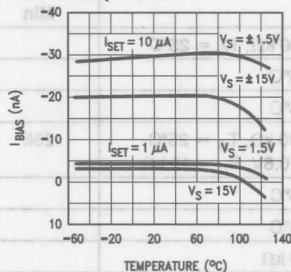
| | | Min | Max | Min | Max |
|--------------------------------|--|-------|--------|-------|--------|
| V _{OS} | R _S ≤ 100 kΩ, T _A = 25°C | | 5 mV | | 6 mV |
| I _{OS} | T _A = 25°C | | 6 nA | | 20 nA |
| I _{bias} | T _A = 25°C | | 10 nA | | 75 nA |
| Large Signal Voltage Gain | R _L = 100 kΩ, T _A = 25°C V _O = ±0.6V, R _L = 10 kΩ | 25k | | 25k | |
| Supply Current | T _A = 25°C | | 8 μA | | 90 μA |
| Power Consumption | T _A = 25°C | | 24 μW | | 270 μW |
| V _{OS} | R _S ≤ 10 kΩ | | 6.5 mV | | 7.5 mV |
| I _{OS} | | | 8 nA | | 25 nA |
| I _{bias} | | | 10 nA | | 80 nA |
| Input Voltage Range | | ±0.6V | | ±0.6V | |
| Large Signal Voltage Gain | V _O = ±0.5V, R _L = 100 kΩ R _L = 10 kΩ | 25k | | 25k | |
| Output Voltage Swing | R _L = 100 kΩ R _L = 10 kΩ | ±0.6V | | ±0.6V | |
| Common Mode Rejection Ratio | R _S ≤ 10 kΩ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | R _S ≤ 10 kΩ | 74 dB | | 74 dB | |
| Supply Current | | | 8 μA | | 90 μA |
| Power Consumption | | | 24 μW | | 270 μW |

| Parameter | Conditions | V _S = ±15V | | | |
|--------------------------------|---|-------------------------|--------|--------------------------|--------|
| | | I _{SET} = 1 μA | | I _{SET} = 10 μA | |
| | | Min | Max | Min | Max |
| V _{OS} | R _S ≤ 100 kΩ, T _A = 25°C | | 5 mV | | 6 mV |
| I _{OS} | T _A = 25°C | | 6 nA | | 20 nA |
| I _{bias} | T _A = 25°C | | 10 nA | | 75 nA |
| Large Signal Voltage Gain | R _L = 100 kΩ, T _A = 25°C V _O = ±10V, R _L = 10 kΩ | 60k | | 60k | |
| Supply Current | T _A = 25°C | | 11 μA | | 100 μA |
| Power Consumption | T _A = 25°C | | 330 μW | | 3 mW |
| V _{OS} | R _S ≤ 100 kΩ | | 6.5 mV | | 7.5 mV |
| I _{OS} | | | 8 nA | | 25 nA |
| I _{bias} | | | 10 nA | | 80 nA |
| Input Voltage Range | | ±13.5V | | ±13.5V | |
| Large Signal Voltage Gain | V _O = ±10V, R _L = 100 kΩ R _L = 10 kΩ | 50k | | 50k | |
| Output Voltage Swing | R _L = 100 kΩ R _L = 10 kΩ | ±12V | | ±12V | |
| Common Mode Rejection Ratio | R _S ≤ 10 kΩ | 70 dB | | 70 dB | |
| Supply Voltage Rejection Ratio | R _S ≤ 10 kΩ | 74 dB | | 74 dB | |
| Supply Current | | | 11 μA | | 100 μA |
| Power Consumption | | | 330 μW | | 3 mW |

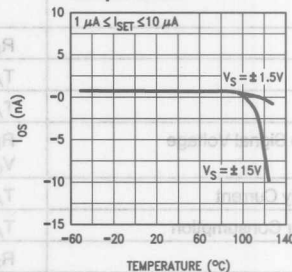
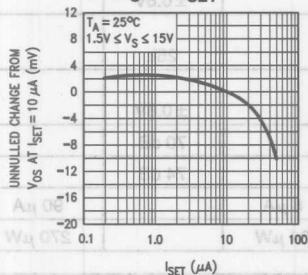
Typical Performance Characteristics

Input Bias Current vs I_{SET} 

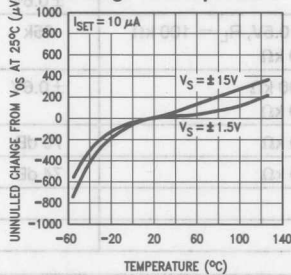
Input Bias Current vs Temperature



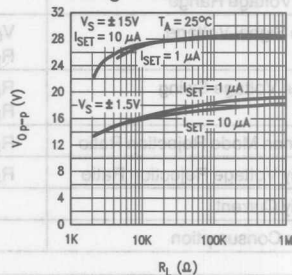
Input Offset Current vs Temperature

Unnull'd Input Offset Voltage Change vs I_{SET} 

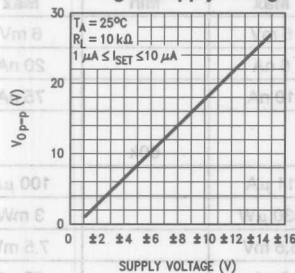
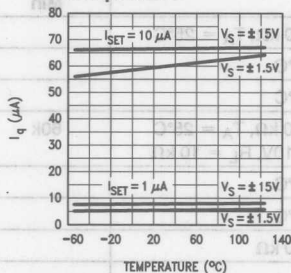
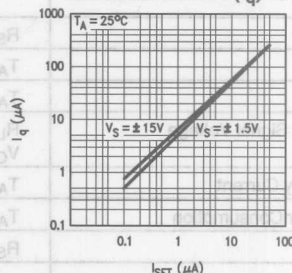
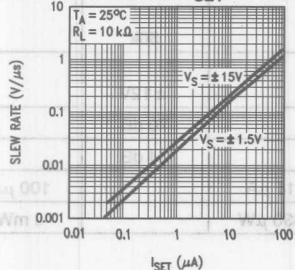
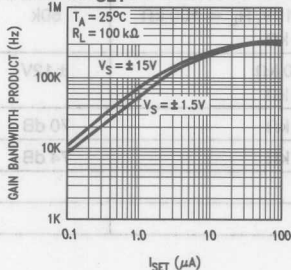
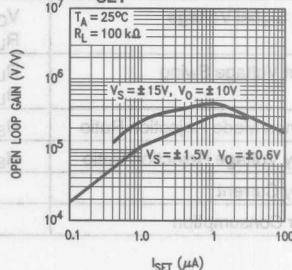
Unnull'd Input Offset Voltage Change vs Temperature



Peak to Peak Output Voltage Swing vs Load Resistance

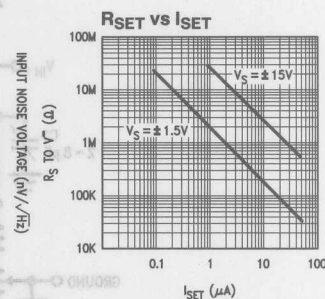
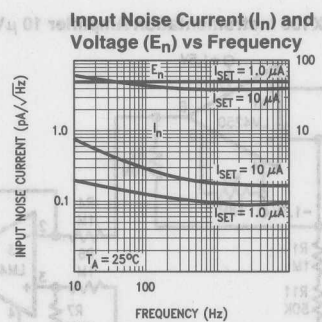
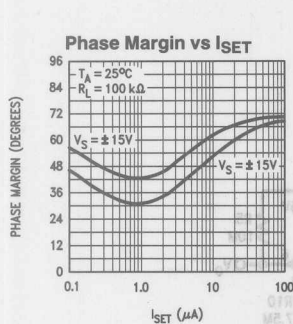


Peak to Peak Output Voltage Swing vs Supply Voltage

Quiescent Current (I_Q) vs TemperatureQuiescent Current (I_Q) vs I_{SET} Slew Rate vs I_{SET} Gain Bandwidth Product vs I_{SET} Open Loop Voltage Gain vs I_{SET} 

TL/H/9300-6

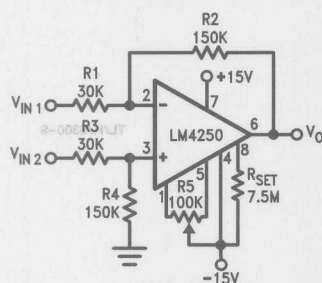
Typical Performance Characteristics (Continued)



TL/H/9300-7

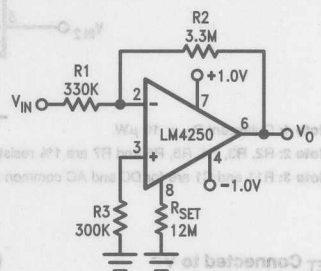
Typical Applications

X5 Difference Amplifier

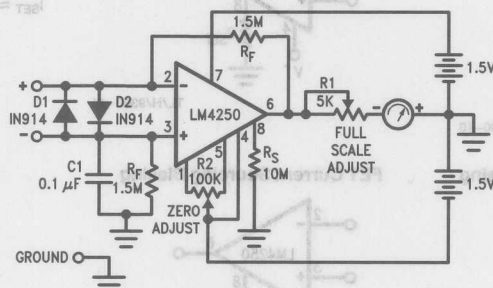
Quiescent $P_D = 0.6\text{ mW}$

TL/H/9300-3

500 Nano-Watt X10 Amplifier

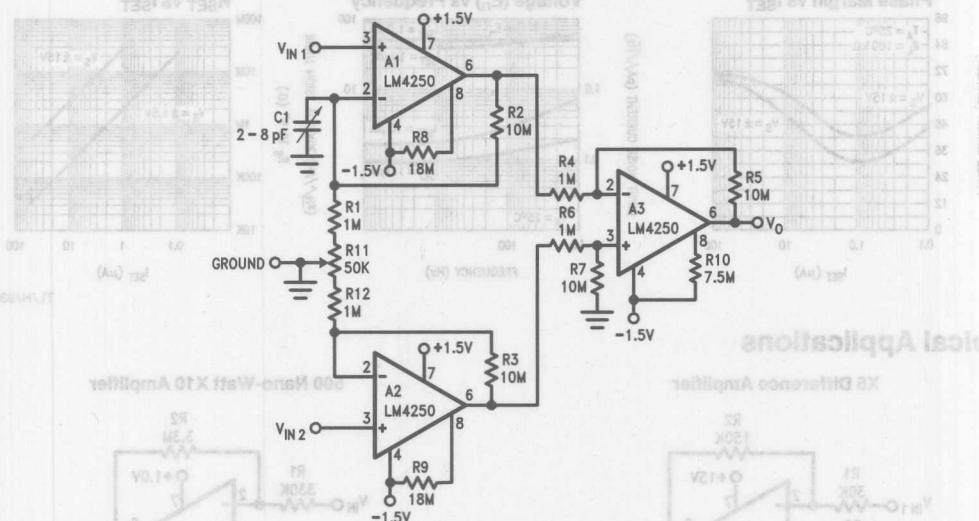
Quiescent $P_D = 500\text{ nW}$

TL/H/9300-4

Floating Input Meter Amplifier
100 nA Full ScaleQuiescent $P_D = 1.8\text{ }\mu\text{W}$ *Meter movement (0–100 μA , 2 k Ω) marked for 0–100 nA full scale.

TL/H/9300-8

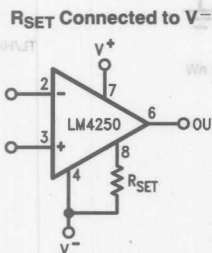
Typical Applications (Continued)

X100 Instrumentation Amplifier 10 μ W

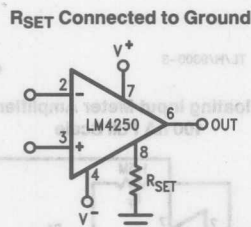
Note 1: Quiescent $P_D = 10 \mu W$.

Note 2: R2, R3, R4, R5, R6 and R7 are 1% resistors.

Note 3: R11 and C1 are for DC and AC common mode rejection adjustments.



TL/H/9300-10



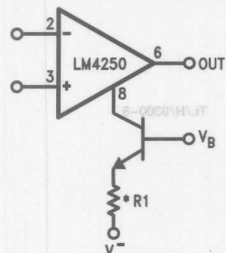
TL/H/9300-11

I_{SET} Equations:

$$I_{SET} \approx \frac{V^+ + |V^-| - 0.5}{R_{SET}} \quad \text{where } R_{SET} \text{ is connected to } V^+.$$

$$I_{SET} \approx \frac{V^+ - 0.5}{R_{SET}} \quad \text{where } R_{SET} \text{ is connected to ground.}$$

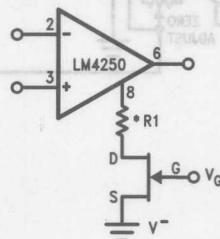
Transistor Current Sourcing Biasing



*R1 limits I_{SET} maximum

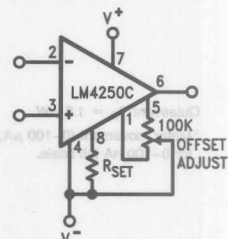
TL/H/9300-12

FET Current Sourcing Biasing



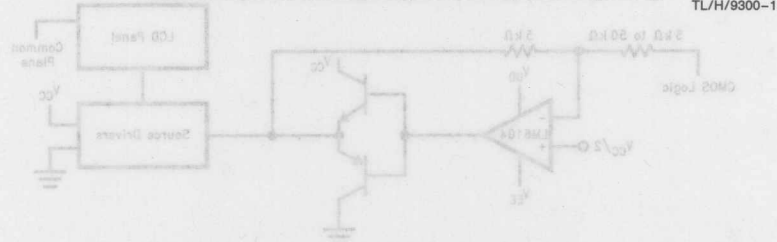
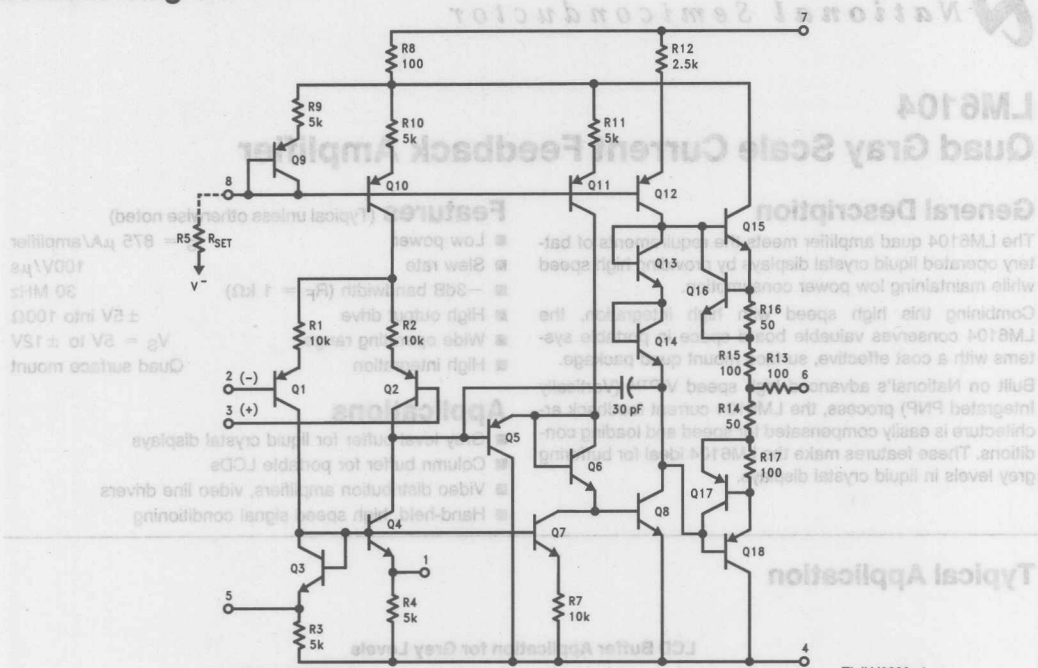
TL/H/9300-13

Offset Null Circuit



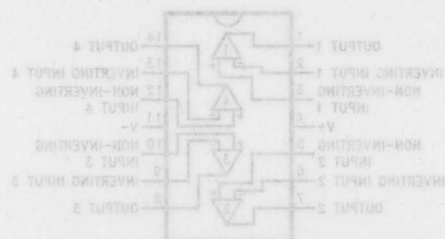
TL/H/9300-14

Schematic Diagram



TL/H/9300-1

Connection Diagram



Order Number LM6104M
See MS Package Number M14A

TL/H/9300-2

LM4250

1

LM6104

Quad Gray Scale Current Feedback Amplifier

General Description

The LM6104 quad amplifier meets the requirements of battery operated liquid crystal displays by providing high speed while maintaining low power consumption.

Combining this high speed with high integration, the LM6104 conserves valuable board space in portable systems with a cost effective, surface mount quad package.

Built on National's advanced high speed VIPTM (Vertically Integrated PNP) process, the LM6104 current feedback architecture is easily compensated for speed and loading conditions. These features make the LM6104 ideal for buffering grey levels in liquid crystal displays.

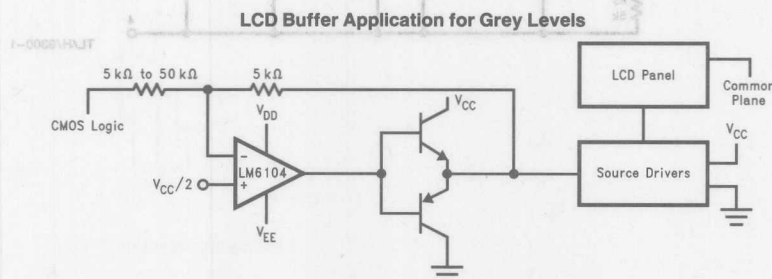
Features (Typical unless otherwise noted)

- Low power $I_S = 875 \mu A/\text{amplifier}$
- Slew rate $100V/\mu s$
- $-3dB$ bandwidth ($R_F = 1 k\Omega$) $30 MHz$
- High output drive $\pm 5V$ into 100Ω
- Wide operating range $V_S = 5V$ to $\pm 12V$
- High integration Quad surface mount

Applications

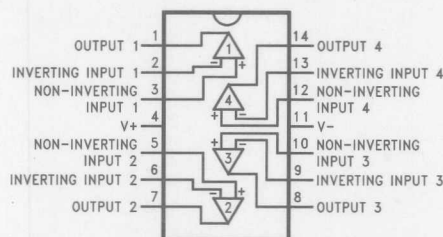
- Grey level buffer for liquid crystal displays
- Column buffer for portable LCDs
- Video distribution amplifiers, video line drivers
- Hand-held, high speed signal conditioning

Typical Application



TL/H/11979-1

Connection Diagram



TL/H/11979-2

Order Number LM6104M
See NS Package Number M14A

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage 24V
Differential Input Voltage $\pm 6V$
Input Voltage \pm Supply Voltage
Inverting Input Current 15 mA
Soldering Information 215°C
Vapor Phase (60s) 220°C
Infrared (15s)

Maximum Junction Temperature

150°C

ESD Rating (Note 2)

2000V

Operating Ratings

Supply Voltage Range 4.75V to 24V
Junction Temperature Range (Note 3) $-20^{\circ} \leq T_J \leq +80^{\circ}C$
LM6104M

Electrical Characteristics

The following specifications apply for $V_+ = 8V$, $V_- = -5V$, $R_L = R_F = 2 k\Omega$ and $0^{\circ} \leq T_J \leq 60^{\circ}C$ unless otherwise noted.

| Symbol | Parameter | Conditions | LM6104M | | Units |
|----------|----------------------------------|--|---------------------|--------------------|----------------|
| | | | Typical (Note 4) | Limits (Note 5) | |
| V_{OS} | Input Offset Voltage | | 10 | 30 | mV max |
| I_B | Inverting Input Bias Current | | 5.0 | 20 | μA max |
| | Non-Inverting Input Bias Current | | 0.5 | 2 | μA max |
| I_S | Supply Current | $V_O = 0V$ | 3.5 | 4.0 | mA max |
| I_{SC} | Output Source Current | $V_O = 0V$ $I_{IN(-)} = -100 \mu A$ | 60 | 45 | mA min |
| | Output Sink Current | $V_O = 0V$ $I_{IN(-)} = 100 \mu A$ | 60 | 45 | mA min |
| V_O | Positive Output Swing | $I_{IN(-)} = -100 \mu A$ | 6.5 | 6.1 | V min |
| | Negative Output Swing | $I_{IN(-)} = 100 \mu A$ | -3.5 | -3.1 | V max |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 4$ to $\pm 10V$ | 70 | 60 | dB min |
| | | 100 mV pp @ 100 kHz | 40 | 30 | dB min |
| R_T | Transresistance | | 10 | 5 | M Ω min |
| SR | Slew Rate | (Note 6) | 100 | 55 | V/ μs min |
| BW | Bandwidth | $A_V = -1$ $R_{IN} = R_F = 2 k\Omega$ | 7.5 | 5.0 | MHz |
| | Amp-to-Amp Isolation | $R_L = 2 k\Omega$ $F = 1 MHz$ | 60 | | dB |
| CMVR | Common Mode Voltage Range | $V_+ - 1.4V$ $V_- + 1.4V$ | | | V |
| CMRR | Common Mode Rejection Ratio | | 60 | | dB |
| t_S | Settling Time | 0.05%, 5V Step, $A_V = -1$ $R_F = R_S = 2 k\Omega$, $V_S = \pm 5V$ | 240 | | ns |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under the conditions.

Note 2: Human body model 1.5 k Ω and 100 pF. This is a class 2 device rating.

Note 3: Thermal resistance of the SO package is 98°C/W. When operating at $T_A = 80^{\circ}C$, maximum power dissipation is 700 mW.

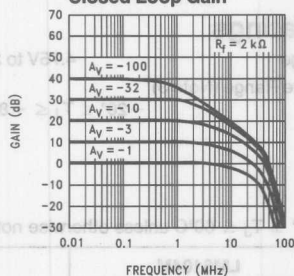
Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at operating temperature extremes.

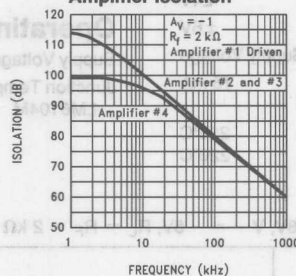
Note 6: $A_V = -1$ with $R_{IN} = R_F = 2 k\Omega$. Slew rate is calculated from the 25% to the 75% point on both rising and falling edges. Output swing is $-0.6V$ to $+5.6V$ and $5.6V$ to $0.6V$.

Typical Performance Characteristics

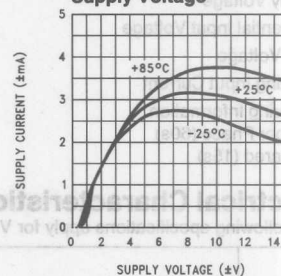
Frequency Response vs Closed Loop Gain



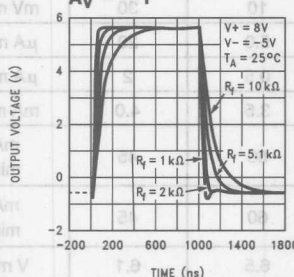
Amplifier to Amplifier Isolation



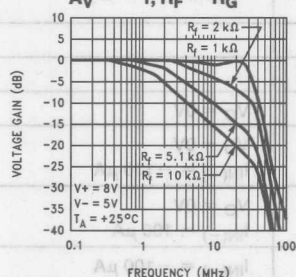
Supply Current vs Supply Voltage



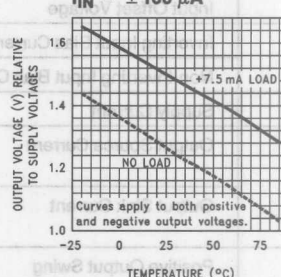
Large Signal Pulse Response



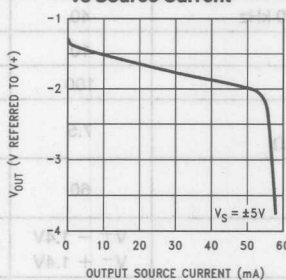
Frequency Response vs Rf



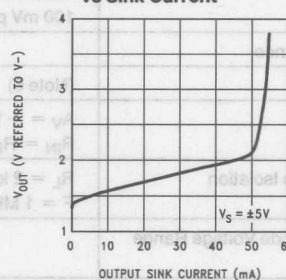
VOUT Referred to Supplies



LM6104 Output Voltage vs Source Current



LM6104 Output Voltage vs Sink Current



Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. Operating ratings indicate conditions for which the device is intended to be functional, but device parameters specifications may not be guaranteed under these conditions.

Note 2: Human body model, 1.5 pF and 100 pF, time is a class 2 device rating.

Note 3: Thermal resistance of the 8-pin package is 88°C/W. When operating at $T_A = 88^\circ \text{C}$, maximum power dissipation is 700 mW.

Note 4: Typical values represent the most likely parameter norm.

Note 5: All limits guaranteed at operating temperature extremes.

Note 6: $A_v = -1$ with $R_{IN} = R_f = 2 \text{ k}\Omega$. Slew rate is calculated from the 20% to 80% point on both rising and falling edges. Output swing is -0.8 V to $+2.8 \text{ V}$ into $2 \text{ k}\Omega$ to 0.5 V .

LM6104 1/81 Form 1

Bandwidth and slew rate are inversely proportional to the value of R_F (see typical curve Frequency Response vs R_F). This makes the amplifier especially easy to compensate for a desired pulse response (see typical curve Large Signal Pulse Response). Increased capacitive load driving capability is also achieved by increasing the value of R_F .

CAPACITIVE FEEDBACK

It is common to place a small lead capacitor in parallel with feedback resistance to compensate voltage feedback amplifiers. Do not place a capacitor across R_F to limit the bandwidth of current feedback amplifiers. The dynamic impedance of capacitors in the feedback path of the LM6104, as with any current feedback amplifier, will cause instability.



LM6118/LM6218

Fast Settling Dual Operational Amplifiers

General Description

The LM6118 series are monolithic fast-settling unity-gain-compensated dual operational amplifiers with ± 20 mA output drive capability. The PNP input stage has a typical bias current of 200 nA, and the operating supply voltage is ± 5 V to ± 20 V.

These dual op amps use slew enhancement with special mirror circuitry to achieve fast response and high gain with low total supply current.

The amplifiers are built on a junction-isolated VIPTM (Vertically Integrated PNP) process which produces fast PNP's that complement the standard NPN's.

Features

- Low offset voltage
- 0.01% settling time
- Slew rate $A_V = -1$
- Slew rate $A_V = +1$
- Gain bandwidth
- Total supply current
- Output drives 50Ω load (± 1 V)

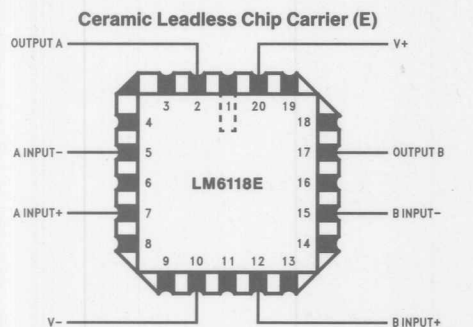
Typical

0.2 mV
400 ns
140 V/ μ s
75 V/ μ s
17 MHz
5.5 mA

Applications

- D/A converters
- Fast integrators
- Active filters

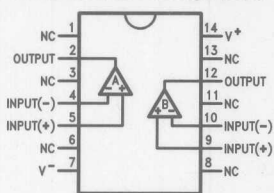
Connection Diagrams and Order Information



Order Number LM6118E/883*
See NS Package Number E20A

TL/H/10254-24

Small Outline Package (WM)

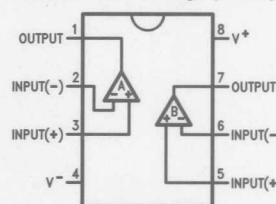


Top View

TL/H/10254-3

Order Number LM6218AWM or LM6218WM
See NS Package Number M14B

Dual-In-Line Package (J or N)

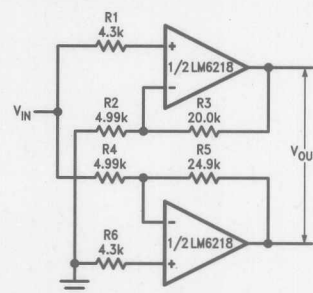


Top View

TL/H/10254-4

Order Number LM6118N, LM6118J/883*,
LM6218AN or LM6218N
See NS Package Number J08A or N08E

Typical Applications



Single-ended input to differential output
 $A_V = 10$, BW = 3.2 MHz
40 Vpp Response = 1.4 MHz
 $V_S = \pm 15$ V

TL/H/10254-1

Wide-Band, Fast-Settling
40 Vpp Amplifier

*Available per SMD #5962-9156501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-------------------------------------|--------------------|
| Total Supply Voltage | 42V |
| Input Voltage | (Note 2) |
| Differential Input Current (Note 3) | ±10 mA |
| Output Current (Note 4) | Internally Limited |
| Power Dissipation (Note 5) | 500 mW |

| | |
|--|-----------------|
| ESD Tolerance (C = 100 pF, R = 1.5 kΩ) | ±2 kV |
| Junction Temperature | 150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Operating Temp. Range

| | |
|---------|-----------------|
| LM6118 | -55°C to +125°C |
| LM6218A | -40°C to +85°C |
| LM6218 | -40°C to +85°C |

Electrical Characteristics $\pm 5V \leq V_S \leq \pm 20V$, $V_{CM} = 0V$, $V_{OUT} = 0V$, $I_{OUT} = 0A$, unless otherwise specified. Limits with standard type face are for $T_J = 25^\circ C$, and **Bold Face Type** are for **Temperature Extremes**.

| Parameter | Conditions | Typ 25°C | LM6118 Limits (Notes 6 & 7) | LM6218A Limits (Note 6) | LM6218 Limits (Note 6) | Units |
|---------------------------------------|--|-------------|-----------------------------------|-------------------------------|------------------------------|------------|
| Input Offset Voltage | $V_S = \pm 15V$ | 0.2 | 1 2 | 1 2 | 3 4 | mV (max) |
| Input Offset Voltage | $V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$ | 0.3 | 1.5 2.5 | 1.5 2.5 | 3.5 4.5 | mV (max) |
| Input Offset Current | $V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$ | 20 | 50 250 | 50 100 | 100 200 | nA (max) |
| Input Bias Current | $V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$ | 200 | 350 950 | 350 950 | 500 1250 | nA (max) |
| Input Common Mode Rejection Ratio | $V^- + 3V \leq V_{CM} \leq V^+ - 3.5V$ $V_S = \pm 20V$ | 100 | 90 85 | 90 85 | 80 75 | dB (min) |
| Positive Power Supply Rejection Ratio | $V^- = -15V$ $5V \leq V^+ \leq 20V$ | 100 | 90 85 | 90 85 | 80 75 | dB (min) |
| Negative Power Supply Rejection Ratio | $V^+ = 15V$ $-20V \leq V^- \leq -5V$ | 100 | 90 85 | 90 85 | 80 75 | dB (min) |
| Large Signal Voltage Gain | $V_{out} = \pm 15V$ $V_S = \pm 20V$ $R_L = 10k$ | 500 | 150 100 | 150 100 | 100 70 | V/mV (min) |
| | $V_{out} = \pm 10V$ $V_S = \pm 15V$ $R_L = 500$ (±20 mA) | 200 | 50 30 | 50 30 | 40 25 | V/mV (min) |
| V_O Output Voltage Swing | Supply = ±20V $R_L = 10k$ | 17.3 | ±17 | ±17 | ±17 | V (min) |
| Total Supply Current | $V_S = \pm 15V$ | 5.5 | 7 7.5 | 7 7.5 | 7 7.5 | mA (max) |
| Output Current Limit | $V_S = \pm 15V$, Pulsed | 65 | 100 | 100 | 100 | mA (max) |
| Slew Rate, $A_v = -1$ | $V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF | 140 | 100 50 | 100 50 | 100 50 | V/μs (min) |
| Slew Rate, $A_v = +1$ | $V_S = \pm 15V$, $V_{out} = \pm 10V$ $R_S = R_f = 2k$, $C_f = 10$ pF | 75 | 50 30 | 50 30 | 50 30 | V/μs (min) |
| Gain-Bandwidth Product | $V_S = \pm 15V$, $f_o = 200$ kHz | 17 | 14 | 14 | 13 | MHz (min) |
| 0.01% Settling Time $A_v = -1$ | $\Delta V_{out} = 10V$, $V_S = \pm 15V$, $R_S = R_f = 2k$, $C_f = 10$ pF | 400 | | | | ns |
| Input Capacitance | Inverter | 5 | | | | pF |
| | Follower | 3 | | | | pF |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage range is $(V^+ - 1V)$ to (V^-) .

Note 3: The inputs are shunted with three series-connected diodes back-to-back for input differential clamping. Therefore differential input voltages greater than about 1.8V will cause excessive current to flow unless limited to less than 10 mA.

Note 4: Current limiting protects the output from a short to ground or any voltage less than the supplies. With a continuous overload, the package dissipation must be taken into account and heat sinking provided when necessary.

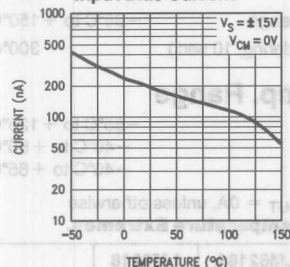
Note 5: Devices must be derated using a thermal resistance of 90°C/W for the N, J and WM packages.

Note 6: Limits are guaranteed by testing or correlation.

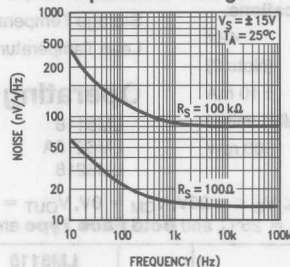
Note 7: A military RETS specification is available on request. At the time of printing, LM6118J/883 and LM6118E/883 RETS spec complied with the **Boldface** limits in this column.

Typical Performance Characteristics

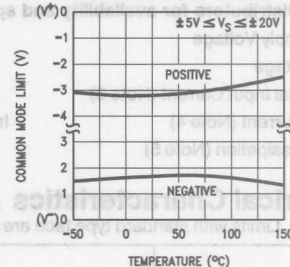
Input Bias Current



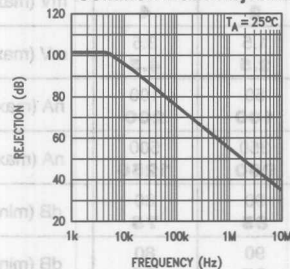
Input Noise Voltage



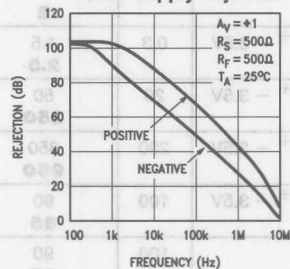
Common Mode Limits



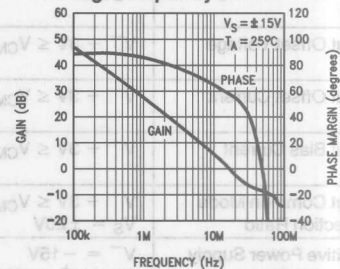
Common Mode Rejection



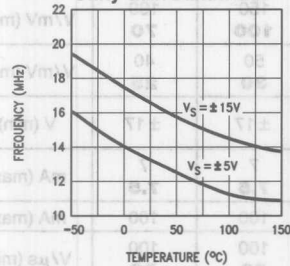
Power Supply Rejection



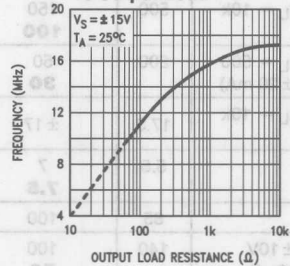
Frequency Response High Frequency



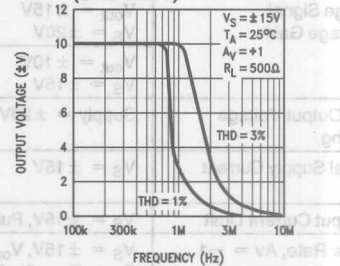
Unity Gain Bandwidth



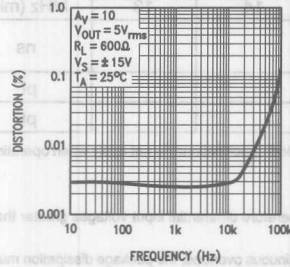
Unity Gain Bandwidth vs Output Load



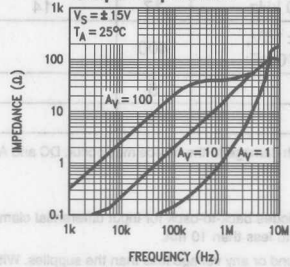
Large Signal Response (Sine Wave)



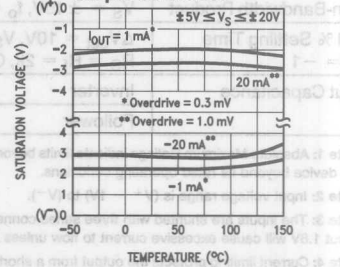
Total Harmonic Distortion

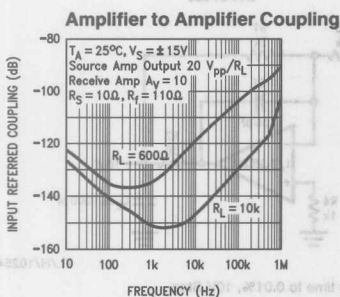
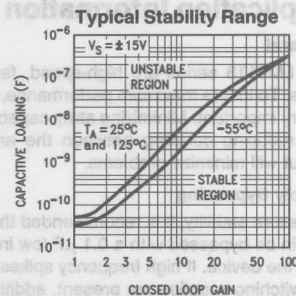
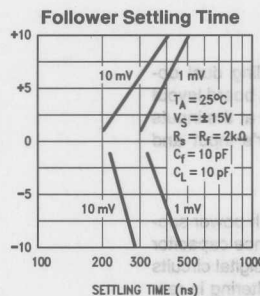
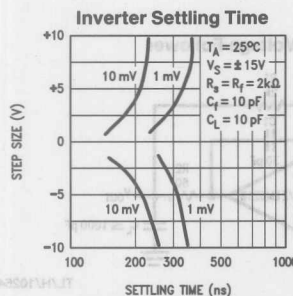
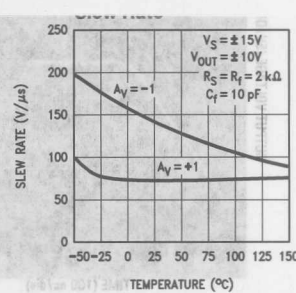
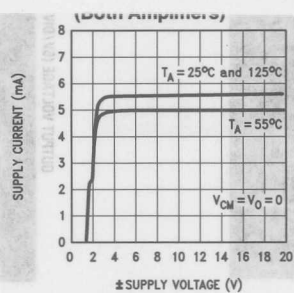
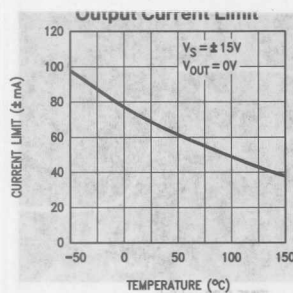
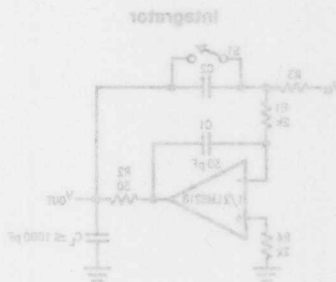
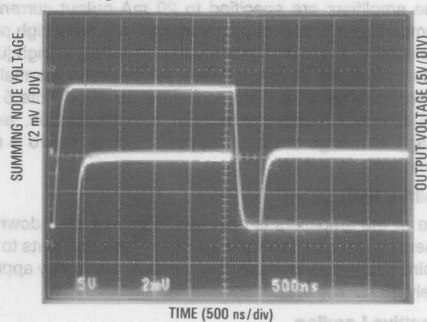


Output Impedance

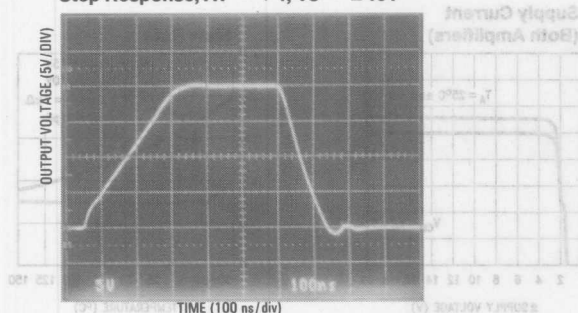


Output Saturation

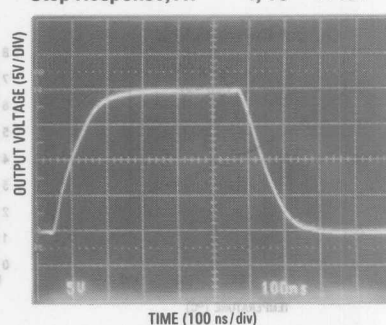


Settling Time, $V_S = \pm 15V$ 

Typical Performance Characteristics (Continued)

Step Response, $A_v = +1$, $V_s = \pm 15V$ 

TL/H/10254-8

Step Response, $A_v = -1$, $V_s = \pm 15V$ 

TL/H/10254-9

Application Information

General

The LM6118 series are high-speed, fast-settling dual op-amps. To insure maximum performance, circuit board layout is very important. Minimizing stray capacitance at the inputs and reducing coupling between the amplifier's input and output will minimize problems.

Supply Bypassing

To assure stability, it is recommended that each power supply pin be bypassed with a $0.1 \mu F$ low inductance capacitor near the device. If high frequency spikes from digital circuits or switching supplies are present, additional filtering is recommended. To prevent these spikes from appearing at the output, R-C filtering of the supplies near the device may be necessary.

Power Dissipation

These amplifiers are specified to 20 mA output current. If accompanied with high supply voltages, relatively high power dissipation in the device will occur, resulting in high junction temperatures. In these cases the package thermal resistance must be taken into consideration. (See Note 5 under Electrical Characteristics.) For high dissipation, an N package with large areas of copper on the pc board is recommended.

Amplifier Shut Down

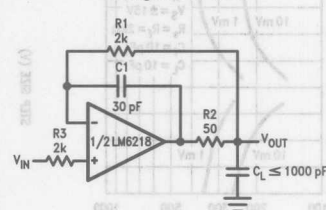
If one of the amplifiers is not used, it can be shut down by connecting both the inverting and non-inverting inputs to the V^- pin. This will reduce the power supply current by approximately 25%.

Capacitive Loading

Maximum capacitive loading is about 50 pF for a closed-loop gain of +1, before the amplifier exhibits excessive ringing and becomes unstable. A curve showing maximum capacitive loads, with different closed-loop gains, is shown in the Typical Performance Characteristics section.

To drive larger capacitive loads at low closed-loop gains, isolate the amplifier output from the capacitive load with 50Ω . Connect a small capacitor directly from the amplifier output to the inverting input. The feedback loop is closed from the isolated output with a series resistor to the inverting input.

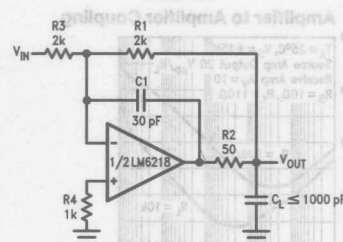
Voltage Follower



TL/H/10254-10

For $C_L = 1000$ pF, Small signal BW = 5 MHz20 V_{p-p} BW = 500 kHz

Inverter

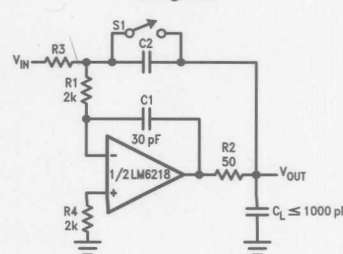


TL/H/10254-11

Settling time to 0.01%, 10V Step

For $C_L = 1000$ pF, settling time ≈ 1500 nsFor $C_L = 300$ pF, settling time ≈ 500 ns

Integrator



TL/H/10254-12

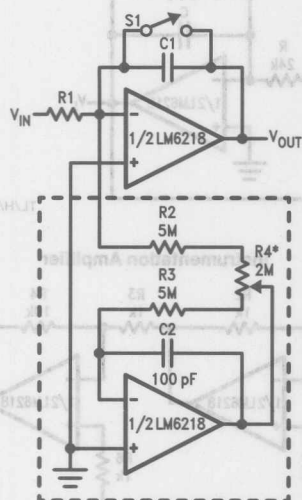
Application Information (Continued)

Examples of unity gain connections for a voltage follower, inverter, and integrator driving capacitive loads up to 1000 pF are shown here. Different R1–C1 time constants and capacitive loads will have an effect on settling times.

Input Bias Current Compensation

Input bias current of the first op amp can be reduced or balanced out by the second op amp. Both amplifiers are laid out in mirror image fashion and in close proximity to each other, thus both input bias currents will be nearly identical

Bias Current Compensation

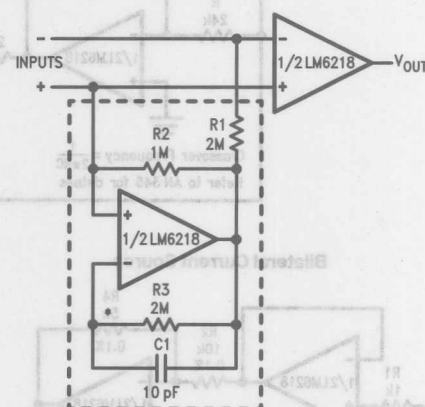


*adjust for zero integrator drift

(a) Inverting Input Bias Compensation for Integrator Application

and will track with temperature. With both op amp inputs at the same potential, a second op amp can be used to convert bias current to voltage, and then back to current feeding the first op amp using large value resistors to reduce the bias current to the level of the offset current.

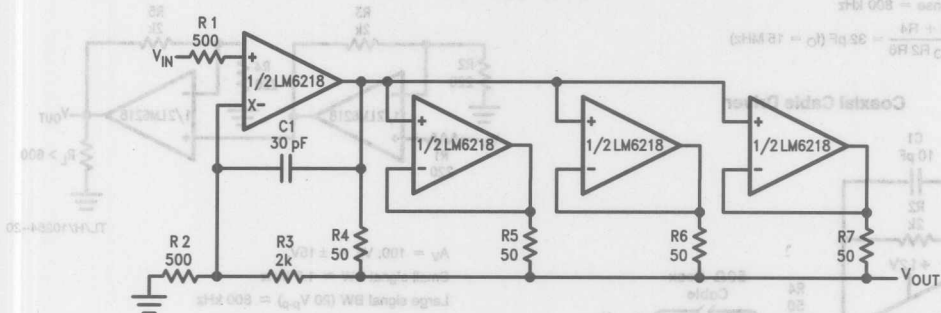
Examples are shown here for an inverting application, (a) where the inputs are at ground potential, and a second circuit (b) for compensating bias currents for both inputs.



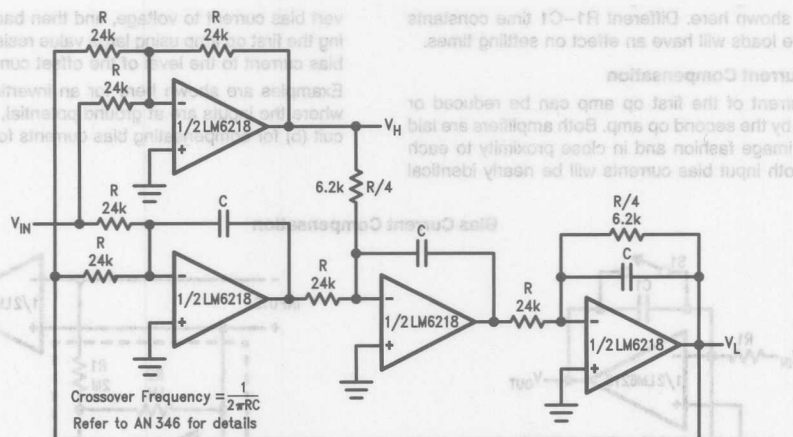
*mount resistor close to input pin to minimize stray capacitance

(b) Compensation to Both Inputs

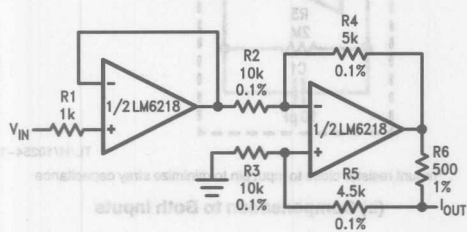
Amplifier/Parallel Buffer



$A_V = +5$, $I_{OUT} \leq 80$ mA
 $V_S = \pm 15$ V, $C_L \leq 0.01$ μ F
 Large and small signal B.W. = 1.3 MHz (THD = 3%)



TL/H/10254-16

Bilateral Current Source

TL/H/10254-17

$$V_S = \pm 15V, -10 \leq V_{IN} \leq 10V$$

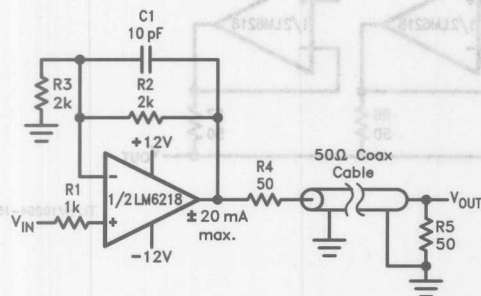
$$\frac{I_{OUT}}{V_{IN}} = \frac{R_4}{R_2 R_6} = \frac{1 \text{ mA}}{1V}$$

$$\text{Output dynamic range} = 10V - R_6 |I_{OUT}|$$

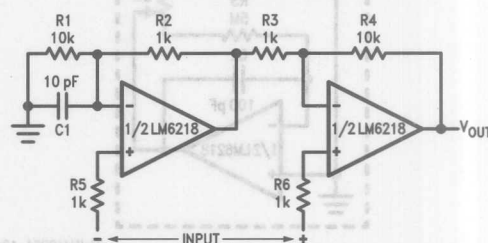
$$R_L = 500\Omega, \text{ small signal BW} = 6 \text{ MHz}$$

$$\text{Large signal response} = 800 \text{ kHz}$$

$$C_{out \text{ equiv.}} = \frac{R_2 + R_4}{2\pi f_O R_2 R_6} = 32 \text{ pF} (f_O = 15 \text{ MHz})$$

Coaxial Cable Driver

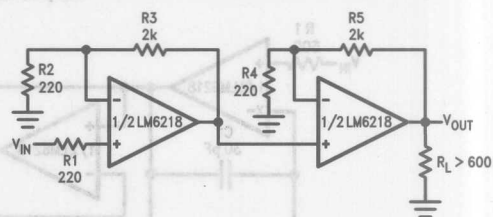
TL/H/10254-19

Small signal (200 mV_{p-p}) BW ≈ 5 MHz**Instrumentation Amplifier**

TL/H/10254-18

$$A_V = 10, V_S = \pm 15V, \text{ All resistors } 0.01\%$$

$$\text{Small signal and large signal (20 V}_{p-p}\text{) B.W.} \approx 800 \text{ kHz}$$

150 MHz Gain-Bandwidth Amplifier

TL/H/10254-20

$$A_V = 100, V_S = \pm 15V,$$

$$\text{Small signal BW} \approx 1.5 \text{ MHz}$$

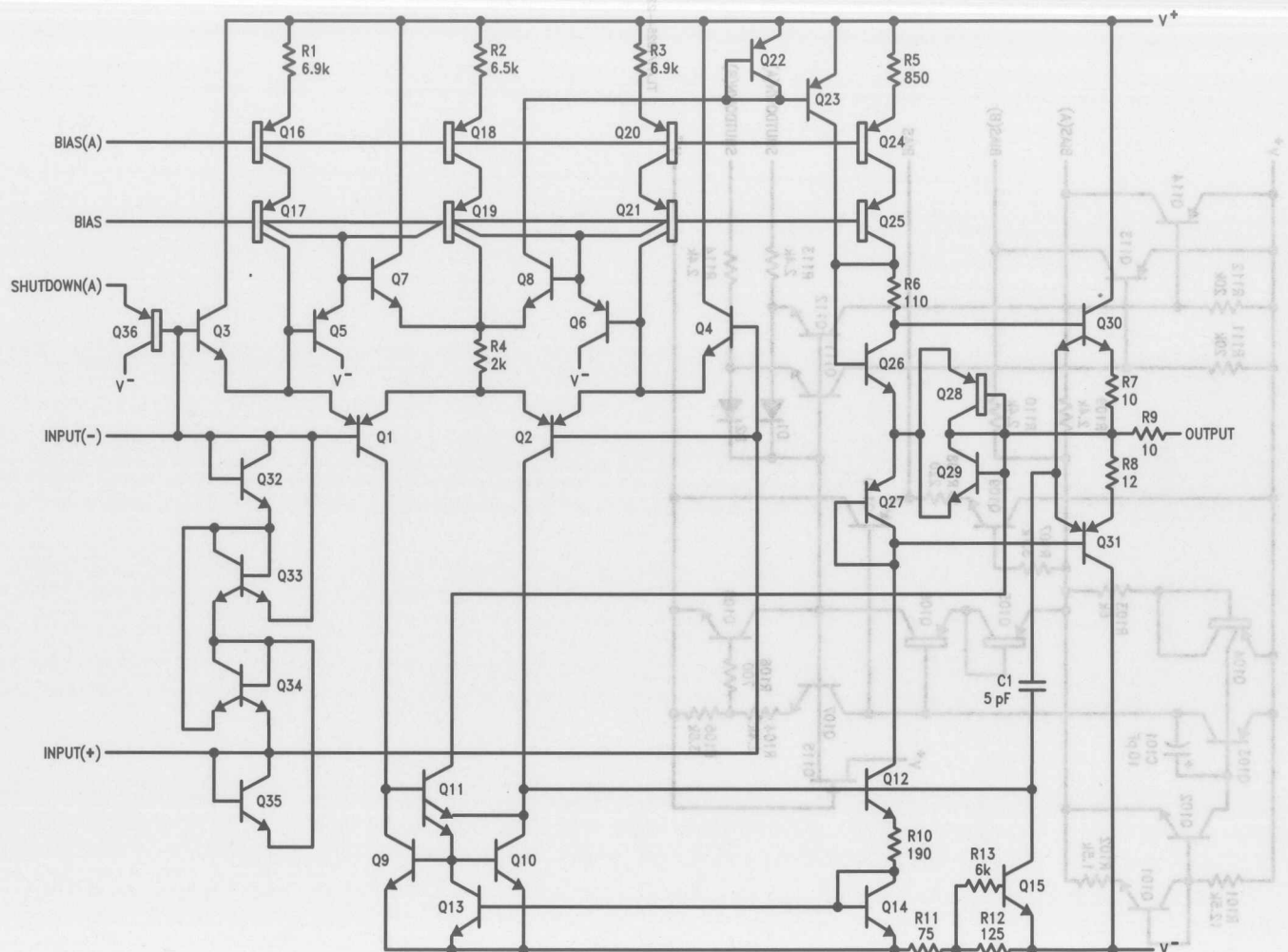
$$\text{Large signal BW (20 V}_{p-p}\text{) } \approx 800 \text{ kHz}$$

Schematic Diagram

1/2 LM6118 (Op Amp A)

(continued) internal circuitry

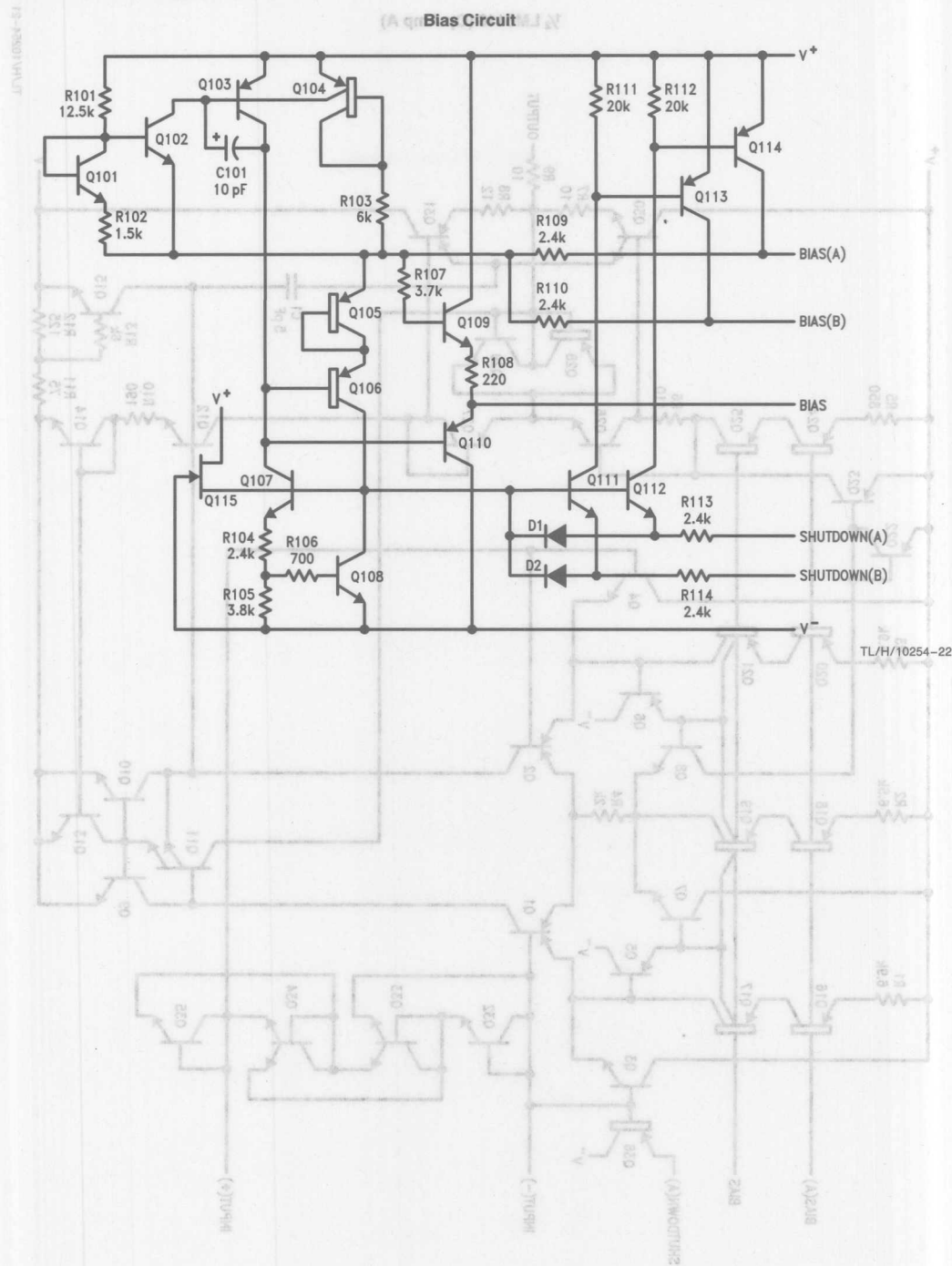
TL/H/10254-21



LM6118/LM6218

Schematic Diagram (Continued)

Schematic Diagram



LM6132 Dual and LM6134 Quad High Speed/Low Power 7 MHz Rail-to-Rail I/O Operational Amplifiers

General Description

Using patent pending circuit topologies, the LM6132/34 provides new levels of speed vs. power performance in applications where low voltage supplies or power limitations previously made compromise necessary. With only 550 $\mu\text{A}/\text{amp}$ supply current, the 7 MHz bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

In addition, the LM6132/34 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6132/34 can also drive large capacitive loads without oscillating.

Operating on supplies of 1.8 to over 24 volts, the LM6132/34 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

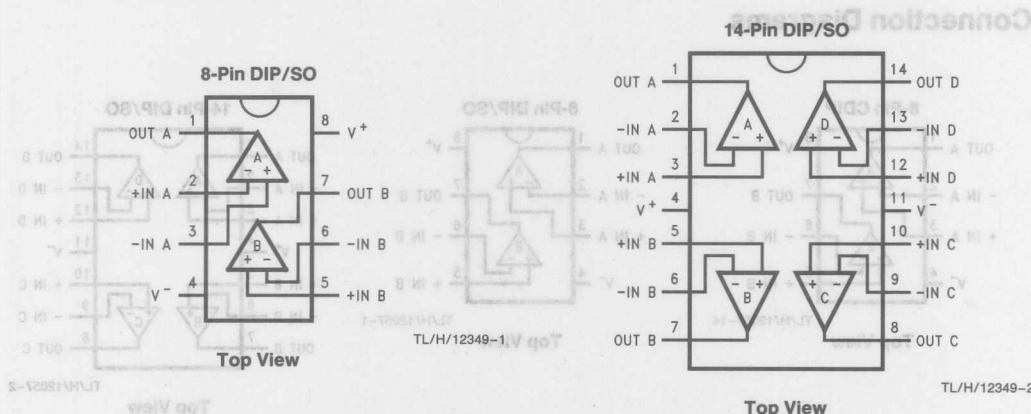
Features (For 5V Supply)

- Rail-to-rail input CMVR -0.25V to 5.25V (Max/Min)
- Rail-to-rail output swing 0.01V to 4.99V (Max/Min)
- Wide gain-bandwidth at 50 KHz 7 MHz (Typ)
- Slew rate $12\text{ V}/\mu\text{s}$ (Typ)
- Low supply current $550\text{ }\mu\text{A}/\text{amp}$ (Typ)
- Wide supply range 1.8V to 24V
- CMRR 107 dB (Typ)
- Gain 108 dB (Typ) with $R_L = 10\text{K}$
- PSRR 87 dB (Typ)

Applications

- Battery operated instrumentation
- 5V instrumentation
- Portable scanners
- Wireless communications

Connection Diagrams



Ordering Information

| Package | Temperature Range | |
|----------------------|----------------------|-------------|
| | Industrial | NSC Drawing |
| 8-Pin Molded DIP | LM6132AIN, LM6132BIN | N08E |
| 8-Pin Small Outline | LM6132AIM, LM6132BIM | M08A |
| 14-Pin Molded DIP | LM6134AIN, LM6134BIN | N14A |
| 14-Pin Small Outline | LM6134AIM, LM6134BIM | M14A |

LM6142 Dual and LM6144 Quad High Speed/Low Power 17 MHz Rail-to-Rail Input-Output Operational Amplifiers

General Description

Using patent pending new circuit topologies, the LM6142/44 provides new levels of performance in applications where low voltage supplies or power limitations previously made compromise necessary. Operating on supplies of 1.8V to over 24V, the LM6142/44 is an excellent choice for battery operated systems, portable instrumentation and others.

The greater than rail-to-rail input voltage range eliminates concern over exceeding the common-mode voltage range. The rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

High gain-bandwidth with 650 $\mu\text{A}/\text{Amplifier}$ supply current opens new battery powered applications where previous higher power consumption reduced battery life to unacceptable levels. The ability to drive large capacitive loads without oscillating functionally removes this common problem.

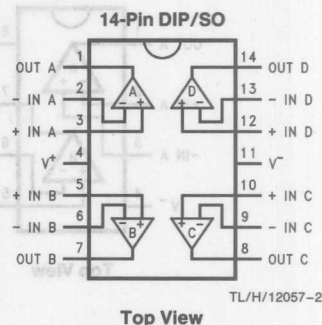
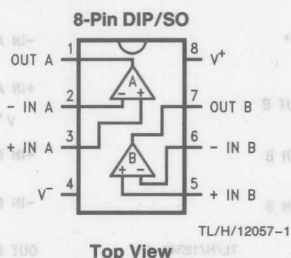
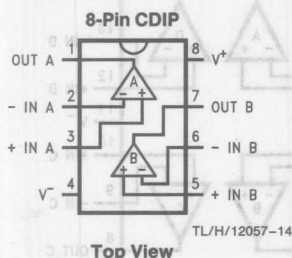
Features At $V_S = 5\text{V}$. Typ unless noted.

- Rail-to-rail input CMVR -0.25V to 5.25V
- Rail-to-rail output swing 0.005V to 4.995V
- Wide gain-bandwidth: 17 MHz at 50 kHz (typ)
- Slew rate:
 - Small signal, $5\text{V}/\mu\text{s}$
 - Large signal, $30\text{V}/\mu\text{s}$
- Low supply current $650 \mu\text{A}/\text{Amplifier}$
- Wide supply range 1.8V to 24V
- CMRR 107 dB
- Gain 108 dB with $R_L = 10\text{k}$
- PSRR 87 dB

Applications

- Battery operated instrumentation
- Depth sounders/fish finders
- Barcode scanners
- Wireless communications
- Rail-to-rail in-out instrumentation amps

Connection Diagrams



Ordering Information

| Package | Temperature Range | | NSC Drawing |
|----------------------|--|---|-------------|
| | Industrial -40°C to $+85^{\circ}\text{C}$ | Military -55°C to $+125^{\circ}\text{C}$ | |
| 8-Pin Molded DIP | LM6142AIN, LM6142BIN | | N08E |
| 8-Pin Small Outline | LM6142AIM, LM6142BIM | | M08A |
| 14-Pin Molded DIP | LM6144AIN, LM6144BIN | | N14A |
| 14-Pin Small Outline | LM6144AIM, LM6144BIM | | M14A |
| 8-Pin CDIP | | LM6142AMJ/883 | D08C |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------|
| ESD Tolerance (Note 2) | 2500V |
| Differential Input Voltage | 15V |
| Voltage at Input/Output Pin (V^+) + 0.3V, (V^-) - 0.3V | |
| Supply Voltage ($V^+ - V^-$) | 35V |
| Current at Input Pin | ± 10 mA |
| Current at Output Pin (Note 3) | ± 25 mA |
| Current at Power Supply Pin | 50 mA |
| Lead Temperature (soldering, 10 sec) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

Operating Ratings (Note 1)

| | |
|--------------------------------------|---|
| Supply Voltage | $1.8V \leq V^+ \leq 24V$ |
| Junction Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LM6142, LM6144 | |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 115°C/W |
| M Package, 8-Pin Surface Mount | 193°C/W |
| N Package, 14-Pin Molded DIP | 81°C/W |
| M Package, 14-Pin Surface Mount | 126°C/W |

5.0V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5.0V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$ to $V^+/2$. **Boldface limits** apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6144AI LM6142AI Limit (Note 6) | LM6144BI LM6142BI Limit (Note 6) | Units |
|------------|---------------------------------------|--------------------------|------------------|---|---|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.3 | 1.0 2.2 | 2.5 3.3 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 3 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 170 | 250 | 300 | nA |
| | | $0V \leq V_{CM} \leq 5V$ | 180 | 280 526 | 526 | nA max |
| I_{OS} | Input Offset Current | | 3 | 30 80 | 30 80 | nA max |
| R_{IN} | Input Resistance, C_M | | 126 | | | $\text{M}\Omega$ |
| $CMRR$ | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 4V$ | 107 | 84 78 | 84 78 | |
| | | $0V \leq V_{CM} \leq 5V$ | 82 79 | 66 64 | 66 64 | dB min |
| $PSRR$ | Power Supply Rejection Ratio | $5V \leq V^+ \leq 24V$ | 87 | 80 78 | 80 78 | |
| V_{CM} | Input Common-Mode Voltage Range | | -0.25 5.25 | 0 5.0 | 0 5.0 | V |
| A_V | Large Signal Voltage Gain | $R_L = 10k$ | 270 70 | 100 33 | 80 25 | V/mV min |
| V_O | Output Swing | $R_L = 100k$ | 0.005 | 0.01 0.013 | 0.01 0.013 | V max |
| | | | 4.995 | 4.98 4.93 | 4.98 4.93 | V min |
| | | $R_L = 10k$ | 0.02 | | | V max |
| | | | 4.97 | | | V min |
| | | $R_L = 2k$ | 0.06 | 0.1 0.133 | 0.1 0.133 | V max |
| | | | 4.90 | 4.86 4.80 | 4.86 4.80 | V min |

to $V^+/2$. **Boldface limits** apply at the temperature extremes. (Continued)

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6144AI LM6142AI Limit (Note 6) | LM6144BI LM6142BI Limit (Note 6) | Units |
|----------|---|---------------|-----------------|---|---|---------|
| I_{SC} | Output Short Circuit Current LM6142 | Sourcing | 13 | 10 | 8 | mA |
| | | | | 4.9 | 4 | min |
| | | Sinking | 24 | 10 | 10 | mA |
| | | | | 5.3 | 5.3 | min |
| I_{SC} | Output Short Circuit Current LM6144 | Sourcing | 8 | 6 | 6 | mA |
| | | | | 3 | 3 | min |
| | | Sinking | 22 | 8 | 8 | mA |
| | | | | 4 | 4 | min |
| I_S | Supply Current | Per Amplifier | 650 | 800 | 800 | μ A |
| | | | | 880 | 880 | max |

5.0V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$ to $V_S/2$. **Boldface limits** apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6144AI LM6142AI Limit (Note 6) | LM6144BI LM6142BI Limit (Note 6) | Units | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|---------------------------------|--|-----------------|---|---|------------------------------|-----------|--|--------------------|------|--|--|--|-----------|--|--|------|--|--|--|-----------|--|-------------------|------|--|--|--|-----------|--|--|-----|--|--|--|-----------|--|--|------|--|--|--|-----------|--|--|-----|--|--|--|
| SR | Slew Rate | 8V_{p-p} @ $V_{CC} 12\text{V}$ $R_S > 1\text{k}\Omega$ | 25 | 15 | 13 | $\text{V}/\mu\text{s}$ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| GBW | Gain-Bandwidth Product | $f = 50\text{kHz}$ | 17 | 10 | 10 | MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ϕ_m | Phase Margin | | 38 | 6 | 6 | Deg | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | Amp-to-Amp Isolation | | 130 | | | dB | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| e_n | Input-Referred Voltage Noise | $f = 1\text{kHz}$ | 16 | | | $\text{nV}/\sqrt{\text{Hz}}$ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| i_n | Input-Referred Current Noise | $f = 1\text{kHz}$ | 0.22 | | | $\text{pA}/\sqrt{\text{Hz}}$ | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| T.H.D. | Total Harmonic Distortion | $f = 10\text{kHz}$, $R_L = 10\text{k}\Omega$ | 0.003 | | | % | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <tr> <td colspan="2">V_{min}</td><td>$R_L = 10\text{k}$</td><td>0.02</td><td></td><td></td><td></td></tr> <tr> <td colspan="2">V_{max}</td><td></td><td>4.97</td><td></td><td></td><td></td></tr> <tr> <td colspan="2">V_{min}</td><td>$R_L = 2\text{k}$</td><td>0.02</td><td></td><td></td><td></td></tr> <tr> <td colspan="2">V_{max}</td><td></td><td>0.1</td><td></td><td></td><td></td></tr> <tr> <td colspan="2">V_{min}</td><td></td><td>0.01</td><td></td><td></td><td></td></tr> <tr> <td colspan="2">V_{max}</td><td></td><td>0.1</td><td></td><td></td><td></td></tr> </table> | | | | | | | V_{min} | | $R_L = 10\text{k}$ | 0.02 | | | | V_{max} | | | 4.97 | | | | V_{min} | | $R_L = 2\text{k}$ | 0.02 | | | | V_{max} | | | 0.1 | | | | V_{min} | | | 0.01 | | | | V_{max} | | | 0.1 | | | |
| V_{min} | | $R_L = 10\text{k}$ | 0.02 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V_{max} | | | 4.97 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V_{min} | | $R_L = 2\text{k}$ | 0.02 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V_{max} | | | 0.1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V_{min} | | | 0.01 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V_{max} | | | 0.1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

2.7V DC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6144AI LM6142AI Limit (Note 6) | LM6144BI LM6142BI Limit (Note 6) | Units |
|----------|---------------------------------|--|-----------------|---|---|----------------------|
| V_{OS} | Input Offset Voltage | | 0.4 | 1.8 4.3 | 2.5 4.3 | mV max |
| I_{Bn} | Input Bias Current | | 150 | 250 526 | 300 526 | nA max |
| I_{OS} | Input Offset Current | | 4 | 30 80 | 30 80 | nA max |
| R_{IN} | Input Resistance | | 128 | | | M Ω |
| $CMRR$ | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 1.8\text{V}$ | 90 | | | dB min |
| | | $0\text{V} \leq V_{CM} \leq 2.7\text{V}$ | 76 | | | |
| $PSRR$ | Power Supply Rejection Ratio | $3\text{V} \leq V^+ \leq 5\text{V}$ | 79 | | | |
| V_{CM} | Input Common-Mode Voltage Range | | -0.25 | 0 | 0 | V min |
| | | | 2.95 | 2.7 | 2.7 | V max |
| A_V | Large Signal Voltage Gain | $R_L = 10\text{k}\Omega$ | 55 | | | V/mV min |
| V_O | Output Swing | $R_L = 10\text{k}\Omega$ | 0.019 | 0.08 0.112 | 0.08 0.112 | V max |
| | | | 2.67 | 2.66 2.25 | 2.66 2.25 | V min |
| I_S | Supply Current | Per Amplifier | 510 | 800 880 | 800 880 | μA max |

2.7V AC Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$ to $V^+/2$. **Boldface** limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6144AI LM6142AI Limit (Note 6) | LM6144BI LM6142BI Limit (Note 6) | Units |
|----------|------------------------|--------------------|-----------------|---|---|-------|
| GBW | Gain-Bandwidth Product | $f = 50\text{kHz}$ | 9 | | | MHz |
| ϕ_m | Phase Margin | | 36 | | | Deg |
| G_m | Gain Margin | | 6 | | | dB |

24V Electrical Characteristics

Unless Otherwise Specified, All Limits Guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 24\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$ to $V_S/2$. **Boldface** limits apply at the temperature extreme

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6144AI LM6142AI Limit (Note 6) | LM6144BI LM6142BI Limit (Note 6) | Units |
|----------|------------------------------------|---|-----------------|---|---|----------------------|
| V_{OS} | Input Offset Voltage | | 1.3 | 2 4.8 | 3.8 4.8 | mV max |
| I_B | Input Bias Current | | 174 | | | nA max |
| I_{OS} | Input Offset Current | | 5 | | | nA max |
| R_{IN} | Input Resistance | | 288 | | | M Ω |
| CMRR | Common Mode | $0\text{V} \leq V_{CM} \leq 23\text{V}$ | 114 | | | dB min |
| | Rejection Ratio | $0\text{V} \leq V_{CM} \leq 24\text{V}$ | 100 | | | |
| PSRR | Power Supply Rejection Ratio | $0\text{V} \leq V_{CM} \leq 24\text{V}$ | 87 | | | |
| V_{CM} | Input Common-Mode Voltage Range | | -0.25 | 0 | 0 | V min |
| | | | 24.25 | 24 | 24 | V max |
| A_V | Large Signal Voltage Gain | $R_L = 10\text{k}$ | 500 | | | V/mV min |
| V_O | Output Swing | $R_L = 10\text{k}\Omega$ | 0.07 | 0.15 0.185 | 0.15 0.185 | V max |
| | | | 23.85 | 23.81 23.62 | 23.81 23.62 | V min |
| I_S | Supply Current | Per Amplifier | 750 | 1100 1150 | 1100 1150 | μA max |
| GBW | Gain-Bandwidth Product | $f = 50\text{kHz}$ | 18 | | | MHz |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, $1.5\text{k}\Omega$ in series with 100pF .

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

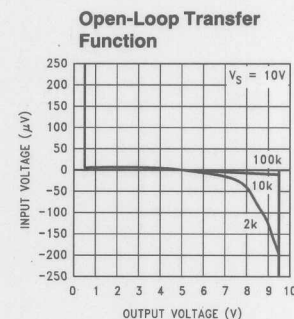
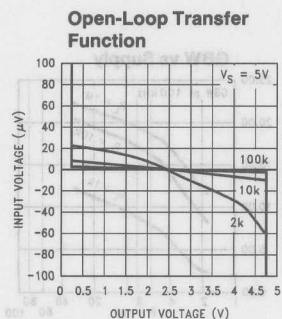
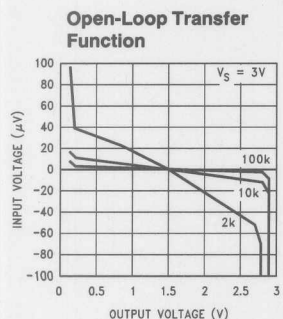
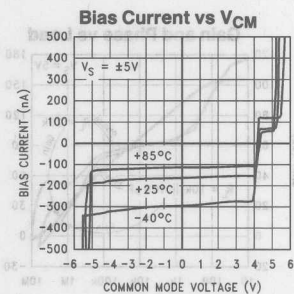
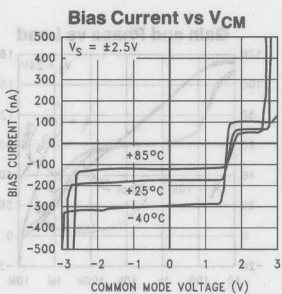
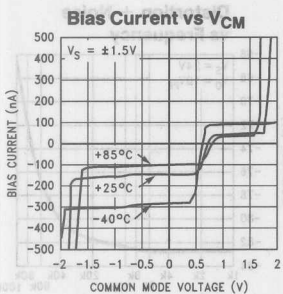
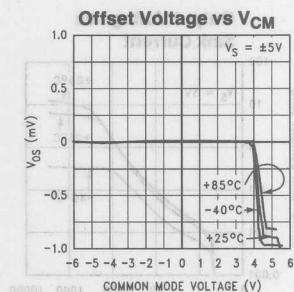
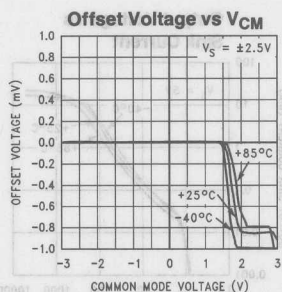
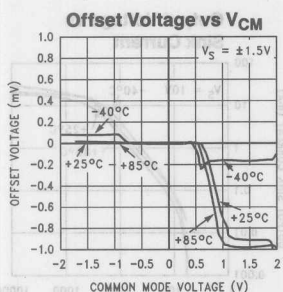
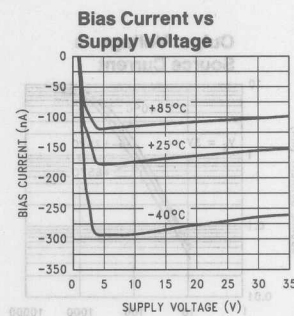
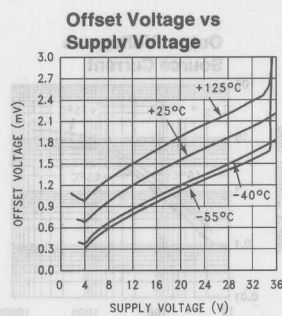
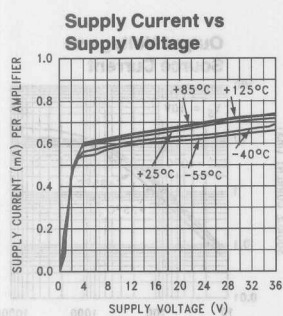
Note 4: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

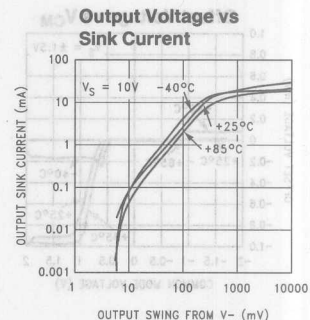
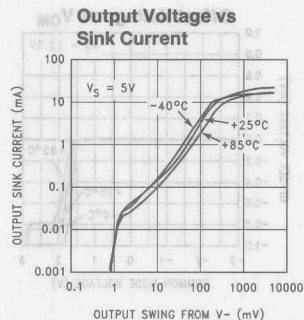
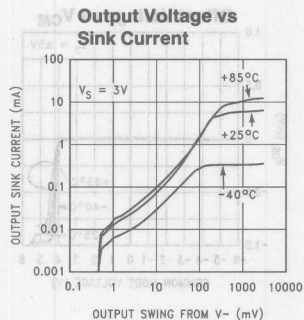
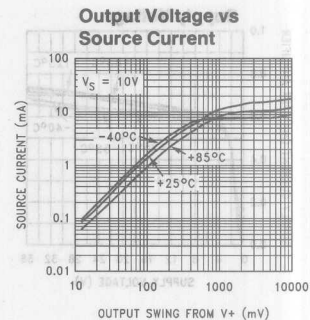
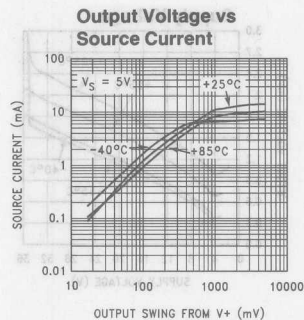
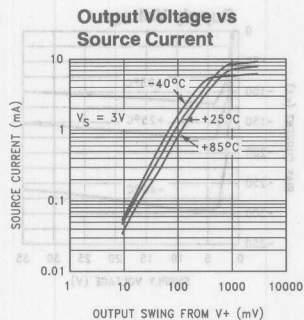
Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: For guaranteed military specifications see military datasheet MNL6142AM-X.

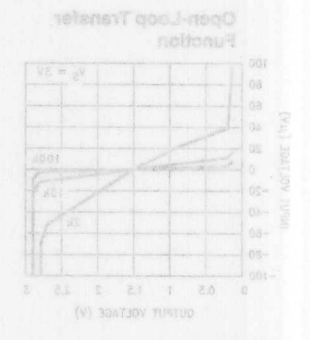
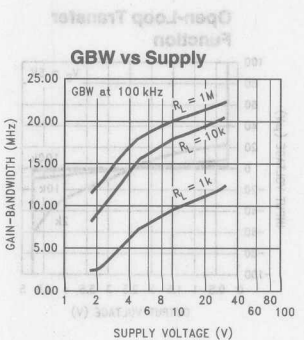
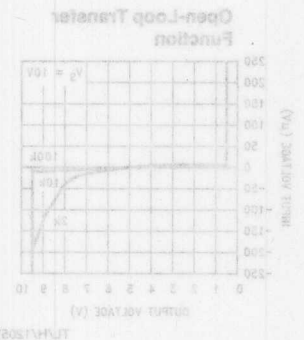
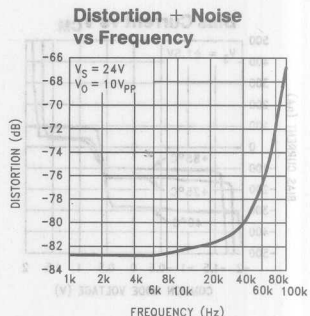
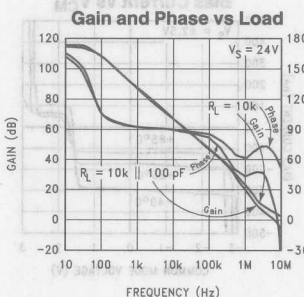
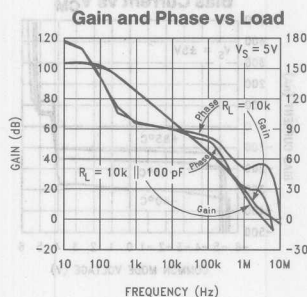
Typical Performance Characteristics $T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ Unless Otherwise Specified



TL/H/12057-3



TL/H/12057-4

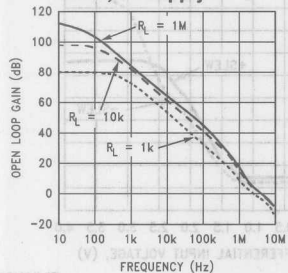


TL/H/12057-11

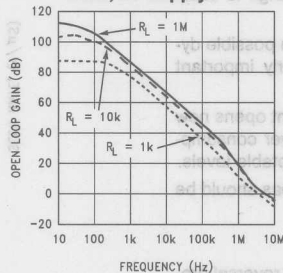
Typical Performance Characteristics

$T_A = 25^\circ\text{C}$, $R_L = 10\text{ k}\Omega$ Unless Otherwise Specified (Continued)

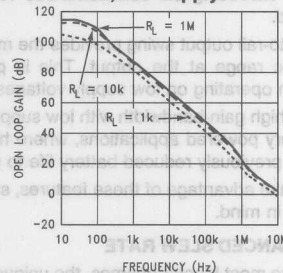
Open Loop Gain vs Load, 3V Supply



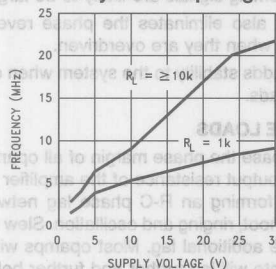
Open Loop Gain vs Load, 5V Supply



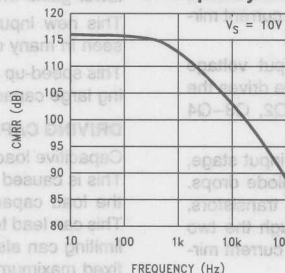
Open Loop Gain vs Load, 24V Supply



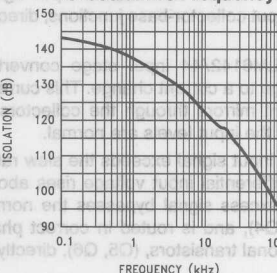
Unity Gain Freq vs V_S



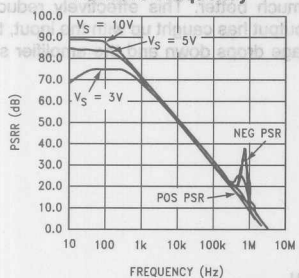
CMRR vs Frequency



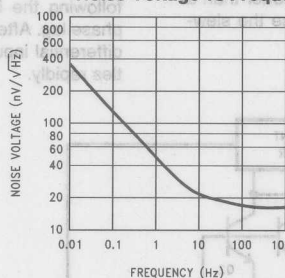
Crosstalk vs Frequency



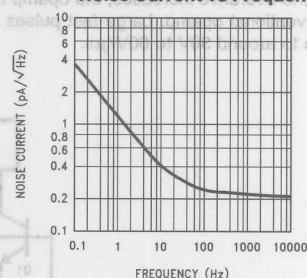
PSRR vs Frequency



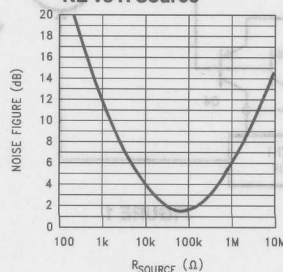
Noise Voltage vs Frequency



Noise Current vs Frequency



NE vs R Source



TL/H/12057-5

TL/H/12057-12

LM6142/44 Application Ideas

The LM6142 brings a new level of ease of use to opamp system design.

With greater than rail-to-rail input voltage range concern over exceeding the common-mode voltage range is eliminated.

Rail-to-rail output swing provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages.

The high gain-bandwidth with low supply current opens new battery powered applications, where high power consumption, previously reduced battery life to unacceptable levels. To take advantage of these features, some ideas should be kept in mind.

ENHANCED SLEW RATE

Unlike most bipolar opamps, the unique phase reversal prevention/speed-up circuit in the input stage causes the slew rate to be very much a function of the input signal amplitude.

Figure 1 shows how excess input signal is routed around the input collector-base junctions, directly to the current mirrors.

The LM6142/44 input stage converts the input voltage change to a current change. This current change drives the current mirrors through the collectors of Q1-Q2, Q3-Q4 when the input levels are normal.

If the input signal exceeds the slew rate of the input stage, the differential input voltage rises above two diode drops. This excess signal bypasses the normal input transistors, (Q1-Q4), and is routed in correct phase through the two additional transistors, (Q5, Q6), directly into the current mirrors.

This rerouting of excess signal allows the slew-rate to increase by a factor of 10 to 1 or more. (See Figure 2.)

As the overdrive increases, the opamp reacts better than a conventional opamp. Large fast pulses will raise the slew-rate to around 30V to 60V/ μ s.

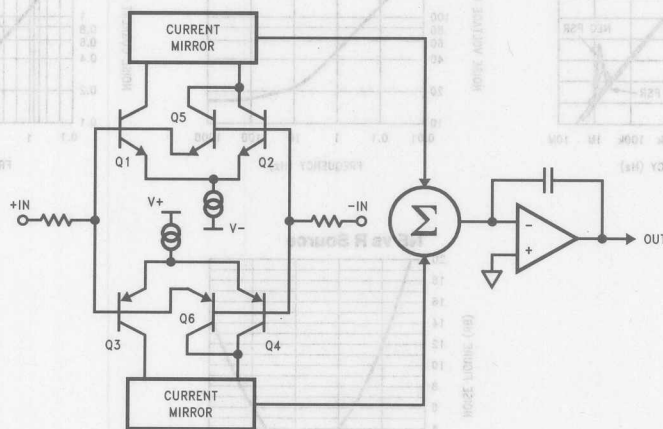
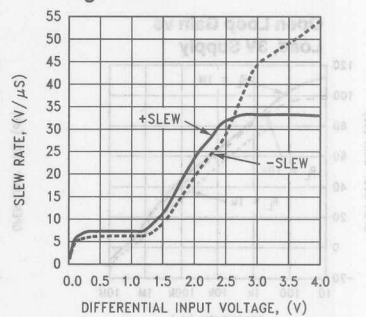


FIGURE 1

Slew Rate vs ΔV_{IN}
 $V_S = \pm 5V$



TL/H/12057-7

FIGURE 2

This effect is most noticeable at higher supply voltages and lower gains where incoming signals are likely to be large.

This new input circuit also eliminates the phase reversal seen in many opamps when they are overdriven.

This speed-up action adds stability to the system when driving large capacitive loads.

DRIVING CAPACITIVE LOADS

Capacitive loads decrease the phase margin of all opamps. This is caused by the output resistance of the amplifier and the load capacitance forming an R-C phase lag network. This can lead to overshoot, ringing and oscillation. Slew rate limiting can also cause additional lag. Most opamps with a fixed maximum slew-rate will lag further and further behind when driving capacitive loads even though the differential input voltage raises. With the LM6142, the lag causes the slew rate to raise. The increased slew-rate keeps the output following the input much better. This effectively reduces phase lag. After the output has caught up with the input, the differential input voltage drops down and the amplifier settles rapidly.

TL/H/12057-6

(continued)

These features allow the LM6142 to drive capacitive loads as large as 1000 pF at unity gain and not oscillate. The scope photos (Figure 3a and 3b) above show the LM6142 driving a 1000 pF load. In Figure 3a, the upper trace is with no capacitive load and the lower trace is with a 1000 pF load. Here we are operating on $\pm 12\text{V}$ supplies with a 20 Vp-p pulse. Excellent response is obtained with a C_f of 10 pF. In Figure 3b, the supplies have been reduced to $\pm 2.5\text{V}$, the pulse is 4 Vp-p and C_f is 39 pF. The best value for the compensation capacitor is best established after the board layout is finished because the value is dependent on board stray capacity, the value of the feedback resistor, the closed loop gain and, to some extent, the supply voltage.

Another effect that is common to all opamps is the phase shift caused by the feedback resistor and the input capacitance. This phase shift also reduces phase margin. This effect is taken care of at the same time as the effect of the capacitive load when the capacitor is placed across the feedback resistor.

The circuit shown in Figure 4 was used for these scope photos.

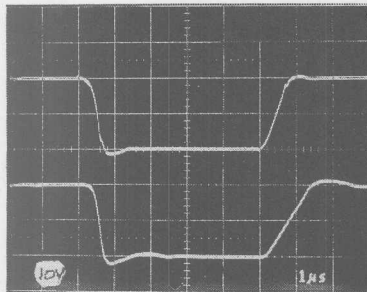


FIGURE 3a

TL/H/12057-8

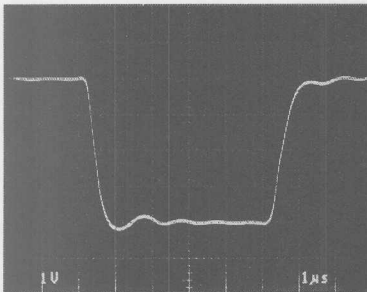


FIGURE 3b

TL/H/12057-9

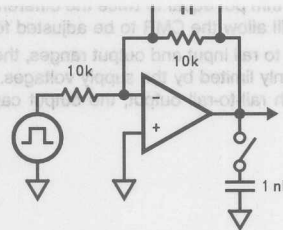


FIGURE 4

TL/H/12057-10

Typical Applications

FISH FINDER/ DEPTH SOUNDER.

The LM6142/44 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 82 dB, make the LM6142/44 a good choice for buffering the inputs of A to D converters.

3 OPAMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 opamp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for single supply systems.

Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so to even get unity gain, the amplifier must be run at high closed loop gains. This raises the noise and drift by the internal gain factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 5). These buffers assure that the input impedance is over 100 M Ω and they eliminate the requirement for precision matched resistors in the input stage. They also assure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of R1-R2 with R3-R4.

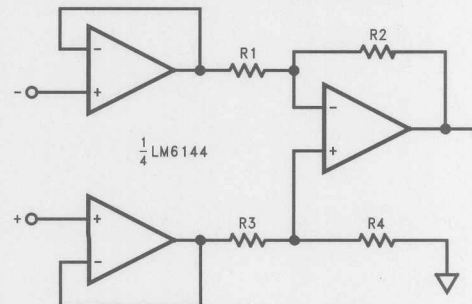


FIGURE 5

TL/H/12057-13

The gain is set by the ratio of $R2/R1$ and $R3$ should equal $R1$ and $R4$ equal $R2$. Making $R4$ slightly smaller than $R2$ and adding a trim pot equal to twice the difference between $R2$ and $R4$ will allow the CMR to be adjusted for optimum.

With both rail to rail input and output ranges, the inputs and outputs are only limited by the supply voltages. Remember that even with rail-to-rail output, the output can not swing

past the supplies so the combined common mode voltage plus the signal should not be greater than the supplies or limiting will occur.

SPICE MACROMODEL

A SPICE macromodel of this and many other National Semiconductor opamps is available at no charge from the NSC Customer Response Group at 800-272-9959.

TLHV15027-10

FIGURE 4

Typical Applications

FISH FINDER/DEPTH SOUNDER.

The LM6142/44 is an excellent choice for battery operated fish finders. The low supply current, high gain-bandwidth and full rail to rail output swing of the LM6142 provides an ideal combination for use in this and similar applications.

ANALOG TO DIGITAL CONVERTER BUFFER

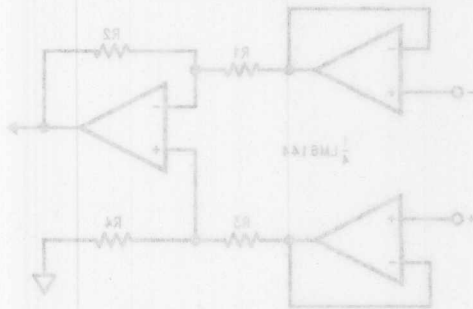
The high capacitive load driving ability, rail-to-rail input and output range with the excellent CMR of 55 dB, make the LM6142/44 a good choice for buffering the inputs to A/D converters.

3 OPAMP INSTRUMENTATION AMP WITH RAIL-TO-RAIL INPUT AND OUTPUT

Using the LM6144, a 3 opamp instrumentation amplifier with rail-to-rail inputs and rail to rail output can be made. These features make these instrumentation amplifiers ideal for signal systems.

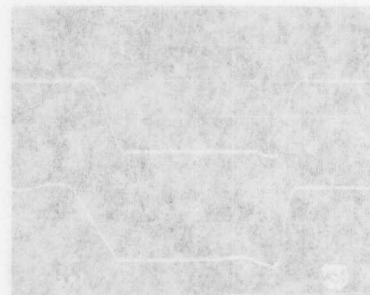
Some manufacturers use a precision voltage divider array of 5 resistors to divide the common-mode voltage to get an input range of rail-to-rail or greater. The problem with this method is that it also divides the signal, so even gain, gain, the amplifier must be run at high closed loop gain. This raises the noise and drift by the internal factor and lowers the input impedance. Any mismatch in these precision resistors reduces the CMR as well. Using the LM6144, all of these problems are eliminated.

In this example, amplifiers A and B act as buffers to the differential stage (Figure 5). These buffers ensure that the input impedance is over 100 MΩ and they eliminate the requirement for precision matched resistors in the input stage. They also ensure that the difference amp is driven from a voltage source. This is necessary to maintain the CMR set by the matching of $R1-R2$ with $R3-R4$.



TLHV15027-10

FIGURE 5



TLHV15027-8

FIGURE 3a



TLHV15027-9

FIGURE 3b

LM6152 Dual and LM6154 Quad High Speed/Low Power 45 MHz Rail-to-Rail I/O Operational Amplifiers

General Description

Using patent pending circuit topologies, the LM6152/54 provides new levels of speed vs power performance in applications where low voltage supplies or power limitations made compromise necessary. With only 1.5 mA/amp supply current, the 45 MHz bandwidth of this device supports new portable applications where higher power devices unacceptably drain battery life.

In addition, the LM6152/54 can be driven by voltages that exceed both power supply rails, thus eliminating concerns over exceeding the common-mode voltage range. The rail-to-rail output swing capability provides the maximum possible dynamic range at the output. This is particularly important when operating on low supply voltages. The LM6152/54 can also drive capacitive loads without oscillating.

Operating on supplies of 1.8V to over 24V, the LM6152/54 is excellent for a very wide range of applications, from battery operated systems with large bandwidth requirements to high speed instrumentation.

Features (For 5V Supply)

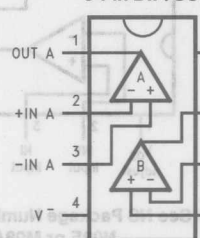
- Rail-to-rail input CMVR: -0.25V to 5.25V (max/min)
- Rail-to-rail output swing: 0.01V to 4.99V (max/min)
- Wide gain-bandwidth: 45 MHz (typ) @ 50 kHz
- Slew rate: 30 V/ μ s (typ)
- Low supply current: 1.5/Amp (typ)
- Wide supply range: 1.8V to 24V
- Fast settling time: 108 dB (typ) with $R_L = 10k$
- PSRR: 87 dB (typ)

Applications

- Portable high speed instrumentation
- 5V signal conditioning amplifiers/ADC buffers
- Bar code scanners
- Wireless communications

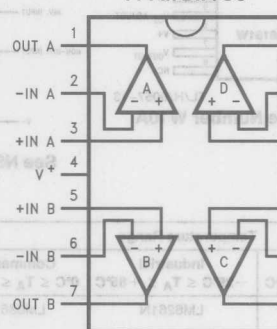
Connection Diagrams

8-Pin DIP/SO



Top View

14-Pin DIP/SO



Top View

Ordering Information

| Package | AD52 | Basic Temp Range | NSC Drawing |
|----------------------|----------------------|------------------------------|-------------|
| | AD1W | Industrial -40°C to +85°C | |
| 8-Pin Molded DIP | LM6142AIN, LM6142BIN | | N08E |
| 8-Pin Small Outline | LM6142AIM, LM6142BIM | | M08A |
| 14-Pin Molded DIP | LM6144AIN, LM6144BIN | | N14A |
| 14-Pin Small Outline | LM6144AIM, LM6144BIM | | M14A |

LM6161/LM6261/LM6361

High Speed Operational Amplifier

General Description

The LM6161 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/ μ s and 50 MHz unity gain stability with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIPTM (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

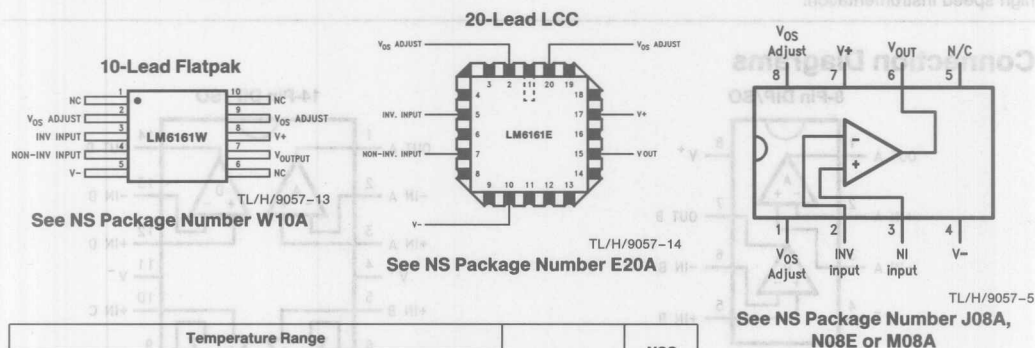
Features

- High slew rate 300 V/ μ s
- High unity gain freq 50 MHz
- Low supply current 5 mA
- Fast settling 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase 0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

Applications

- Video amplifier
- High-frequency filter
- Wide-bandwidth signal conditioning
- Radar
- Sonar

Connection Diagrams



| Temperature Range | | | Package | NSC Drawing |
|---|--|--|--------------------------|-------------|
| Military -55°C ≤ T _A ≤ +125°C | Industrial -25°C ≤ T _A ≤ +85°C | Commercial 0°C ≤ T _A ≤ +70°C | | |
| | LM6261N | LM6361N | 8-Pin Molded DIP | N08E |
| LM6161J/883 5962-8962101PA | | LM6361J | 8-Pin Ceramic DIP | J08A |
| | LM6261M | LM6361M | 8-Pin Molded Surface Mt. | M08A |
| LM6161E/883 5962-89621012A | | | 20-Lead LCC | E20A |
| LM6161W/883 5962-8962101HA | | | 10-Pin Ceramic Flatpak | W10A |

Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|--------------------------------|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 8) | $\pm 8V$ |
| Common-Mode Voltage Range (Note 10) | $(V^+ - 0.7V)$ to $(V^- - 7V)$ |
| Output Short Circuit to GND (Note 1) | Continuous |
| Soldering Information | |
| Dual-In-Line Package (N, J) | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package (M) | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | |
|--------------------------|-----------------|
| Storage Temp Range | -65°C to +150°C |
| Max Junction Temperature | 150°C |

| | |
|-------------------------------|------------|
| ESD Tolerance (Notes 6 and 7) | $\pm 700V$ |
|-------------------------------|------------|

Operating Ratings (Note 12)

| | |
|----------------------------|--|
| Temperature Range (Note 2) | |
| LM6161 | $-55^\circ C \leq T_J \leq +125^\circ C$ |
| LM6261 | $-25^\circ C \leq T_J \leq +85^\circ C$ |
| LM6361 | $0^\circ C \leq T_J \leq +70^\circ C$ |
| Supply Voltage Range | 4.75V to 32V |

DC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15V$, $V_{CM} = 0$, $R_L \geq 100\text{ k}\Omega$ and $R_S = 50\Omega$ unless otherwise noted.

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | Typ | LM6161 | LM6261 | LM6361 | Units |
|-------------------|---------------------------------------|--|-------|------------------------|-----------------------|-----------------------|------------------|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| V_{OS} | Input Offset Voltage | | 5 | 7 10 | 7 9 | 20 22 | mV Max |
| V_{OS} Drift | Input Offset Voltage Average Drift | | 10 | | | | $\mu V/^\circ C$ |
| I_b | Input Bias Current | | 2 | 3 6 | 3 5 | 5 6 | μA Max |
| I_{OS} | Input Offset Current | | 150 | 350 800 | 350 600 | 1500 1900 | nA Max |
| I_{OS} Drift | Input Offset Current Average Drift | | 0.4 | | | | nA/°C |
| R_{IN} | Input Resistance | Differential | 325 | | | | k Ω |
| C_{IN} | Input Capacitance | $A_V = +1$ @ 10 MHz | 1.5 | | | | pF |
| A_{VOL} | Large Signal Voltage Gain | $V_{OUT} = \pm 10V$, $R_L = 2\text{ k}\Omega$ (Note 9) | 750 | 550 300 | 550 400 | 400 350 | V/V Min |
| | | $R_L = 10\text{ k}\Omega$ (Note 9) | 2900 | | | | V/V |
| V_{CM} | Input Common-Mode Voltage Range | Supply = $\pm 15V$ | +14.0 | +13.9 +13.8 | +13.9 +13.8 | +13.8 +13.7 | Volts Min |
| | | | -13.2 | -12.9 -12.7 | -12.9 -12.7 | -12.8 -12.7 | Volts Min |
| | | | | | | | |
| | | Supply = $\pm 5V$ (Note 4) | 4.0 | 3.9 3.8 | 3.9 3.8 | 3.8 3.7 | Volts Min |
| | | | 1.8 | 2.0 2.2 | 2.0 2.2 | 2.1 2.2 | Volts Max |
| | | | | | | | |
| CMRR | Common-Mode Rejection Ratio | $-10V \leq V_{CM} \leq +10V$ | 94 | 80 74 | 80 76 | 72 70 | dB Min |
| PSRR | Power Supply Rejection Ratio | $\pm 10V \leq V \leq \pm 16V$ | 90 | 80 74 | 80 76 | 72 70 | dB Min |
| V_O | Output Voltage Swing | Supply = $\pm 15V$ and $R_L = 2\text{ k}\Omega$ | +14.2 | +13.5 +13.3 | +13.5 +13.3 | +13.4 +13.3 | Volts Min |
| | | | -13.4 | -13.0 -12.7 | -13.0 -12.8 | -12.9 -12.8 | Volts Min |

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = $\pm 15V$, $V_{CM} = 0$, $R_L \geq 100\text{ k}\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Type | LM6161 | LM6261 | LM6361 | Units |
|-------------------|----------------------------------|---|------|------------------------|-------------------|-------------------|--------------|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| V_O (Continued) | Output Voltage Swing (Continued) | Supply = $\pm 5V$ and $R_L = 2\text{ k}\Omega$ (Note 4) | 4.2 | 3.5 3.3 | 3.5 3.3 | 3.4 3.3 | Volts Min |
| | | | 1.3 | 1.7 2.0 | 1.7 1.9 | 1.8 1.9 | Volts Max |
| | Output Short Circuit Current | Source | 65 | 30 20 | 30 25 | 30 25 | mA Min |
| | | Sink | 65 | 30 20 | 30 25 | 30 25 | mA Min |
| I_S | Supply Current | | 5.0 | 6.5 6.8 | 6.5 6.7 | 6.8 6.9 | mA Max |

AC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15V$, $V_{CM} = 0$, $R_L \geq 100\text{ k}\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Type | LM6161 | LM6261 | LM6361 | Units |
|------------|------------------------|---|------|------------------------|-------------------|-------------------|-------------------------|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| GBW | Gain-Bandwidth Product | @ $f = 20\text{ MHz}$ | 50 | 40 30 | 40 35 | 35 32 | MHz Min |
| | | Supply = $\pm 5V$ | 35 | | | | MHz |
| SR | Slew Rate | $A_V = +1$ (Note 8) | 300 | 200 180 | 200 180 | 200 180 | V/ μs Min |
| | | Supply = $\pm 5V$ (Note 8) | 200 | | | | V/ μs |
| PBW | Power Bandwidth | $V_{OUT} = 20\text{ V}_{PP}$ | 4.5 | | | | MHz |
| t_S | Settling Time | 10V Step to 0.1% $A_V = -1$, $R_L = 2\text{ k}\Omega$ | 120 | | | | ns |
| ϕ_m | Phase Margin | | 45 | | | | Deg |
| A_D | Differential Gain | NTSC, $A_V = +4$ | <0.1 | | | | % |
| ϕ_D | Differential Phase | NTSC, $A_V = +4$ | 0.1 | | | | Deg |
| e_{np-p} | Input Noise Voltage | $f = 10\text{ kHz}$ | 15 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_{np-p} | Input Noise Current | $f = 10\text{ kHz}$ | 1.5 | | | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/W , the molded plastic SO (M) package is 155°C/W , and the cerdip (J) package is 125°C/W . All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS} , V_{OS} Drift, and Input Voltage Noise.

Note 5: $C_L \leq 5\text{ pF}$.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS} , I_{OS} , and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω .

Note 8: $V_{IN} = 8V$ step. For supply = $\pm 5V$, $V_{IN} = 5V$ step.

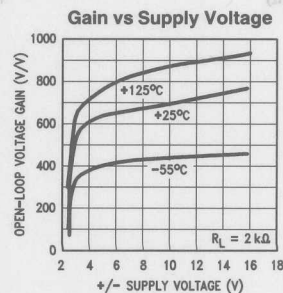
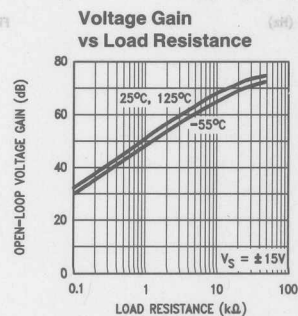
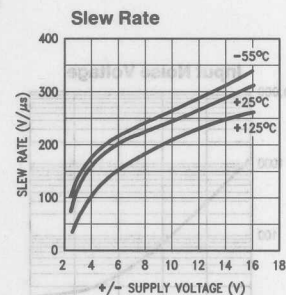
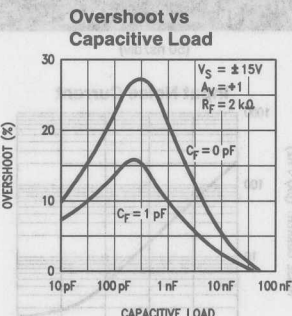
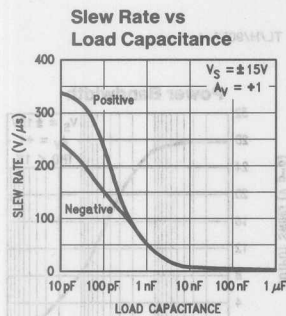
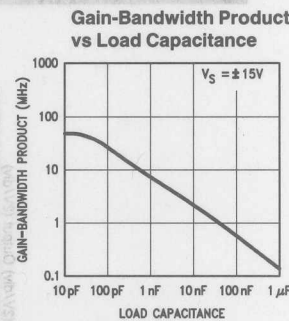
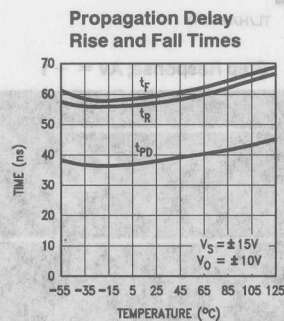
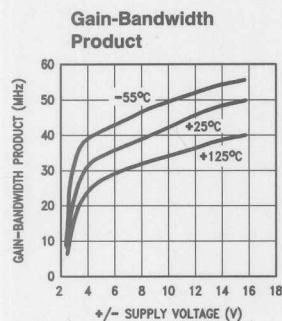
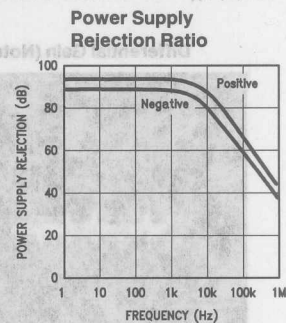
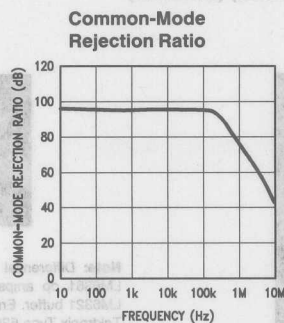
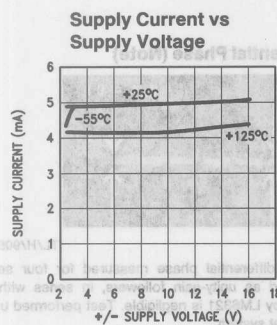
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V^+ and either input pin must not exceed $36V$.

Note 11: A military RETS electrical test specification is available on request. At the time of printing, the RETS6161X specs complied with all **Boldface** limits in this column.

Note 12: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Typical Performance Characteristics ($R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

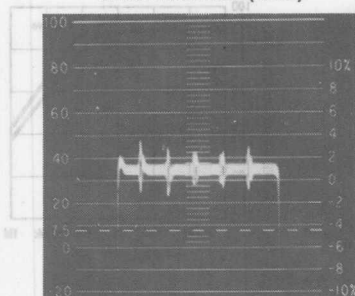


TL/H/9057-6

Typical Performance Characteristics

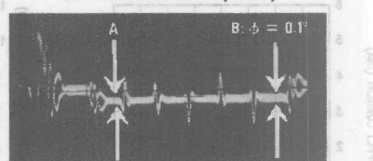
($R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9057-7

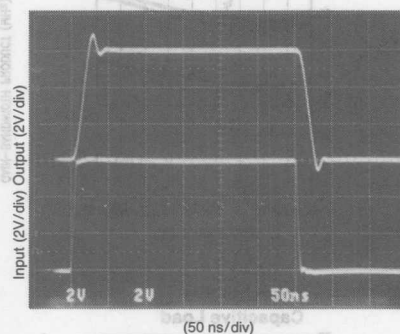
Differential Phase (Note)



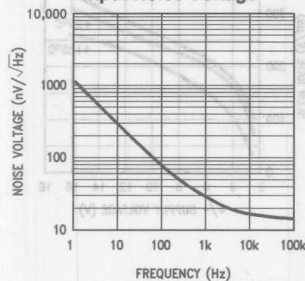
TL/H/9057-8

Note: Differential gain and differential phase measured for four series LM6361 op amps configured as unity-gain followers, in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

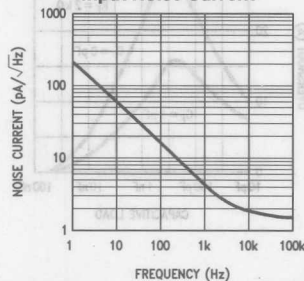
Step Response; $A_v = +1$



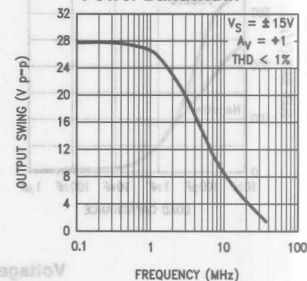
Input Noise Voltage



Input Noise Current



Power Bandwidth

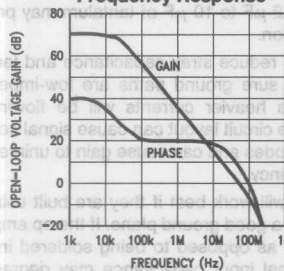


TL/H/9057-9

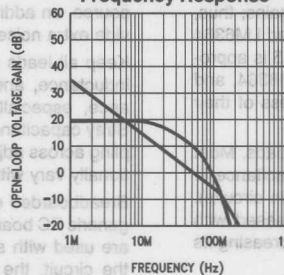
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

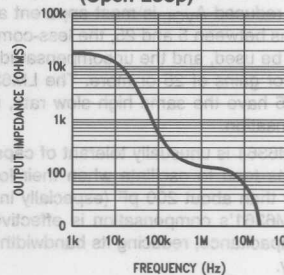
Open-Loop Frequency Response



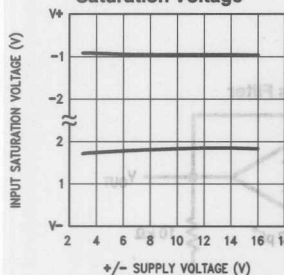
Open-Loop Frequency Response



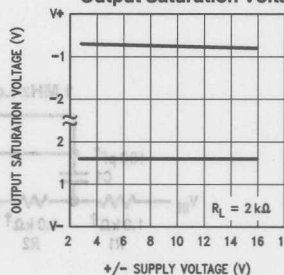
**Output Impedance
(Open-Loop)**



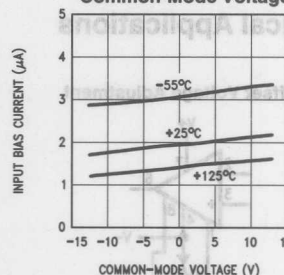
Common-Mode Input Saturation Voltage



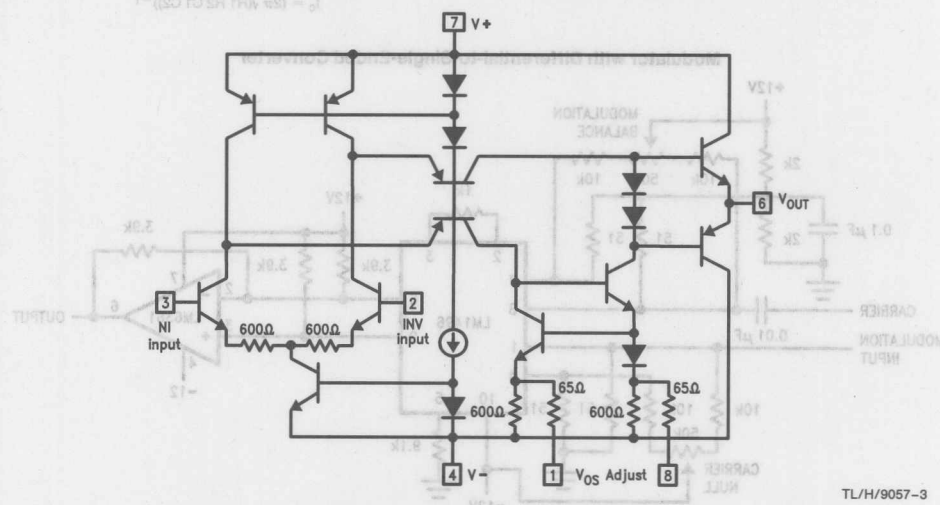
Output Saturation Voltage



Bias Current vs Common-Mode Voltage



Simplified Schematic



generation resistors to the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, for gains between 5 and 25, the less-compensated LM6364 should be used, and the uncompensated LM6365 is appropriate for gains of 25 or more. The LM6361, LM6364, and LM6365 have the same high slew rate, regardless of their compensation.

The LM6361 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (especially in low-gain circuits). The LM6361's compensation is effectively increased with load capacitance, reducing its bandwidth and increasing its stability.

Power supply bypassing is not as critical for the LM6361 as it is for other op amps in its speed class. Bypassing will,

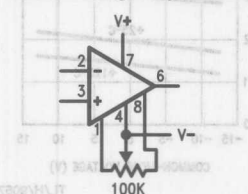
recommended for every design, 0.1 μ F to 0.1 μ F ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μ F to 10 μ F of tantalum may provide extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling across adjacent nodes and can cause gain to unintentionally vary with frequency.

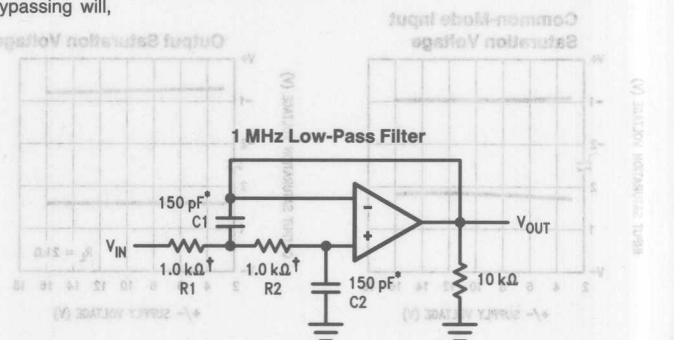
Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

Typical Applications

Offset Voltage Adjustment



TL/H/9057-4



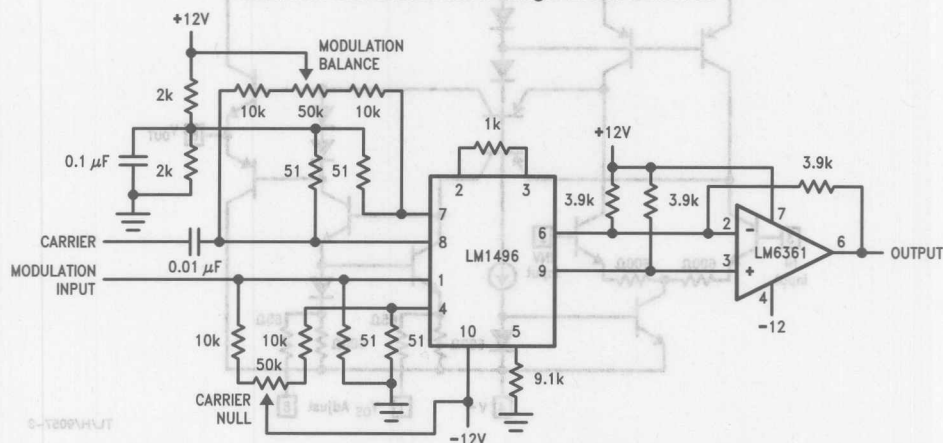
TL/H/9057-10

†1% tolerance

*Matching determines filter precision

$$f_c = (2\pi \sqrt{R1 R2 C1 C2})^{-1}$$

Modulator with Differential-to-Single-Ended Converter



TL/H/9057-11

LM6162/LM6262/LM6362

High Speed Operational Amplifier

General Description

The LM6362 family of high-speed amplifiers exhibits an excellent speed-power product, delivering 300 V/ μ s and 100 MHz gain-bandwidth product (stable for gains as low as +2 or ≥ 1) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIPTM (Vertically Integrated PNP) process which provides fast transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

- High slew rate
- High gain-bandwidth product

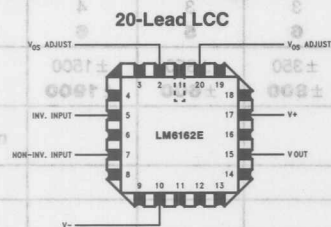
300 V/ μ s
100 MHz

- Low supply current 5 mA
- Fast settling time 120 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase <0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load
- Well behaved; easy to apply

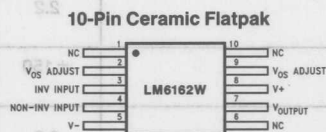
Applications

- Video amplifier
- Wide-bandwidth signal conditioning for image processing (FAX, scanners, laser printers)
- Hard disk drive preamplifier
- Error amplifier for high-speed switching regulator

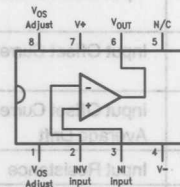
Connection Diagrams



Top View
See NS Package Number E20A



Top View
See NS Package Number W10A



See NS Package Number N08E, M08A or J08A

| Temperature Range | | | Package | NSC Drawing |
|--|---|---|--------------------------|-------------|
| Military -55°C $\leq T_A \leq$ +125°C | Industrial -25°C $\leq T_A \leq$ +85°C | Commercial 0°C $\leq T_A \leq$ +70°C | | |
| LM6162N | LM6262N | LM6362N | 8-Pin Molded DIP | N08E |
| LM6162J/883 5962-9216501PA | | | 8-Pin Ceramic DIP | J08A |
| LM6162E/883 5962-92165012A | LM6262M | LM6362M | 8-Pin Molded Surface Mt. | M08A |
| | | | 20-Lead LCC | E20A |
| LM6162W/883 5962-9216501HA | | | 10-Pin Ceramic Flatpak | W10A |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|--------------------------------------|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 2) | $\pm 8V$ |
| Common-Mode Input Voltage (Note 3) | ($V^+ - 0.7V$) to ($V^- + 0.3V$) |
| Output Short Circuit to GND (Note 4) | Continuous |
| Soldering Information | |
| Dual-In-Line Package (N) | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package (M) | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | |
|---------------------------|--|
| Storage Temperature Range | $-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ |
| Max Junction Temperature | 150°C |
| ESD Tolerance (Note 5) | $\pm 1100V$ |

Operating Ratings

| | |
|----------------------------|--|
| Temperature Range (Note 6) | |
| LM6162 | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| LM6262 | $-25^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LM6362 | $0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$ |
| Supply Voltage Range | 4.75V to 32V |

DC Electrical Characteristics

These limits apply for supply voltage = $\pm 15V$, $V_{CM} = 0V$, and $R_L \geq 100\text{ k}\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM6162 Limit (Note 8) | LM6262 Limit (Note 8) | LM6362 Limit (Note 8) | Units |
|--|---------------------------------------|--|---------------------|--|--|--|------------------------------|
| V_{OS} | Input Offset Voltage | | ± 3 | ± 5 ± 8 | ± 5 ± 8 | ± 13 ± 15 | mV max |
| $\frac{\Delta V_{OS}}{\Delta T_{emp}}$ | Input Offset Voltage Average Drift | | 7 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_{bias} | Input Bias Current | | 2.2 | 3 6 | 3 5 | 4 6 | μA max |
| I_{OS} | Input Offset Current | | ± 150 | ± 350 ± 800 | ± 350 ± 600 | ± 1500 ± 1900 | nA max |
| $\frac{\Delta I_{OS}}{\Delta T_{emp}}$ | Input Offset Current Average Drift | | 0.3 | | | | nA/ $^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 180 | | | | k Ω |
| C_{IN} | Input Capacitance | | 2.0 | | | | pF |
| A_{VOL} | Large Signal Voltage Gain | $V_{OUT} = \pm 10V$, $R_L = 2\text{ k}\Omega$ (Note 9) | 1400 | 1000 500 | 1000 700 | 800 650 | V/V min |
| | | $R_L = 10\text{ k}\Omega$ | 6500 | | | | V/V |
| V_{CM} | Input Common-Mode Voltage Range | Supply = $\pm 15V$ | +14.0 | +13.9 +13.8 | +13.9 +13.8 | +13.8 +13.7 | V min |
| | | | -13.2 | -12.9 -12.7 | -12.9 -12.7 | -12.9 -12.8 | V max |
| | | | | | | | |
| | | Supply = +5V (Note 10) | 4.0 | 3.9 3.8 | 3.9 3.8 | 3.8 3.7 | V min |
| | | | 1.6 | 1.8 2.0 | 1.8 2.0 | 1.9 2.0 | V max |
| | | | | | | | |
| CMRR | Common-Mode Rejection Ratio | $-10V \leq V_{CM} \leq +10V$ | 100 | 83 79 | 83 79 | 76 74 | dB min |
| PSRR | Power Supply Rejection Ratio | $\pm 10V \leq V_S \leq \pm 16V$ | 93 | 83 79 | 83 79 | 76 74 | dB min |
| V_O | Output Voltage Swing | Supply = $\pm 15V$, $R_L = 2\text{ k}\Omega$ | +14.2 | +13.5 +13.3 | +13.5 +13.3 | +13.4 13.3 | V min |
| | | | -13.4 | -13.0 -12.7 | -13.0 -12.8 | -12.9 -12.8 | V max |

DC Electrical Characteristics (Continued)

These limits apply for supply voltage = $\pm 15\text{V}$, $V_{\text{CM}} = 0\text{V}$, and $R_L \geq 100\text{ k}\Omega$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM6162 Limit (Note 8) | LM6262 Limit (Note 8) | LM6362 Limit (Note 8) | Units |
|------------------|---------------------------------|---|---------------------|-----------------------------|-----------------------------|-----------------------------|-----------|
| V_O | Output Voltage Swing | Supply = $+5\text{V}$ and $R_L = 2\text{ k}\Omega$ (Note 10) | 4.2 | 3.5 3.3 | 3.5 3.3 | 3.4 3.3 | V min |
| | | | 1.3 | 1.7 2.0 | 1.7 1.9 | 1.8 1.9 | V max |
| I_{osc} | Output Short Circuit Current | Sourcing | 65 | 30 20 | 30 25 | 30 25 | mA min |
| | | Sinking | 65 | 30 20 | 30 25 | 30 25 | mA min |
| I_S | Supply Current | | 5.0 | 6.5 6.8 | 6.5 6.7 | 6.8 6.9 | mA max |

AC Electrical Characteristics

These limits apply for supply voltage = $\pm 15\text{V}$, $V_{\text{CM}} = 0\text{V}$, $R_L \geq 100\text{ k}\Omega$, and $C_L \leq 5\text{ pF}$, unless otherwise specified. Limits in standard typeface are for $T_A = T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM6162 Limit (Note 8) | LM6262 Limit (Note 8) | LM6362 Limit (Note 8) | Units |
|----------|------------------------|--|---------------------|-----------------------------|-----------------------------|-----------------------------|-------------------------|
| GBW | Gain-Bandwidth Product | $f = 20\text{ MHz}$ | 100 | 80 55 | 80 65 | 75 65 | MHz min |
| | | Supply = $\pm 5\text{V}$ | 70 | | | | MHz |
| SR | Slew Rate | $A_V = +2$ (Note 11) | 300 | 200 180 | 200 180 | 200 180 | V/ μs min |
| | | Supply = $\pm 5\text{V}$ | 200 | | | | V/ μs |
| PBW | Power Bandwidth | $V_{\text{OUT}} = 20\text{ V}_{\text{PP}}$ | 4.5 | | | | MHz |
| t_s | Settling Time | 10V step, to 0.1% $A_V = -1$, $R_L = 2\text{ k}\Omega$ | 100 | | | | ns |
| ϕ_m | Phase Margin | $A_V = +2$ | 45 | | | | deg |
| | Differential Gain | NTSC, $A_V = +2$ | <0.1 | | | | % |
| | Differential Phase | NTSC, $A_V = +2$ | <0.1 | | | | deg |
| e_n | Input Noise Voltage | $f = 10\text{ kHz}$ | 10 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input Noise Current | $f = 10\text{ kHz}$ | 1.2 | | | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: The ESD protection circuitry between the inputs will begin to conduct when the differential input voltage reaches 8V.

Note 3: a) In addition, the voltage between the V^+ pin and either input pin must not exceed 36V.

b) When the voltage applied to an input pin is driven more than 0.3V below the negative supply pin voltage, a substrate diode begins to conduct. Current through this pin must then be kept less than 20 mA to limit damage from self-heating.

Note 4: Although the output current is internally limited, continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

Note 5: This value is the average voltage that the weakest pin combinations can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model, 100 pF in series with 1500 Ω .

Note 6: The typical thermal resistance, junction-to-ambient, of the molded plastic DIP (N package) is 105°C/W . For the molded plastic SO (M package), use 155°C/W . All numbers apply for packages soldered directly into a printed circuit board.

Note 7: Typical values are for $T_J = 25^\circ\text{C}$, and represent the most likely parametric norm.

Note 8: Limits are guaranteed, by testing or correlation.

Note 9: Voltage Gain is the total output swing (20V) divided by the magnitude of the input signal required to produce that swing.

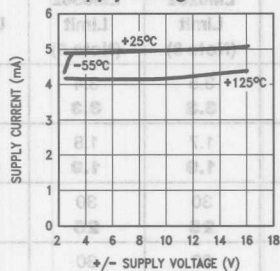
Note 10: For single-supply operation, the following conditions apply: $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 2.5\text{V}$, $V_{\text{OUT}} = 2.5\text{V}$. Pin 1 and Pin 8 (V_{OS} Adjust pins) are each connected to pin 4 (V^-) to realize maximum output swing. This connection will increase the offset voltage.

Note 11: $V_{\text{IN}} = 10\text{V}$ step. For $\pm 5\text{V}$ supplies, $V_{\text{IN}} = 1\text{V}$ step.

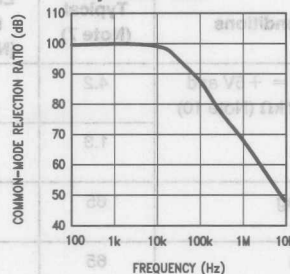
Note 12: A military RETS electrical test specification is available on request.

Typical Performance Characteristics $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise noted

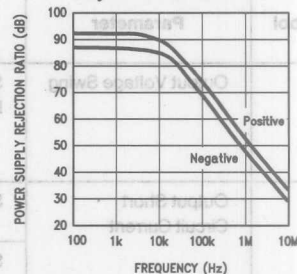
Supply Current vs Supply Voltage



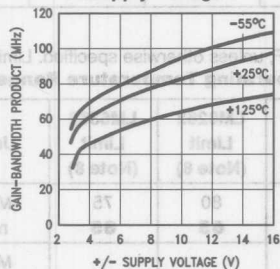
Common-Mode Rejection Ratio



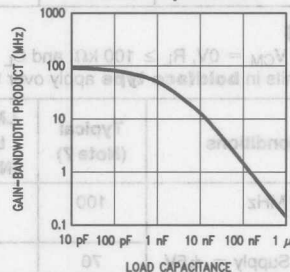
Power Supply Rejection Ratio



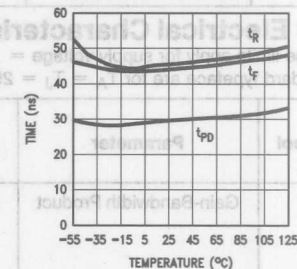
Gain-Bandwidth Product vs Supply Voltage



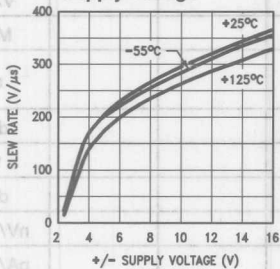
Gain-Bandwidth Product vs Load Capacitance



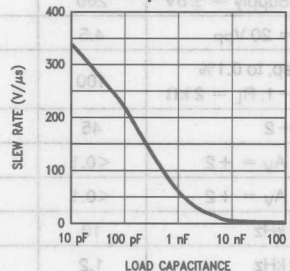
Propagation Delay, Rise and Fall Times



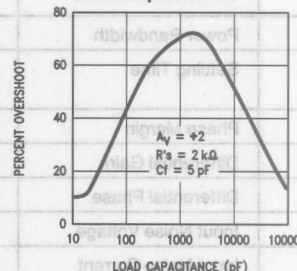
Slew Rate vs Supply Voltage



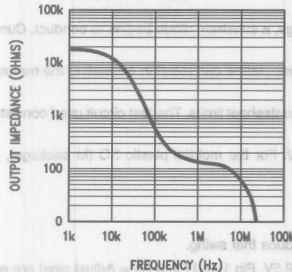
Slew Rate vs Load Capacitance



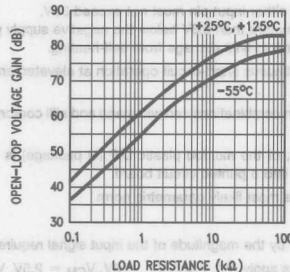
Overshoot vs Load Capacitance



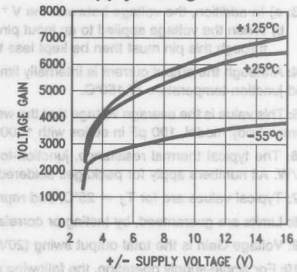
Output Impedance (Open-Loop)



Voltage Gain vs Load Resistance



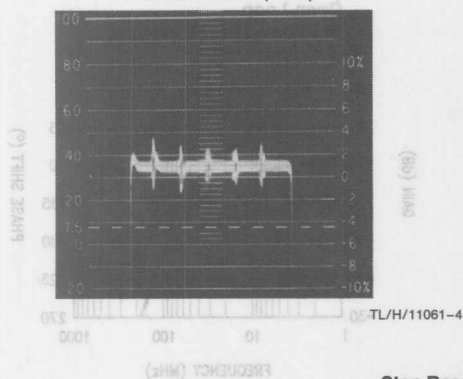
Voltage Gain vs Supply Voltage



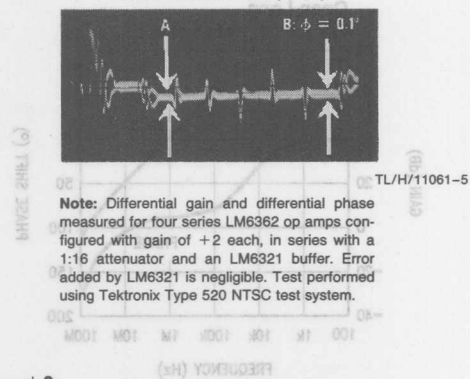
Typical Performance Characteristics (Continued)

 $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise noted

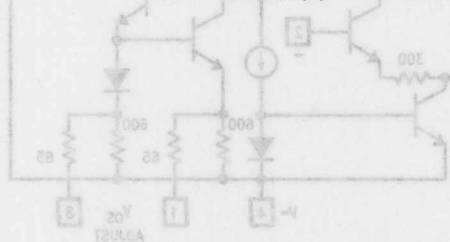
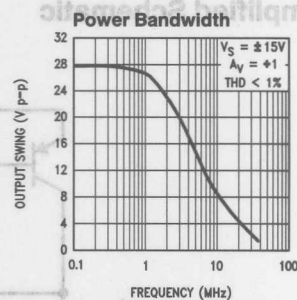
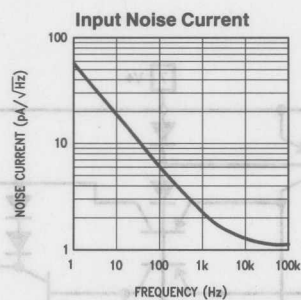
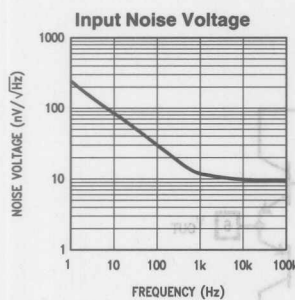
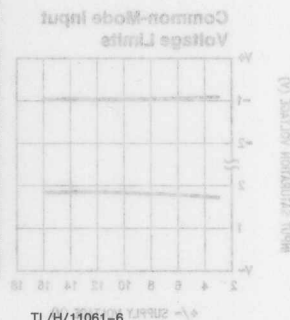
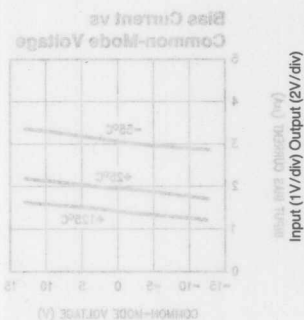
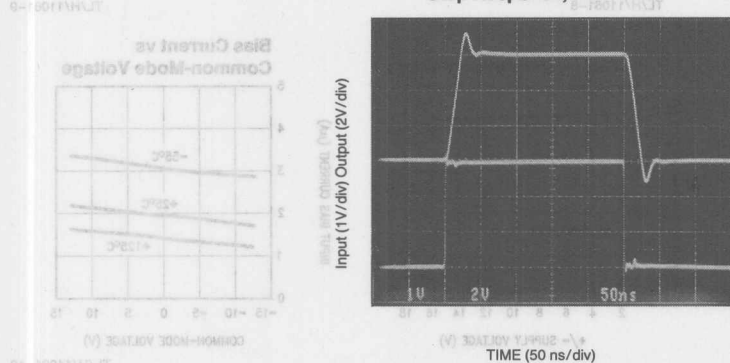
Differential Gain (Note)

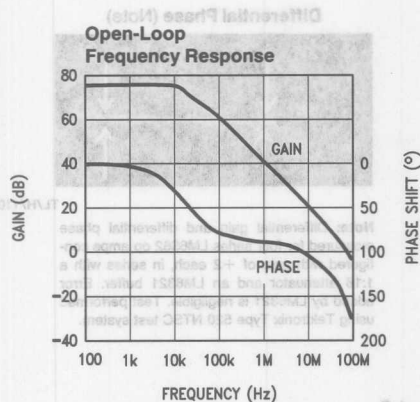


Differential Phase (Note)

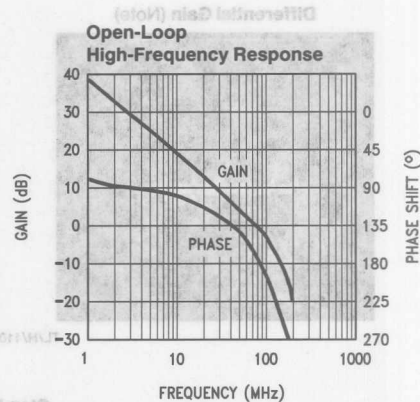


Note: Differential gain and differential phase measured for four series LM6362 op amps configured with gain of +2 each, in series with a 1:16 attenuator and an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

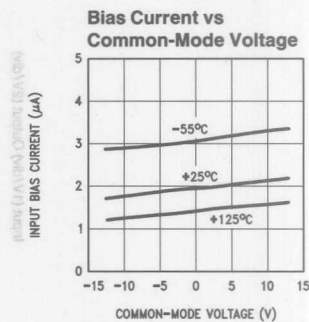
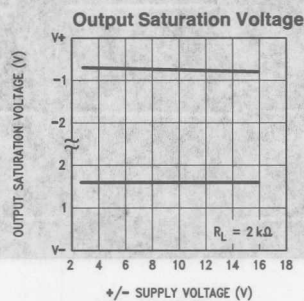
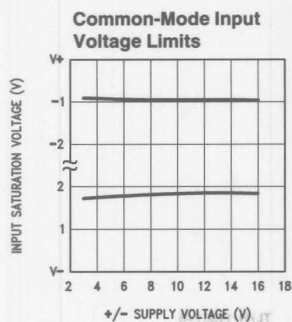
Step Response; $A_v = +2$ 



TL/H/11061-8

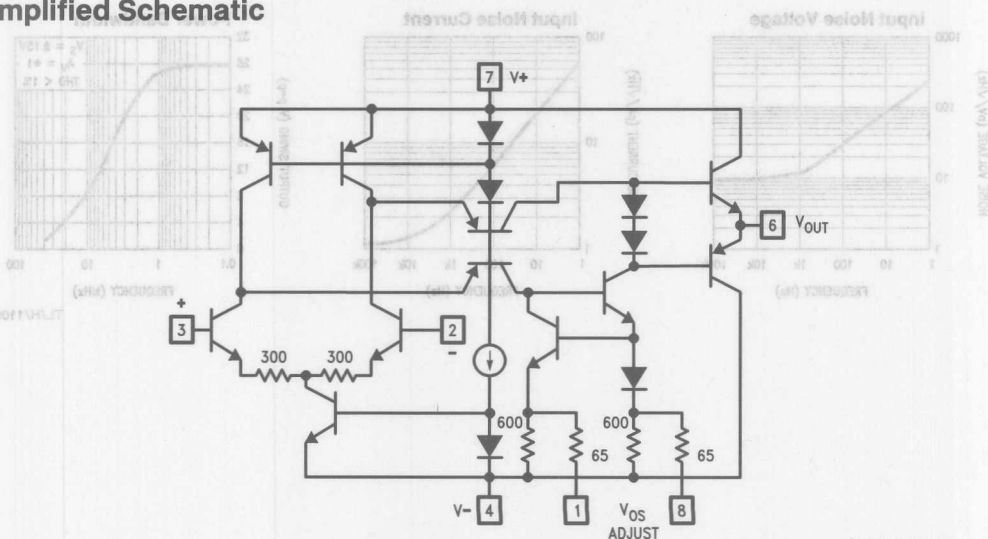


TL/H/11061-9



TL/H/11061-10

Simplified Schematic



TL/H/11061-1

still offers stability at gains of 2 (and -1) or greater over the specified ranges of temperature, power supply voltage, and load. Since this decompensation involved reducing the emitter-degeneration resistors in the op amp's input stage, the DC precision has been increased in the form of lower offset voltage and higher open-loop gain.

Other op amps in this family include the LM6361, LM6364, and LM6365. If unity-gain stability is required, the LM6361 should be used. The LM6364 has been decompensated for operation at gains of 5 or more, with corresponding greater gain-bandwidth product (125 MHz, typical) and DC precision. The fully-uncompensated LM6365 offers gain-bandwidth product of 725 MHz, typical, and is stable for gains of 25 or more. All parts in this family, regardless of compensation, have the same high slew rate of $300 \text{ V}/\mu\text{s}$ (typ).

The LM6362 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6362 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing may occur in low-gain circuits with large capacitive loads.

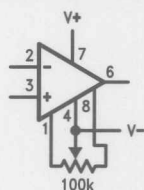
will improve the stability and transient response of the LM6362, and is recommended for every design. $0.01 \mu\text{F}$ to $0.1 \mu\text{F}$ ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional $2.2 \mu\text{F}$ to $10 \mu\text{F}$ of tantalum may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling from one pin, input or lead to another, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit frequency response. At low gains ($+2$ or -1), a feedback capacitor C_f from output to inverting input will compensate for the phase lag caused by capacitance at the inverting input. Typically, values from 2 pF to 5 pF work well; however, best results can be obtained by observing the amplifier pulse response and optimizing C_f for the particular layout.

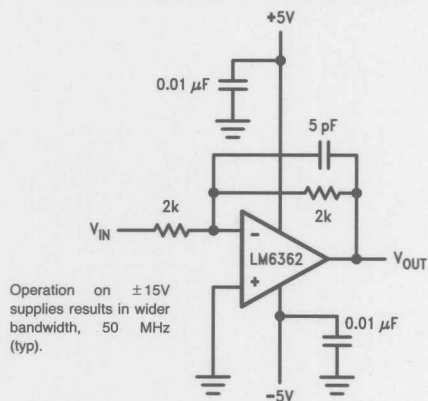
Typical Applications

Offset Voltage Adjustment



TL/H/11061-11

Inverting Amplifier, 30 MHz Bandwidth



TL/H/11061-12

LM6164/LM6264/LM6364

High Speed Operational Amplifier

General Description

The LM6164 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300V per μ s and 175 MHz GBW (stable down to gains as low as +5) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VJPTM (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

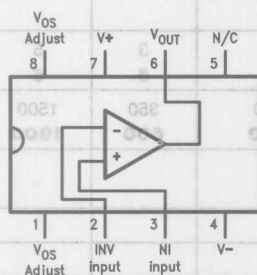
Features

- High slew rate 300 V/ μ s
- High GBW product 175 MHz
- Low supply current 5 mA
- Fast settling 100 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase <0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load

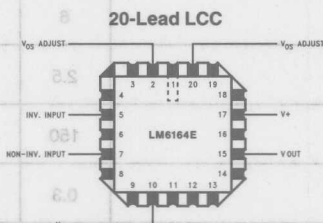
Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

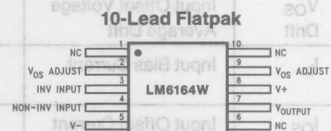
Connection Diagrams



NS Package Number
J08A, M08A or N08E



Top View
NS Package Number E20A



Top View
NS Package Number W10A

| Temperature Range | | | Package | NSC Drawing |
|--|---|---|--------------------------|-------------|
| Military $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | Industrial $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ | Commercial $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | | |
| LM6164J/883 5962-8962401PA | LM6264N | LM6364N | 8-Pin Molded DIP | N08E |
| LM6164E/883 5962-89624012A | | LM6364M | 8-Pin Ceramic DIP | J08A |
| LM6164W/883 5962-8962401HA | | | 8-Pin Molded Surface Mt. | M08A |
| | | | 20-Lead LCC | E20A |
| | | | 10-Pin Ceramic Flatpak | W10A |

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|--------------------------------|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 6) | $\pm 8V$ |
| Common-Mode Input Voltage (Note 10) | $(V^+ - 0.7V)$ to $(V^- - 7V)$ |
| Output Short Circuit to Gnd (Note 1) | Continuous |
| Soldering Information | |
| Dual-In-Line Package (N, J) | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package (M) | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | |
|-----------------------------------|---|
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Max Junction Temperature (Note 2) | 150°C |
| ESD Tolerance (Notes 6 & 7) | $\pm 700V$ |

Operating Ratings

| | |
|----------------------------|--|
| Temperature Range (Note 2) | |
| LM6164 | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| LM6264 | $-25^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LM6364 | $0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$ |
| Supply Voltage Range | 4.75V to 32V |

DC Electrical Characteristics The following specifications apply for Supply Voltage = $\pm 15V$, $V_{CM} = 0$, $R_L \geq 100\text{ k}\Omega$ and $R_S = 50\Omega$ unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typ | LM6164 | LM6264 | LM6364 | Units |
|-------------------|---------------------------------------|--|-------|------------------------|-----------------------|-----------------------|------------------------------|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| V_{OS} | Input Offset Voltage | | 2 | 4 6 | 4 6 | 9 11 | mV max |
| V_{OS} Drift | Input Offset Voltage Average Drift | | 6 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_b | Input Bias Current | | 2.5 | 3 6 | 3 5 | 5 6 | μA max |
| I_{OS} | Input Offset Current | | 150 | 350 800 | 350 600 | 1500 1900 | mA max |
| I_{OS} Drift | Input Offset Current Average Drift | | 0.3 | | | | nA/ $^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 100 | | | | k Ω |
| C_{IN} | Input Capacitance | | 3.0 | | | | pF |
| A_{VOL} | Large Signal Voltage Gain | $V_{OUT} = \pm 10V$, $R_L = 2\text{ k}\Omega$ (Note 9) | 2.5 | 1.8 0.9 | 1.8 1.2 | 1.3 1.1 | V/mV min |
| | | $R_L = 10\text{ k}\Omega$ | 9 | | | | |
| V_{CM} | Input Common-Mode Voltage Range | Supply = $\pm 15V$ | +14.0 | +13.9 +13.8 | +13.9 +13.8 | +13.8 +13.7 | V min |
| | | | -13.5 | -13.3 -13.1 | -13.3 -13.1 | -13.2 -13.1 | V min |
| | | Supply = +5V (Note 4) | 4.0 | 3.9 3.8 | 3.9 3.8 | 3.8 3.7 | V min |
| | | | 1.5 | 1.7 1.9 | 1.7 1.9 | 1.8 1.9 | V max |
| | | | | | | | |
| CMRR | Common-Mode Rejection Ratio | $-10V \leq V_{CM} \leq +10V$ | 105 | 86 80 | 86 82 | 80 78 | dB min |
| PSRR | Power Supply Rejection Ratio | $\pm 10V \leq V \pm \leq \pm 16V$ | 96 | 86 80 | 86 82 | 80 78 | dB min |

| Symbol | Parameter | Conditions | Typ | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | Units |
|----------|---------------------------------|--|-------|------------------------|------------------------|------------------------|-----------|
| V_O | Output Voltage Swing | Supply = +5V and $R_L = 2\text{ k}\Omega$ | +14.2 | +13.5 + 13.3 | +13.5 + 13.3 | +13.4 + 13.3 | V min |
| | | | -13.4 | -13.0 - 12.7 | -13.0 - 12.8 | -12.9 - 12.8 | V min |
| | | Supply = +5V and $R_L = 2\text{ k}\Omega$ (Note 9) | 4.2 | 3.5 3.3 | 3.5 3.3 | 3.4 3.3 | V min |
| | | | 1.3 | 1.7 2.0 | 1.7 1.9 | 1.8 1.9 | V max |
| I_{SC} | Output Short Circuit Current | Source | 65 | 30 20 | 30 25 | 30 25 | mA min |
| | | Sink | 65 | 30 20 | 30 25 | 30 25 | mA min |
| I_S | Supply Current | | 5.0 | 6.5 6.8 | 6.5 6.7 | 6.8 6.9 | mA min |
| | | | | | | | |
| | | | | | | | |

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (D) is 100°C/Watt, the molded plastic SO (M) package is 150°C/Watt, and the conformed (L) package is 25°C/Watt. All numbers apply to packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or computation.

Note 4: For single supply operation, the following conditions apply: $V_+ = 5V$, $V_- = 0V$, $V_{CM} = 2.5V$, $V_{OUT} = 2.5V$, $R_{IN} = 1\text{ k}\Omega$, $R_{IN} = 1\text{ k}\Omega$ (Adjust) are each connected to $R_{IN} + (V_-)$ to realize maximum output swing. This connection will degrade V_{OS} .

Note 5: $C_L \leq 5\text{ pF}$.

Note 6: In order to conserve optimum AC performance, the input stage was designed without protective clamping. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS} , I_{CM} , and I_{SC}).

Note 7: The average voltage that the resistor pin combination (those involving R_{IN} or R_{IN}) can withstand and still conform to the data sheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω.

Note 8: $V_{IN} = 1V$ step. For supply = $\pm 5V$, $V_{IN} = 1V$ step.

Note 9: Voltage gain is the total output swing (20V) divided by the input signal applied to produce that swing.

Note 10: The voltage between V_+ and V_- must not exceed 50V.

Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6364/LM6364 RETS spec complied with the following:

Note 12: In this column, the LM6364/LM6364 may also be procured as Standard Military Drawing # 22925-0101/01A.

| Symbol | Parameter | Conditions | Typ | LM6164 Limit (Notes 3, 11) | LM6264 Limit (Note 3) | LM6364 Limit (Note 3) | Units |
|-------------|------------------------|---|------|----------------------------------|-----------------------------|-----------------------------|------------------------|
| GBW | Gain-Bandwidth Product | $F = 20 \text{ MHz}$ | 175 | 140 | 140 | 120 | MHz |
| V | | Supply = $\pm 5\text{V}$ | 120 | | | | min |
| SR | Slew Rate | $A_V = +5$ (Note 8) | 300 | 200 | 200 | 200 | V/ μs |
| | | Supply = $\pm 5\text{V}$ | 200 | 180 | 180 | 180 | min |
| PBW | Power Bandwidth | $V_{OUT} = 20 V_{PP}$ | 4.5 | | | | MHz |
| T_S | Settling Time | 10V Step to 0.1% $A_V = -4, R_L = 2 \text{ k}\Omega$ | 100 | | | | ns |
| ϕ_m | Phase Margin | $A_V = +5$ | 45 | | | | Deg |
| A_{Dm} | Differential Gain | NTSC, $A_V = +10$ | <0.1 | | | | % |
| ϕ_{Dm} | Differential Phase | NTSC, $A_V = +10$ | <0.1 | | | | Deg |
| e_{np-p} | Input Noise Voltage | $F = 10 \text{ kHz}$ | 8 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_{np-p} | Input Noise Current | $F = 10 \text{ kHz}$ | 1.5 | | | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is 105°C/Watt, the molded plastic SO (M) package is 155°C/Watt, and the cerdip (J) package is 125°C/Watt. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: Limits are guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: $V_+ = 5\text{V}$, $V_- = 0\text{V}$, $V_{CM} = 2.5\text{V}$, $V_{OUT} = 2.5\text{V}$. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V_-) to realize maximum output swing. This connection will degrade V_{OS} .

Note 5: $C_L \leq 5 \text{ pF}$.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS} , I_{OS} , and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500 Ω .

Note 8: $V_{IN} = 4\text{V}$ step. For supply = $\pm 5\text{V}$, $V_{IN} = 1\text{V}$ step.

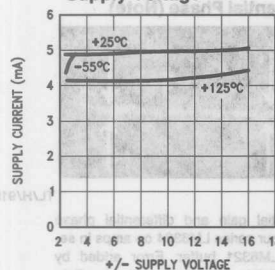
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V_+ and either input pin must not exceed 36V.

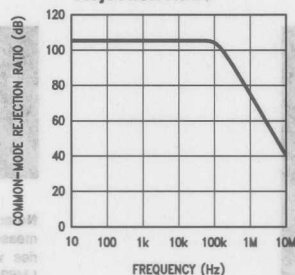
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6164J/883 RETS spec complied with the **Boldface** limits in this column. The LM6164J/883 may also be procured as Standard Military Drawing #5962-8962401PA.

Typical Performance Characteristics ($R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified)

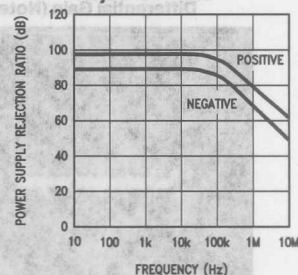
Supply Current vs Supply Voltage



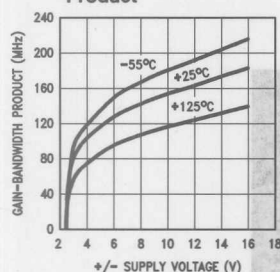
Common-Mode Rejection Ratio



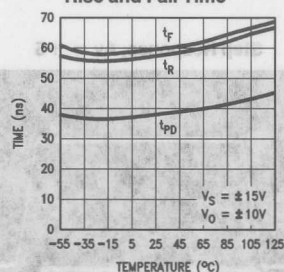
Power Supply Rejection Ratio



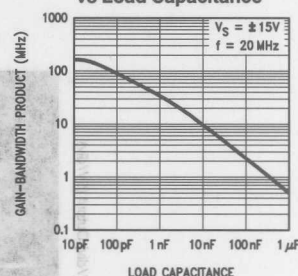
Gain-Bandwidth Product



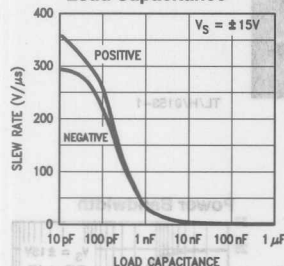
Propagation Delay Rise and Fall Time



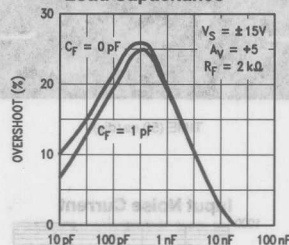
Gain-Bandwidth Product vs Load Capacitance



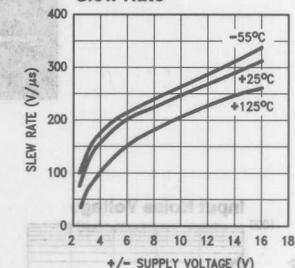
Slew Rate vs Load Capacitance



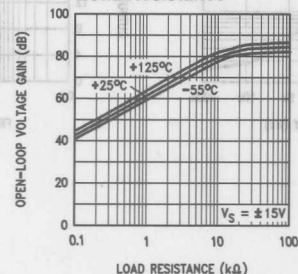
Overshoot vs Load Capacitance



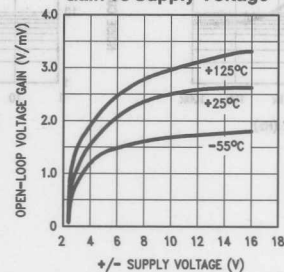
Slew Rate



Voltage Gain vs Load Resistance



Gain vs Supply Voltage

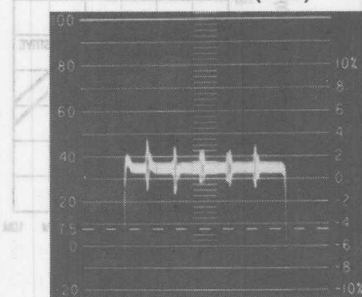


TL/H/9153-5

Typical Performance Characteristics

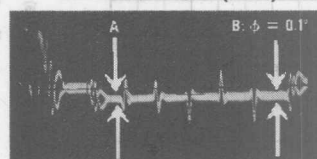
($R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified) (Continued)

Differential Gain (Note)



TL/H/9153-6

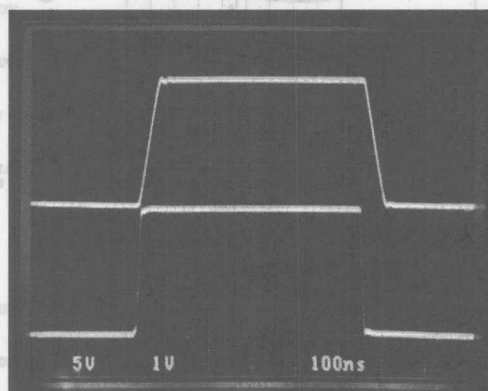
Differential Phase (Note)



TL/H/9153-7

Note: Differential gain and differential phase measured for four series LM6364 op amps in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system. Configured with a gain of +5 (each output attenuated by 80%)

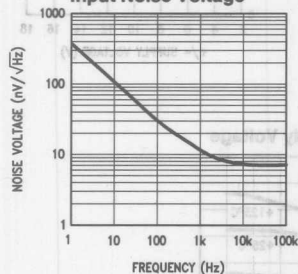
Step Response; $A_v = +5$



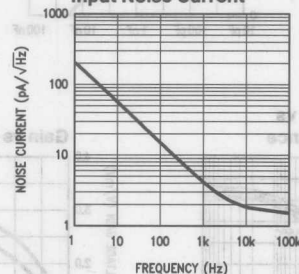
TIME (50 ns/div)

TL/H/9153-1

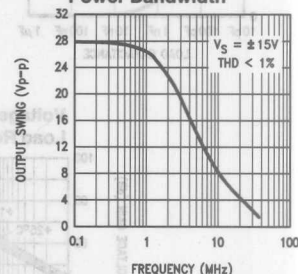
Input Noise Voltage



Input Noise Current



Power Bandwidth

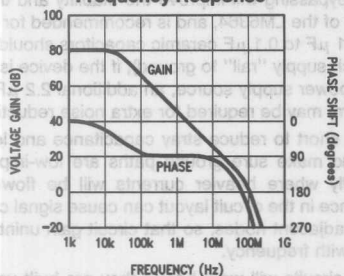


TL/H/9153-9

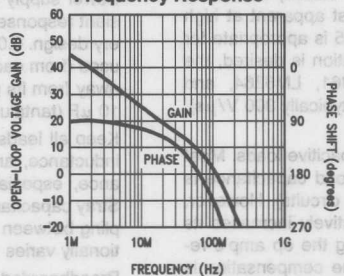
Typical Performance Characteristics

(R_L = 10 kΩ, T_A = 25°C unless otherwise specified) (Continued)

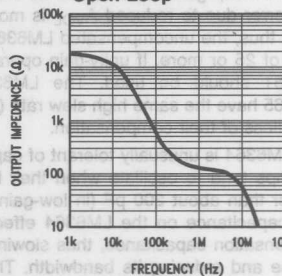
Open-Loop Frequency Response



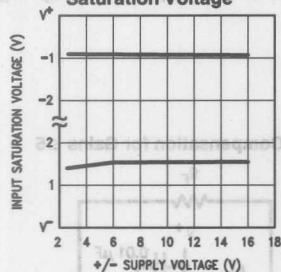
Open-Loop Frequency Response



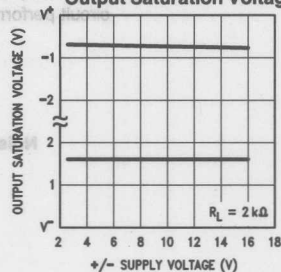
**Output Resistance
Open-Loop**



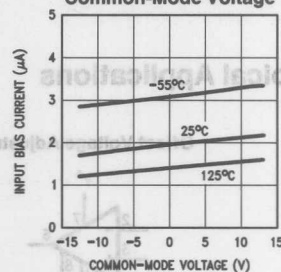
Common-Mode Input Saturation Voltage



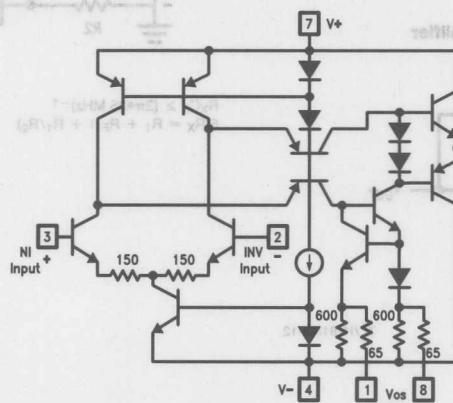
Output Saturation Voltage



Bias Current vs Common-Mode Voltage



Simplified Schematic



er (over specified ranges of temperature, power supply voltage, and load). Since this compensation involved adding emitter-degeneration resistors in the op amp's input stage, the open-loop gain was reduced as the stability increased. Gain error due to reduced A_{VOL} is most apparent at high gains; thus, the uncompensated LM6365 is appropriate for gains of 25 or more. If unity-gain operation is desired, the LM6361 should be used. The LM6361, LM6364, and LM6365 have the same high slew rate (typically 300 V/ μ s), regardless of their compensation.

The LM6364 is unusually tolerant of capacitive loads. Most op amps tend to oscillate when their load capacitance is greater than about 200 pF (in low-gain circuits). However, load capacitance on the LM6364 effectively increases its compensation capacitance, thus slowing the op amp's response and reducing its bandwidth. The compensation is not ideal, though, and ringing or oscillation may occur in low-gain circuits with large capacitive loads. To overcompensate the LM6364 for operation at gains less than 5, a

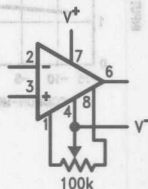
the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 5.

Power supply bypassing will improve the stability and transient response of the LM6364, and is recommended for every design. 0.01 μ F to 0.1 μ F ceramic capacitors should be used (from each supply "rail" to ground); if the device is far away from its power supply source, an additional 2.2 μ F to 10 μ F (tantalum) may be required for extra noise reduction. Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, so that circuit gain unintentionally varies with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

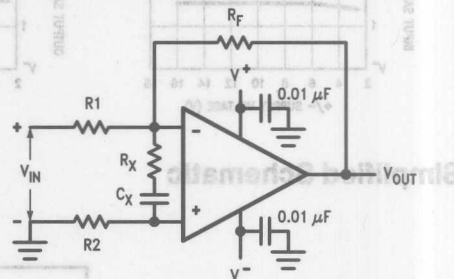
Typical Applications

Offset Voltage Adjustment



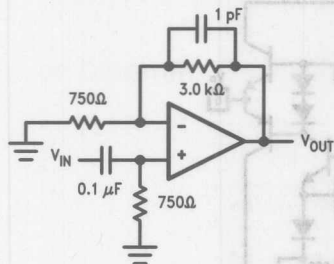
TL/H/9153-10

Noise-Gain Compensation for Gains ≤ 5



TL/H/9153-11

Video-Bandwidth Amplifier



TL/H/9153-12

$$R_X C_X \geq (2\pi \cdot 25 \text{ MHz})^{-1}$$

$$5 R_X = R_1 + R_F(1 + R_1/R_2)$$



LM6165/LM6265/LM6365 High Speed Operational Amplifier

General Description

The LM6165 family of high-speed amplifiers exhibits an excellent speed-power product in delivering 300 V/ μ s and 725 MHz GBW (stable for gains as low as +25) with only 5 mA of supply current. Further power savings and application convenience are possible by taking advantage of the wide dynamic range in operating supply voltage which extends all the way down to +5V.

These amplifiers are built with National's VIPTM (Vertically Integrated PNP) process which produces fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

Features

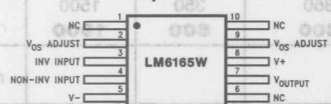
- High slew rate 300 V/ μ s
- High GBW product 725 MHz
- Low supply current 5 mA
- Fast settling 80 ns to 0.1%
- Low differential gain <0.1%
- Low differential phase <0.1°
- Wide supply range 4.75V to 32V
- Stable with unlimited capacitive load

Applications

- Video amplifier
- Wide-bandwidth signal conditioning
- Radar
- Sonar

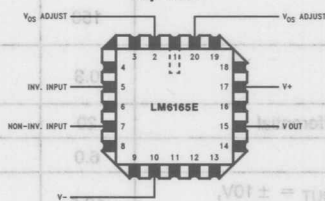
Connection Diagrams

**10-Lead Flatpak
Top View**

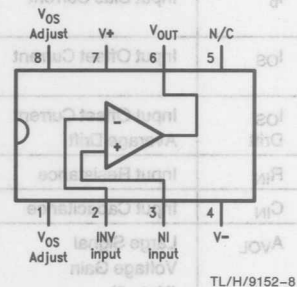


Order Number LM6165W/883
See NS Package Number W10A

**20-Lead LCC
Top View**



Order Number LM6165E/883
See NS Package Number E20A



Order Number LM6165J/883
See NS Package Number J08A

Order Number LM6365M
See NS Package Number M08A

Order Number LM6265N or
LM6365N
See NS Package Number N08E

| Temperature Range | | | Package | NSC Drawing |
|---|--|--|--------------------------|-------------|
| Military -55°C ≤ T _A ≤ +125°C | Industrial -25°C ≤ T _A ≤ +85°C | Commercial 0°C ≤ T _A ≤ +70°C | | |
| | LM6265N | LM6365N | 8-Pin Molded DIP | N08E |
| LM6165J/883 5962-8962501PA | | | 8-Pin Ceramic DIP | J08A |
| | | LM6365M | 8-Pin Molded Surface Mt. | M08A |
| LM6165E/883 5962-89625012A | | | 20-Lead LCC | E20A |
| LM6165W/883 5962-8962501HA | | | 10-Pin Ceramic Flatpak | W10A |

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|--------------------------------|
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 6) | $\pm 8V$ |
| Common-Mode Voltage Range (Note 10) | $(V^+ - 0.7V)$ to $(V^- - 7V)$ |
| Output Short Circuit to GND (Note 1) | Continuous |
| Soldering Information | |
| Dual-In-Line Package (N, J) | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package (M) | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | |
|-----------------------------------|---|
| Storage Temp Range | -65°C to $+150^\circ\text{C}$ |
| Max Junction Temperature (Note 2) | 150°C |
| ESD Tolerance (Notes 6 and 7) | $\pm 700V$ |

Operating Ratings

| | |
|----------------------------|--|
| Temperature Range (Note 2) | |
| LM6165, LM6165J/883 | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| LM6265 | $-25^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LM6365 | $0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$ |
| Supply Voltage Range | 4.75V to 32V |

DC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15V$, $V_{CM} = 0$, $R_L \geq 100\text{ k}\Omega$ and $R_S = 50\Omega$ unless otherwise noted.

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typ | LM6165 Limit (Notes 3, 11) | LM6265 Limit (Note 3) | LM6365 Limit (Note 3) | Units |
|-------------------|--|---|-------|----------------------------------|-----------------------------|-----------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 1 | 3 4 | 3 4 | 6 7 | mV Max |
| V_{OS} Drift | Input Offset Voltage Average Drift | | 3 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_b | Input Bias Current | | 2.5 | 3 6 | 3 5 | 5 6 | μA Max |
| I_{OS} | Input Offset Current | | 150 | 350 800 | 350 600 | 1500 1900 | nA Max |
| I_{OS} Drift | Input Offset Current Average Drift | | 0.3 | | | | nA/ $^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 20 | | | | k Ω |
| C_{IN} | Input Capacitance | | 6.0 | | | | pF |
| A_{VOL} | Large Signal Voltage Gain (Note 9) | $V_{OUT} = \pm 10V$, $R_L = 2\text{ k}\Omega$ | 10.5 | 7.5 5.0 | 7.5 6.0 | 5.5 5.0 | V/mV Min |
| V_{CM} | Input Common-Mode Voltage Range | Supply = $\pm 15V$ | +14.0 | +13.9 +13.8 | +13.9 +13.8 | +13.8 +13.7 | V Min |
| | | | -13.6 | -13.4 -13.2 | -13.4 -13.2 | -13.3 -13.2 | V Min |
| | | Supply = +5V (Note 4) | 4.0 | 3.9 3.8 | 3.9 3.8 | 3.8 3.7 | V Min |
| | | | 1.4 | 1.6 1.8 | 1.6 1.8 | 1.7 1.8 | V Max |
| | | | | | | | |
| | | | | | | | |
| CMRR | Common-Mode Rejection Ratio | $-10V \leq V_{CM} \leq +10V$ | 102 | 88 82 | 88 84 | 80 78 | dB Min |
| PSRR | Power Supply Rejection Ratio | $\pm 10V \leq V \leq \pm 16V$ | 104 | 88 82 | 88 84 | 80 78 | dB Min |
| V_O | Output Voltage Swing | Supply = $\pm 15V$, $R_L = 2\text{ k}\Omega$ | +14.2 | +13.5 +13.3 | +13.5 +13.3 | +13.4 +13.3 | V Min |
| | | | -13.4 | -13.0 -12.7 | -13.0 -12.8 | -12.9 -12.8 | V Min |

DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = $\pm 15\text{V}$, $V_{\text{CM}} = 0$, $R_{\text{L}} \geq 100\text{ k}\Omega$ and $R_{\text{S}} = 50\Omega$ unless otherwise noted.

Boldface limits apply for $T_{\text{A}} = T_{\text{J}} = T_{\text{MIN}}$ to T_{MAX} ; all other limits $T_{\text{A}} = T_{\text{J}} = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typ | LM6165 | LM6265 | LM6365 | Units |
|-------------------------------|-------------------------------------|---|-----|------------------------|-------------------|-------------------|-----------|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| V_{O} (Continued) | Output Voltage Swing (Continued) | Supply = $+5\text{V}$ $R_{\text{L}} = 2\text{ k}\Omega$ (Note 4) | 4.2 | 3.5 3.3 | 3.5 3.3 | 3.4 3.3 | V Min |
| | | | 1.3 | 1.7 2.0 | 1.7 1.9 | 1.8 1.9 | V Max |
| | Output Short Circuit Current | Source | 65 | 30 20 | 30 25 | 30 25 | mA Min |
| | | Sink | 65 | 30 20 | 30 25 | 30 25 | mA Min |
| I_{S} | Supply Current | | 5.0 | 6.5 6.8 | 6.5 6.7 | 6.8 6.9 | mA Max |

AC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15\text{V}$, $V_{\text{CM}} = 0$, $R_{\text{L}} \geq 100\text{ k}\Omega$ and $R_{\text{S}} = 50\Omega$ unless otherwise noted.

Boldface limits apply for $T_{\text{A}} = T_{\text{J}} = T_{\text{MIN}}$ to T_{MAX} ; all other limits $T_{\text{A}} = T_{\text{J}} = 25^\circ\text{C}$. (Note 5)

| Symbol | Parameter | Conditions | Typ | LM6165 | LM6265 | LM6365 | Units |
|-------------------|----------------------------|--|------|------------------------|-------------------|-------------------|-------------------------|
| | | | | Limit (Notes 3, 11) | Limit (Note 3) | Limit (Note 3) | |
| GBW | Gain Bandwidth | $F = 20\text{ MHz}$ | 725 | 575 350 | 575 | 500 | MHz Min |
| | Product | Supply = $\pm 5\text{V}$ | 500 | | | | |
| SR | Slew Rate | $A_{\text{V}} = +25$ (Note 8) | 300 | 200 180 | 200 | 200 | V/ μs Min |
| | | Supply = $\pm 5\text{V}$ | 200 | | | | |
| PBW | Power Bandwidth Product | $V_{\text{OUT}} = 20\text{ V}_{\text{PP}}$ | 4.5 | | | | MHz |
| t_{S} | Settling Time | 10V Step to 0.1% $A_{\text{V}} = -25$, $R_{\text{L}} = 2\text{ k}\Omega$ | 80 | | | | ns |
| ϕ_{m} | Phase Margin | $A_{\text{V}} = +25$ | 45 | | | | Deg |
| A_{D} | Differential Gain | NTSC, $A_{\text{V}} = +25$ | <0.1 | | | | % |
| ϕ_{D} | Differential Phase | NTSC, $A_{\text{V}} = +25$ | <0.1 | | | | Deg |
| $e_{\text{np-p}}$ | Input Noise Voltage | $F = 10\text{ kHz}$ | 5 | | | | nV/ $\sqrt{\text{Hz}}$ |
| $i_{\text{np-p}}$ | Input Noise Current | $F = 10\text{ kHz}$ | 1.5 | | | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Continuous short-circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C .

Note 2: The typical junction-to-ambient thermal resistance of the molded plastic DIP (N) is $105^\circ\text{C}/\text{Watt}$, and the molded plastic SO (M) package is $155^\circ\text{C}/\text{Watt}$, and the cerdip (J) package is $125^\circ\text{C}/\text{Watt}$. All numbers apply for packages soldered directly into a printed circuit board.

Note 3: All limits guaranteed by testing or correlation.

Note 4: For single supply operation, the following conditions apply: $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 2.5\text{V}$, $V_{\text{OUT}} = 2.5\text{V}$. Pin 1 & Pin 8 (V_{OS} Adjust) are each connected to Pin 4 (V^-) to realize maximum output swing. This connection will degrade V_{OS} .

Note 5: $C_{\text{L}} \leq 5\text{ pF}$.

Note 6: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors and probable degradation of the input parameters (especially V_{OS} , I_{OS} , and Noise).

Note 7: The average voltage that the weakest pin combinations (those involving Pin 2 or Pin 3) can withstand and still conform to the datasheet limits. The test circuit used consists of the human body model of 100 pF in series with 1500Ω .

Note 8: $V_{\text{IN}} = 0.8\text{V}$ step. For supply = $\pm 5\text{V}$, $V_{\text{IN}} = 0.2\text{V}$ step.

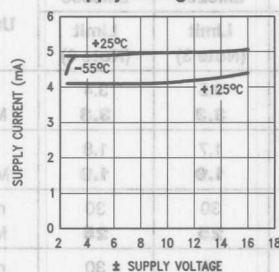
Note 9: Voltage Gain is the total output swing (20V) divided by the input signal required to produce that swing.

Note 10: The voltage between V^+ and either input pin must not exceed 36V .

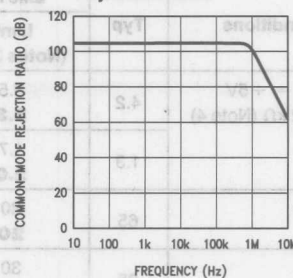
Note 11: A military RETS electrical test specification is available on request. At the time of printing, the LM6165J/883 RETS spec complied with the **Boldface** limits in this column. The LM6165J/883 may also be procured as Standard Military Drawing #5962-8962501PA.

Typical Performance Characteristics $R_L = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ unless otherwise specified

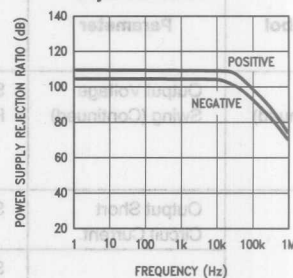
Supply Current vs Supply Voltage



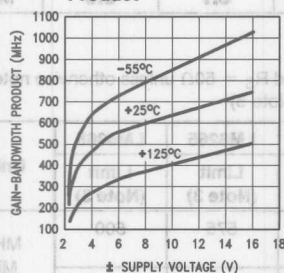
Common-Mode Rejection Ratio



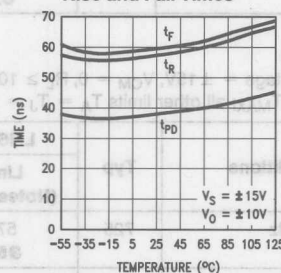
Power Supply Rejection Ratio



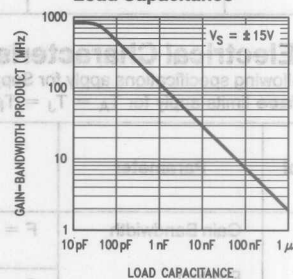
Gain-Bandwidth Product



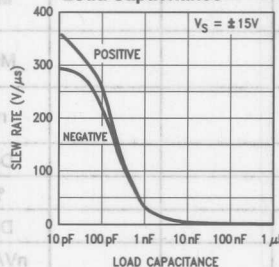
Propagation Delay, Rise and Fall Times



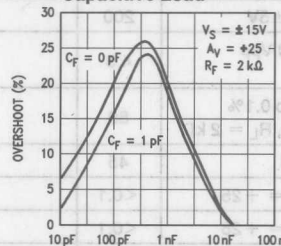
Gain-Bandwidth Product vs Load Capacitance



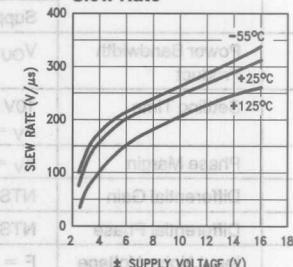
Slew Rate vs Load Capacitance



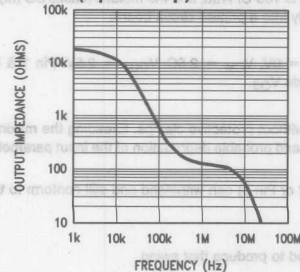
Overshoot vs Capacitive Load



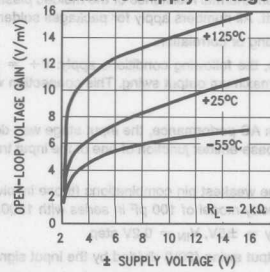
Slew Rate



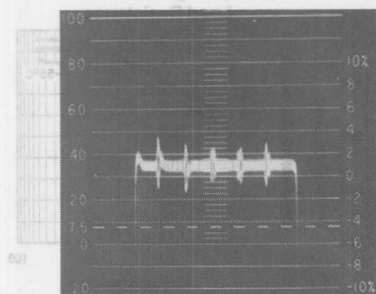
Output Impedance (Open-Loop)



Gain vs Supply Voltage

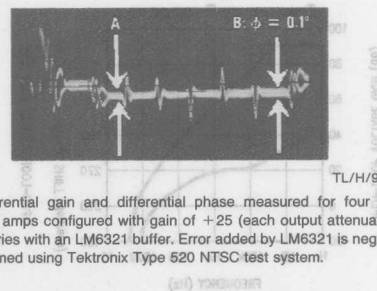


Differential Gain (Note)



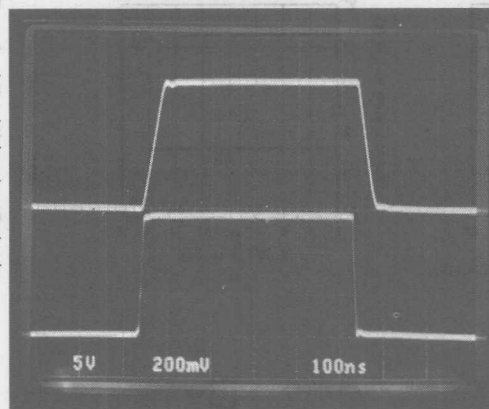
TL/H/9152-6

Differential Phase (Note)



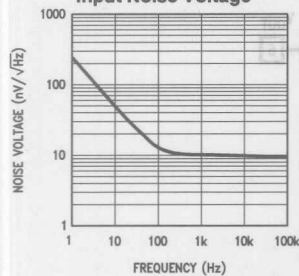
TL/H/9152-7

Note: Differential gain and differential phase measured for four series LM6365 op amps configured with gain of +25 (each output attenuated by 96%), in series with an LM6321 buffer. Error added by LM6321 is negligible. Test performed using Tektronix Type 520 NTSC test system.

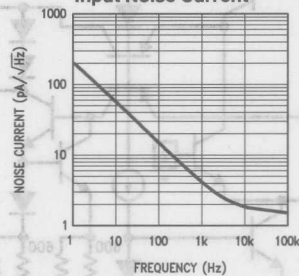
Step Response; $A_v = +25$ 

TL/H/9152-1

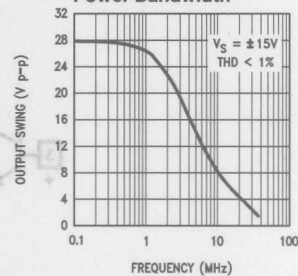
Input Noise Voltage



Input Noise Current



Power Bandwidth



TL/H/9152-9

Applications Tips

The LM6365 is stable for gains of 25 or greater. The LM6361 and LM6364, specified in separate datasheets, are compensated versions of the LM6365. The LM6361 is unity-gain stable, while the LM6364 is stable for gains as low as 5. The LM6361, and LM6364 have the same high slew rate as the LM6365, typically 300 V/ μ s.

To use the LM6365 for gains less than 25, a series resistor-capacitor network should be added between the input pins (as shown in the Typical Applications, Noise Gain Compensation) so that the high-frequency noise gain rises to at least 25.

Power supply bypassing will improve stability and transient response of the LM6365, and is recommended for every design. 0.01 μ F to 0.1 μ F ceramic capacitors should be

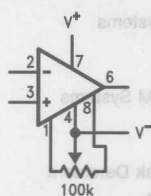
used (from each supply "rail" to ground); an additional 2.2 μ F to 10 μ F (tantalum) may be required for extra noise reduction.

Keep all leads short to reduce stray capacitance and lead inductance, and make sure ground paths are low-impedance, especially where heavier currents will be flowing. Stray capacitance in the circuit layout can cause signal coupling between adjacent nodes, and can cause circuit gain to unintentionally vary with frequency.

Breadboarded circuits will work best if they are built using generic PC boards with a good ground plane. If the op amps are used with sockets, as opposed to being soldered into the circuit, the additional input capacitance may degrade circuit performance.

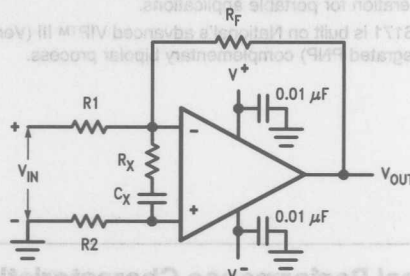
Typical Applications

Offset Voltage Adjustment



TL/H/9152-11

Noise-Gain Compensation



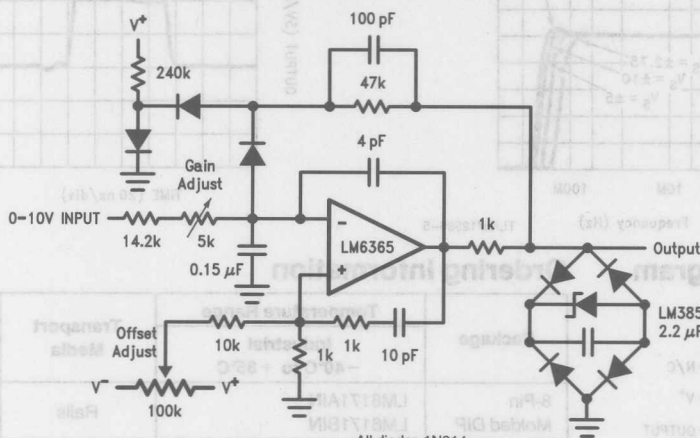
TL/H/9152-12

$$R_X C_X \geq 1/(2\pi \cdot 25 \text{ MHz})$$

$$[R_1 + R_F (1 + R_1/R_2)] = 25 R_X$$

1 MHz Voltage-to-Frequency Converter

($f_{OUT} = 1 \text{ MHz}$ for $V_{IN} = 10 \text{ V}$)



All diodes 1N914

TL/H/9152-13



LM6171 High Speed Low Power Low Distortion Voltage Feedback Amplifier

General Description

The LM6171 is a high speed unity-gain stable voltage feedback amplifier. It offers a high slew rate of $3600\text{V}/\mu\text{s}$ and a unity-gain bandwidth of 100MHz while consuming only 2.5mA of supply current. The LM6171 has very impressive AC and DC performance which is a great benefit for high speed signal processing and video applications.

The $\pm 15\text{V}$ power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM6171 has high output current drive, low SFDR and THD, ideal for ADC/DAC systems. The LM6171 is specified for $\pm 5\text{V}$ operation for portable applications.

The LM6171 is built on National's advanced VIPTM III (Vertically Integrated PNP) complementary bipolar process.

Features (Typical Unless Otherwise Noted)

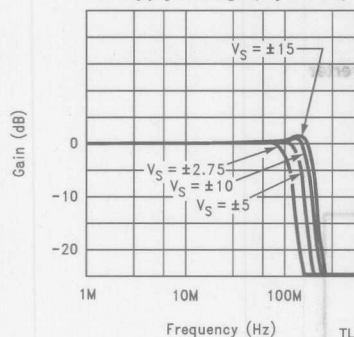
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate $3600\text{V}/\mu\text{s}$
- Wide Unity-Gain-Bandwidth Product 100MHz
- -3dB Frequency @ $A_V = +2$ 62MHz
- Low Supply Current 2.5mA
- High CMRR 110dB
- High Open Loop Gain 90dB
- Specified for $\pm 15\text{V}$ and $\pm 5\text{V}$ Operation

Applications

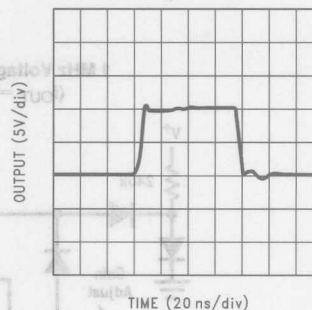
- Multimedia Broadcast Systems
- Line Drivers, Switchers
- Video Amplifiers
- NTSC, PAL® and SECAM Systems
- ADC/DAC Buffers
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- Instrumentation Amplifier
- Active Filters

Typical Performance Characteristics

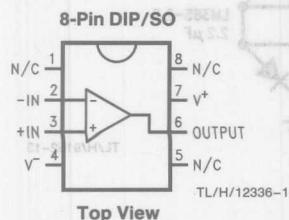
Closed Loop Frequency Response vs Supply Voltage ($A_V = +1$)



Large Signal Pulse Response
 $A_V = +1$, $V_S = \pm 15$



Connection Diagram



Ordering Information

| Package | Temperature Range | Transport Media | NSC Drawing |
|------------------------|------------------------------|-----------------|-------------|
| | Industrial -40°C to +85°C | | |
| 8-Pin Molded DIP | LM6171AIN LM6171BIN | Rails | N08E |
| 8-Pin Small Outline | LM6171AIM, LM6171BIM | Rails | M08A |
| | LM6171AIMX, LM6171BIMX | Tape and Reel | |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|---|
| ESD Tolerance (Note 2) | 2.5 kV |
| Supply Voltage ($V^+ - V^-$) | 36V |
| Differential Input Voltage (Note 11) | $\pm 10V$ |
| Common-Mode Voltage Range | $V^+ - 1.4V$ to $V^- + 1.4V$ |
| Output Short Circuit to Ground (Note 3) | Continuous |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Maximum Junction Temperature (Note 4) | 150°C |

Operating Ratings (Note 1)

| | |
|--------------------------------------|---|
| Supply Voltage | $2.75V \leq V^+ \leq 18V$ |
| Junction Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LM6171AI, LM6171BI | |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 108°C/W |
| M Package, 8-Pin Surface Mount | 172°C/W |

 $\pm 15V$ DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$, and $R_L = 1\text{ k}\Omega$. **Boldface** limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6171AI Limit (Note 6) | LM6171BI Limit (Note 6) | Units |
|---------------|------------------------------------|--------------------------|-----------------|-------------------------------|-------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 1.5 | 3 5 | 6 8 | mV max |
| $TC_{V_{OS}}$ | Input Offset Voltage Average Drift | | 6 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 1 | 3 4 | 3 4 | μA max |
| I_{OS} | Input Offset Current | | 0.03 | 2 3 | 2 3 | μA max |
| R_{IN} | Input Resistance | Common Mode | 40 | | | $\text{M}\Omega$ |
| | | Differential Mode | 4.9 | | | |
| R_O | Open Loop Output Resistance | | 14 | | | Ω |
| CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm 10V$ | 110 | 80 75 | 75 70 | dB min |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 15V - \pm 5V$ | 95 | 85 80 | 80 75 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | CMRR $\geq 60\text{ dB}$ | ± 13.5 | | | V |
| A_V | Large Signal Voltage Gain (Note 7) | $R_L = 1\text{ k}\Omega$ | 90 | 80 70 | 80 70 | dB min |
| | | $R_L = 100\Omega$ | 83 | 70 60 | 70 60 | dB min |
| V_O | Output Swing | $R_L = 1\text{ k}\Omega$ | 13.3 | 12.5 12 | 12.5 12 | V min |
| | | | -13.3 | -12.5 -12 | -12.5 -12 | V max |
| | | $R_L = 100\Omega$ | 11.6 | 9 8.5 | 9 8.5 | V min |
| | | | -10.5 | -9 -8.5 | -9 -8.5 | V max |

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6171AI Limit (Note 6) | LM6171BI Limit (Note 6) | Units |
|----------|---|-----------------------------|-----------------|-------------------------------|-------------------------------|-----------|
| | Continuous Output Current (Open Loop) (Note 8) | Sourcing, $R_L = 100\Omega$ | 116 | 90 85 | 90 85 | mA min |
| | | Sinking, $R_L = 100\Omega$ | 105 | 90 85 | 90 85 | mA max |
| | Continuous Output Current (in Linear Region) | Sourcing, $R_L = 10\Omega$ | 100 | | | mA |
| | | Sinking, $R_L = 10\Omega$ | 80 | | | mA |
| I_{SC} | Output Short Circuit Current | Sourcing | 135 | | | mA |
| | | Sinking | 135 | | | mA |
| I_S | Supply Current | | 2.5 | 4 4.5 | 4 4.5 | mA max |

$\pm 15V$ AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = +15V$, $V^- = -15V$, $V_{CM} = 0V$, and $R_L = 1\text{ k}\Omega$. **Boldface** limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6171AI Limit (Note 6) | LM6171BI Limit (Note 6) | Units |
|----------|---------------------------------|---|-----------------|-------------------------------|-------------------------------|----------------|
| SR | Slew Rate (Note 9) | $A_V = +2$, $V_{IN} = 13\text{ V}_{PP}$ | 3600 | | | $V/\mu s$ |
| | | $A_V = +2$, $V_{IN} = 10\text{ V}_{PP}$ | 3000 | | | |
| GBW | Unity Gain-Bandwidth Product | | 100 | | | MHz |
| | | $A_V = +1$ | 160 | | | MHz |
| | | $A_V = +2$ | 62 | | | MHz |
| ϕ_m | Phase Margin | | 40 | | | deg |
| t_s | Settling Time (0.1%) | $A_V = -1$, $V_{OUT} = \pm 5V$ $R_L = 500\Omega$ | 35 | | | ns |
| | Propagation Delay | $V_{IN} = \pm 5V$, $R_L = 500\Omega$, $A_V = -2$ | 6 | | | ns |
| A_D | Differential Gain (Note 10) | | 0.03 | | | % |
| ϕ_D | Differential Phase (Note 10) | | 0.5 | | | deg |
| e_n | Input-Referred Voltage Noise | $f = 1\text{ kHz}$ | 12 | | | nV/\sqrt{Hz} |
| i_n | Input-Referred Current Noise | $f = 1\text{ kHz}$ | 1 | | | pA/\sqrt{Hz} |

±5V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V_+ = +5\text{V}$, $V_- = -5\text{V}$, $V_{CM} = 0\text{V}$, and $R_L = 1\text{ k}\Omega$. **Boldface** limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6171AI Limit (Note 6) | LM6171BI Limit (Note 6) | Units |
|-------------|---|---|-----------------|-------------------------------|-------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 1.2 | 3 5 | 6 8 | mV max |
| $TC V_{OS}$ | Input Offset Voltage Average Drift | | 4 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 1 | 2.5 3.5 | 2.5 3.5 | μA max |
| I_{OS} | Input Offset Current | | 0.03 | 1.5 2.2 | 1.5 2.2 | μA max |
| R_{IN} | Input Resistance | Common Mode | 40 | | | $\text{M}\Omega$ |
| | | Differential Mode | 4.9 | | | |
| R_O | Open Loop Output Resistance | | 14 | | | Ω |
| CMRR | Common Mode Rejection Ratio | $V_{CM} = \pm 2.5\text{V}$ | 105 | 80 75 | 75 70 | dB min |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 15\text{V}$ to $\pm 5\text{V}$ | 95 | 85 80 | 80 75 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | CMRR $\geq 60\text{ dB}$ | ± 3.7 | | | V |
| A_V | Large Signal Voltage Gain (Note 7) | $R_L = 1\text{ k}\Omega$ | 84 | 75 65 | 75 65 | dB min |
| | | $R_L = 100\Omega$ | 80 | 70 60 | 70 60 | dB min |
| V_O | Output Swing | $R_L = 1\text{ k}\Omega$ | 3.5 | 3.2 3 | 3.2 3 | V min |
| | | | -3.4 | -3.2 -3 | -3.2 -3 | V max |
| | | $R_L = 100\Omega$ | 3.2 | 2.8 2.5 | 2.8 2.5 | V min |
| | | | -3.0 | -2.8 -2.5 | -2.8 -2.5 | V max |
| | | | | | | |
| | | | | | | |
| | Continuous Output Current (Open Loop) (Note 8) | Sourcing, $R_L = 100\Omega$ | 32 | 28 25 | 28 25 | mA min |
| | | Sinking, $R_L = 100\Omega$ | 30 | 28 25 | 28 25 | mA max |
| I_{SC} | Output Short Circuit Current | Sourcing | 130 | | | mA |
| | | Sinking | 100 | | | mA |
| I_S | Supply Current | | 2.3 | 3 3.5 | 3 3.5 | mA max |

±5V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = +5\text{V}$, $V^- = -5\text{V}$, $V_{CM} = 0\text{V}$, and $R_L = 1\text{ k}\Omega$. **Boldface** limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LM6171AI Limit (Note 6) | LM6171BI Limit (Note 6) | Units |
|----------|------------------------------|--|-----------------|-------------------------------|-------------------------------|--------------------------------------|
| SR | Slew Rate (Note 9) | $A_V = +2$, $V_{IN} = 3.5\text{ V}_{PP}$ | 750 | | | $\text{V}/\mu\text{s}$ |
| GBW | Unity Gain-Bandwidth Product | | 70 | | | MHz |
| | −3 dB Frequency | $A_V = +1$ | 130 | | | MHz |
| | | $A_V = +2$ | 45 | | | |
| ϕ_m | Phase Margin | | 57 | | | deg |
| t_s | Settling Time (0.1%) | $A_V = -1$, $V_{OUT} = +1\text{V}$, $R_L = 500\Omega$ | 48 | | | ns |
| | Propagation Delay | $V_{IN} = \pm 1\text{V}$, $R_L = 500\Omega$, $A_V = -2$ | 8 | | | ns |
| A_D | Differential Gain (Note 10) | | 0.04 | | | % |
| ϕ_D | Differential Phase (Note 10) | | 0.7 | | | deg |
| e_n | Input-Referred Voltage Noise | $f = 1\text{ kHz}$ | 11 | | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| i_n | Input-Referred Current Noise | $f = 1\text{ kHz}$ | 1 | | | $\frac{\text{pA}}{\sqrt{\text{Hz}}}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF.

Note 3: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Large signal voltage gain is the total output swing divided by the input signal required to produce that swing. For $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 5\text{V}$. For $V_S = +5\text{V}$, $V_{OUT} = +1\text{V}$.

Note 8: The open loop output current is the output swing with the 100 Ω load resistor divided by that resistor.

Note 9: Slew rate is the average of the rising and falling slew rates.

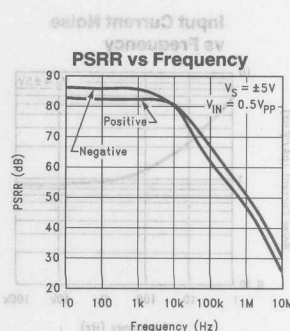
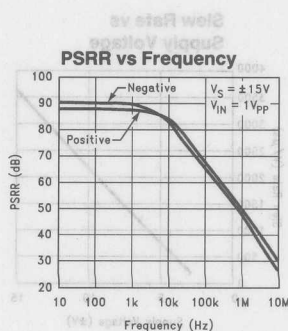
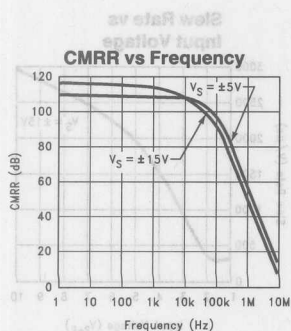
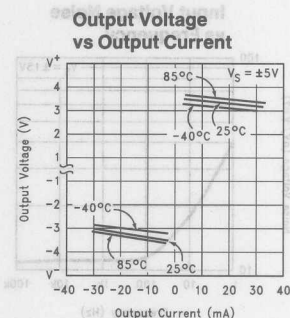
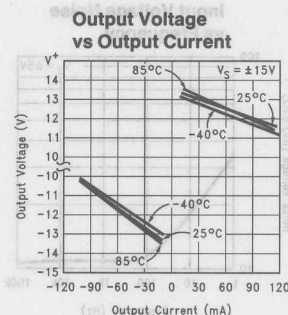
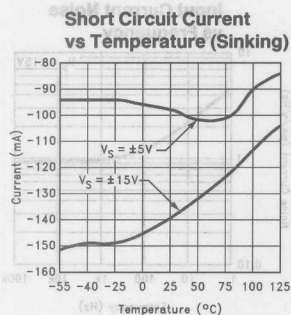
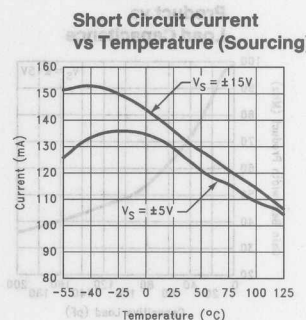
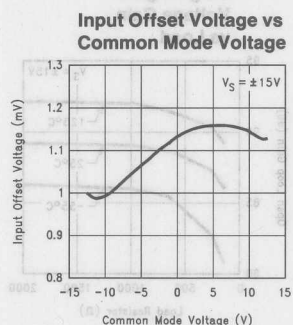
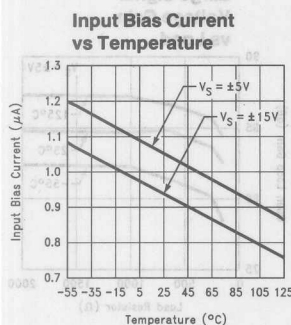
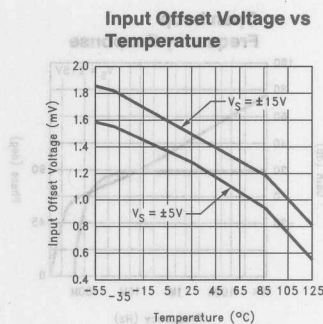
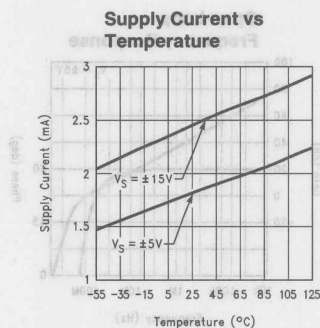
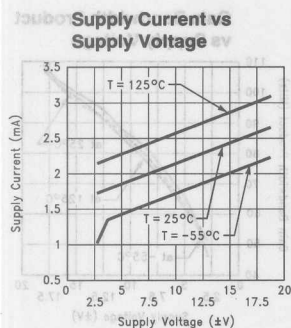
Note 10: Differential gain and phase are measured with $A_V = +2$, $V_{IN} = 1\text{ V}_{PP}$ at 3.58 MHz and both input and output 75 Ω terminated.

Note 11: Differential input voltage is measured at $V_S = \pm 15\text{V}$.

| | | | | | | |
|----------|--------|--------|--------|-----------------------------|---|-----|
| V | -2.5 | -2.5 | -2.5 | | | |
| x_{am} | -2.5 | -2.5 | -2.5 | | | |
| A_m | 28 | 28 | 28 | Sourcing, $R_L = 100\Omega$ | Continuous Output Current (Open Loop) (Note 8) | |
| x_{am} | 28 | 28 | 28 | Sinking, $R_L = 100\Omega$ | | |
| A_m | | | 150 | Sourcing | Output Short | 150 |
| A_m | | | 100 | Sinking | Circuit Current | 100 |
| A_m | 3 | 3 | 2.5 | | Supply Current | 3 |
| x_{am} | 2.5 | 2.5 | 2.5 | | | |

Typical Performance Characteristics

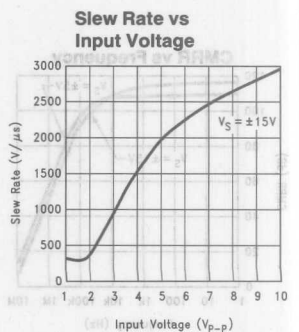
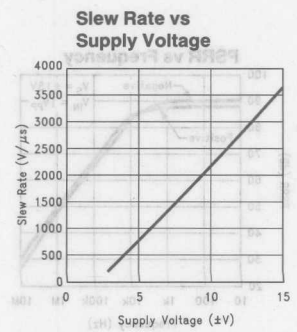
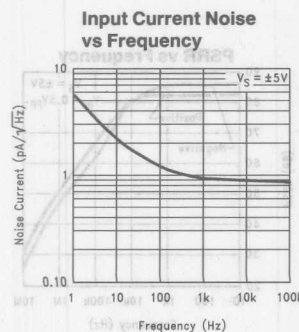
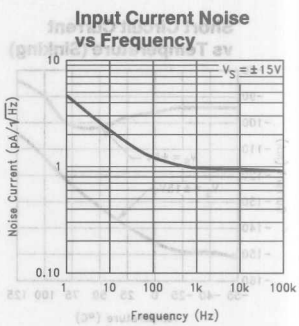
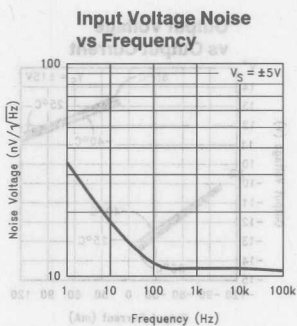
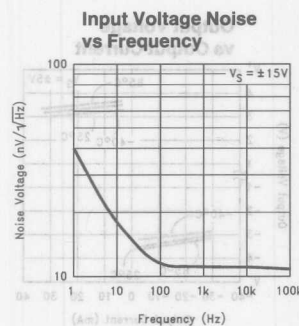
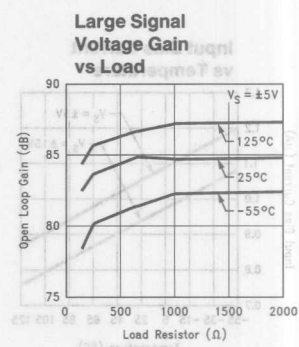
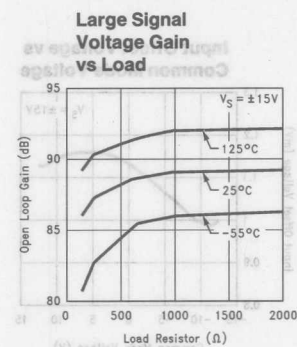
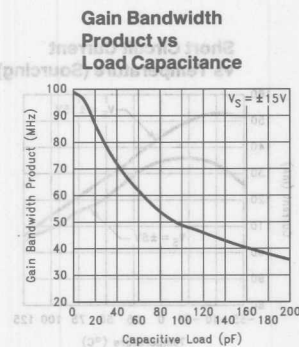
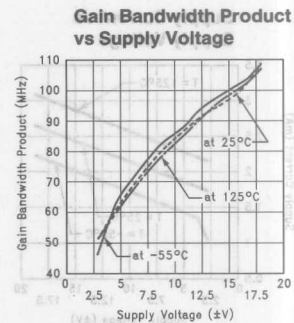
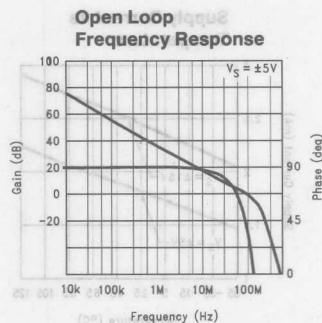
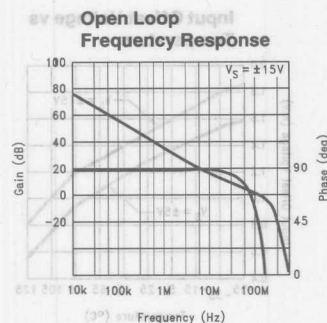
Unless otherwise noted, $T_A = 25^\circ\text{C}$



TL/H/12336-3

Typical Performance Characteristics

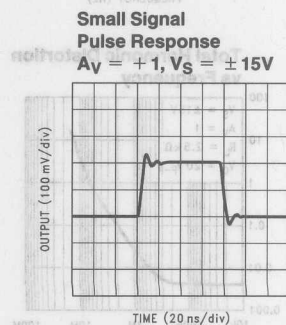
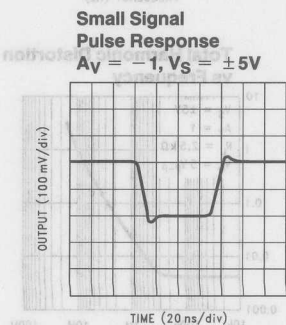
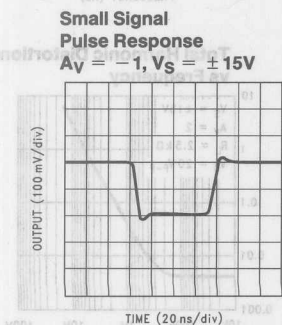
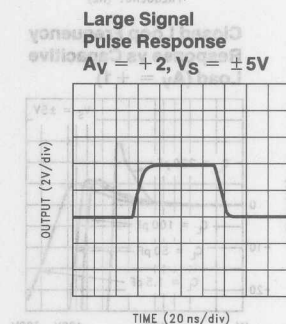
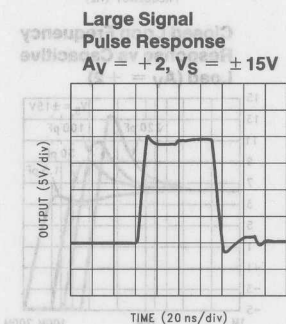
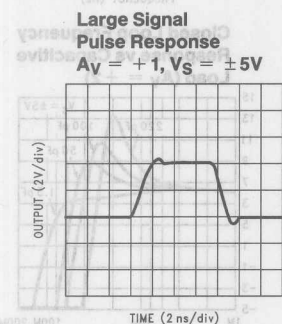
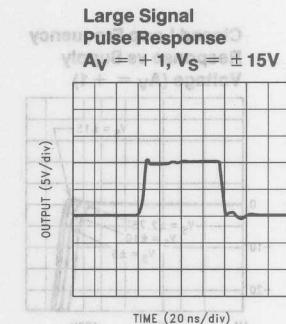
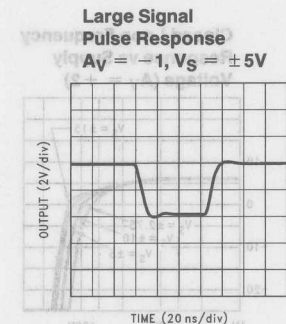
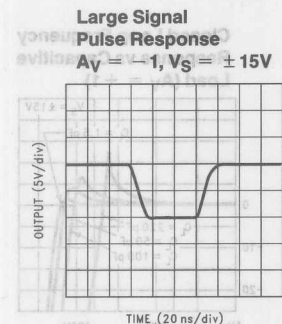
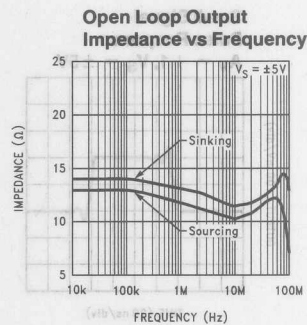
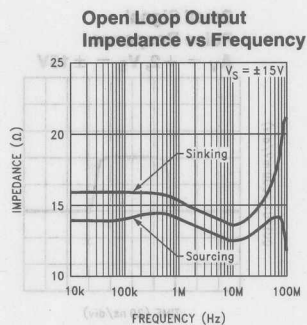
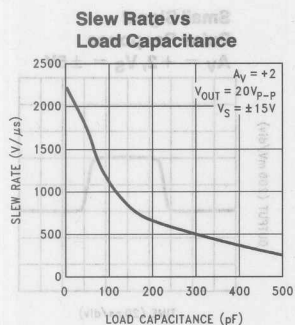
Unless otherwise noted, $T_A = 25^\circ\text{C}$ (Continued)



TL/H/12336-4

Typical Performance Characteristics

Unless otherwise noted, $T_A = 25^\circ\text{C}$ (Continued)

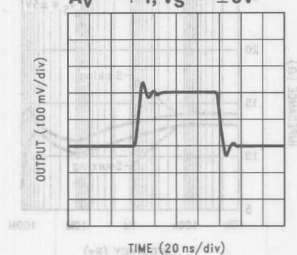


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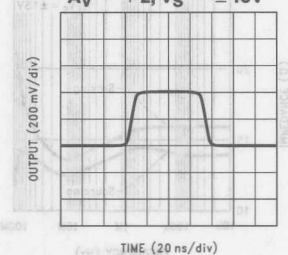
Typical Performance Characteristics

Unless otherwise noted, $T_A = 25^\circ\text{C}$ (Continued)

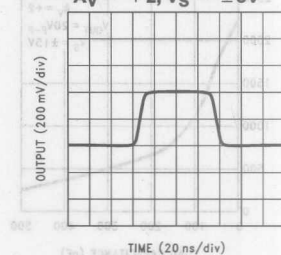
Small Signal Pulse Response
 $A_V = +1, V_S = \pm 5\text{V}$



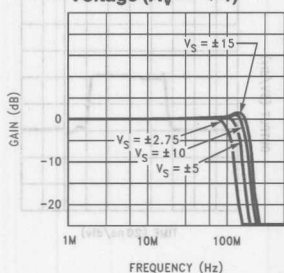
Small Signal Pulse Response
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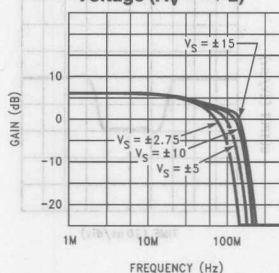
Small Signal Pulse Response
 $A_V = +2, V_S = \pm 5\text{V}$



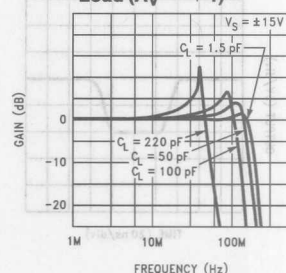
Closed Loop Frequency Response vs Supply Voltage ($A_V = +1$)



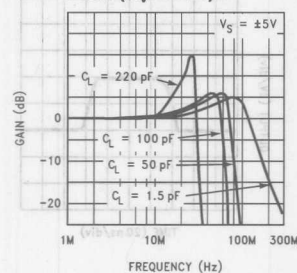
Closed Loop Frequency Response vs Supply Voltage ($A_V = +2$)



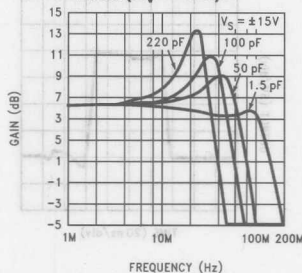
Closed Loop Frequency Response vs Capacitive Load ($A_V = +1$)



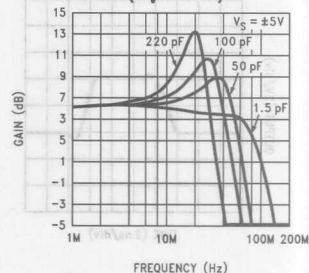
Closed Loop Frequency Response vs Capacitive Load ($A_V = +1$)



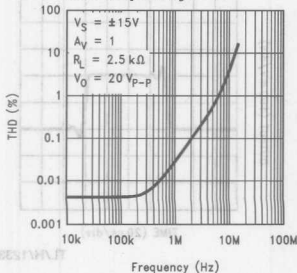
Closed Loop Frequency Response vs Capacitive Load ($A_V = +2$)



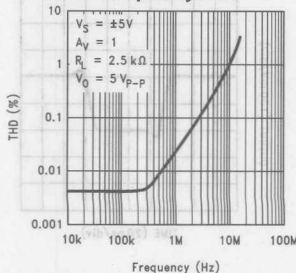
Closed Loop Frequency Response vs Capacitive Load ($A_V = +2$)



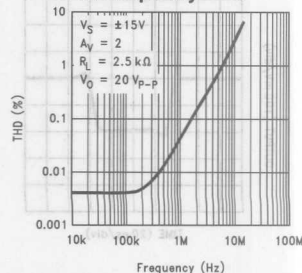
Total Harmonic Distortion vs Frequency



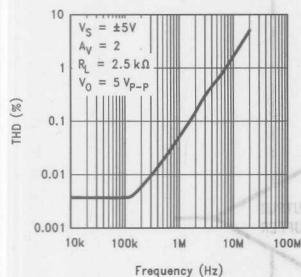
Total Harmonic Distortion vs Frequency



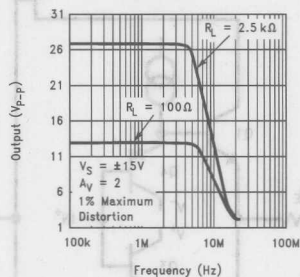
Total Harmonic Distortion vs Frequency



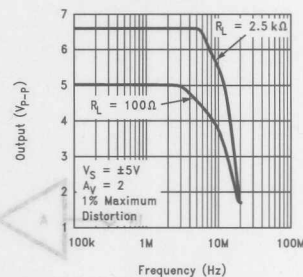
Total Harmonic Distortion vs Frequency



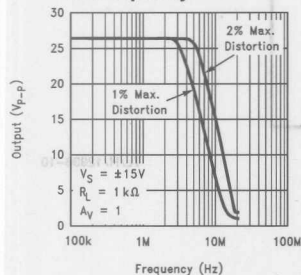
Undistorted Output Swing vs Frequency



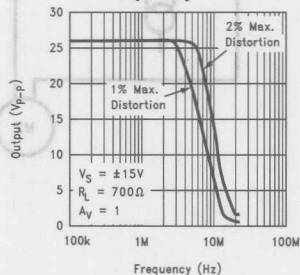
Undistorted Output Swing vs Frequency



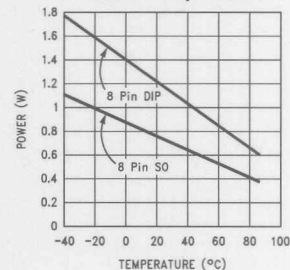
Undistorted Output Swing vs Frequency



Undistorted Output Swing vs Frequency

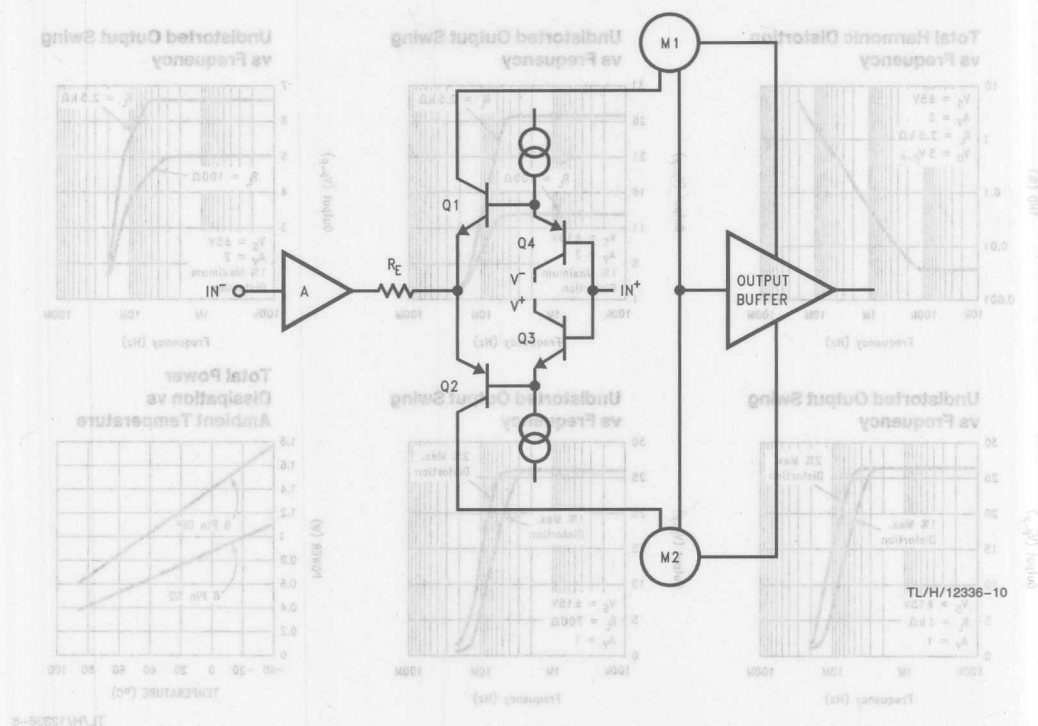


Total Power Dissipation vs Ambient Temperature



TL/H/12336-8

LM6171 Simplified Schematic



Application Information

LM6171 Performance Discussion

The LM6171 is a high speed, unity-gain stable voltage feedback amplifier. It consumes only 2.5 mA supply current while providing a gain-bandwidth product of 100 MHz and a slew rate of 3600V/ μ s. It also has other great features such as low differential gain and phase and high output current. The LM6171 is a good choice in high speed circuits.

The LM6171 is a true voltage feedback amplifier. Unlike current feedback amplifiers (CFAs) with a low inverting input impedance and a high non-inverting input impedance, both inputs of voltage feedback amplifiers (VFAs) have high impedance nodes. The low impedance inverting input in CFAs will couple with feedback capacitor and cause oscillation. As a result, CFAs cannot be used in traditional op amp circuits such as photodiode amplifiers, I-to-V converters and integrators.

LM6171 Circuit Operation

The class AB input stage in LM6171 is fully symmetrical and has a similar slewing characteristic to the current feedback amplifiers. In the LM6171 Simplified Schematic, Q1 through Q4 form the equivalent of the current feedback input buffer, R_E the equivalent of the feedback resistor, and stage A buffers the inverting input. The triple-buffered output stage isolates the gain stage from the load to provide low output impedance.

LM6171 Slew Rate Characteristic

The slew rate of LM6171 is determined by the current available to charge and discharge an internal high impedance node capacitor. The current is the differential input voltage divided by the total degeneration resistor R_E . Therefore, the slew rate is proportional to the input voltage level, and the higher slew rates are achievable in the lower gain configurations.

When a very fast large signal pulse is applied to the input of an amplifier, some overshoot or undershoot occurs. By placing an external series resistor such as 1 k Ω to the input of LM6171, the bandwidth is reduced to help lower the overshoot.

Layout Consideration

PRINTED CIRCUIT BOARDS AND HIGH SPEED OP AMPS

There are many things to consider when designing PC boards for high speed op amps. Without proper caution, it is very easy and frustrating to have excessive ringing, oscillation and other degraded AC performance in high speed circuits. As a rule, the signal traces should be short and wide to provide low inductance and low impedance paths. Any unused board space needs to be grounded to reduce stray signal pickup. Critical components should also be grounded at a common point to eliminate voltage drop. Sockets add capacitance to the board and can affect frequency performance. It is better to solder the amplifier directly into the PC board without using any socket.

USING PROBES

Active (FET) probes are ideal for taking high frequency measurements because they have wide bandwidth, high input impedance and low input capacitance. However, the probe ground leads provide a long ground loop that will pro-

duce errors in measurement. Instead, the probes can be grounded directly by removing the ground leads and probe jackets and using scope probe jacks.

COMPONENTS SELECTION AND FEEDBACK RESISTOR

It is important in high speed applications to keep all component leads short because wires are inductive at high frequency. For discrete components, choose carbon composition-type resistors and mica-type capacitors. Surface mount components are preferred over discrete components for minimum inductive effect.

Large values of feedback resistors can couple with parasitic capacitance and cause undesirable effects such as ringing or oscillation in high speed amplifiers. For LM6171, a feedback resistor of 510 Ω gives optimal performance.

Compensation for Input Capacitance

The combination of an amplifier's input capacitance with the gain setting resistors adds a pole that can cause peaking or oscillation. To solve this problem, a feedback capacitor with a value

$$C_F > (R_G \times C_{IN})/R_F$$

can be used to cancel that pole. For LM6171, a feedback capacitor of 2 pF is recommended. Figure 1 illustrates the compensation circuit.

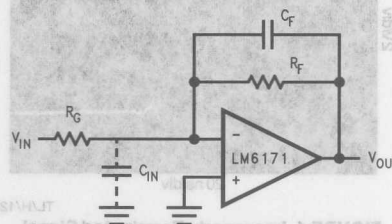


FIGURE 1. Compensating for Input Capacitance

Power Supply Bypassing

Bypassing the power supply is necessary to maintain low power supply impedance across frequency. Both positive and negative power supplies should be bypassed individually by placing 0.01 μ F ceramic capacitors directly to power supply pins and 2.2 μ F tantalum capacitors close to the power supply pins.

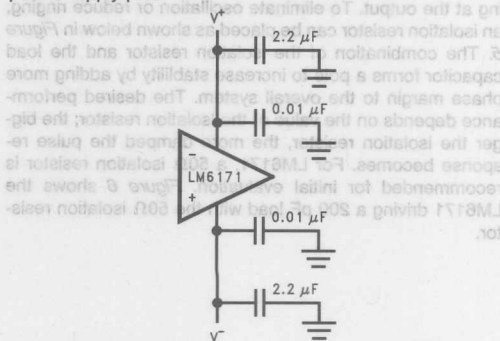


FIGURE 2. Power Supply Bypassing

Application Information (Continued)

Termination

In high frequency applications, reflections occur if signals are not properly terminated. *Figure 3* shows a properly terminated signal while *Figure 4* shows an improperly terminated signal.

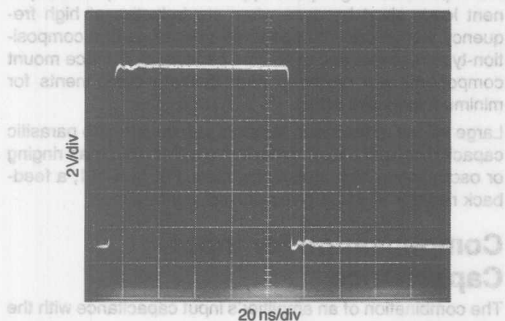


FIGURE 3. Properly Terminated Signal

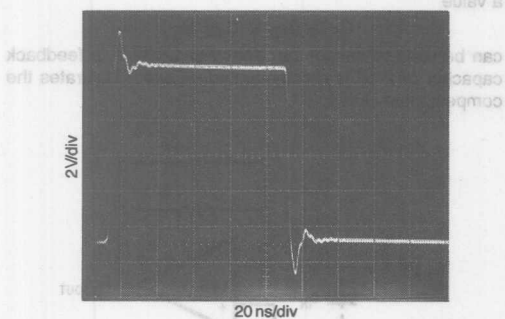


FIGURE 4. Improperly Terminated Signal

To minimize reflection, coaxial cable with matching characteristic impedance to the signal source should be used. The other end of the cable should be terminated with the same value terminator or resistor. For the commonly used cables, RG59 has 75Ω characteristic impedance, and RG58 has 50Ω characteristic impedance.

Driving Capacitive Loads

Amplifiers driving capacitive loads can oscillate or have ringing at the output. To eliminate oscillation or reduce ringing, an isolation resistor can be placed as shown below in *Figure 5*. The combination of the isolation resistor and the load capacitor forms a pole to increase stability by adding more phase margin to the overall system. The desired performance depends on the value of the isolation resistor; the bigger the isolation resistor, the more damped the pulse response becomes. For LM6171, a 50Ω isolation resistor is recommended for initial evaluation. *Figure 6* shows the LM6171 driving a 200 pF load with the 50Ω isolation resistor.

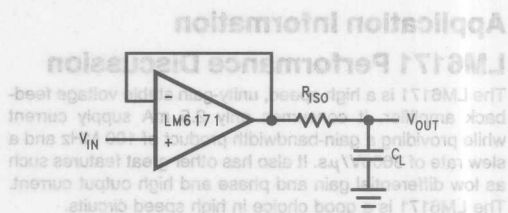
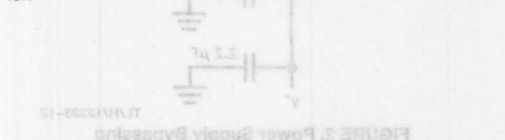


FIGURE 5. Isolation Resistor Used to Drive Capacitive Load

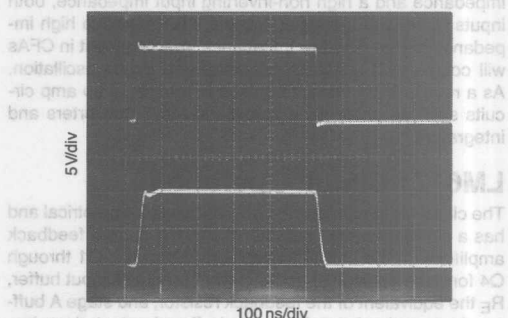


FIGURE 6. The LM6171 Driving a 200 pF Load with a 50Ω Isolation Resistor

Power Dissipation

The maximum power allowed to dissipate in a device is defined as:

$$P_D = (T_{J(max)} - T_A) / \theta_{JA}$$

Where P_D is the power dissipation in a device

$T_{J(max)}$ is the maximum junction temperature

T_A is the ambient temperature

θ_{JA} is the thermal resistance of a particular package

For example, for the LM6171 in a SO-8 package, the maximum power dissipation at 25°C ambient temperature is 730 mW.

Thermal resistance, θ_{JA} , depends on parameters such as die size, package size and package material. The smaller the die size and package, the higher θ_{JA} becomes. The 8-pin DIP package has a lower thermal resistance (108°C/W) than that of 8-pin SO (172°C/W). Therefore, for higher dissipation capability, use an 8-pin DIP package.

The total power dissipated in a device can be calculated as:

$$P_D = P_Q + P_L$$

P_Q is the quiescent power dissipated in a device with no load connected at the output. P_L is the power dissipated in the device with a load connected at the output; it is not the power dissipated by the load.

Furthermore,

$$P_Q = \text{supply current} \times \text{total supply voltage with no load}$$

$$P_L = \text{output current} \times (\text{voltage difference between supply voltage and output voltage of the same supply})$$

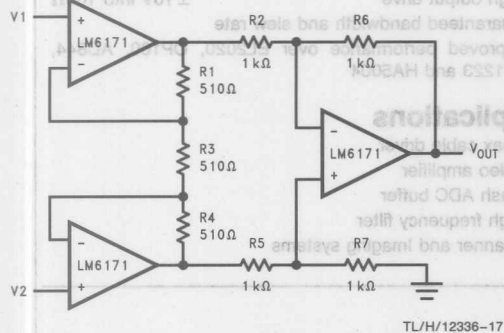
Application Information (Continued)

For example, the total power dissipated by the LM6171 with $V_S = \pm 15V$ and output voltage of 10V into 1 k Ω load resistor (one end tied to ground) is

$$\begin{aligned} P_D &= P_Q + P_L \\ &= (2.5 \text{ mA}) \times (30V) + (10 \text{ mA}) \times (15V - 10V) \\ &= 75 \text{ mW} + 50 \text{ mW} \\ &= 125 \text{ mW} \end{aligned}$$

Application Circuits

Fast Instrumentation Amplifier

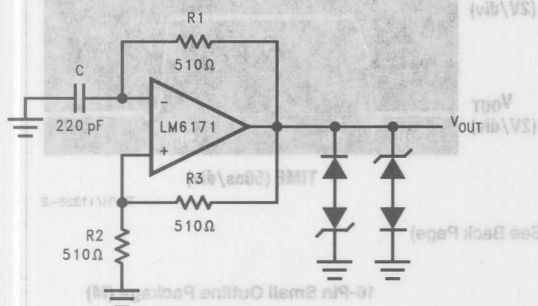


$$V_{IN} = V_2 - V_1$$

$$\text{if } R_6 = R_2, R_7 = R_5 \text{ and } R_1 = R_4$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_6}{R_2} \left(1 + 2 \frac{R_1}{R_3} \right) = 3$$

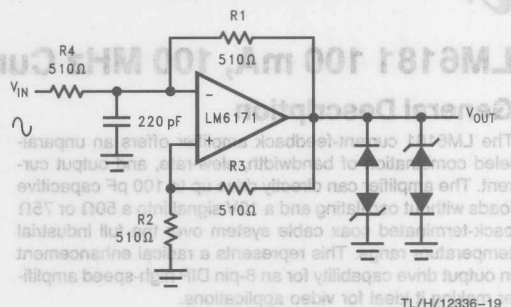
Multivibrator



$$f = \frac{1}{2 \left(R_1 C \ln \left(1 + 2 \frac{R_2}{R_3} \right) \right)}$$

$$f = 4 \text{ MHz}$$

Pulse Width Modulator



Design Kit

A design kit is available for the LM6171. The design kit contains:

- High Speed Evaluation Board
- LM6171 in 8-pin DIP Package
- LM6171 Datasheet
- Pspice Macromodel Diskette With the LM6171 Macro-model
- An Amplifier Selection Guide

Pitch Pack

A pitch pack is available for the LM6171. The pitch pack contains:

- High Speed Evaluation Board
- LM6171 in 8-pin DIP Package
- LM6171 Datasheet
- Pspice Macromodel Diskette With the LM6171 Macro-model

Contact your local National Semiconductor sales office to obtain a pitch pack.

LM6181 100 mA, 100 MHz Current Feedback Amplifier

General Description

The LM6181 current-feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. The amplifier can directly drive up to 100 pF capacitive loads without oscillating and a 10V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for an 8-pin DIP high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIF™ II (Vertically Integrated PNP) process, the LM6181 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at $A_V = -1$, 60 MHz at $A_V = -10$. With a slew rate of 2000V/μs, 2nd harmonic distortion of -50 dBc at 10 MHz and settling time of 50 ns (0.1%) the LM6181 dynamic performance makes it ideal for data acquisition, high speed ATE, and precision pulse amplifier applications.

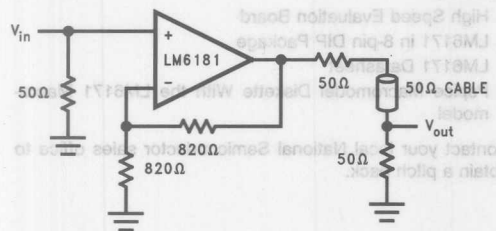
Features (Typical unless otherwise noted)

- Slew rate 2000 V/μs
- Settling time (0.1%) 50 ns
- Characterized for supply ranges ±5V and ±15V
- Low differential gain and phase error 0.05%, 0.04°
- High output drive ±10V into 100Ω
- Guaranteed bandwidth and slew rate
- Improved performance over EL2020, OP160, AD844, LT1223 and HA5004

Applications

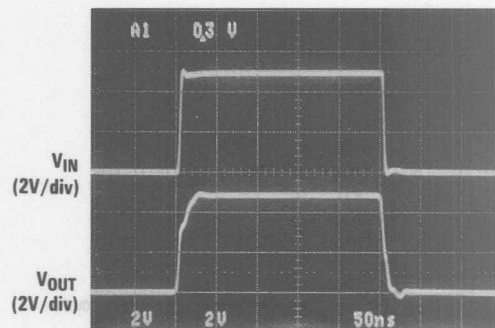
- Coax cable driver
- Video amplifier
- Flash ADC buffer
- High frequency filter
- Scanner and Imaging systems

Typical Application



Cable Driver

TL/H/11328-1

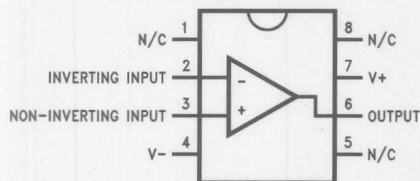


TIME (50ns/div)

TL/H/11328-2

Connection Diagrams (For Ordering Information See Back Page)

8-Pin Dual-In-Line Package (N)/ Small Outline (M-8)

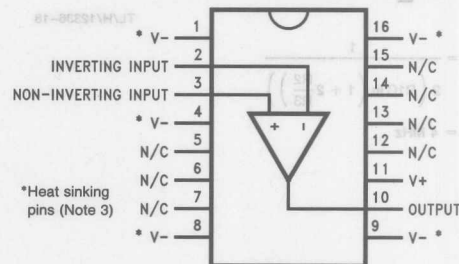


TL/H/11328-3

Order Number LM6181IN, LM6181AIN,
LM6181AMN, LM6181AIM-8, LM6181IM-8
or LM6181AMJ/883

See NS Package Number J08A, M08A or N08E

16-Pin Small Outline Package (M)



TL/H/11328-4

Order Number LM6181IM or LM6181AIM
See NS Package Number M16A

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|----------------------|
| Supply Voltage | $\pm 18V$ |
| Differential Input Voltage | $\pm 6V$ |
| Input Voltage | \pm Supply Voltage |
| Inverting Input Current | 15 mA |
| Soldering Information | |
| Dual-In-Line Package (N) Soldering (10 sec) | 260°C |
| Small Outline Package (M) | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

| | |
|------------------------------|--|
| Storage Temperature Range | $-65^{\circ}\text{C} \leq T_J \leq +150^{\circ}\text{C}$ |
| Maximum Junction Temperature | 150°C |
| ESD Rating (Note 2) | $\pm 3000V$ |

Operating Ratings

| | |
|--|--|
| Supply Voltage Range | 7V to 32V |
| Junction Temperature Range (Note 3) | |
| LM6181AM | $-55^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ |
| LM6181AI, LM6181I | $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$ |
| Thermal Resistance (θ_{JA} , θ_{JC}) | |
| 8-pin DIP (N) | 102°C/W, 42°C/W |
| 8-pin SO (M-8) | 153°C/W, 42°C/W |
| 16-pin SO (M) | 70°C/W, 38°C/W |

$\pm 15V$ DC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15V$, $R_F = 820\Omega$, and $R_L = 1\text{ k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | LM6181AM | | LM6181AI | | LM6181I | | Units |
|-----------------------|---|----------------------------------|---------------------|--------------------|---------------------|--------------------|---------------------|--------------------|-------------|
| | | | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | |
| V _{OS} | Input Offset Voltage | | 2.0 | 3.0 4.0 | 2.0 | 3.0 3.5 | 3.5 | 5.0 5.5 | mV max |
| TC V _{OS} | Input Offset Voltage Drift | | 5.0 | | 5.0 | | 5.0 | | μV/°C |
| I _B | Inverting Input Bias Current | | 2.0 | 5.0 12.0 | 2.0 | 5.0 12.0 | 5.0 | 10 17.0 | μA max |
| | Non-Inverting Input Bias Current | | 0.5 | 1.5 3.0 | 0.5 | 1.5 3.0 | 2.0 | 3.0 5.0 | μA max |
| TC I _B | Inverting Input Bias Current Drift | | 30 | | 30 | | 30 | | nA/°C |
| | Non-Inverting Input Bias Current Drift | | 10 | | 10 | | 10 | | nA/°C |
| I _B PSR | Inverting Input Bias Current Power Supply Rejection | V _S = ±4.5V, ±16V | 0.3 | 0.5 3.0 | 0.3 | 0.5 3.0 | 0.3 | 0.75 4.5 | μA/V max |
| | Non-Inverting Input Bias Current Power Supply Rejection | V _S = ±4.5V, ±16V | 0.05 | 0.5 1.5 | 0.05 | 0.5 1.5 | 0.05 | 0.5 3.0 | |
| I _B CMR | Inverting Input Bias Current Common Mode Rejection | −10V ≤ V _{CM} ≤ +10V | 0.3 | 0.5 0.75 | 0.3 | 0.5 0.75 | 0.3 | 0.75 1.0 | μA/V max |
| | Non-Inverting Input Bias Current Common Mode Rejection | −10V ≤ V _{CM} ≤ +10V | 0.1 | 0.5 0.5 | 0.1 | 0.5 0.5 | 0.1 | 0.5 0.5 | |
| CMRR | Common Mode Rejection Ratio | −10V ≤ V _{CM} ≤ +10V | 60 | 50 50 | 60 | 50 50 | 60 | 50 50 | dB min |
| PSRR | Power Supply Rejection Ratio | V _S = ±4.5V, ±16V | 80 | 70 70 | 80 | 70 70 | 80 | 70 65 | dB min |
| R _O | Output Resistance | A _V = −1, f = 300 kHz | 0.2 | | 0.2 | | 0.2 | | Ω |
| R _{IN} | Non-Inverting Input Resistance | | 10 | | 10 | | 10 | | MΩ min |
| V _O | Output Voltage Swing | R _L = 1 kΩ | 12 | 11 11 | 12 | 11 11 | 12 | 11 11 | V min |
| | | R _L = 100Ω | 11 | 10 7.5 | 11 | 10 8.0 | 11 | 10 8.0 | |
| I _{SC} | Output Short Circuit Current | | 130 | 100 75 | 130 | 100 85 | 130 | 100 85 | mA min |

± 15V DC Electrical Characteristics (Continued)

The following specifications apply for Supply Voltage = $\pm 15\text{V}$, $R_F = 820\Omega$, and $R_L = 1\text{ k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | LM6181AM | | LM6181AI | | LM6181I | | Units |
|----------|---------------------------------|----------------------------|--|-------------------|--|-------------------|--|--------------------|-------------------------|
| | | | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | |
| Z_T | Transimpedance | $R_L = 1\text{ k}\Omega$ | 1.8 | 1.0 0.5 | 1.8 | 1.0 0.5 | 1.8 | 0.8 0.4 | $\text{M}\Omega$ min |
| | | $R_L = 100\Omega$ | 1.4 | 0.8 0.4 | 1.4 | 0.8 0.4 | 1.4 | 0.7 0.35 | |
| I_S | Supply Current | No Load, $V_O = 0\text{V}$ | 7.5 | 10 10 | 7.5 | 10 10 | 7.5 | 10 10 | mA max |
| V_{CM} | Input Common Mode Voltage Range | | $V^+ - 1.7\text{V}$ $V^- + 1.7\text{V}$ | | $V^+ - 1.7\text{V}$ $V^- + 1.7\text{V}$ | | $V^+ - 1.7\text{V}$ $V^- + 1.7\text{V}$ | | V |

± 15V AC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15\text{V}$, $R_F = 820\Omega$, $R_L = 1\text{ k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | LM6181AM | | LM6181AI | | LM6181I | | Units |
|------------|---|--|---------------------|-------------------|---------------------|-------------------|---------------------|-------------------|-------------------------------|
| | | | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | |
| BW | Closed Loop Bandwidth -3 dB | $A_V = +2$ | 100 | | 100 | | 100 | | MHz min |
| | | $A_V = +10$ | 80 | | 80 | | 80 | | |
| | | $A_V = -1$ | 100 | 80 | 100 | 80 | 100 | 80 | |
| | | $A_V = -10$ | 60 | | 60 | | 60 | | |
| PBW | Power Bandwidth | $A_V = -1, V_O = 5\text{ V}_{PP}$ | 60 | | 60 | | 60 | | |
| SR | Slew Rate | Overdriven | 2000 | | 2000 | | 2000 | | $\text{V}/\mu\text{s}$ min |
| | | $A_V = -1, V_O = \pm 10\text{V}$, $R_L = 150\Omega$ (Note 6) | 1400 | 1000 | 1400 | 1000 | 1400 | 1000 | |
| t_s | Settling Time (0.1%) | $A_V = -1, V_O = \pm 5\text{V}$, $R_L = 150\Omega$ | 50 | | 50 | | 50 | | ns |
| t_r, t_f | Rise and Fall Time | $V_O = 1\text{ V}_{PP}$ | 5 | | 5 | | 5 | | |
| t_p | Propagation Delay Time | $V_O = 1\text{ V}_{PP}$ | 6 | | 6 | | 6 | | |
| $i_{n(+)}$ | Non-Inverting Input Noise Current Density | $f = 1\text{ kHz}$ | 3 | | 3 | | 3 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| $i_{n(-)}$ | Inverting Input Noise Current Density | $f = 1\text{ kHz}$ | 16 | | 16 | | 16 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| e_n | Input Noise Voltage Density | $f = 1\text{ kHz}$ | 4 | | 4 | | 4 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | Second Harmonic Distortion | $2\text{ V}_{PP}, 10\text{ MHz}$ | -50 | | -50 | | -50 | | dBc |
| | Third Harmonic Distortion | $2\text{ V}_{PP}, 10\text{ MHz}$ | -55 | | -55 | | -55 | | |
| | Differential Gain | $R_L = 150\Omega$, $A_V = +2$, NTSC | 0.05 | | 0.05 | | 0.05 | | % |
| | Differential Phase | $R_L = 150\Omega$, $A_V = +2$, NTSC | 0.04 | | 0.04 | | 0.04 | | Deg |

± 5V DC Electrical Characteristics

The following specifications apply for Supply Voltage = ±5V, $R_F = 820\Omega$, and $R_L = 1\text{ k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | LM6181AM | | LM6181AI | | LM6181I | | Units |
|--------------|---|--|--|---------------------|--|---------------------|--|---------------------|-------------------------------|
| | | | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | |
| V_{OS} | Input Offset Voltage | | 1.0 | 2.0 3.0 | 1.0 | 2.0 2.5 | 1.0 | 3.0 3.5 | mV max |
| $TC V_{OS}$ | Input Offset Voltage Drift | | 2.5 | | 2.5 | | 2.5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Inverting Input Bias Current | | 5.0 | 10 22 | 5.0 | 10 22 | 5.0 | 17.5 27.0 | μA max |
| | Non-Inverting Input Bias Current | | 0.25 | 1.5 1.5 | 0.25 | 1.5 1.5 | 0.25 | 3.0 5.0 | μA max |
| $TC I_B$ | Inverting Input Bias Current Drift | | 50 | | 50 | | 50 | | nA/ $^\circ\text{C}$ |
| | Non-Inverting Input Bias Current Drift | | 3.0 | | 3.0 | | 3.0 | | nA/ $^\circ\text{C}$ |
| I_B PSR | Inverting Input Bias Current Power Supply Rejection | $V_S = \pm 4.0\text{V}, \pm 6.0\text{V}$ | 0.3 | 0.5 0.5 | 0.3 | 0.5 0.5 | 0.3 | 1.0 1.0 | $\mu\text{A}/\text{V}$ max |
| | Non-Inverting Input Bias Current Power Supply Rejection | $V_S = \pm 4.0\text{V}, \pm 6.0\text{V}$ | 0.05 | 0.5 0.5 | 0.05 | 0.5 0.5 | 0.05 | 0.5 0.5 | $\mu\text{A}/\text{V}$ max |
| I_B CMR | Inverting Input Bias Current Common Mode Rejection | $-2.5\text{V} \leq V_{CM} \leq +2.5\text{V}$ | 0.3 | 0.5 1.0 | 0.3 | 0.5 1.0 | 0.3 | 1.0 1.5 | $\mu\text{A}/\text{V}$ max |
| | Non-Inverting Input Bias Current Common Mode Rejection | $-2.5\text{V} \leq V_{CM} \leq +2.5\text{V}$ | 0.12 | 0.5 1.0 | 0.12 | 0.5 0.5 | 0.12 | 0.5 0.5 | $\mu\text{A}/\text{V}$ max |
| CMRR | Common Mode Rejection Ratio | $-2.5\text{V} \leq V_{CM} \leq +2.5\text{V}$ | 57 | 50 47 | 57 | 50 47 | 57 | 50 47 | dB min |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 4.0\text{V}, \pm 6.0\text{V}$ | 80 | 70 70 | 80 | 70 70 | 80 | 64 64 | dB min |
| R_O | Output Resistance | $A_V = -1, f = 300\text{ kHz}$ | 0.25 | | 0.25 | | 0.25 | | Ω |
| R_{IN} | Non-Inverting Input Resistance | | 8 | | 8 | | 8 | | M Ω min |
| V_O | Output Voltage Swing | $R_L = 1\text{ k}\Omega$ | 2.6 | 2.25 2.2 | 2.6 | 2.25 2.25 | 2.6 | 2.25 2.25 | V min |
| | | $R_L = 100\Omega$ | 2.2 | 2.0 2.0 | 2.2 | 2.0 2.0 | 2.2 | 2.0 2.0 | V min |
| I_{SC} | Output Short Circuit Current | | 100 | 75 70 | 100 | 75 70 | 100 | 75 70 | mA min |
| Z_T | Transimpedance | $R_L = 1\text{ k}\Omega$ | 1.4 | 0.75 0.35 | 1.4 | 0.75 0.4 | 1.0 | 0.6 0.3 | M Ω min |
| | | $R_L = 100\Omega$ | 1.0 | 0.5 0.25 | 1.0 | 0.5 0.25 | 1.0 | 0.4 0.2 | M Ω min |
| I_S | Supply Current | No Load, $V_O = 0\text{V}$ | 6.5 | 8.5 8.5 | 6.5 | 8.5 8.5 | 6.5 | 8.5 8.5 | mA max |
| V_{CM} | Input Common Mode Voltage Range | | $V^+ - 1.7\text{V}$ $V^- + 1.7\text{V}$ | | $V^+ - 1.7\text{V}$ $V^- + 1.7\text{V}$ | | $V^+ - 1.7\text{V}$ $V^- + 1.7\text{V}$ | | V |

| Symbol | Parameter | Conditions | LM6181A | | LM6181A1 | | LM61811 | | Units |
|------------|---|---|---------------------|-------------------|---------------------|-------------------|---------------------|-------------------|------------------------|
| | | | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | Typical (Note 4) | Limit (Note 5) | |
| BW | Closed Loop Bandwidth —3 dB | $A_V = +2$ | 50 | | 50 | | 50 | | MHz min |
| | | $A_V = +10$ | 40 | | 40 | | 40 | | |
| | | $A_V = -1$ | 55 | 35 | 55 | 35 | 55 | 35 | |
| | | $A_V = -10$ | 35 | | 35 | | 35 | | |
| PBW | Power Bandwidth | $A_V = -1, V_O = 4 V_{PP}$ | 40 | | 40 | | 40 | | |
| SR | Slew Rate | $A_V = -1, V_O = \pm 2V,$ $R_L = 150\Omega$ (Note 6) | 500 | 375 | 500 | 375 | 500 | 375 | V/ μ s min |
| t_s | Settling Time (0.1%) | $A_V = -1, V_O = \pm 2V,$ $R_L = 150\Omega$ | 50 | | 50 | | 50 | | ns |
| t_r, t_f | Rise and Fall Time | $V_O = 1 V_{PP}$ | 8.5 | | 8.5 | | 8.5 | | |
| t_p | Propagation Delay Time | $V_O = 1 V_{PP}$ | 8 | | 8 | | 8 | | |
| $i_{n(+)}$ | Non-Inverting Input Noise Current Density | $f = 1 \text{ kHz}$ | 3 | | 3 | | 3 | | pA/ $\sqrt{\text{Hz}}$ |
| $i_{n(-)}$ | Inverting Input Noise Current Density | $f = 1 \text{ kHz}$ | 16 | | 16 | | 16 | | pA/ $\sqrt{\text{Hz}}$ |
| e_n | Input Noise Voltage Density | $f = 1 \text{ kHz}$ | 4 | | 4 | | 4 | | nV/ $\sqrt{\text{Hz}}$ |
| | Second Harmonic Distortion | $2 V_{PP}, 10 \text{ MHz}$ | -45 | | -45 | | -45 | | dBc |
| | Third Harmonic Distortion | $2 V_{PP}, 10 \text{ MHz}$ | -55 | | -55 | | -55 | | |
| | Differential Gain | $R_L = 150\Omega$ $A_V = +2$ NTSC | 0.063 | | 0.063 | | 0.063 | | % |
| | Differential Phase | $R_L = 150\Omega$ $A_V = +2$ NTSC | 0.16 | | 0.16 | | 0.16 | | Deg |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 k Ω .

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) package soldered directly into a PC board is 102°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total 2 in² 1 oz. copper trace. The 16-pin S.O. (M) package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V⁻ for proper operation. The typical junction-to-ambient thermal resistance of the S.O. (M-8) package soldered directly into a PC board is 153°C/W.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 6: Measured from +25% to +75% of output waveform.

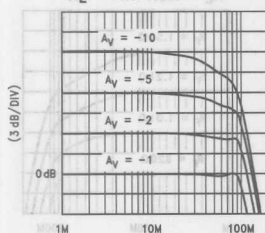
Note 7: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of $\pm 130 \text{ mA}$ over a long term basis may adversely affect reliability.

Note 8: For guaranteed Military Temperature Range parameters see RETS6181X.

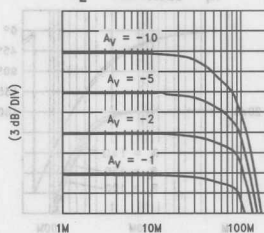
Typical Performance Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

LM6181

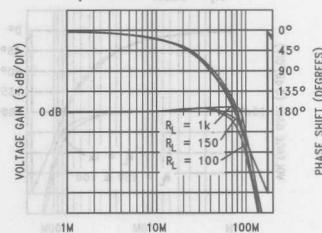
**CLOSED-LOOP
FREQUENCY RESPONSE**
 $V_S = \pm 15\text{V}; R_f = 820\Omega$;
 $R_L = 1\text{k}\Omega$



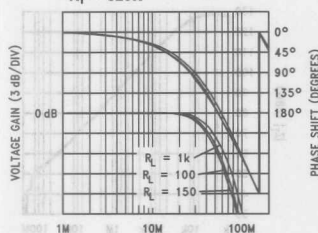
**CLOSED-LOOP
FREQUENCY RESPONSE**
 $V_S = \pm 15\text{V}; R_f = 820\Omega$;
 $R_L = 150\Omega$



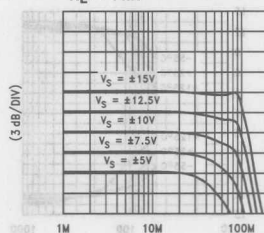
**UNITY GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 15\text{V}; A_V = +1$;
 $R_f = 820\Omega$



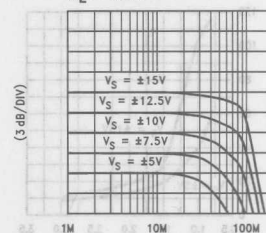
**UNIT GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 5\text{V}; A_V = +1$;
 $R_f = 820\Omega$



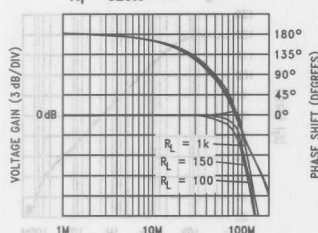
**FREQUENCY RESPONSE
vs SUPPLY VOLTAGE**
 $A_V = -1; R_f = 820\Omega$;
 $R_L = 1\text{k}\Omega$



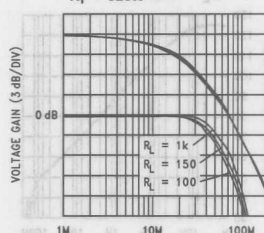
**FREQUENCY RESPONSE
vs SUPPLY VOLTAGE**
 $A_V = -1; R_f = 820\Omega$;
 $R_L = 150\Omega$



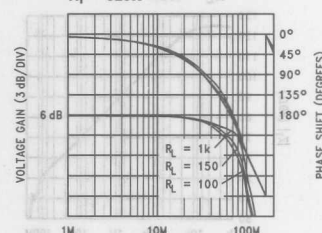
**INVERTING GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 15\text{V}; A_V = -1$;
 $R_f = 820\Omega$



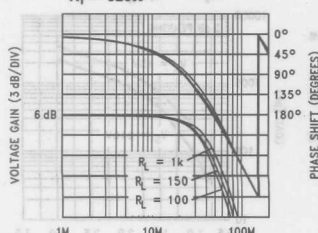
**INVERTING GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 5\text{V}; A_V = -1$;
 $R_f = 820\Omega$



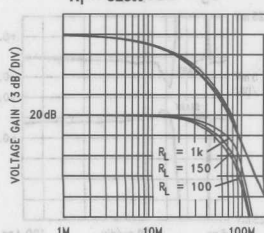
**NON-INVERTING GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 15\text{V}; A_V = +2$;
 $R_f = 820\Omega$



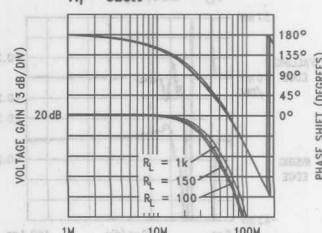
**NON-INVERTING GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 5\text{V}; A_V = +2$;
 $R_f = 820\Omega$



**INVERTING GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 15\text{V}; A_V = -10$;
 $R_f = 820\Omega$



**INVERTING GAIN
FREQUENCY RESPONSE**
 $V_S = \pm 5\text{V}; A_V = -10$;
 $R_f = 820\Omega$



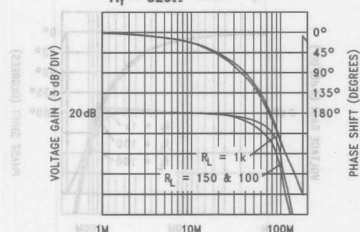
1

TL/H/11328-5

Typical Performance Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted (Continued)

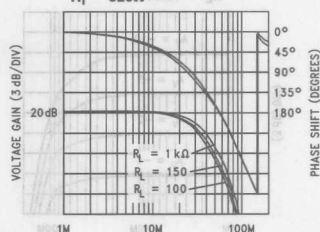
NON-INVERTING GAIN FREQUENCY RESPONSE

$V_S = \pm 15\text{V}; A_V = +10;$
 $R_F = 820\Omega$



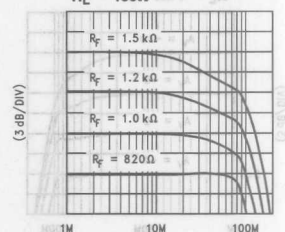
NON-INVERTING GAIN FREQUENCY RESPONSE

$V_S = \pm 5\text{V}; A_V = +10;$
 $R_F = 820\Omega$



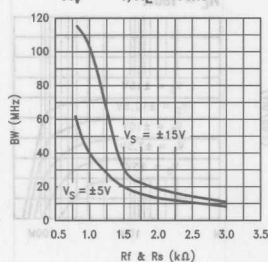
NON-INVERTING GAIN FREQUENCY COMPENSATION

$V_S = \pm 15\text{V}; A_V = +2;$
 $R_L = 150\Omega$

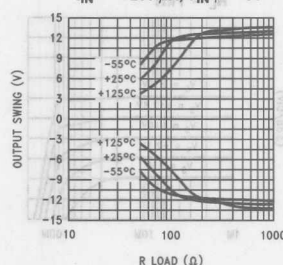


BANDWIDTH vs R_F & R_S

$V_S = \pm 15\text{V}; A_V = -1; R_L = 1\text{k}\Omega$

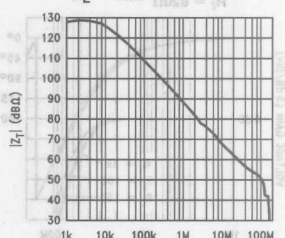


OUTPUT SWING vs R_LOAD PULSED, $V_S = \pm 15\text{V},$ $I_{IN} = \pm 200\mu\text{A}, V_{IN} = 0\text{V}$



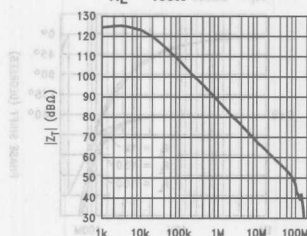
TRANSIMPEDANCE vs FREQUENCY

$V_S = \pm 15\text{V};$
 $R_L = 1\text{k}\Omega$



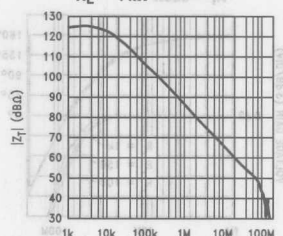
TRANSIMPEDANCE vs FREQUENCY

$V_S = \pm 15\text{V};$
 $R_L = 100\Omega$



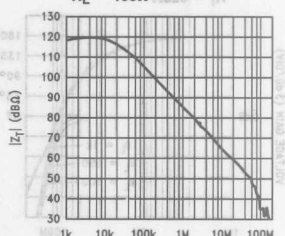
TRANSIMPEDANCE vs FREQUENCY

$V_S = \pm 5\text{V};$
 $R_L = 1\text{k}\Omega$



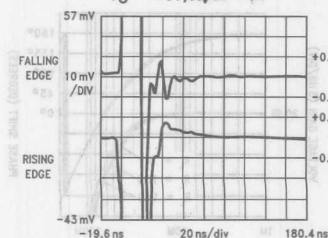
TRANSIMPEDANCE vs FREQUENCY

$V_S = \pm 5\text{V};$
 $R_L = 100\Omega$



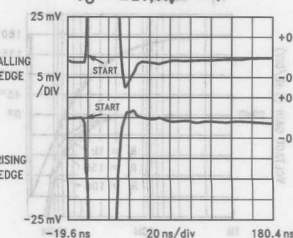
SETTLING RESPONSE

$V_S = \pm 15\text{V}; R_L = 150\Omega;$
 $V_O = \pm 5\text{V}; A_V = -1$



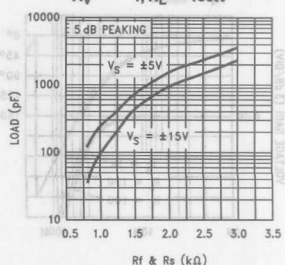
SETTLING RESPONSE

$V_S = \pm 5\text{V}; R_L = 150\Omega;$
 $V_O = \pm 2\text{V}; A_V = -1$

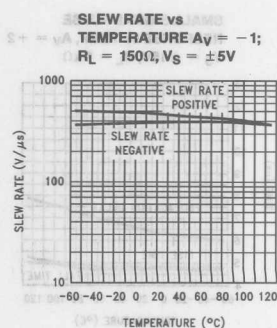
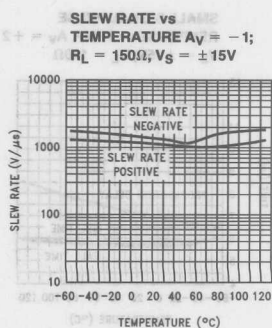
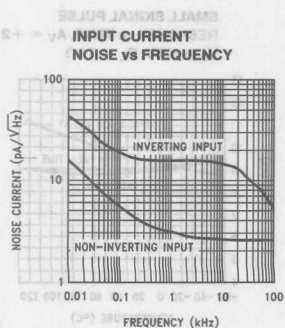
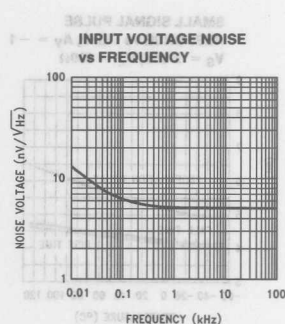
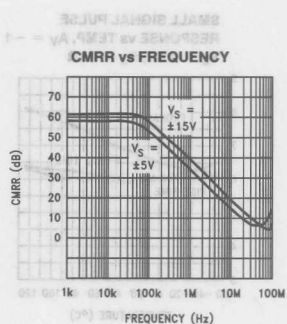
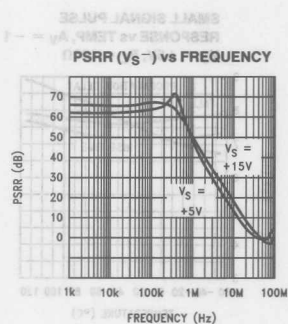
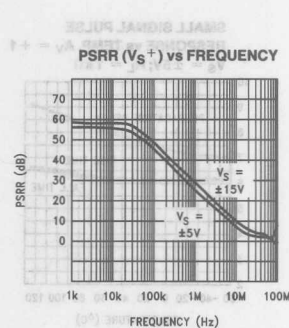
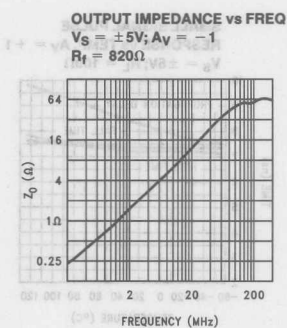
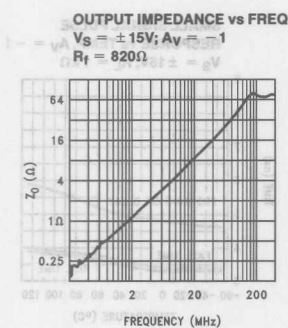
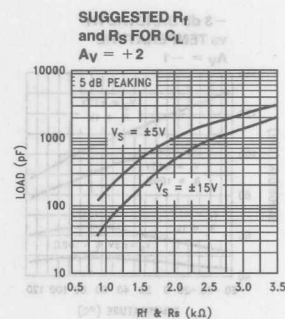
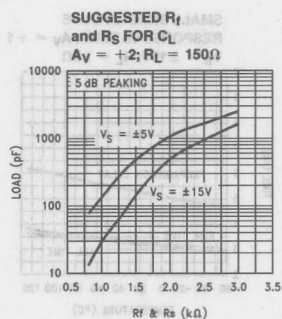
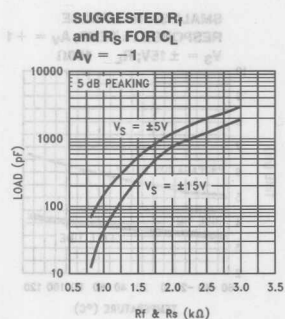


SUGGESTED R_F and R_S for C_L

$A_V = -1; R_L = 150\Omega$

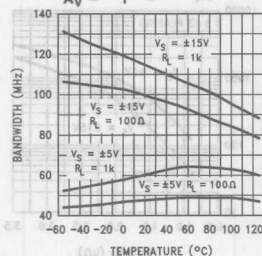


Typical Performance Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted (Continued)

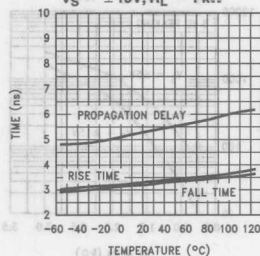


Typical Performance Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted (Continued)

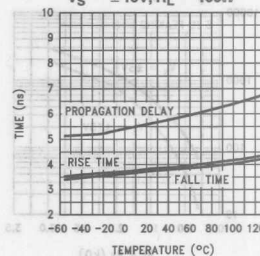
**-3 dB BANDWIDTH
RESPONSE vs TEMPERATURE**
 $A_V = -1$



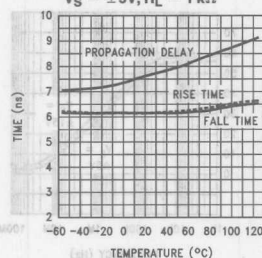
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +1$**
 $V_S = \pm 15\text{V}; R_L = 1\text{k}\Omega$



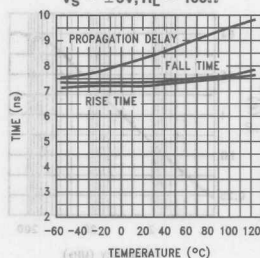
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +1$**
 $V_S = \pm 15\text{V}; R_L = 100\Omega$



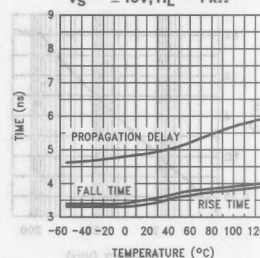
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +1$**
 $V_S = \pm 5\text{V}; R_L = 1\text{k}\Omega$



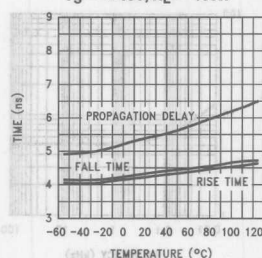
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +1$**
 $V_S = \pm 5\text{V}; R_L = 100\Omega$



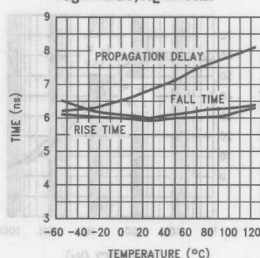
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = -1$**
 $V_S = \pm 15\text{V}; R_L = 1\text{k}\Omega$



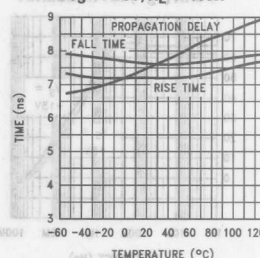
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = -1$**
 $V_S = \pm 15\text{V}; R_L = 100\Omega$



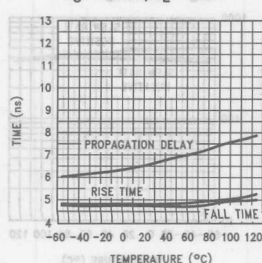
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = -1$**
 $V_S = \pm 5\text{V}; R_L = 1\text{k}\Omega$



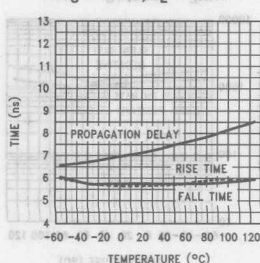
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = -1$**
 $V_S = \pm 5\text{V}; R_L = 100\Omega$



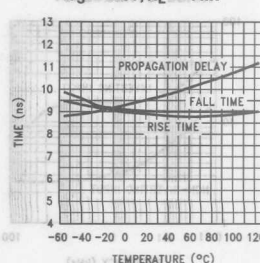
**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +2$**
 $V_S = \pm 15\text{V}; R_L = 1\text{k}\Omega$



**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +2$**
 $V_S = \pm 15\text{V}; R_L = 100\Omega$

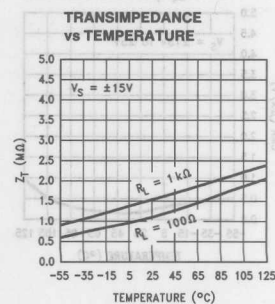
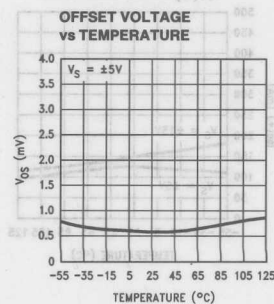
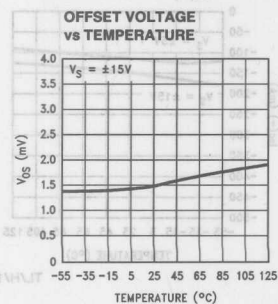
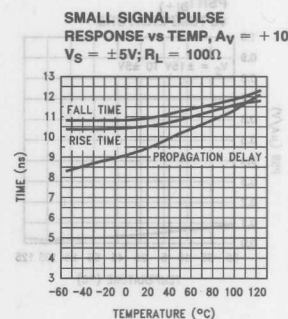
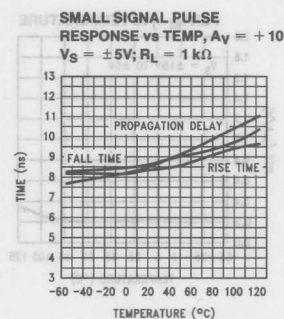
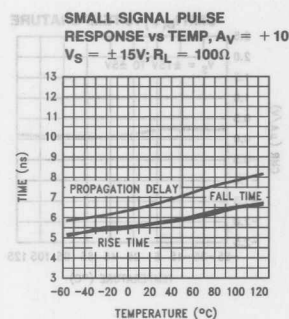
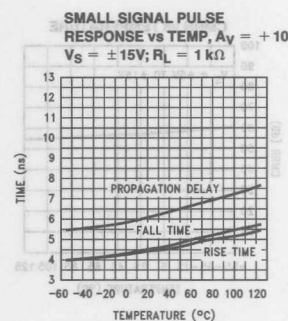
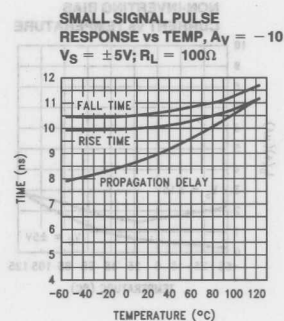
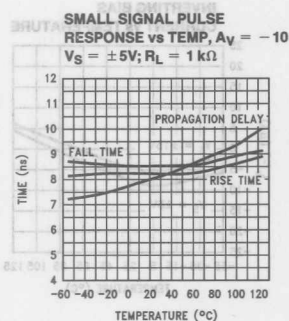
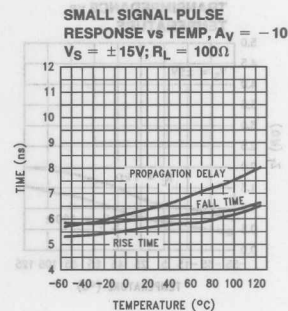
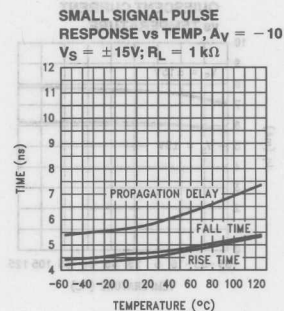
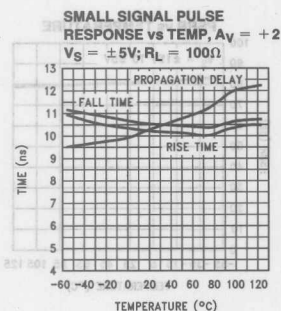


**SMALL SIGNAL PULSE
RESPONSE vs TEMP, $A_V = +2$**
 $V_S = \pm 5\text{V}; R_L = 1\text{k}\Omega$

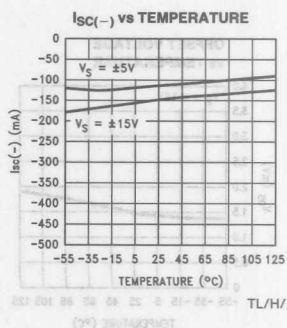
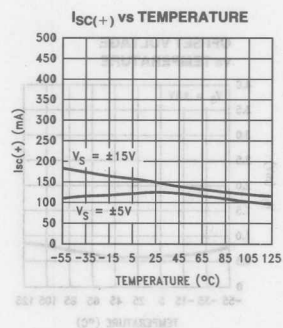
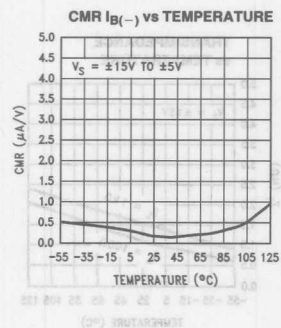
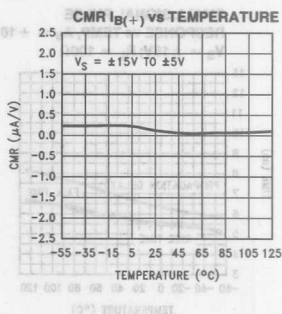
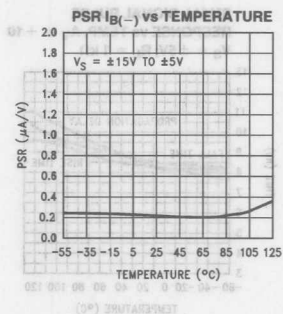
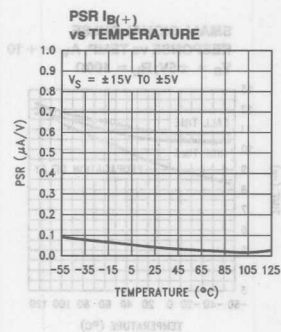
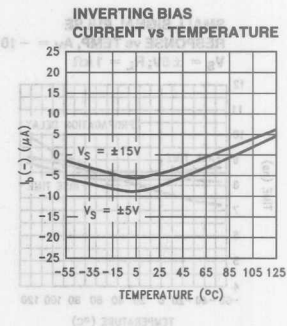
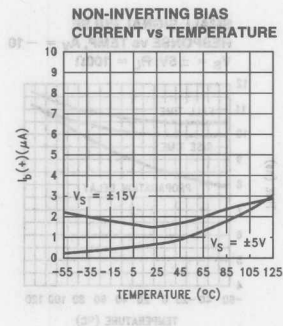
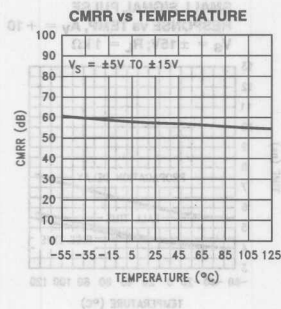
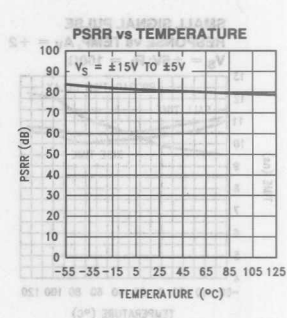
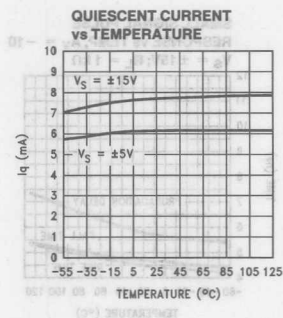
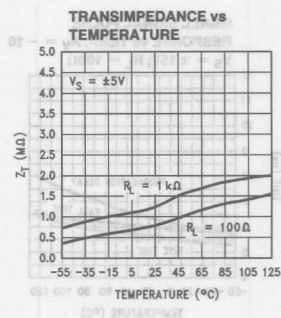


Typical Performance Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted (Continued)

LM6181



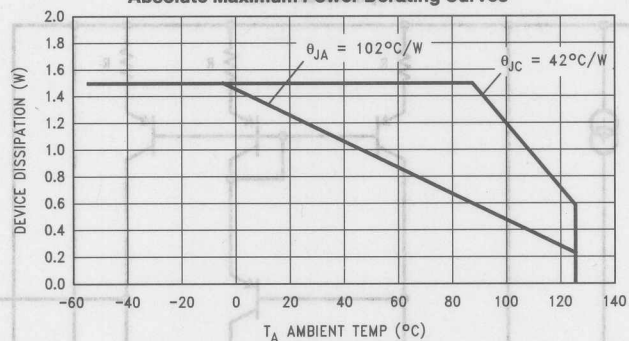
TL/H/11328-8



TL/H/11328-9

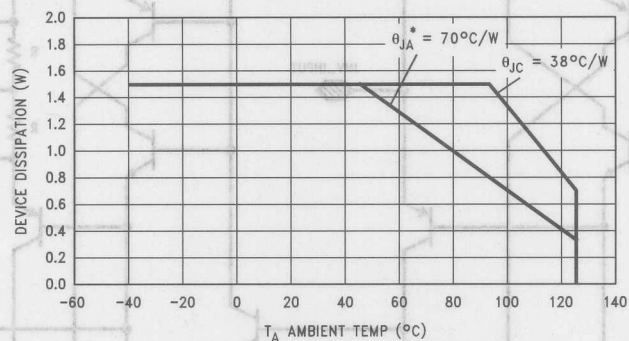
Typical Performance Characteristics

Absolute Maximum Power Derating Curves



TL/H/11328-30

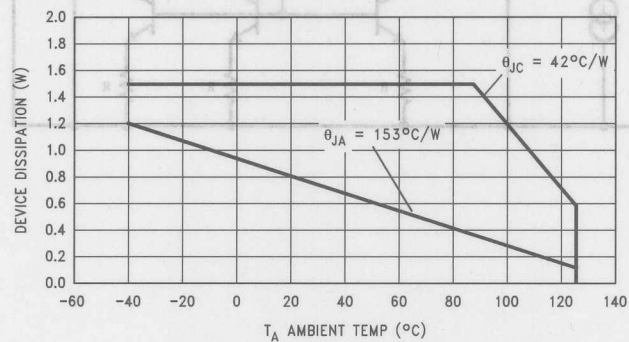
N-Package



TL/H/11328-31

M-Package

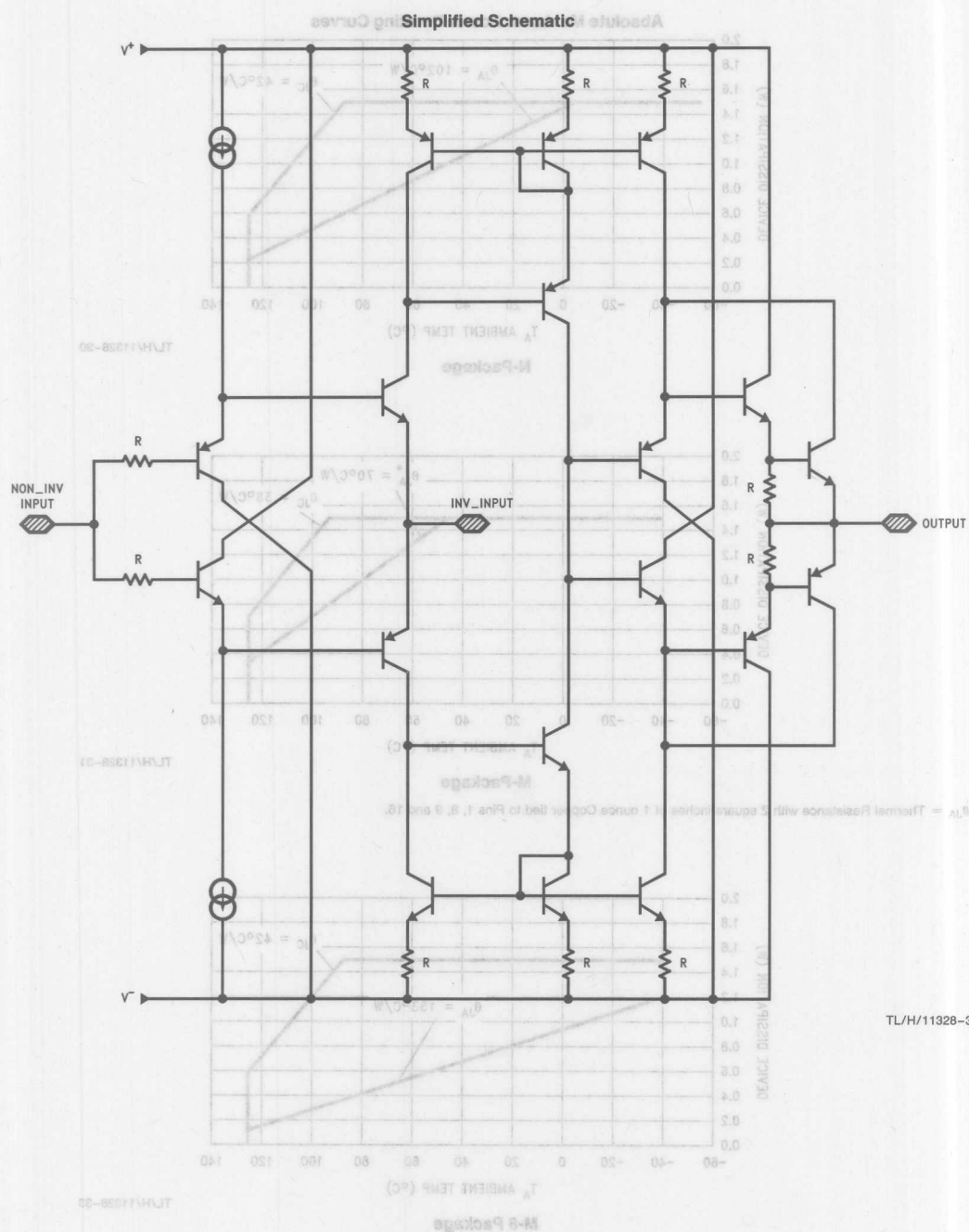
* θ_{JA} = Thermal Resistance with 2 square inches of 1 ounce Copper tied to Pins 1, 8, 9 and 16.



TL/H/11328-33

M-8 Package

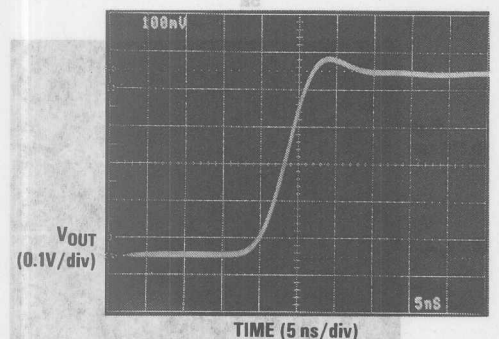
Typical Performance Characteristics (Continued)



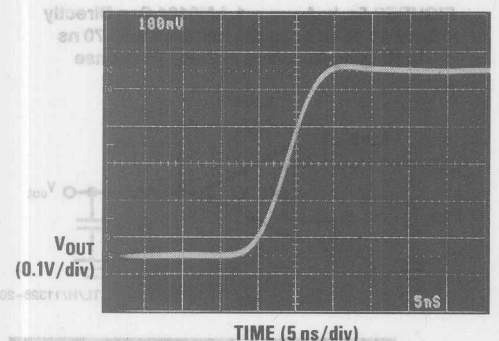
Typical Applications

CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6181, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed-loop gain. Figures 1a and 1b illustrate that for closed loop gains of -1 and -5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.



1a



1b

FIGURES 1a, 1b: Variation of Closed Loop Gain from -1 to -5 Yields Similar Responses

The closed-loop bandwidth of the LM6181 depends on the feedback resistance, R_f . Therefore, R_s and not R_f , must be varied to adjust for the desired closed-loop gain as in Figure 2.

Typical Applications (Continued)

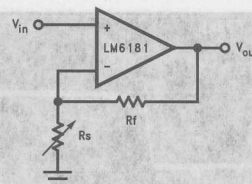


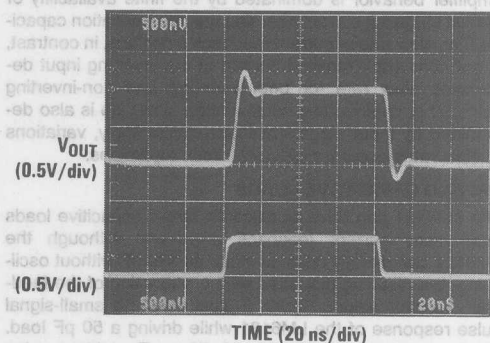
FIGURE 2. R_s Is Adjusted to Obtain the Desired Closed Loop Gain, A_{vCL}

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. $10\text{ }\mu\text{F}$ tantalum and $0.1\text{ }\mu\text{F}$ ceramic bypass capacitors are recommended for each supply pin. The bypass capacitors should be placed as close to the amplifier pins as possible ($0.5''$ or less).

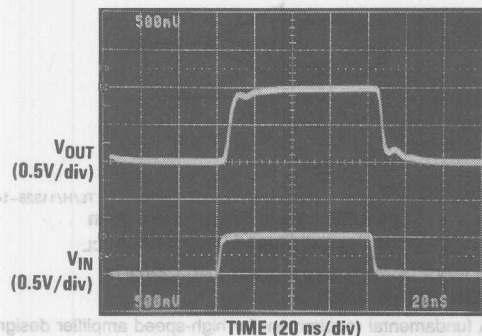
FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f , is a dominant factor in compensating the LM6181. For general applications the LM6181 will maintain specified performance with an 820Ω feedback resistor. Although this value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are 2 and the feedback resistors are 820Ω , and 1640Ω , respectively. Figures 3a and 3b illustrate the effect of increasing R_f while maintaining the same closed-loop gain—the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6181 (see -3 dB bandwidth vs R_f typical curves) and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed loop gains, due to 2nd order effects. For example Figure 4 illustrates reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed loop gain of 25.



3a: $R_f = 820\Omega$

Typical Applications (Continued)



3b: $R_f = 1640\Omega$

FIGURES 3a, b: Increasing Compensation with Increasing R_f

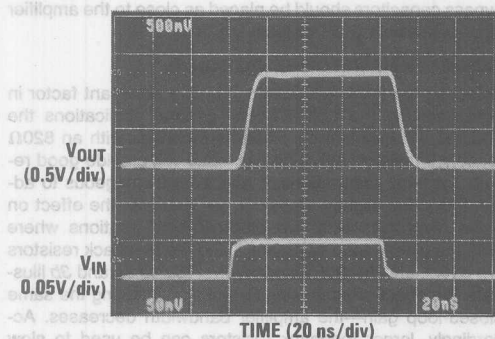


FIGURE 4: Reducing R_f for Large Closed Loop Gains, $R_f = 500\Omega$

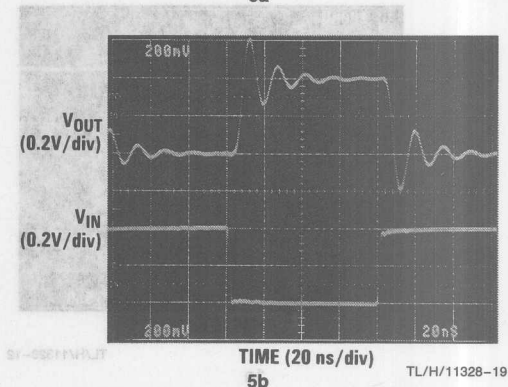
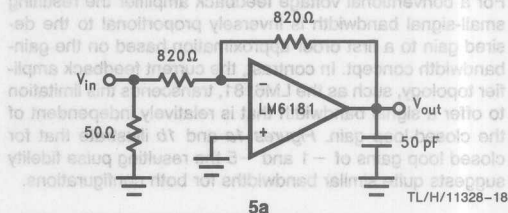
SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input determines slew rate for both inverting and non-inverting gains. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

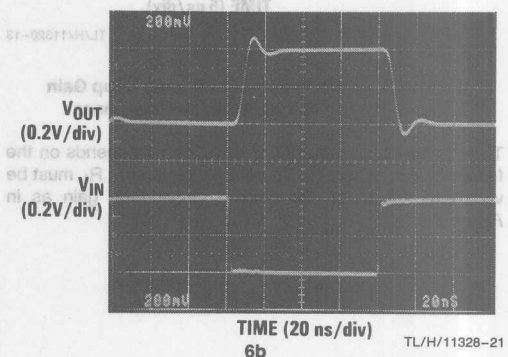
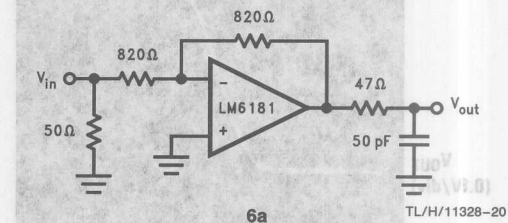
DRIVING CAPACITIVE LOADS

The LM6181 can drive significantly larger capacitive loads than many current feedback amplifiers. Although the LM6181 can directly drive as much as 100 pF without oscillating, the resulting response will be a function of the feedback resistor value. Figure 5 illustrates the small-signal pulse response of the LM6181 while driving a 50 pF load. Ringing persists for approximately 70 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see typical curves Suggested R_f and R_s for C_L), or resistive isolation can be used (10 Ω –51 Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 6 illustrates the improvement obtained with using a 47 Ω isolation resistor.



FIGURES 5a, b: $A_v = -1$, LM6181 Can Directly Drive 50 pF of Load Capacitance with 70 ns of Ringing Resulting in Pulse Response

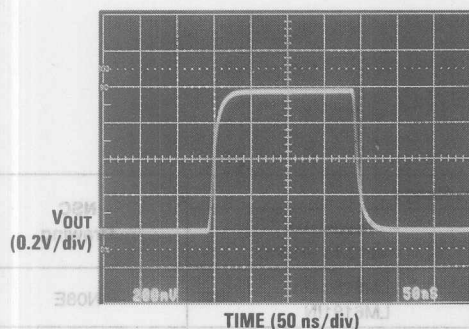
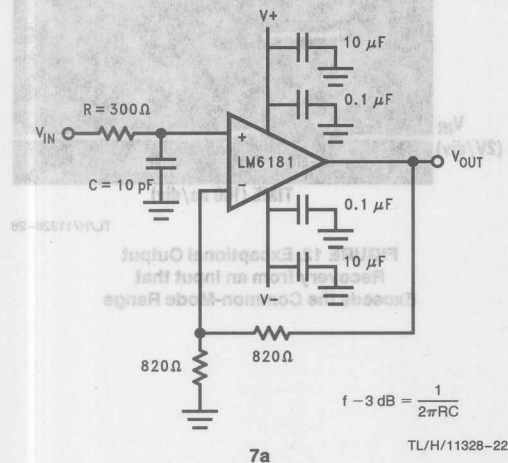


FIGURES 6a, b: Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and R_s Could Be Increased to Maintain $A_v = -1$ and Improve Pulse Response Characteristics.

Typical Applications (Continued)

CAPACITIVE FEEDBACK

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f . This compensation serves to reduce the amplifier's peaking in the frequency domain which equivalently tames the transient response. To limit the bandwidth of current feedback amplifiers, do not use a capacitor across R_f . The dynamic impedance of capacitors in the feedback loop reduces the amplifier's stability. Instead, reduced peaking in the frequency response, and bandwidth limiting can be accomplished by adding an RC circuit, as illustrated in Figure 7b.



FIGURES 7a, b: RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response

Typical Performance Characteristics

OVERDRIVE RECOVERY

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The typical recovery times for open-loop, closed-loop, and input common-mode voltage range overdrive conditions are illustrated in Figures 9, 11 and 12, respectively.

The open-loop circuit of Figure 8 generates an overdrive response by allowing the $\pm 0.5\text{V}$ input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times shown in Figure 9 are 5 ns and 25 ns, respectively.

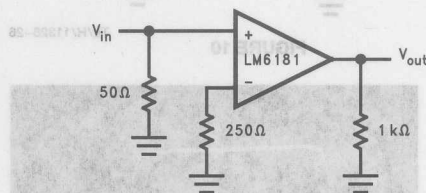


FIGURE 8

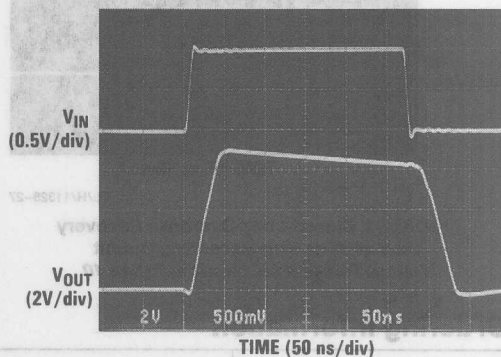


FIGURE 9. Open-Loop Overdrive Recovery Time of 5 ns, and 25 ns from Test Circuit in Figure 8

the amplifier output into overdrive. Figure 11 displays the typical 30 ns recovery time to a linear output value.

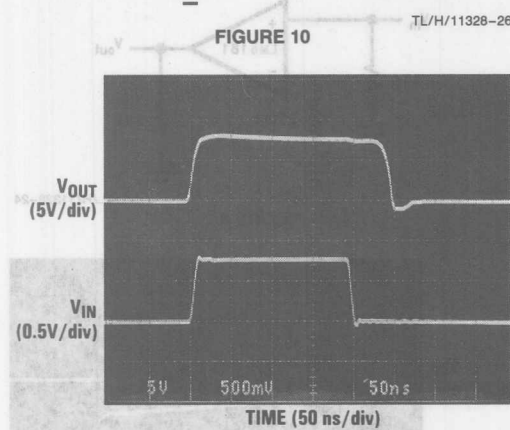
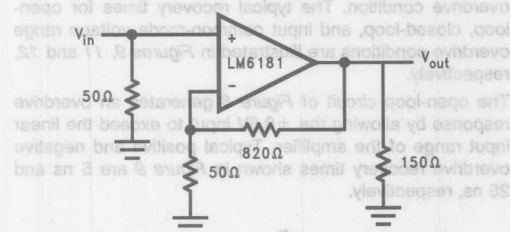


FIGURE 11. Closed-Loop Overdrive Recovery
Time of 30 ns from Exceeding Output
Voltage Range from Circuit in Figure 10

ceeded by a 5V pulse resulting in a typical recovery time of 310 ns shown in Figure 12. The LM6181 supply voltage is $\pm 5V$.

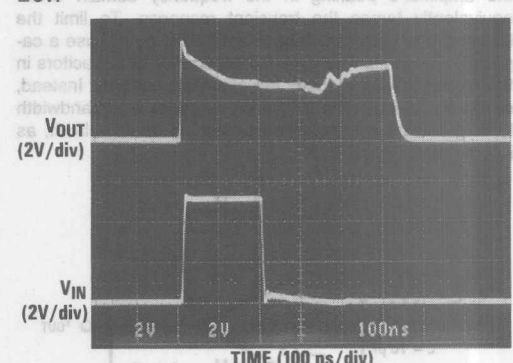


FIGURE 12. Exceptional Output Recovery from an Input that Exceeds the Common-Mode Range

Ordering Information

| Package | Temperature Range | | NSC Drawing |
|---------------------------------------|-----------------------------|------------------------------|-------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | |
| 8-Pin Molded DIP | LM6181AMN | LM6181AIN LM6181IN | N08E |
| 8-Pin Small Outline Molded Package | | LM6181AIM-8 LM6181IM-8 | M08A |
| 16-Pin Small Outline | | LM6181AIM LM6181IM | M16A |
| 8-Pin Ceramic DIP | LM6181AMJ/883 | | J08A |

LM6182 Dual 100 mA Output, 100 MHz Current Feedback Amplifier

General Description

The LM6182 dual current feedback amplifier offers an unparalleled combination of bandwidth, slew-rate, and output current. Each amplifier can directly drive a 2V signal into a 50Ω or 75Ω back-terminated coax cable system over the full industrial temperature range. This represents a radical enhancement in output drive capability for a dual 8-pin high-speed amplifier making it ideal for video applications.

Built on National's advanced high-speed VIP IITM (Vertically Integrated PNP) process, the LM6182 employs current-feedback providing bandwidth that does not vary dramatically with gain; 100 MHz at $A_v = -1$, 60 MHz at $A_v = -10$. With a slew rate of 2000 V/μsec, 2nd harmonic distortion of -50 dBc at 10 MHz and settling time of 50 ns (0.1%), the two independent amplifiers of the LM6182 offer performance that is ideal for data acquisition, high-speed ATE, and precision pulse amplifier applications.

See the LM6181 data sheet for a single amplifier with these same features.

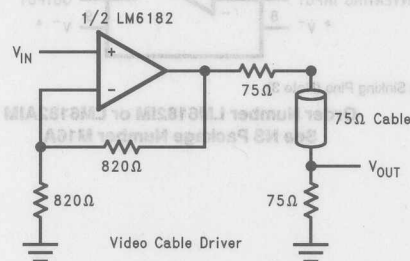
Features (Typical unless otherwise noted)

- Slew Rate 2000 V/μs
- Closed Loop Bandwidth 100 MHz
- Settling Time (0.1%) 50 ns
- Low Differential Gain and Phase Error 0.05%, 0.04°
- $R_L = 150\Omega$
- Low Offset Voltage 2 mV
- High Output Drive $\pm 10V$ into 150Ω
- Characterized for Supply Ranges $\pm 5V$ and $\pm 15V$
- Improved Performance over OP260 and LT1229

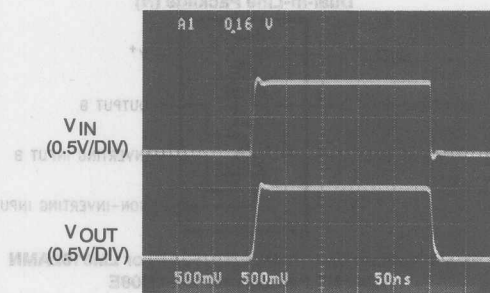
Applications

- Coax Cable Driver
- Professional Studio Video Equipment
- Flash ADC Buffer
- PC and Workstation Video Boards
- Facsimile and Imaging Systems

Typical Application



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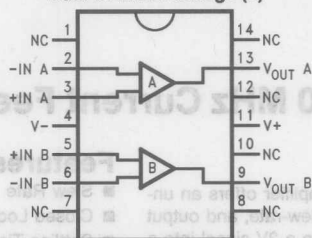


TIME (50ns/DIV)

TL/H/11926-2

Connection Diagrams

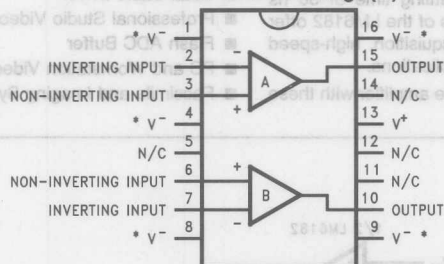
Dual-In-Line Package (J)



Order Number LM6182AMJ/883
See NS Package Number J14A

TL/H/11926-51

Small Outline Package (M)

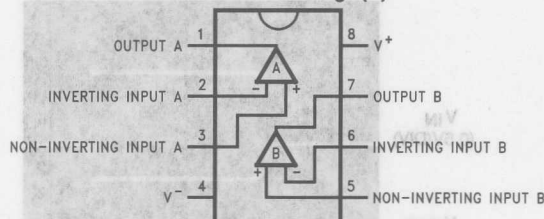


*Heat Sinking Pins (Note 3)

Order Number LM6182IM or LM6182AIM
See NS Package Number M16A

TL/H/11926-4

Dual-In-Line Package (N)



Order Number LM6182IN, LM6182AIN or LM6182AMN
See NS Package Number N08E

TL/H/11926-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------------------|
| Supply Voltage | $\pm 18\text{V}$ |
| Differential Input Voltage | $\pm 6\text{V}$ |
| Input Voltage | $\pm \text{Supply Voltage}$ |
| Inverting Input Current | 15 mA |
| Output Short Circuit | (Note 4) |
| Soldering Information | |
| Dual-In-Line Package (N) Soldering (10s) | 260°C |

Small Outline Package (M)

Vapor Phase (60s) 215°C

Infrared (15s) 220°C

Storage Temperature Range $-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$

Junction Temperature 150°C

ESD Rating (Note 2) $\pm 2000\text{V}$ **Operating Ratings**

Supply Voltage Range 7V to 32V

Junction Temperature Range (Note 3)

LM6182AM $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ LM6182AI, LM6182I $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ **$\pm 15\text{V DC}$ Electrical Characteristics**

The following specifications apply for supply voltage = $\pm 15\text{V}$, $V_{\text{cm}} = V_O = 0\text{V}$, $R_f = 820\Omega$, and $R_L = 1\text{k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LM6182AM | LM6182AI | LM6182I | Units |
|--------------|--|---|---------------------|-------------------|-------------------|-------------------|------------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | Limit (Note 6) | |
| V_{OS} | Input Offset Voltage | | 2.0 | 3.0 | 3.0 | 5.0 | mV |
| | | | | 4.0 | 3.5 | 5.5 | max |
| TCV_{OS} | Input Offset Voltage Drift | | 5.0 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Inverting Input Bias Current | | 2.0 | 5.0 | 5.0 | 10.0 | μA |
| | | | | 12.0 | 12.0 | 17.0 | max |
| TCI_B | Inverting Input Bias Current Drift | | 0.75 | 2.0 | 2.0 | 3.0 | nA/ $^\circ\text{C}$ |
| | | | | 4.0 | 4.0 | 5.0 | |
| I_B PSR | Inverting Input Bias Current Power Supply Rejection | $\pm 4.5\text{V} \leq V_S \leq \pm 16\text{V}$ | 0.1 | 0.5 | 0.5 | 0.75 | $\mu\text{A}/\text{V}$ |
| | | | | 3.0 | 3.0 | 4.5 | max |
| I_B CMR | Inverting Input Bias Current Common Mode Rejection | $\pm 4.5\text{V} \leq V_S \leq \pm 16\text{V}$ | 0.05 | 0.5 | 0.5 | 0.5 | $\mu\text{A}/\text{V}$ |
| | | | | 1.5 | 1.5 | 3.0 | max |
| I_B CMR | Inverting Input Bias Current Common Mode Rejection | $-10\text{V} \leq V_{\text{CM}} \leq +10\text{V}$ | 0.15 | 0.5 | 0.5 | 0.75 | $\mu\text{A}/\text{V}$ |
| | | | | 1.0 | 1.0 | 1.5 | max |
| I_B CMR | Inverting Input Bias Current Common Mode Rejection | $-10\text{V} \leq V_{\text{CM}} \leq +10\text{V}$ | 0.1 | 0.5 | 0.5 | 0.5 | $\mu\text{A}/\text{V}$ |
| | | | | 1.0 | 1.0 | 1.5 | max |
| CMRR | Common Mode Rejection Ratio | $-10\text{V} \leq V_{\text{CM}} \leq +10\text{V}$ | 60 | 50 | 50 | 50 | dB |
| | | | | 47 | 47 | 47 | min |
| PSRR | Power Supply Rejection Ratio | $\pm 4.5\text{V} \leq V_S \leq \pm 16\text{V}$ | 80 | 70 | 70 | 70 | dB |
| | | | | 67 | 67 | 65 | min |
| R_O | Output Resistance | $A_V = -1$ $f = 300\text{ kHz}$ | 0.2 | | | | Ω |
| R_{IN} | Non-Inverting Input Resistance | | 10 | | | | M Ω |
| V_O | Output Voltage Swing | $R_L = 1\text{ k}\Omega$ | 12 | 11 | 11 | 11 | V |
| | | $R_L = 150\Omega$ | 11 | 9.5 | 9.5 | 9.5 | min |
| | | | | 10 | 10 | 10 | |
| | | | | 5.6 | 6.0 | 6.0 | |

± 15V DC Electrical Characteristics (Continued) The following specifications apply for supply voltage = $\pm 15\text{V}$, $V_{\text{cm}} = V_{\text{O}} = 0\text{V}$, $R_{\text{f}} = 820\Omega$, and $R_{\text{L}} = 1\text{k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_{\text{J}} = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LM6182AM | LM6182AI | LM6182I | Units |
|-----------------|---------------------------------|---|--|-------------------|--------------------|-------------------|-------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | Limit (Note 6) | |
| I_{SC} | Output Short Circuit Current | | 100 | 70 37.5 | 70 40 | 70 40 | mA min |
| Z_{T} | Transimpedance | $R_{\text{L}} = 1\text{k}\Omega$ | 1.8 | 1.0 0.4 | 1.0 0.5 | 0.8 0.4 | $\text{M}\Omega$ min |
| | | $R_{\text{L}} = 150\Omega$ | 1.4 | 0.8 0.3 | 0.8 0.35 | 0.7 0.3 | |
| I_{S} | Supply Current | No Load, $V_{\text{IN}} = 0\text{V}$ Both Amplifiers | 15 | 20 22 | 20 22 | 20 22 | mA max |
| V_{CM} | Input Common Mode Voltage Range | | $V^{+} - 1.7\text{V}$ $V^{-} + 1.7\text{V}$ | | | | V |

± 15V AC Electrical Characteristics The following specifications apply for supply voltage = $\pm 15\text{V}$, $V_{\text{cm}} = V_{\text{O}} = 0\text{V}$, $R_{\text{f}} = 820\Omega$, and $R_{\text{L}} = 1\text{k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_{\text{J}} = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LM6182AM | LM6182AI | LM6182I | Units |
|---------------------------------|---|---|---------------------|-------------------|-------------------|-------------------|-------------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | Limit (Note 6) | |
| X_{t} | Crosstalk Rejection | (Note 7) | 93 | | | | dB |
| BW | Closed Loop Bandwidth - 3 dB | $A_{\text{V}} = +2$ | 100 | | | | MHz |
| | | $A_{\text{V}} = +10$ | 75 | | | | |
| | | $A_{\text{V}} = -1$ | 100 | | | | |
| | | $A_{\text{V}} = -10$ | 60 | | | | |
| | Closed Loop Bandwidth 0.1 dB Flat, $R_{\text{SOURCE}} = 200\Omega$ | $A_{\text{V}} = +2$, $R_{\text{L}} = 150\Omega$ | 35 | | | | dB |
| PBW | Power Bandwidth | $A_{\text{V}} = -1$, $V_{\text{O}} = 5\text{V}_{\text{PP}}$ | 60 | | | | dB |
| SR | Slew Rate | Overdriven | 2000 | | | | $\text{V}/\mu\text{s}$ min |
| | | $A_{\text{V}} = -1$, $V_{\text{O}} = \pm 10\text{V}$ $R_{\text{L}} = 150\Omega$, (Note 8) | 1400 | 1000 | 1000 | 1000 | |
| t_{S} | Settling Time (0.1%) | $A_{\text{V}} = -1$, $V_{\text{O}} = \pm 5\text{V}$ $R_{\text{L}} = 150\Omega$ | 50 | | | | ns |
| t_{r} , t_{f} | Rise and Fall Time | $V_{\text{O}} = 1\text{V}_{\text{PP}}$ | 5 | | | | ns |
| t_{p} | Propagation Delay Time | $V_{\text{O}} = 1\text{V}_{\text{PP}}$ | 6 | | | | ns |
| $i_{\text{n}}(+)$ | Non-Inverting Input Noise Current Density | $f = 1\text{kHz}$ | 3 | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| $i_{\text{n}}(-)$ | Inverting Input Noise Current Density | $f = 1\text{kHz}$ | 16 | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| e_{n} | Input Noise Voltage Density | $f = 1\text{kHz}$ | 4 | | | | $\text{nV}/\sqrt{\text{Hz}}$ |
| | Second Harmonic Distortion | $V_{\text{O}} = 2\text{V}_{\text{PP}}$, $f = 10\text{MHz}$ $A_{\text{V}} = +2$ | -50 | | | | dBc |
| | Third Harmonic Distortion | $V_{\text{O}} = 2\text{V}_{\text{PP}}$, $f = 10\text{MHz}$ $A_{\text{V}} = +2$ | -55 | | | | dBc |
| | Differential Gain | $R_{\text{L}} = 150\Omega$ $A_{\text{V}} = +2$, NTSC | 0.05 | | | | % |
| | Differential Phase | $R_{\text{L}} = 150\Omega$ $A_{\text{V}} = +2$, NTSC | 0.04 | | | | Deg |
| THD | Total Harmonic Distortion | $V_{\text{O}} = 2\text{V}_{\text{PP}}$, $A_{\text{V}} = +2$, $f = 10\text{MHz}$, $R_{\text{L}} = 150\Omega$ | 0.58 | | | | % |

±5V DC Electrical Characteristics The following specifications apply for supply voltage = $\pm 5V$, $V_{cm} = V_O = 0V$, $R_f = 820\Omega$, and $R_L = 1\text{ k}\Omega$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LM6182AM | LM6182AI | LM6182I | Units |
|--------------|--|---|------------------------------|--------------------|---------------------|---------------------|------------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | Limit (Note 6) | |
| V_{OS} | Input Offset Voltage | | 1.0 | 2.0 3.0 | 2.0 2.5 | 3.0 3.5 | mV max |
| TCV_{OS} | Input Offset Voltage Drift | | 2.5 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Inverting Input Bias Current | | 5.0 | 10 22 | 10 22 | 17.5 27.0 | μA max |
| | Non-Inverting Input Bias Current | | 0.25 | 1.5 3.0 | 1.5 3.0 | 3.0 5.0 | |
| TCI_B | Inverting Input Bias Current Drift | | 50 | | | | $\text{nA}/^\circ\text{C}$ |
| | Non-Inverting Input Bias Current Drift | | 3.0 | | | | |
| I_B PSR | Inverting Input Bias Current Power Supply Rejection | $\pm 4V \leq V_S \leq \pm 6V$ | 0.3 | 0.5 1.0 | 0.5 1.0 | 0.75 1.5 | $\mu\text{A}/V$ max |
| | Non-Inverting Input Bias Current Power Supply Rejection | $\pm 4V \leq V_S \leq \pm 6V$ | 0.05 | 0.5 1.0 | 0.5 1.0 | 0.5 1.5 | |
| I_B CMR | Inverting Input Bias Current Common Mode Rejection | $-2.5V \leq V_{CM} \leq +2.5V$ | 0.3 | 0.5 1.0 | 0.5 1.0 | 1.0 1.5 | $\mu\text{A}/V$ max |
| | Non-Inverting Input Bias Current Common Mode Rejection | $-2.5V \leq V_{CM} \leq +2.5V$ | 0.12 | 0.5 1.0 | 0.5 1.0 | 0.5 1.5 | |
| CMRR | Common Mode Rejection Ratio | $-2.5V \leq V_{CM} \leq +2.5V$ | 57 | 50 47 | 50 47 | 50 47 | dB |
| PSRR | Power Supply Rejection Ratio | $\pm 4V \leq V_S \leq \pm 6V$ | 80 | 70 67 | 70 67 | 64 60 | min |
| R_O | Output Resistance | $A_V = -1$ $f = 300\text{ kHz}$ | 0.25 | | | | Ω |
| R_{IN} | Non-Inverting Input Resistance | | 8 | | | | $\text{M}\Omega$ |
| V_O | Output Voltage Swing | $R_L = 1\text{ k}\Omega$ | 2.6 | 2.25 2.0 | 2.25 2.0 | 2.25 2.0 | V |
| | | $R_L = 150\Omega$ | 2.2 | 2.0 1.8 | 2.0 1.8 | 2.0 1.8 | min |
| I_{SC} | Output Short Circuit Current | | 100 | 65 35 | 65 40 | 65 40 | mA min |
| Z_T | Transimpedance | $R_L = 1\text{ k}\Omega$ | 1.4 | 0.75 0.3 | 0.75 0.35 | 0.6 0.3 | $\text{M}\Omega$ |
| | | $R_L = 150\Omega$ | 1.0 | 0.5 0.2 | 0.5 0.25 | 0.4 0.2 | min |
| I_S | Supply Current | No Load, $V_{IN} = 0V$ Both Amplifiers | 17 13 | 17 18.5 | 17 18.5 | 17 18.5 | mA max |
| V_{CM} | Input Common Mode Voltage Range | | $V^+ - 1.7V$ $V^- + 1.7V$ | | | | V |

| Symbol | Parameter | Conditions | Typical (Note 5) | LM6182AM | LM6182AI | LM6182I | Units |
|------------|--|--|---------------------|-------------------|-------------------|-------------------|------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | Limit (Note 6) | |
| Xt | Crosstalk Rejection | (Note 7) | 92 | | | | dB |
| BW | Closed Loop Bandwidth – 3 dB | $A_V = +2$ | 50 | | | | |
| | | $A_V = +10$ | 40 | | | | |
| | | $A_V = -1$ | 55 | | | | |
| | | $A_V = -10$ | 35 | | | | |
| | Closed Loop Bandwidth 0.1 dB Flat, $R_{SOURCE} = 200\Omega$ | $A_V = +2, R_L = 150\Omega$ | 15 | | | | |
| PBW | Power Bandwidth | $A_V = -1, V_O = 4 V_{PP}$ | 40 | | | | |
| SR | Slew Rate | $A_V = -1, V_O = \pm 2V$ $R_L = 150\Omega$, (Note 8) | 500 | 375 | 375 | 375 | V/ μ s min |
| t_s | Settling Time (0.1%) | $A_V = -1, V_O = \pm 2V$ $R_L = 150\Omega$ | 50 | | | | ns |
| t_r, t_f | Rise and Fall Time | $V_O = 1 V_{PP}$ | 8.5 | | | | |
| t_p | Propagation Delay Time | $V_O = 1 V_{PP}$ | 8 | | | | |
| in(+) | Non-Inverting Input Noise Current Density | $f = 1 \text{ kHz}$ | 3 | | | | pA/ $\sqrt{\text{Hz}}$ |
| in(-) | Inverting Input Noise Current Density | $f = 1 \text{ kHz}$ | 16 | | | | pA/ $\sqrt{\text{Hz}}$ |
| e_n | Input Noise Voltage Density | $f = 1 \text{ kHz}$ | 4 | | | | nV/ $\sqrt{\text{Hz}}$ |
| | Second Harmonic Distortion | $V_O = 2 V_{PP}, f = 10 \text{ MHz}$ $A_V = +2$ | -45 | | | | dBc |
| | Third Harmonic Distortion | $V_O = 2 V_{PP}, f = 10 \text{ MHz}$ $A_V = +2$ | -55 | | | | |
| | Differential Gain | $R_L = 150\Omega$ $A_V = +2$, NTSC | 0.06 | | | | % |
| | Differential Phase | $R_L = 150\Omega$ $A_V = +2$, NTSC | 0.16 | | | | Deg |
| THD | Total Harmonic Distortion | $V_O = 2 V_{PP}, A_V = +2$, $f = 5 \text{ MHz}, R_L = 150\Omega$ | 0.36 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model 100 pF and 1.5 k Ω .

Note 3: The typical junction-to-ambient thermal resistance of the molded plastic DIP(N) soldered directly into a PC board is 95°C/W. The junction-to-ambient thermal resistance of the S.O. surface mount (M) package mounted flush to the PC board is 70°C/W when pins 1, 4, 8, 9 and 16 are soldered to a total of 2 in² 1 oz copper trace. The S.O. (M) package must have pin 4 and at least one of pins 1, 8, 9, or 16 connected to V– for proper operation.

Note 4: Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowable junction temperature of 150°C. Each amplifier of the LM6182 is short circuit current limited to 100 mA typical.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**boldface type**).

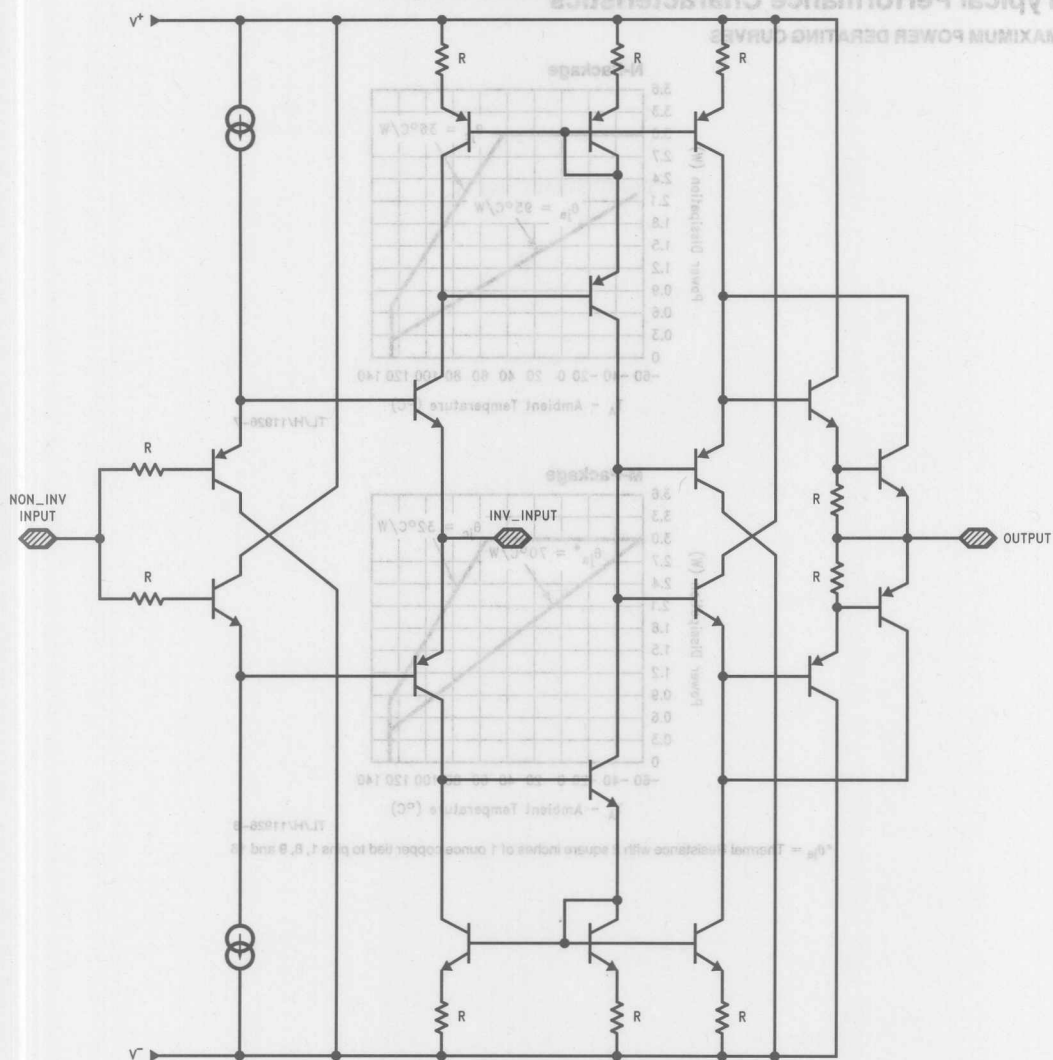
Note 7: Each amp excited in turn with 100 kHz to produce $V_O = 2 V_{PP}$. Results are input referred.

Note 8: Measured from +25% to +75% of output waveform.

Note 9: Also available per the Standard Military Drawing, 5962-9460301MCA.

Note 10: For guaranteed military specifications see military datasheet MNL6182AM-X.

Simplified Schematic 1/2 LM6182

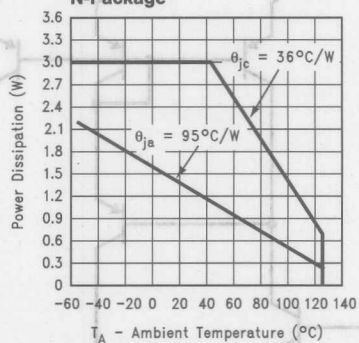


TL/H/11926-6

Typical Performance Characteristics

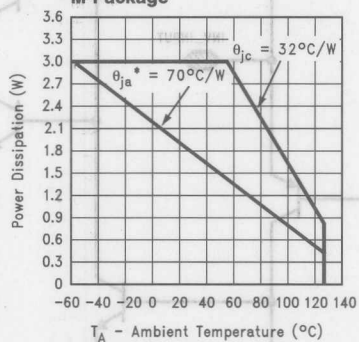
MAXIMUM POWER DERATING CURVES

N-Package



TL/H/11926-7

M-Package



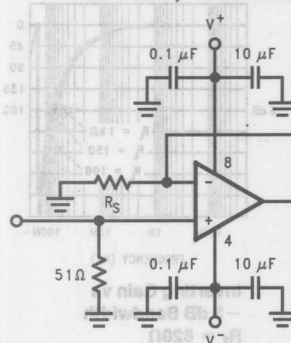
TL/H/11926-8

* θ_{ja} = Thermal Resistance with 2 square inches of 1 ounce copper tied to pins 1, 8, 9 and 16

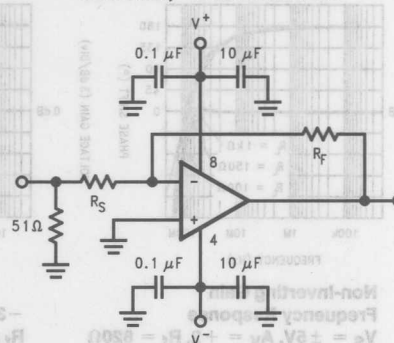
Typical Performance Characteristics (Continued)

TYPICAL PERFORMANCE TEST CIRCUITS

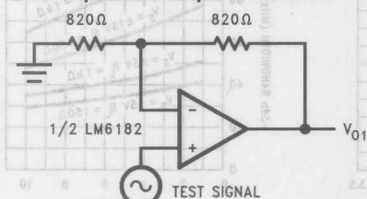
Non-Inverting:
Small Signal Pulse Response,
Slew Rate, -3 dB Bandwidth



Inverting:
Small Signal Pulse Response,
Slew Rate, -3 dB Bandwidth



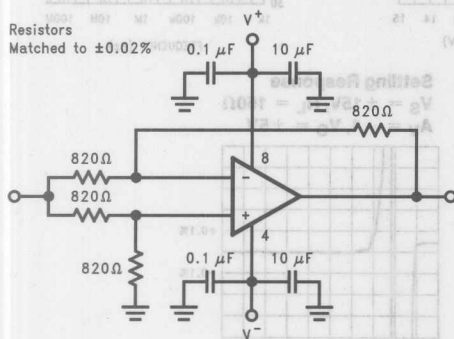
Amplifier-to-Amplifier Isolation



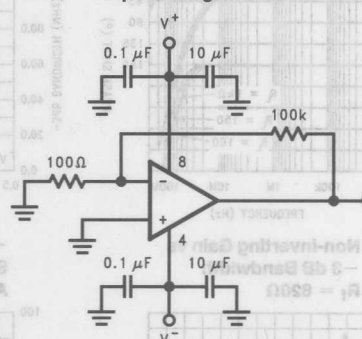
$$X_T (\text{Crosstalk Rejection}) = \frac{V_{01}}{V_{02}}$$

CMRR

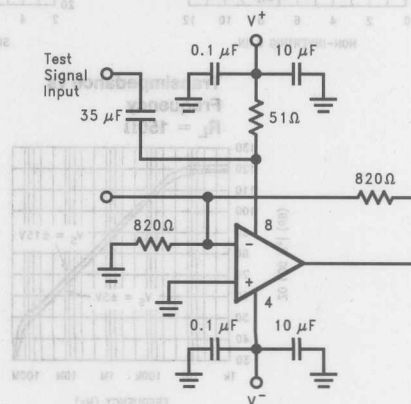
Resistors
Matched to $\pm 0.02\%$



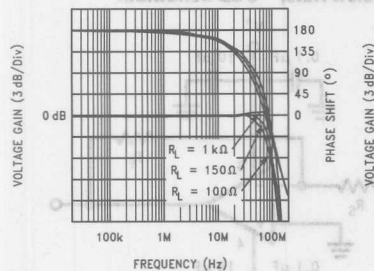
Input Voltage Noise



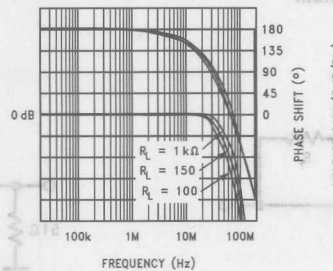
PSRR (VS+)



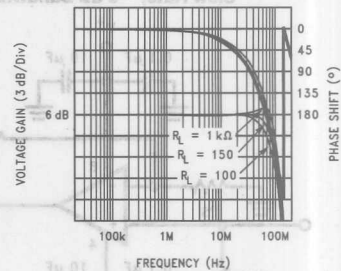
frequency response
 $V_S = \pm 15V, A_V = -1, R_f = 820\Omega$



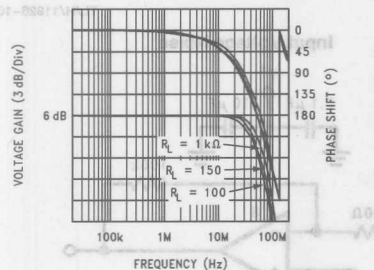
frequency response
 $V_S = \pm 5V, A_V = -1, R_f = 820\Omega$



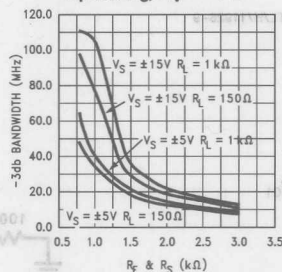
Frequency Response
 $V_S = \pm 15V, A_V = +2, R_f = 820\Omega$



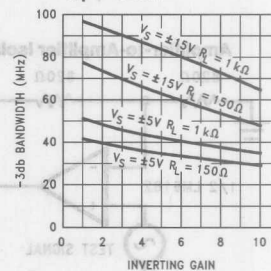
Non-Inverting Gain
Frequency Response
 $V_S = \pm 5V, A_V = +2, R_f = 820\Omega$



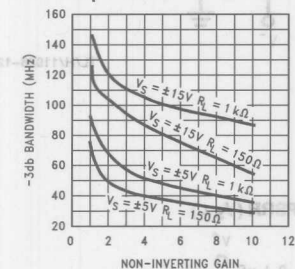
-3 dB Bandwidth vs
 R_f and $R_S, A_V = +2$



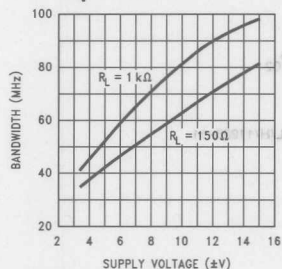
Inverting Gain vs
-3 dB Bandwidth
 $R_f = 820\Omega$



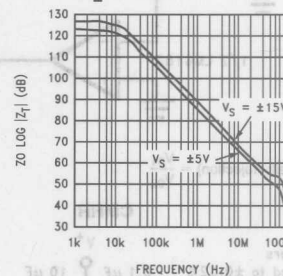
Non-Inverting Gain vs
-3 dB Bandwidth
 $R_f = 820\Omega$



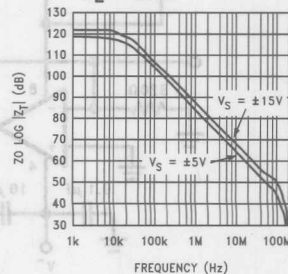
-3 dB Bandwidth vs
Supply Voltage
 $A_V = -1$



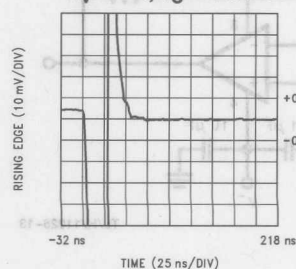
Transimpedance vs
Frequency
 $R_L = 1k\Omega$



Transimpedance vs
Frequency
 $R_L = 150\Omega$

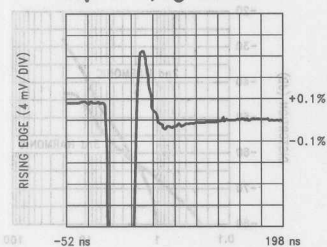


Settling Response
 $V_S = \pm 15V, R_L = 150\Omega$
 $A_V = -1, V_O = \pm 5V$

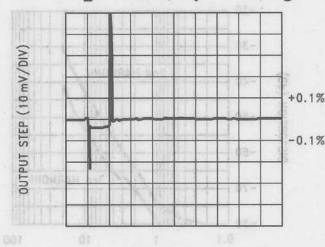


Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25^\circ C$ unless otherwise noted.

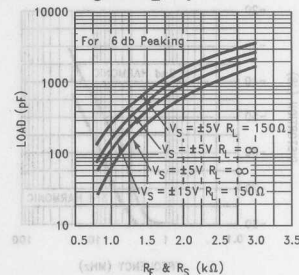
Settling Response
 $V_S = \pm 5V$, $R_L = 150\Omega$
 $A_V = -1$, $V_O = \pm 2V$



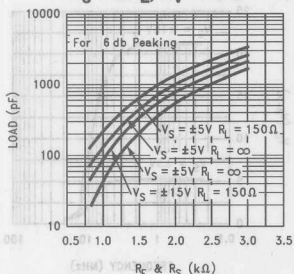
Long Term Settling Time Response $V_S = \pm 15V$,
 $R_L = 150\Omega$, $A_V = -1$, $V_O = \pm 5V$



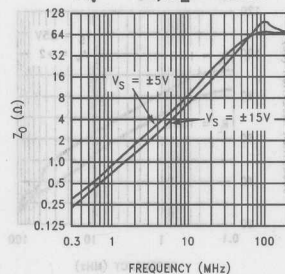
Suggested R_f and R_s for C_L , $A_V = 1$



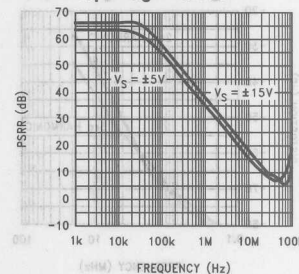
Suggested R_f and R_s for C_L , $A_V = +2$



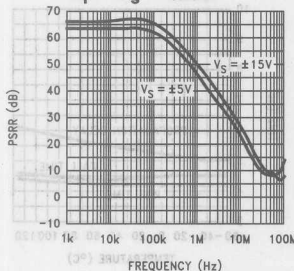
Output Impedance vs Frequency
 $A_V = -1$, $R_L = 820\Omega$



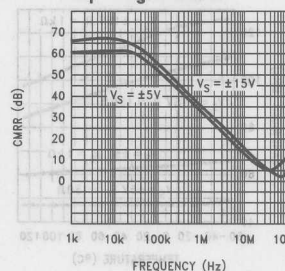
**PSRR (V_{S+}) vs Frequency, $A_V = 2$,
 $R_f = R_s = 820\Omega$**



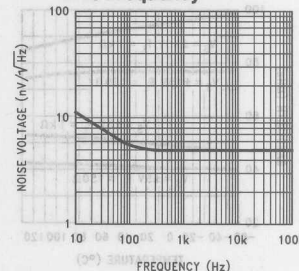
**PSRR (V_{S-}) vs Frequency, $A_V = 2$,
 $R_f = R_s = 820\Omega$**



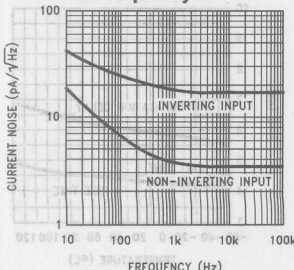
CMRR vs Frequency
 $R_f = R_s = 820\Omega$



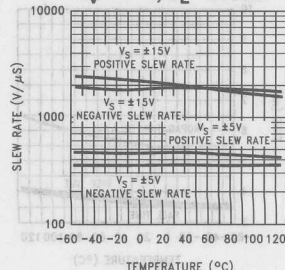
Input Voltage Noise vs Frequency



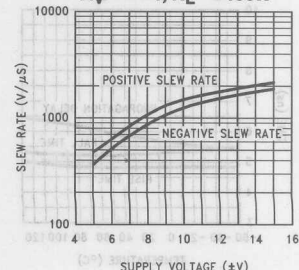
Input Current Noise vs Frequency



Slew Rate vs Temperature
 $A_V = -1$, $R_L = 150\Omega$



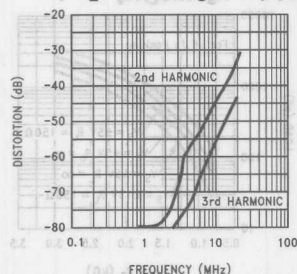
Slew Rate vs Supply Voltage
 $A_V = -1$, $R_L = 150\Omega$



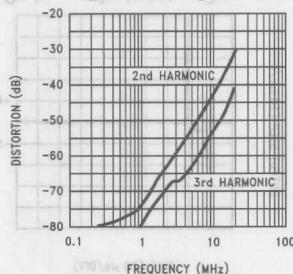
TL/H/11926-16

Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25^\circ C$ unless otherwise noted.

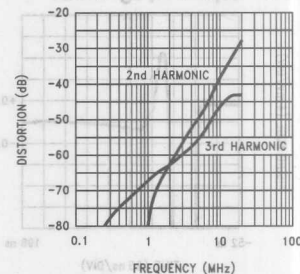
Distortion vs Frequency
 $V_S = \pm 15V, A_V = +2,$
 $R_L = 150\Omega, V_O = 2V_{p-p}$



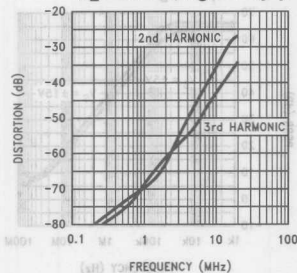
Distortion vs Frequency
 $V_S = \pm 15V, A_V = -1,$
 $R_L = 150\Omega, V_O = 2V_{p-p}$



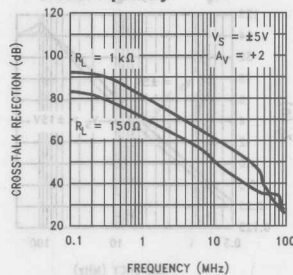
Distortion vs Frequency
 $V_S = \pm 5V, A_V = +2,$
 $R_L = 150\Omega, V_O = 2V_{p-p}$



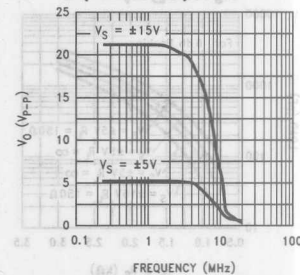
Distortion vs Frequency
 $V_S = \pm 5V, A_V = -1,$
 $R_L = 150\Omega, V_O = 2V_{p-p}$



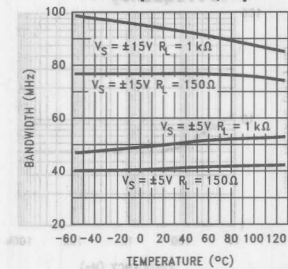
Crosstalk Rejection vs Frequency



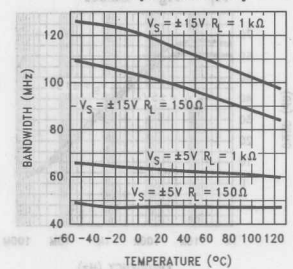
Maximum Output Voltage Swing vs Frequency (THD ≤ 1%)



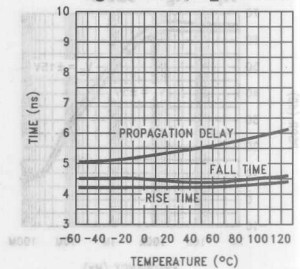
-3 dB Bandwidth vs Temperature, $A_V = -1$



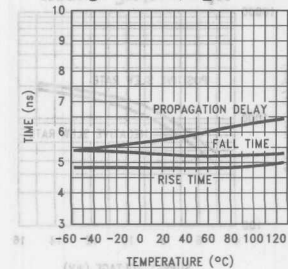
-3 dB Bandwidth vs Temperature, $A_V = +2$



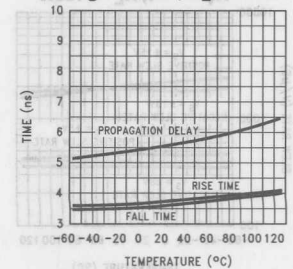
**Small Signal Pulse Response vs Temperature, $A_V = -1,$
 $V_S = \pm 15V, R_L = 1k\Omega$**



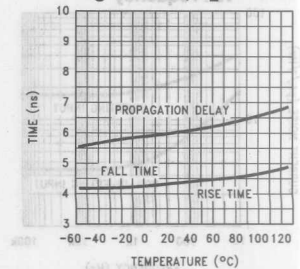
**Small Signal Pulse Response vs Temperature, $A_V = -1,$
 $V_S = \pm 15V, R_L = 150\Omega$**



**Small Signal Pulse Response vs Temperature, $A_V = +2,$
 $V_S = \pm 15V, R_L = 1k\Omega$**

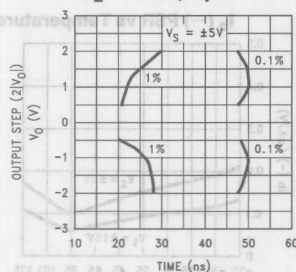


**Small Signal Pulse Response vs Temperature, $A_V = +2,$
 $V_S = \pm 15V, R_L = 150\Omega$**

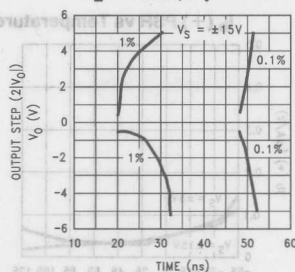


Typical Performance Characteristics (Continued) $V_S = \pm 15V$ and $T_A = 25^\circ C$ unless otherwise noted.

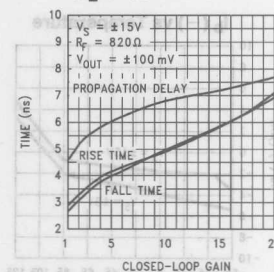
**Settling Time vs
Output Step, $R_F = 820\Omega$
 $R_L = 150\Omega$, $A_V = -1$**



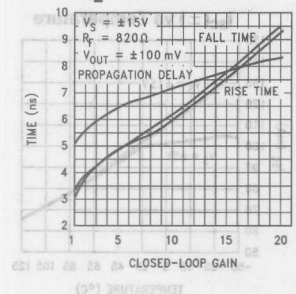
**Settling Time vs
Output Step, $R_F = 820\Omega$
 $R_L = 150\Omega$, $A_V = -1$**



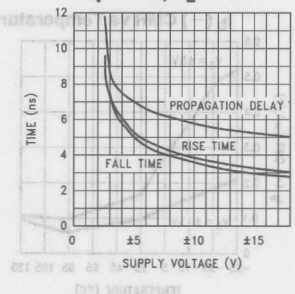
**Small Signal Pulse Response
vs Closed-Loop Gain
 $R_L = 1k$**



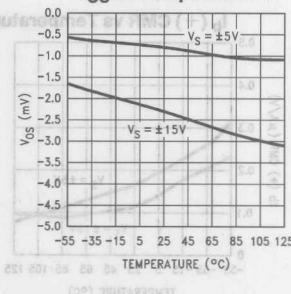
**Small Signal Pulse Response
vs Closed-Loop Gain
 $R_L = 150\Omega$**



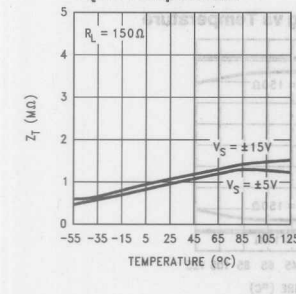
**Small Signal Pulse Response
vs Supply Voltage
 $A_V = +2$, $R_L = 1k$**



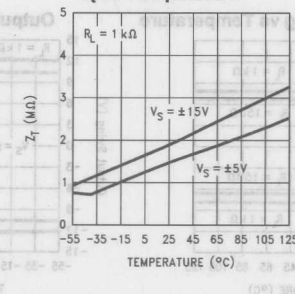
V_{OS} vs Temperature



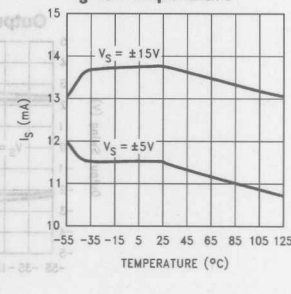
Z_t vs Temperature



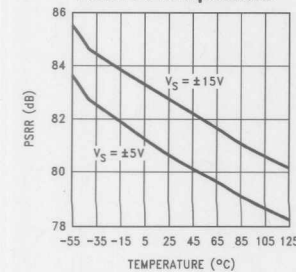
Z_t vs Temperature



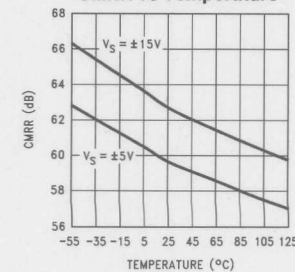
I_S vs Temperature



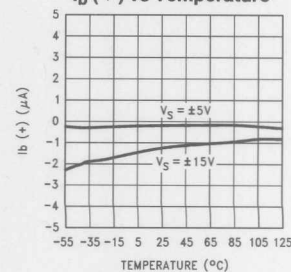
PSRR vs Temperature



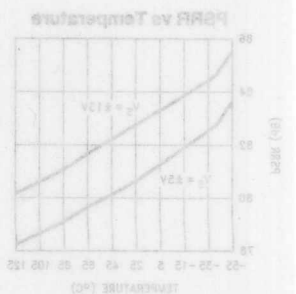
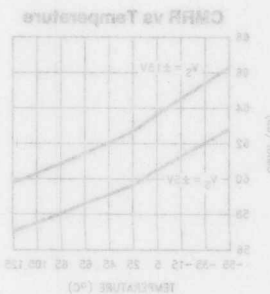
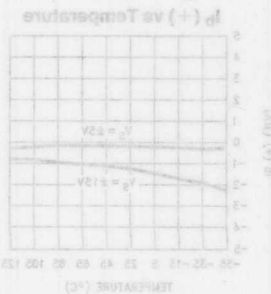
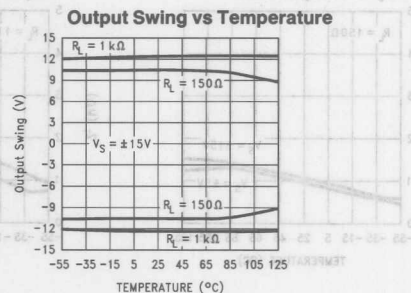
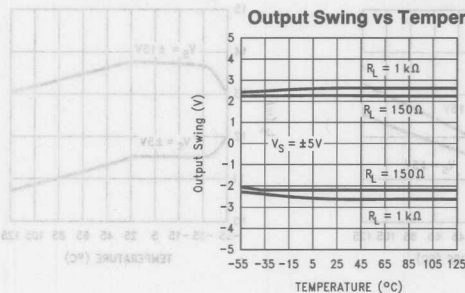
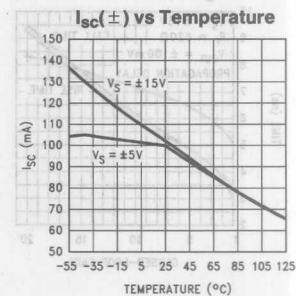
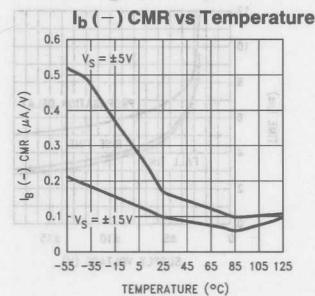
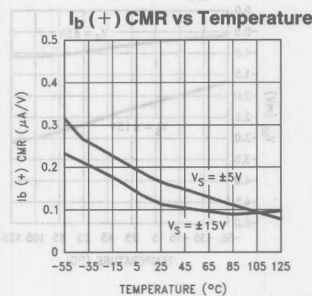
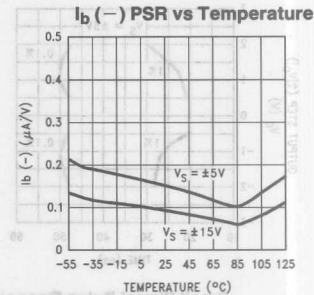
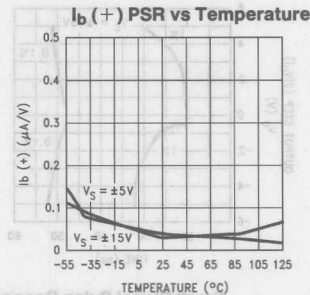
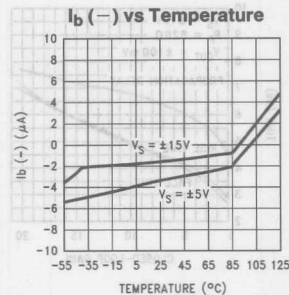
CMRR vs Temperature



$I_b (+)$ vs Temperature



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Typical Applications

CURRENT FEEDBACK TOPOLOGY

For a conventional voltage feedback amplifier the resulting small-signal bandwidth is inversely proportional to the desired gain to a first order approximation based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6182, transcends this limitation to offer a signal bandwidth that is relatively independent of the closed loop gain. Figures 1A and 1B illustrate that for closed loop gains of -1 and -5 the resulting pulse fidelity suggests quite similar bandwidths for both configurations.

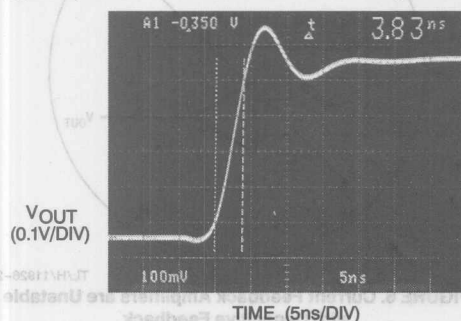


FIGURE 1A. $A_V = -1$

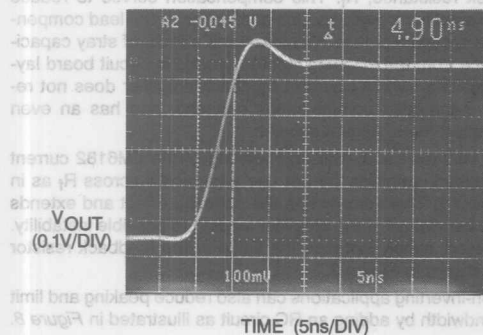
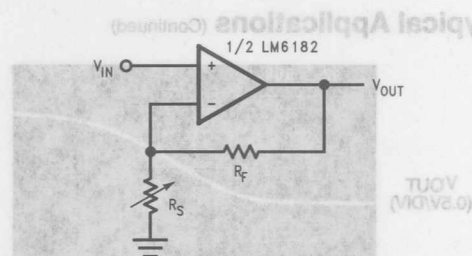


FIGURE 1B. $A_V = -5$

FIGURE 1A, 1B. Variation of Closed-Loop Gain from -1 to -5 Yields Similar Responses.

FEEDBACK RESISTOR SELECTION: R_f

Selecting the feedback resistor, R_f , is a dominant factor in compensating the LM6182. For general applications the LM6182 will maintain specified performance with an 820Ω feedback resistor. The closed-loop bandwidth of the LM6182 depends on the feedback resistance, R_f . Therefore, R_s , and not R_f , is varied to adjust for the desired closed-loop gain as demonstrated in Figure 2.



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FIGURE 2. R_f Sets Amplifier Bandwidth and R_s Is Adjusted to Obtain the Desired Closed-Loop Gain, A_V .

Although this R_f value will provide good results for most applications, it may be advantageous to adjust this value slightly. Consider, for instance, the effect on pulse responses with two different configurations where both the closed-loop gains are $+2$ and the feedback resistors are 820Ω , and 1640Ω , respectively. Figures 3A and 3B illustrate the effect of increasing R_f while maintaining the same closed-loop gain – the amplifier bandwidth decreases. Accordingly, larger feedback resistors can be used to slow down the LM6182 and reduce overshoot in the time domain response. Conversely, smaller feedback resistance values than 820Ω can be used to compensate for the reduction of bandwidth at high closed-loop gains, due to 2nd order effects. For example Figures 4A and 4B illustrate reducing R_f to 500Ω to establish the desired small signal response in an amplifier configured for a closed-loop gain of $+25$.

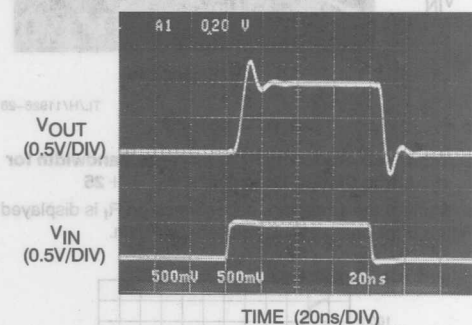


FIGURE 3A. $R_f = 820\Omega$

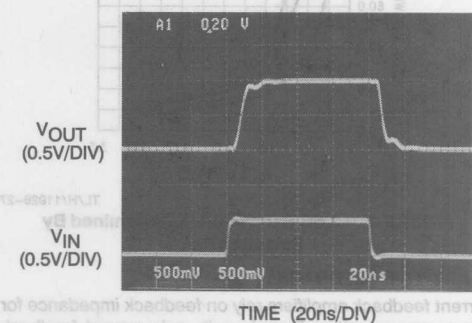


FIGURE 3B. $R_f = 1640\Omega$

FIGURE 3A, 3B. Increase Compensation by Increasing R_f , $A_V = +2$

Typical Applications (Continued)

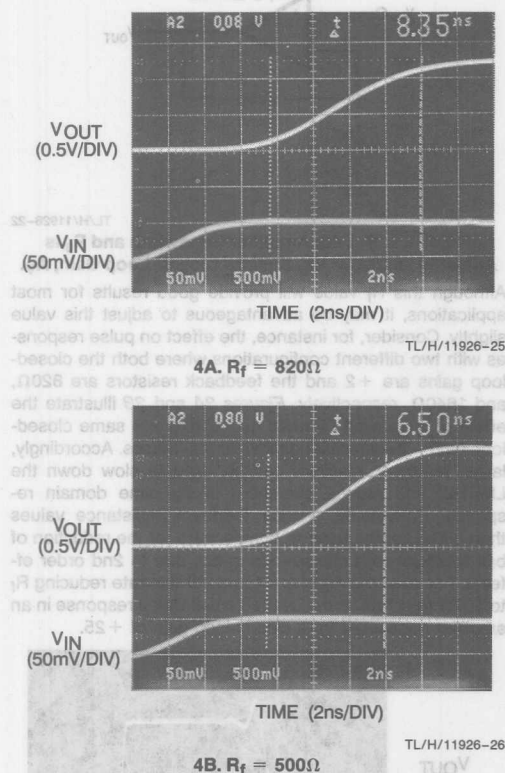


FIGURE 4A, 4B. Reducing R_f to Increase Bandwidth for Large Closed-Loop Gains, $A_v = +25$

The extent of the amplifier's dependence on R_f is displayed in Figure 5 for one particular closed-loop gain.

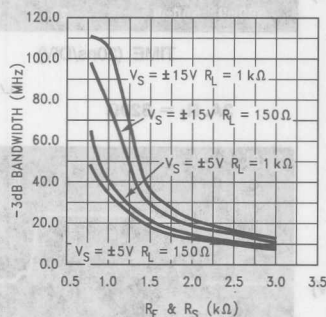


FIGURE 5. -3 dB Bandwidth Is Determined By Selecting R_f .

CAPACITIVE FEEDBACK

Current feedback amplifiers rely on feedback impedance for proper compensation. Even in unity gain current feedback amplifiers require a feedback resistor. LM6182 performance

is specified for a feedback resistance of 820Ω . Decreasing the feedback impedance below 820Ω extends the amplifier's bandwidth leading to possible instability. Capacitive feedback should therefore not be used because the impedance of a capacitor decreases with increasing frequency.

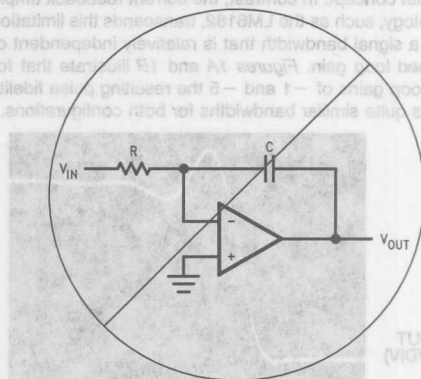


FIGURE 6. Current Feedback Amplifiers are Unstable with Capacitive Feedback

For voltage feedback amplifiers it is quite common to place a small lead compensation capacitor in parallel with feedback resistance, R_f . This compensation serves to reduce the amplifier's peaking. One application of the lead compensation capacitor is to counteract the effects of stray capacitance from the inverting input to ground in circuit board layouts. The LM6182 current feedback amplifier does not require this lead compensation capacitor and has an even simpler, more elegant solution.

To limit the bandwidth and peaking of the LM6182 current feedback amplifier, do not use a capacitor across R_f as in Figure 7. This actually has the opposite effect and extends the bandwidth of the amplifier leading to possible instability. Instead, simply increase the value of the feedback resistor as shown in Figure 3.

Non-inverting applications can also reduce peaking and limit bandwidth by adding an RC circuit as illustrated in Figure 8.

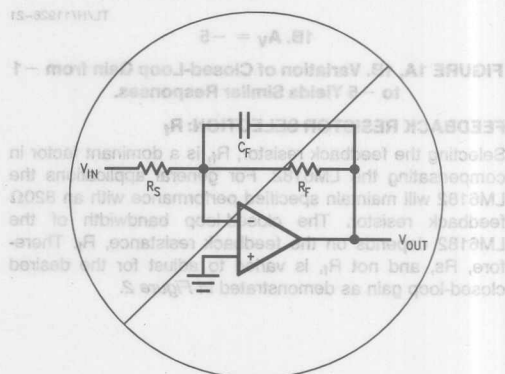


FIGURE 7. Compensation Capacitors Are Not Used with the LM6182, Instead Simply Increase R_f to Compensate

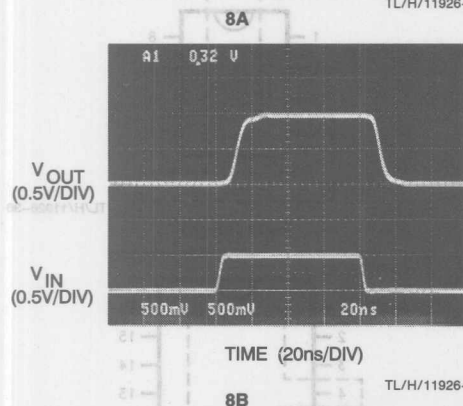
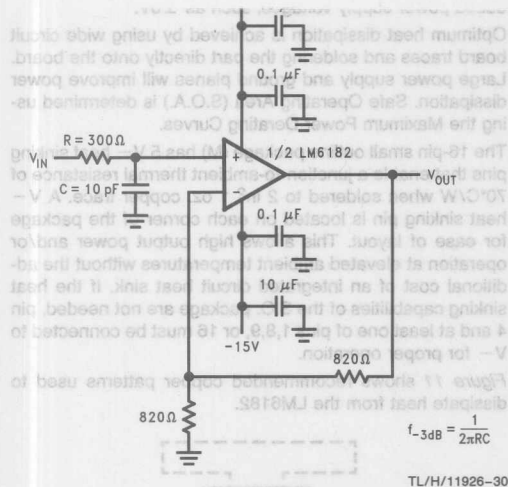


FIGURE 8A, 8B. RC Limits Amplifier Bandwidth to 50 MHz, Eliminating Peaking in the Resulting Pulse Response as Compared to Figure 3A

SLEW RATE CONSIDERATIONS

The slew rate characteristics of current feedback amplifiers are different than traditional voltage feedback amplifiers. In voltage feedback amplifiers, slew rate limiting or non-linear amplifier behavior is dominated by the finite availability of the 1st stage tail current charging the compensation capacitor. The slew rate of current feedback amplifiers, in contrast, is not constant. Transient current at the inverting input is proportional to the current available to the amplifier's com-

mon mode not necessarily the tail current. The non-inverting configuration slew rate is also determined by input stage limitations. Accordingly, variations of slew rates occur for different circuit topologies.

DRIVING CAPACITIVE LOADS

The LM6182 can drive significantly larger capacitive loads than many current feedback amplifiers. This is extremely valuable for simplifying the design of coax-cable drivers. Although the LM6182 can directly drive as much as 100 pF of load capacitance without oscillating, the resulting response will be a function of the feedback resistor value. Figure 9B illustrates the small-signal pulse response of the LM6182 while driving a 50 pF load. Ringing persists for approximately 100 ns. To achieve pulse responses with less ringing either the feedback resistor can be increased (see Typical Performance Characteristics "Suggested R_f and R_s for C_L "), or resistive isolation can be used (10Ω–51Ω typically works well). Either technique, however, results in lowering the system bandwidth.

Figure 10B illustrates the improvement obtained by using a 47Ω isolation resistor.

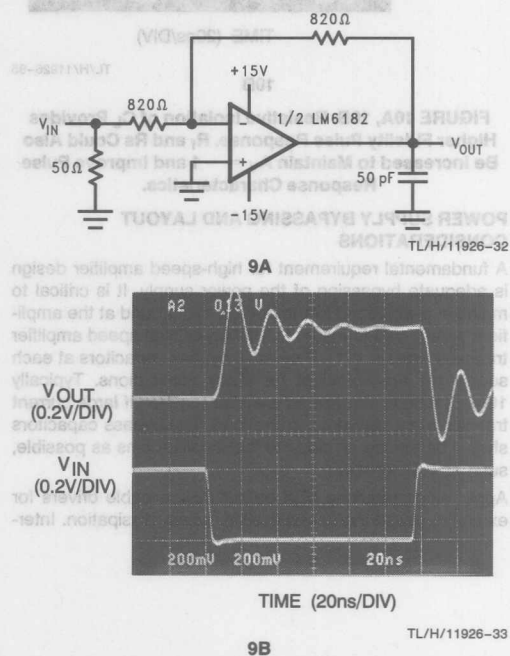
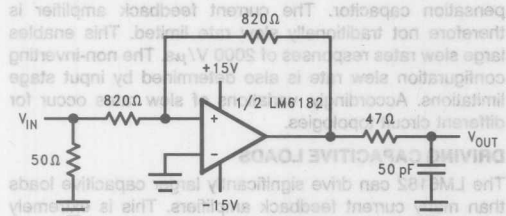


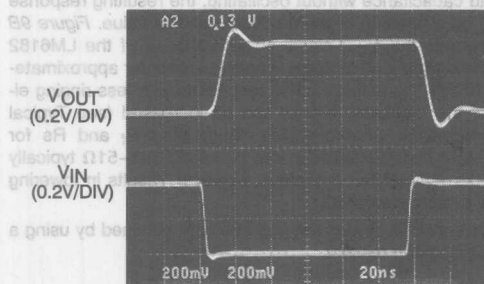
FIGURE 9A, 9B. $A_V = -1$, LM6182 Can Directly Drive 50 pF of Load Capacitance with 100 ns of Ringing Resulting in Pulse Response

Typical Applications (Continued)



10A

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10B

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FIGURE 10A, 10B. Resistive Isolation of C_L Provides Higher Fidelity Pulse Response. R_f and R_s Could Also Be Increased to Maintain $A_v = -1$ and Improve Pulse Response Characteristics.

POWER SUPPLY BYPASSING AND LAYOUT CONSIDERATIONS

A fundamental requirement for high-speed amplifier design is adequate bypassing of the power supply. It is critical to maintain a wideband low-impedance to ground at the amplifiers supply pins to insure the fidelity of high speed amplifier transient signals. 0.1 μ F ceramic bypass capacitors at each supply pin are sufficient for many applications. Typically 10 μ F tantalum capacitors are also required if large current transients are delivered to the load. The bypass capacitors should be placed as close to the amplifier pins as possible, such as 0.5" or less.

Applications requiring high output power, cable drivers for example, cause increased internal power dissipation. Inter-

nal power dissipation can be minimized by operating at reduced power supply voltages, such as ± 5 V.

Optimum heat dissipation is achieved by using wide circuit board traces and soldering the part directly onto the board. Large power supply and ground planes will improve power dissipation. Safe Operating Area (S.O.A.) is determined using the Maximum Power Derating Curves.

The 16-pin small outline package (M) has 5 V— heat sinking pins that enable a junction-to-ambient thermal resistance of 70°C/W when soldered to 2 in² 1 oz. copper trace. A V— heat sinking pin is located on each corner of the package for ease of layout. This allows high output power and/or operation at elevated ambient temperatures without the additional cost of an integrated circuit heat sink. If the heat sinking capabilities of the S.O. package are not needed, pin 4 and at least one of pins 1, 8, 9, or 16 must be connected to V— for proper operation.

Figure 11 shows recommended copper patterns used to dissipate heat from the LM6182.

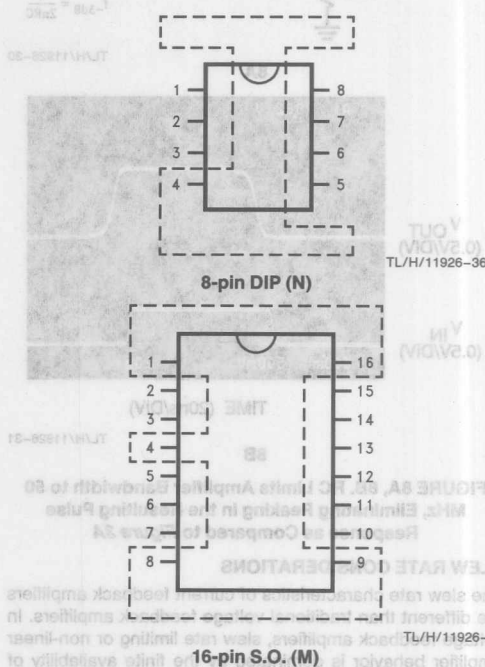
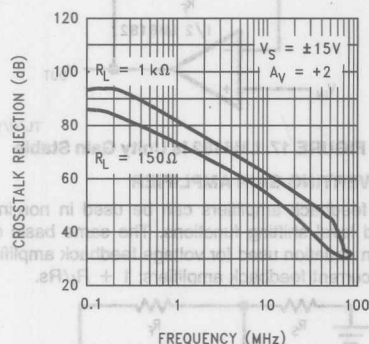


FIGURE 11. Copper Heatsink Layouts

Typical Applications (Continued)

CROSSTALK REJECTION

The LM6182 has an excellent crosstalk rejection value of 62 dB at 10 MHz. This value is made possible because the LM6182 amplifiers share no common circuitry other than the supply. High frequency crosstalk that does appear is primarily caused by the magnetic and capacitive coupling of the internal bond wires. Bond wires connect the die to the package lead frame. The amount of current flowing through the bond wires is proportional to the amount of crosstalk. Therefore, crosstalk rejection ratings will degrade when driving heavy loads. Figure 12 and shows a 10 dB difference for two different loads.



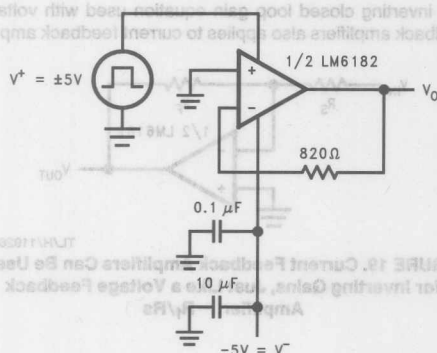
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FIGURE 12. Crosstalk Rejection

The LM6182 crosstalk effect is minimized in applications that cascade the amplifiers by preceding amplifier A with amplifier B.

START-UP TIME

Using the circuit in Figure 13, the LM6182 demonstrated a start-up time of 50 ns.



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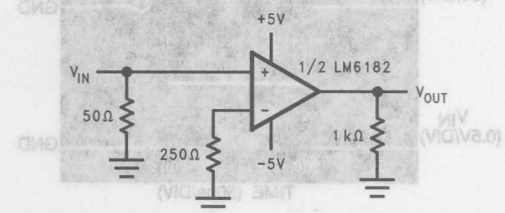
FIGURE 13. Start-Up Test Circuit

OVERDRIVE RECOVERY

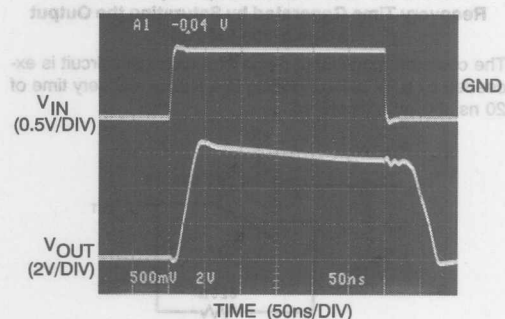
The LM6182 is an excellent choice for high speed applications needing fast overdrive recovery. Nanosecond recovery times allow the LM6182 to protect subsequent stages from excessive input saturation and possible damage.

When the output or input voltage range of a high speed amplifier is exceeded, the amplifier must recover from an overdrive condition. The non-linear output voltage remains as long as the overdrive condition persists. Linear operation resumes after the overdrive condition is removed. Overdrive recovery time is the delay before an amplifier returns to linear operation. The typical recovery times for exceeding open loop, closed loop, and input common-mode voltage ranges are illustrated in Figures 14, 15, and 16.

The open-loop circuit of Figure 14 generates an overdrive response by allowing the $\pm 0.5V$ input to exceed the linear input range of the amplifier. Typical positive and negative overdrive recovery times are 5 ns and 30 ns, respectively.



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FIGURE 14. Open Loop Overdrive Recovery Times of 5 ns and 30 ns

The large closed-loop gain configuration in Figure 15 forces the amplifier output into overdrive. The typical recovery time to a linear output value is 15 ns.

Typical Applications (Continued)

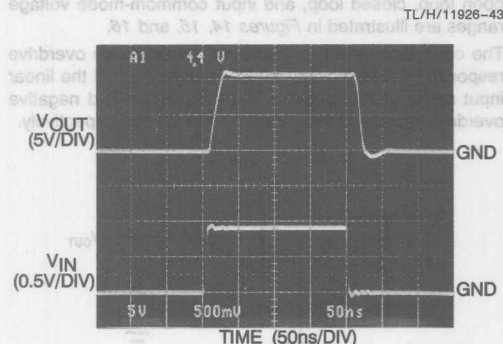
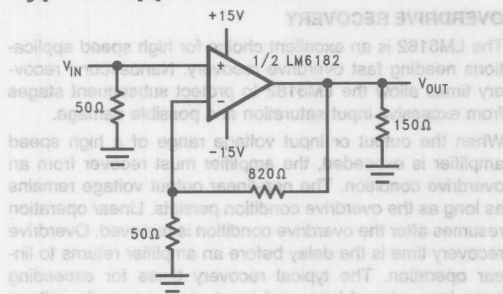


FIGURE 15. 15 ns Closed Loop Output Overdrive Recovery Time Generated by Saturating the Output Stage of the LM6182

The common-mode input range of a unity-gain circuit is exceeded by a 4V pulse resulting in a typical recovery time of 20 ns shown in Figure 16.

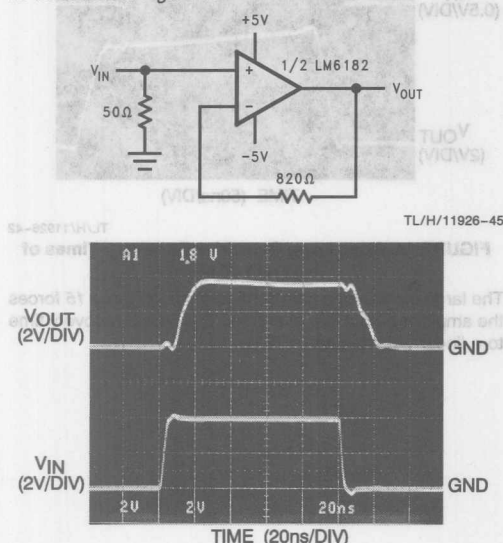


FIGURE 16. Output Recovery from an Input that Exceeds the Common-Mode Range

SPICE MACROMODEL

A spice macromodel is available for the LM6182. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Application Circuits

UNITY GAIN AMPLIFIER

The LM6182 current feedback amplifier is unity gain stable. The feedback resistor, R_f , is required to maintain the LM6182's dynamic performance.

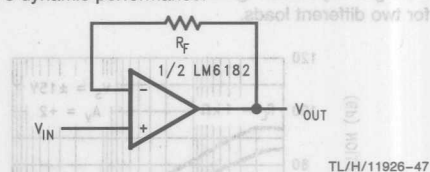


FIGURE 17. LM6182 Is Unity Gain Stable

NON-INVERTING GAIN AMPLIFIER

Current feedback amplifiers can be used in non-inverting gain and level shifting functions. The same basic closed-loop gain equation used for voltage feedback amplifiers applies to current feedback amplifiers: $1 + R_f/R_s$.



FIGURE 18. Non-Inverting Closed Loop Gain is Determined with the Same Equation Voltage Feedback Amplifiers Use: $1 + R_f/R_s$

INVERTING GAIN AMPLIFIER

The inverting closed loop gain equation used with voltage feedback amplifiers also applies to current feedback amplifiers.

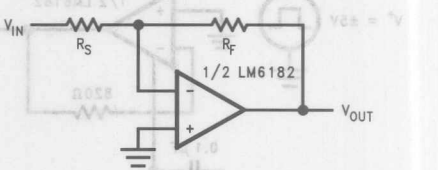
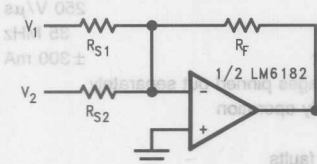


FIGURE 19. Current Feedback Amplifiers Can Be Used for Inverting Gains, Just Like a Voltage Feedback Amplifier: $-R_f/R_s$

Typical Application Circuits (Continued)

SUMMING AMPLIFIER

The current feedback topology of the LM6182 provides significant performance advantages over a conventional voltage feedback amplifier used in a standard summing circuit. Using a voltage feedback amplifier, the bandwidth of the summing circuit in Figure 20 is limited by the highest gain needed for either signal V1 or V2. If the LM6182 amplifier is used instead, wide circuit bandwidth can be maintained relatively independent of gain requirements.



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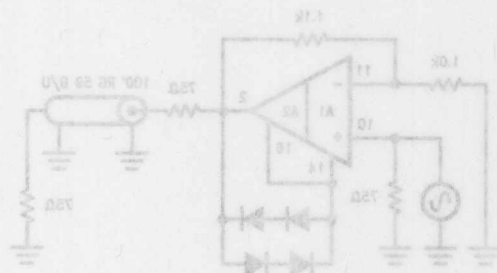
FIGURE 20. LM6182 Allows the Summing Circuit to Meet the Requirements of Wide Bandwidth Systems Independent of Signal Gain

Ordering Information

| Package | Temperature Range | | NSC Drawing |
|----------------------------|-----------------------------|------------------------------|-------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | |
| 8-pin Molded DIP | LM6182AMN | LM6182AIN LM6182IN | N08E |
| 16-pin Small Outline | | LM6182AIM LM6182IM | M16A |

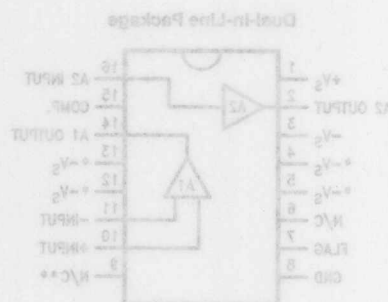
If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office or Distributors for availability and specifications.

Typical Application



TL/H/11926-50

Connection Diagram



LM6313 High Speed, High Power Operational Amplifier

General Description

The LM6313 is a high-speed, high-power operational amplifier. This operational amplifier features a 35 MHz small signal bandwidth, and 250 V/ μ s slew rate. A compensation pin is included for adjusting the open loop bandwidth. The input stage (A1) and output stage (A2) are pinned out separately, and can be used independently. The operational amplifier is designed for low impedance loads and will deliver ± 300 mA. The LM6313 has both overcurrent and thermal shutdown protection with an error flag to signal both these fault conditions.

These amplifiers are built with National's VIPTM (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

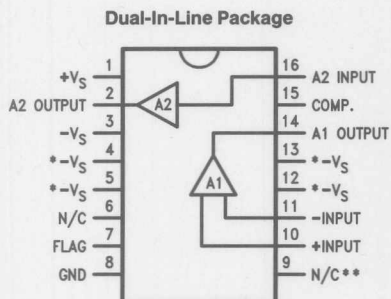
Features

- High slew rate 250 V/ μ s
- Wide bandwidth 35 MHz
- Peak output current ± 300 mA
- Input and output stages pinned out separately
- Single or dual supply operation
- Thermal protection
- Error flag warns of faults
- Wide supply voltage range ± 5 V to ± 15 V

Applications

- High speed ATE pin driver
- Data acquisition
- Driving capacitive loads
- Flash A-D input driver
- Precision 50 Ω –75 Ω video line driver
- Laser diode driver

Connection Diagram



Top View

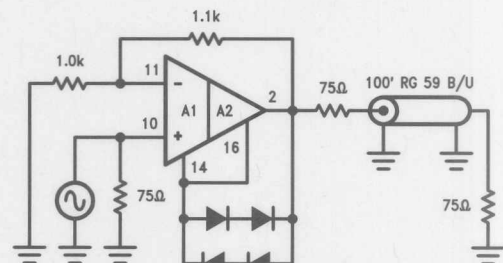
Order Number LM6313N
See NS Package Number N16A

*Heat sink pins

See Note 5 and Applications.

**Do not ground or otherwise connect to this pin.

Typical Application



TL/H/10521-2

Absolute Maximum Ratings (Note 1)

| | | | |
|---|--|---|-------------|
| Total Supply Voltage ($+V_S$ to $-V_S$) | 36V (± 18) | Lead Temperature (Soldering, 5 seconds) | 260°C |
| A1 Differential Input Voltage (Note 2) | $\pm 7V$ | ESD Tolerance (Note 4) | $\pm 600V$ |
| A1 Input Voltage | ($V^+ - 0.7$) to ($V^- - 7V$) | Pins 10 and 11 | $\pm 1500V$ |
| A2 Input to Output Voltage | $\pm 7V$ | All Other Pins | |
| A2 Input Voltage | $\pm V_S$ | Operating Temperature Range | 0°C to 70°C |
| Flag Output Voltage | GND to $+V_S$ | LM6313N | |
| Short-Circuit to Ground | (Note 3) | Thermal Derating Information (Note 5) | |
| Storage Temperature Range | $-65^\circ C \leq T \leq +150^\circ C$ | θ_{JA} | 40°C/W |
| | | T_J (Max) | 125°C |

Operational Amplifier DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ C$, and Supply Voltage $V_S = \pm 15V$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0V$, $R_S = 50\Omega$, the circuit configured as in Figure 1.

| Symbol | Parameter | Conditions | Typical | 25°C Limit | 0°C to 70°C Limit | Units |
|--------------------------|------------------------------------|--|----------------|----------------|------------------------------|-------------------|
| V_{OS} | Input Offset Voltage | | 5 | 20 | 22 | mV (Max) |
| $\Delta V_{OS}/\Delta T$ | Average Input Offset Voltage Drift | | 10 | | | $\mu V/^\circ C$ |
| I_b | Input Bias Current | | 2 | 5 | 7 | μA (Max) |
| I_{OS} | Input Offset Current | | 0.15 | 1.5 | 1.9 | μA (Max) |
| $\Delta I_{OS}/\Delta T$ | Average Input Offset Current Drift | | 0.4 | | | nA/°C |
| R_{IN} | Input Resistance | Differential | 325 | | | k Ω |
| C_{IN} | Input Capacitance | $A_V = +1, f = 10 \text{ MHz}$ | 2.2 | | | pF |
| V_{CM} | Common-Mode Voltage Range | | +14.2 -13.2 | +13.8 -12.8 | +13.7 -12.7 | V (Min) |
| A_{V1} | Voltage Gain 1 | $R_L = 1 \text{ k}\Omega, V_O = \pm 10V$ | 6000 | 2500 | 2000 | V/V (Min) |
| A_{V2} | Voltage Gain 2 | $R_L = 50\Omega, V_O = \pm 8V$ | 5000 | 2000 | 1500 | |
| CMRR | Common-Mode Rejection Ratio | $-10V \leq V_{CM} \leq +10V$ | 90 | 72 | 70 | dB (Min) |
| PSRR | Power Supply Rejection Ratio | $\pm 5V \leq V_S \leq \pm 16V$ | 90 | 72 | 70 | dB (Min) |
| V_{O1} | Output Voltage Swing 1 | $R_L = 1 \text{ k}\Omega$ | 13.1 | 11.8 | 11.2 | $\pm V$ (Min) |
| V_{O2} | Output Voltage Swing 2 | $R_L = 100\Omega$ | 12.0 | 10.5 | 10.0 | |
| V_{O3} | Output Voltage Swing 3 | $R_L = 50\Omega$ | 11.0 | 9.0 | 8.5 | |
| I_S | Supply Current | $T_J = 0^\circ C$ $T_J = 25^\circ C$ $T_J = 125^\circ C$ | 18 | 23 | 24 21 | mA (Max) |
| I_{SC} | Peak Short-Circuit Output | (See Figure 3) | 300 | | | mA |

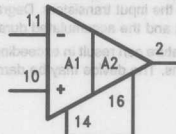


FIGURE 1

TL/H/10521-3

Electrical Characteristics (Continued)

Operational Amplifier AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, and Supply Voltage $V_S = \pm 15\text{V}$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0\text{V}$, $R_S = 50\Omega$, the circuit configured as in *Figure 1*.

| Symbol | Parameter | Conditions | Typical | Units |
|--------|------------------------|--|---------|------------------------------|
| GBW | Gain-Bandwidth Product | @ $f = 30\text{ MHz}$ | 35 | MHz |
| SR | Slew Rate | $A_V = -1$, $R_L = 50\Omega$ (Note 6) | 250 | $\text{V}/\mu\text{s}$ |
| PBW | Power Bandwidth | $V_{OUT} = 20\text{ V}_{PP}$ | 3.0 | MHz |
| t_s | Settling Time | 10V Step to 0.1% (See <i>Figure 2</i>) | 200 | ns |
| | Phase Margin | $A_V = -1$, $R_L = 1\text{ k}\Omega$, $C_L = 50\text{ pF}$ | 53 | Deg |
| | Differential Gain | | 0.1 | % |
| | Differential Phase | | 0.1 | Deg |
| e_n | Input Noise Voltage | $f = 10\text{ kHz}$ | 14 | $\text{nV}/\sqrt{\text{Hz}}$ |
| i_n | Input Noise Current | $f = 10\text{ kHz}$ | 1.8 | $\text{pA}/\sqrt{\text{Hz}}$ |

A1 DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, and Supply Voltage $V_S = \pm 15\text{V}$. **Boldface** limits apply at temperature extremes. $V_{CM} = 0\text{V}$, $R_S = 50\Omega$.

| Symbol | Parameter | Conditions | Typical | 25°C Limit | 0°C to 70°C Limit | Units |
|-----------|------------------------------|--|-------------|-------------|----------------------------|---------------------------|
| A_{VOL} | Large Signal Voltage Gain | $V_{OUT} = \pm 10\text{V}$, $R_L = 2\text{ k}\Omega$ $V_{OUT} = \pm 10\text{V}$, $R_L = \infty$ | 650 6000 | 300 2500 | 250 2000 | V/V (Min) |
| CMRR | Common-Mode Rejection Ratio | $-10\text{V} \leq V_{CM} \leq +10\text{V}$ | 90 | 72 | 70 | dB (Min) |
| PSRR | Power Supply Rejection Ratio | $\pm 5\text{V} \leq V_S \leq \pm 16\text{V}$ | 90 | 72 | 70 | dB (Min) |
| I_{SC} | Output Short Circuit Current | | ± 60 | ± 30 | ± 25 | mA (Min) |

A1 AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, and Supply Voltage $V_S = \pm 15\text{V}$. **Boldface** limits apply at temperature extremes. $R_S = 50\Omega$.

| Symbol | Parameter | Conditions | Typical | 25°C Limit | Units |
|--------|----------------|---|---------|------------|------------------------------|
| GBW | Gain-Bandwidth | $f = 30\text{ MHz}$ | 37 | 25 | MHz (Min) |
| SR | Slew Rate | $A_V = +1$, $R_L = 100\text{ k}\Omega$, $\pm 4\text{ V}_{IN}$, $\pm 2\text{ V}_{OUT}$ | 250 | 150 | $\text{V}/\mu\text{s}$ (Min) |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test condition listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: In order to achieve optimum AC performance, the input stage was designed without protective clamps. Exceeding the maximum differential input voltage results in reverse breakdown of the base-emitter junction of one of the input transistors. Degradation of the input parameters (especially V_{OS} , I_{OS} , and Noise) is proportional to the level of the externally limited breakdown current and the accumulated duration of the breakdown condition.

Note 3: Continuous short-circuit operation of A1 at elevated temperature can result in exceeding the maximum allowed junction temperature of 125°C . A2 contains current limit and thermal shutdown to protect against fault conditions. The device may be damaged by shorts to the supplies.

Note 4: Human body model, $C = 100\text{ pF}$, $R_S = 1500\Omega$.

Electrical Characteristics (Continued)

A2 DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, and Supply Voltage $V_S = \pm 15\text{V}$. **Boldface** limits apply at temperature extremes. $R_S = 50\Omega$.

| Symbol | Parameter | Conditions | Typical | 25°C Limit | 0°C to 70°C Limit | Units |
|----------|------------------------------|---|----------------------|---------------------|--|---------------------|
| A_{V1} | Voltage Gain 1 | $R_L = 1\text{ k}\Omega$, $V_{IN} = \pm 10\text{V}$ | 0.99 | 0.97 | 0.95 | V/mV (Min) |
| A_{V2} | Voltage Gain 2 | $R_L = 50\Omega$, $V_{IN} = \pm 10\text{V}$ | 0.9 | 0.85 | 0.82 | V/V (Min) |
| V_{OS} | Offset Voltage | $R_L = 1\text{ k}\Omega$ | 15 | 70 | 100 | mV (Max) |
| I_b | Input Bias Current | $R_L = 1\text{ k}\Omega$, $R_S = 10\text{ k}\Omega$ | 1 | 6 | 8 | μA (Max) |
| R_{IN} | Input Resistance | $R_L = 50\Omega$ | 5 | | | M Ω |
| C_{IN} | Input Capacitance | | 3.5 | | | pF |
| R_O | Output Resistance | $I_{OUT} = \pm 10\text{ mA}$ | 3.5 | 5.0 | 8.0 | Ω (Min) |
| V_O | Voltage Output Swing | $R_L = 1\text{ k}\Omega$ $R_L = 100\Omega$ $R_L = 50\Omega$ | 13.7 12.5 11.0 | 13.0 10.5 9.0 | 12.7 10.0 8.5 | V (Min) |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 5\text{V}$ to $\pm 16\text{V}$ | 70 | 60 | 50 | dB (Min) |

A2 AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, and Supply Voltage $V_S = \pm 15\text{V}$. **Boldface** limits apply at temperature extremes. $R_S = 50\Omega$.

| Symbol | Parameter | Conditions | Typical | 25°C Limit | Units |
|----------------|----------------------------|---|-------------|------------|------------------------|
| SR 1 SR 2 | Slew Rate 1 Slew Rate 2 | $V_{IN} = \pm 11\text{V}$, $R_L = 1\text{ k}\Omega$ $V_{IN} = \pm 11\text{V}$, $R_L = 50\Omega$ (Note 7) | 1200 750 | | V/ μs (Min) |
| BW | -3 dB Bandwidth | $V_{IN} = \pm 100\text{ mVpp}$ $R_L = 50\Omega$, $C_L \leq 10\text{ pF}$ | 65 | 30 | MHz (Min) |
| t_r t_f | Rise Time Fall Time | $R_L = 1\text{ k}\Omega$, $C_L \leq 10\text{ pF}$ $V_O = 100\text{ mVpp}$ | 8 | | ns |
| P_D | Propagation Delay | $R_L = 50\Omega$, $C_L \leq 10\text{ pF}$ $V_O = 100\text{ mVpp}$ | 4 | | ns |
| | Overshoot | $R_L = 1\text{ k}\Omega$, $C_L = 100\text{ pF}$ $R_L = 50\Omega$, $C_L = 1000\text{ pF}$ | 13 21 | | % |

Additional (A2) Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_A = 25^\circ\text{C}$, and Supply Voltage $V_S = \pm 15\text{V}$. **Boldface** limits apply at temperature extremes.

| Symbol | Parameter | Conditions | Typical | 25°C Limit | 0°C to 70°C Limit | Units |
|----------|------------------------------|--|---------|------------|-------------------|---------------------|
| V_{OL} | Flag Pin Output Low Voltage | I_{SINK} Flag Pin = $500\text{ }\mu\text{A}$ | 220 | 340 | 400 | mV (Max) |
| I_{OH} | Flag Pin Output High Current | V_{OH} Flag Pin = 15V (Note 8) | 0.01 | 10 | 20 | μA (Max) |

Note 5: For operation at elevated temperature, these devices must be derated to insure $T_J \leq 125^\circ\text{C}$. $T_J = T_A + (P_D \times \theta_{JA})$. θ_{JA} for the N package mounted flush to the PCB, is 40°C/W when pins 4, 5, 12 and 13 are soldered to a total of 2 in^2 of copper trace.

Note 6: Measured between $\pm 5\text{V}$.

Note 7: $V_{IN} = \pm 9\text{V}$ step input, measured between $\pm 5\text{V}$ out.

Note 8: The error flag is set during current limit or thermal shut-down. The flag is an open collector, low on fault.

Settling Time Test Circuit

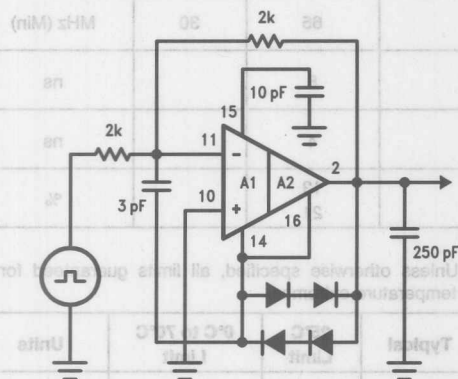
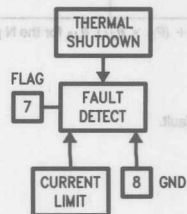


FIGURE 2

Protection Circuit Block Diagram



TL/H/10521-7

MAXIMUM CURRENT vs JUNCTION TEMPERATURE

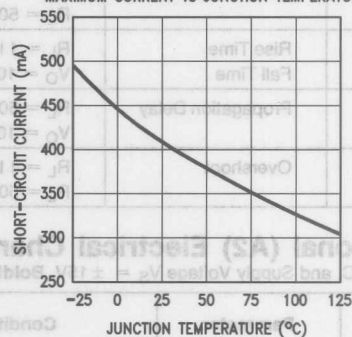
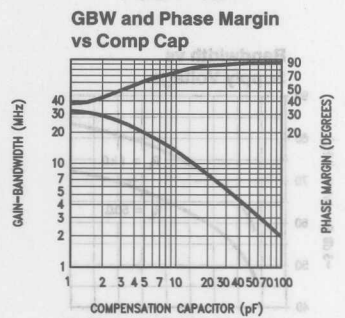
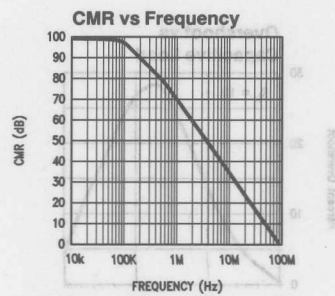
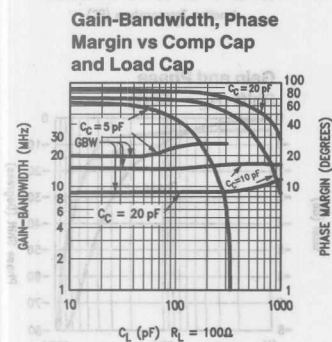
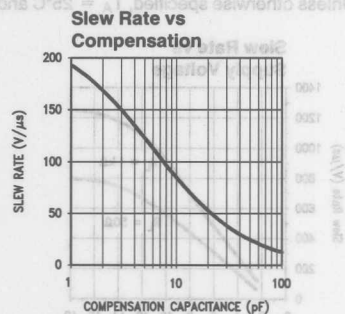
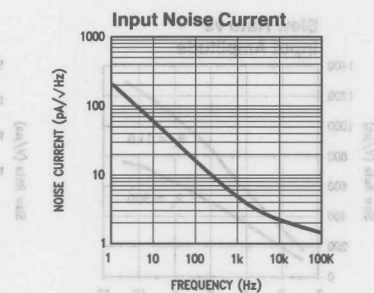
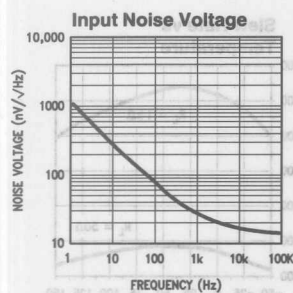
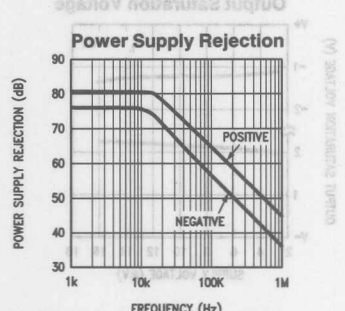
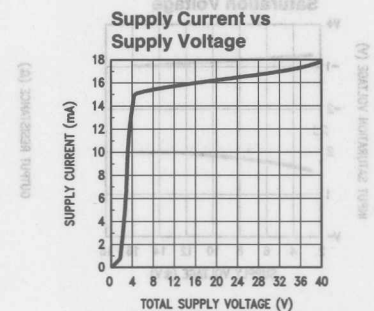
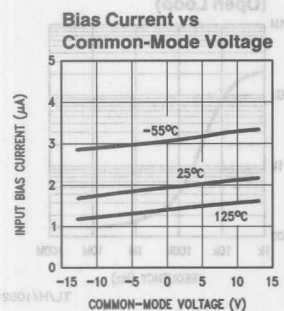
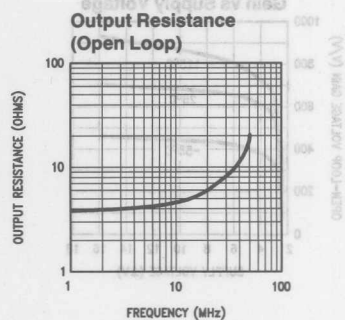
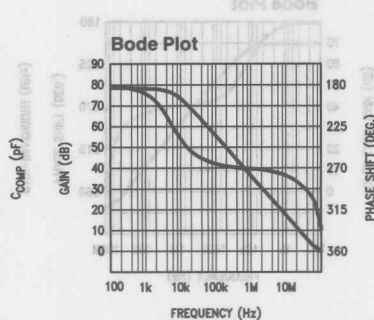
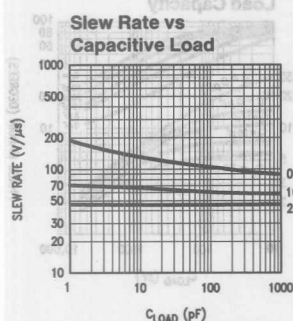


FIGURE 3

Typical Performance Characteristics Op Amp

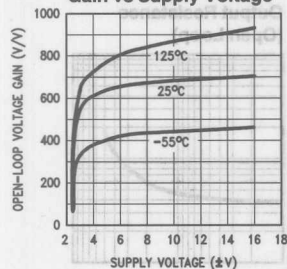
(Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{ k}\Omega$.)



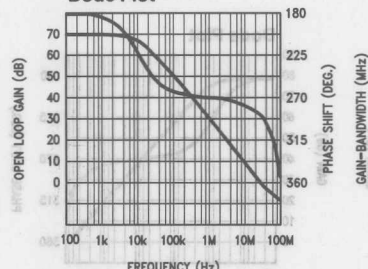
Typical Performance Characteristics A1 Only

(Unless otherwise specified, $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, and $R_L = 10\text{ k}\Omega$.)

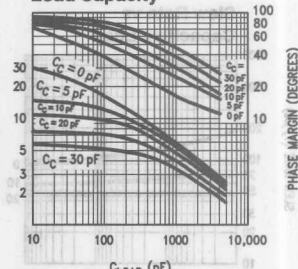
Gain vs Supply Voltage



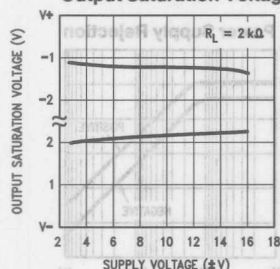
Bode Plot



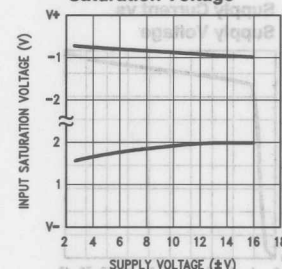
Gain-Bandwidth and Phase Margin vs Load Capacity



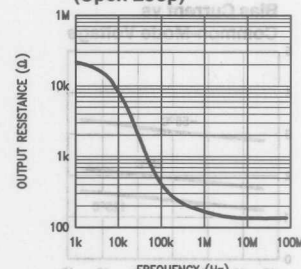
Output Saturation Voltage



Common-Mode Input Saturation Voltage



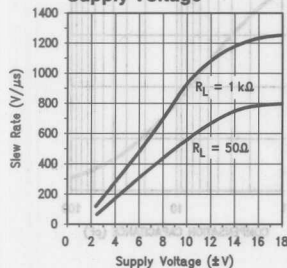
Output Resistance (Open Loop)



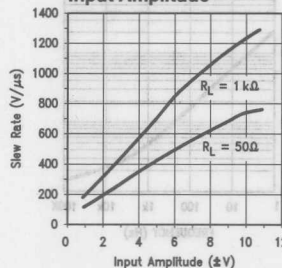
Typical Performance Characteristics A2 Only

(Unless otherwise specified, $T_A = 25^\circ\text{C}$ and $V_S = \pm 15\text{V}$.)

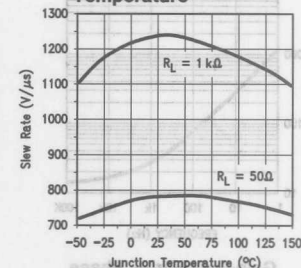
Slew Rate vs Supply Voltage



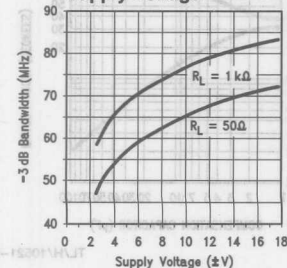
Slew Rate vs Input Amplitude



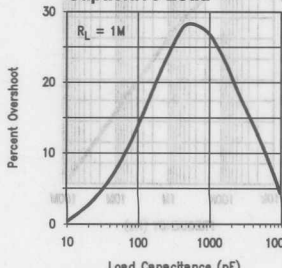
Slew Rate vs Temperature



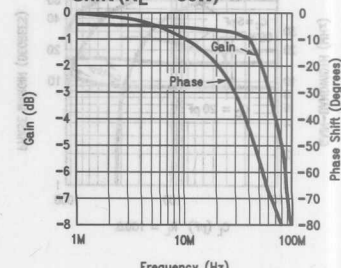
Bandwidth vs Supply Voltage



Overshoot vs Capacitive Load



Gain and Phase Shift ($R_L = 50\Omega$)



Application Hints

The LM6313 is a high-speed, high power operational amplifier that is designed for driving low-impedance loads such as 50 Ω and 75 Ω cables. Available in the standard, low cost, 16-pin DIP, this amplifier will drive back terminated video cables with up to 10 Vp-p. The ability to add additional compensation allows the LM6313 to drive capacitive loads of any size at bandwidths previously possible only with very expensive hybrid devices.

The LM6313 is excellent for driving high-speed flash A-to-D converters that require low-impedance drive at high frequencies. At 1 MHz, when used as a buffer, the LM6313 output impedance is below 0.1 Ω . This very low output impedance also means that cables can be accurately back-terminated by just placing the characteristic impedance in series with the LM6313 output.

OVER-VOLTAGE PROTECTION

If the LM6313 is being operated on supply voltages of greater than $\pm 5V$, the possibility of damaging the output stage transistors exists. At higher supply voltages, if the output is shorted or excessive power dissipation causes the output stage to shut down, the maximum A2 input-to-output voltage, can be exceeded. This occurs when the input stage tries to drive the output while the output is at ground. To prevent this from happening, an easy solution is to place diodes around the output stage (See Figure 4). This will limit the maximum differential voltage to about 1.3V. Any signal diode, such as the 1N914 or the 1N4148 will work fine.

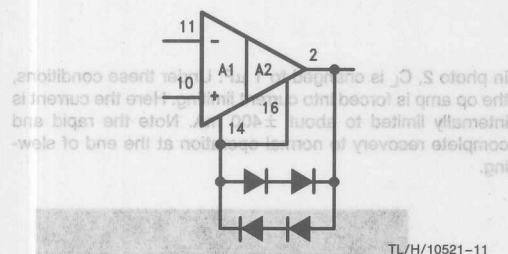


FIGURE 4

TL/H/10521-11

HEAT SINKING

When driving a low impedance load such as 50 Ω , and operating from $\pm 15V$ supplies, the internal power dissipation of the LM6313 can rise above 3W. To prevent overheating of the chip, which would cause the thermal protection circuitry to shut the system down, the following guidelines should be followed:

1. Reduce the supply voltage. The LM6313 will operate with little change in performance, except output voltage swing, on $\pm 5V$ supplies. This will reduce the dissipation to the level where no precautions against overheating are necessary for loads of 10 Ω or more.
2. Solder pins 4, 5, 12 and 13 to copper traces which are at least 0.100 inch wide and have a total area of at least 2 square inches, to obtain a θ_{JA} of 40°C/W. These four pins are connected to the back of the chip and will be at V_- . They should not be used as a V_- connection unless pin 3 is also connected to this same point.

SUPPLY BYPASSING

Because of the large currents required to drive low-impedance loads, supply bypassing as close as possible to the I.C. is important. At 50 MHz, a few inches of wire or circuit trace can have 20 Ω or 30 Ω of inductive reactance. This inductance in series with a 0.1 μF bypass capacitor can resonate at 1 MHz to 2 MHz and just appear as an inductor at higher frequencies. A 0.1 μF and a 10 μF to 15 μF capacitor connected in parallel and as close as possible to the LM6313 supply pins, from each supply to ground, will give best performance.

SELECTION OF COMPENSATION CAPACITOR

The compensation pin, pin 15, makes it possible to drive any load at any closed loop gain without stability problems. In most cases, where the gain is -1 or greater and the load is resistive, no compensation capacitor is required. When used at unity gain or when driving reactive loads, a small capacitor of 5 pF to 20 pF will insure optimum performance. The easiest way to determine the best value of compensation capacitor is to temporarily connect a trimmer capacitor (typical range of 2 pF to 15 pF) between pin 15, and ground, and adjust it for little or no overshoot at the output while driving the input with a square wave.

If the actual load capacitance is known, the typical graphs "Gain-Bandwidth and Phase Margin vs. Load Capacitance" can be used to select a value.

VIDEO CABLE DRIVER

The LM6313 is ideally suited for driving 50 Ω or 75 Ω cables. Unlike a buffer that requires a separate gain stage to make up for the losses involved in termination, the LM6313 gain can be set to 1 plus the line losses when the transmission line is end-terminated. If back-termination is needed, adding the line impedance in series with the output and raising the gain to 2 plus the expected line losses will provide a 0 dB loss system. Figure 5 illustrates the back and end terminated video system including compensation for line losses. The excellent stability of the LM6313 with changes in supply voltages allow running the amplifier on unregulated supplies. The typical change in phase shift when the supplies are changed from $\pm 5V$ to $\pm 15V$ is less than 3° at 10 MHz.

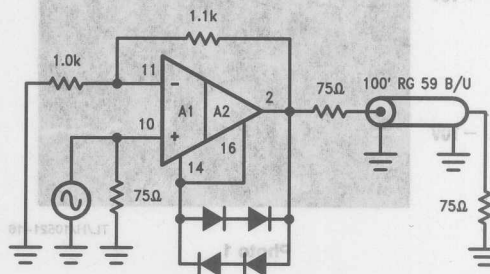


FIGURE 5

TL/H/10521-12

Application Hints (Continued)

LASER DIODE MODULATOR

Figure 6 is a minimum component count example of a video modulator for a CW laser diode. This example biases the diode at 200 mA and modulates the current at ± 200 mA per volt of signal. If it is desired to reduce power consumption and ± 5 V supplies are available, all that is necessary is to change R2 to 5 k Ω and R4 to 15 Ω .

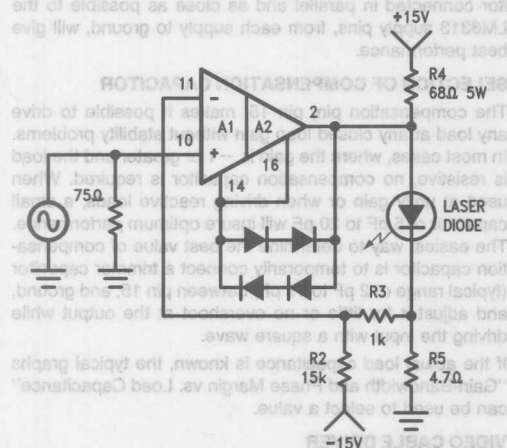


FIGURE 6

In photo 1, C_L is 1000 pF. The LM6313 is slewing at 250 V/ μ s, from -5 V to $+5$ V. The slew rate is 450 V/ μ s from $+5$ V to -5 V. This requires the op amp to deliver 450 mA into the load and remain stable.

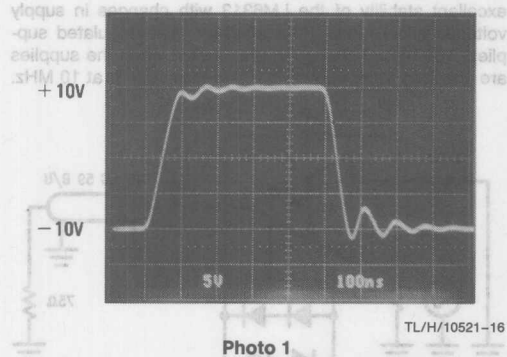


Photo 1

CAPACITIVE LOAD DRIVING

Figure 7 is the circuit used to demonstrate the ability of the LM6313 to drive capacitive loads at speeds not previously possible with monolithic op amps.

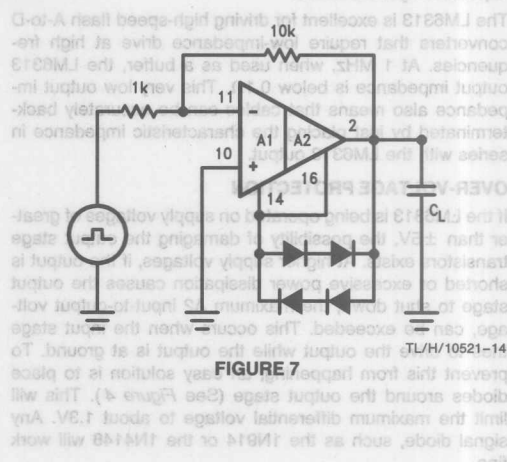


FIGURE 7

In photo 2, C_L is changed to 1 μ F. Under these conditions, the op amp is forced into current limiting. Here the current is internally limited to about ± 400 mA. Note the rapid and complete recovery to normal operation at the end of slewing.

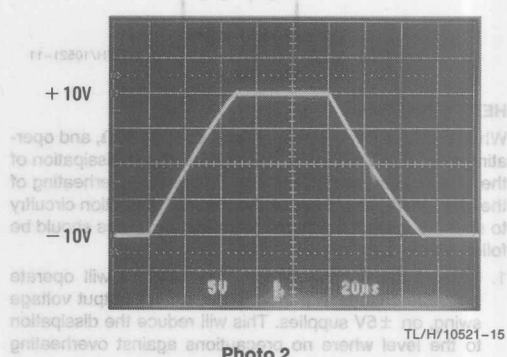


Photo 2

LM7121

Tiny Very High Speed Low Power Voltage Feedback Amplifier

General Description

The LM7121 is a high performance operational amplifier which addresses the increasing AC performance needs of video and imaging applications. Its tiny size and low power make it ideal for portable applications.

The LM7121 can operate over a wide dynamic range of supply voltages, from $\pm 15V$ to $\pm 5V$. It offers an excellent speed-power product delivering $1000V/\mu s$ and 200 MHz unity gain stability. Another key feature of this operational amplifier is stability while driving unlimited capacitive loads.

Due to its Tiny SOT23-5 package, the LM7121 is ideal for designs where space and weight are the critical parameters. The benefits of the tiny package are evident in small portable electronic devices, such as cameras, and PC video cards. Tiny amplifiers are so small that they can be placed anywhere on a board close to the signal source or near the input to an A/D converter.

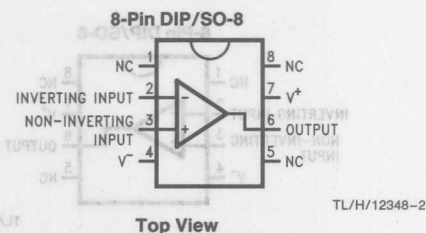
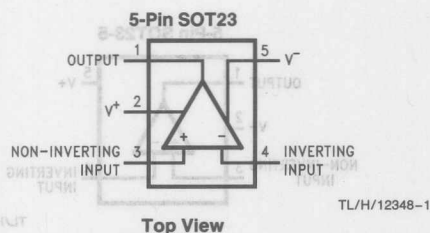
Features (Typical unless otherwise noted)

- Easy to use Voltage Feedback Topology
- Stable with unlimited capacitive loads
- Tiny SOT23-5 package—typical circuit layout takes half the space of SO-8 designs
- Unity Gain Frequency 200 MHz
- Slew Rate $1000V/\mu s$
- Characterized for Supply Voltages $\pm 5V$ and $\pm 15V$
- Low Supply Current 5 mA

Applications

- Scanners, Color Fax, Digital copier
- Portable Video Equipment
- Cable Drivers
- Digital Cameras
- ADC/DAC Buffers

Connection Diagram



Ordering Information

| Package | Temperature Range Industrial, $-40^{\circ}C$ to $+85^{\circ}C$ | NSC Drawing Number | Transport Media |
|---------------------|---|-----------------------|--------------------|
| 8-Pin Molded DIP | LM7121AIN, LM7121BIN | N08E | Rails |
| 8-Pin Small Outline | LM7121AIM, LM7121BIM | M08A | Rails |
| | LM7121AIMX, LM7121BIMX | | Tape and Reel |
| 5-Pin SOT 23-5 | LM7121AIM5, LM7121BIM5 | MA05A | Rails |
| | LM7121AIM5X, LM7121BIM5X | | Tape and Reel |

LM7131

Tiny High Speed Single Supply Operational Amplifier

General Description

The LM7131 is a high speed bipolar operational amplifier available in a tiny SOT23-5 package. This makes the LM7131 ideal for space and weight critical designs. Single supply voltages of 3V and 5V provides good video performance, wide bandwidth, low distortion, and high PSRR and CMRR. This makes the amplifier an excellent choice for desktop and portable video and computing applications. The amplifier is supplied in DIPs, surface mount 8-pin packages, and tiny SOT23-5 packages.

Tiny amplifiers are so small they can be placed anywhere on a board close to the signal source or next to an A-to-D input. Good high speed performance at low voltage makes the LM7131 a preferred part for battery powered designs.

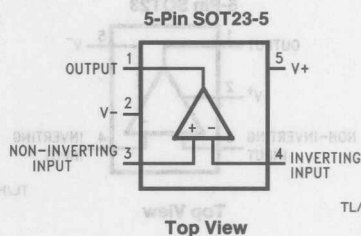
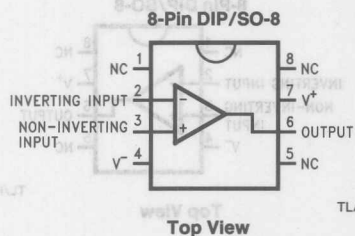
Features

- Tiny SOT23-5 package saves space-typical circuit layouts take half the space of SO-8 designs.
- Guaranteed specs at 3V, 5V, and $\pm 5V$ supplies
- Typical supply current 7.0 mA at 5V, 6.5 mA at 3V
- 4V output swing with +5V single supply
- Typical total harmonic distortion of 0.1% at 4 MHz
- 70 MHz Gain-Bandwidth Product
- 90 MHz -3 dB bandwidth at 3V and 5V, Gain = $+1$
- Designed to drive popular video A/D converters
- 40 mA output can drive 50Ω loads
- Differential gain and phase 0.25% and 0.75° at $A_V = +2$

Applications

- Driving video A/D converters
- Video output for portable computers and PDAs
- Desktop teleconferencing
- High fidelity digital audio
- Video cards

Connection Diagrams



| Package | Ordering Information | NSC Drawing Number | Package Marking | Supplied as |
|----------------|----------------------|--------------------|-----------------|----------------------------|
| 8-Pin DIP | LM7131ACN | N08E | LM7131ACN | rails |
| 8-Pin DIP | LM7131BCN | N08E | LM7131BCN | rails |
| 8-Pin SO-8 | LM7131ACM | M08A | LM7131ACM | rails |
| 8-Pin SO-8 | LM7131BCM | M08A | LM7131BCM | rails |
| 8-Pin SO-8 | LM7131ACMX | M08A | LM7131ACM | 2.5k units tape and reel |
| 8-Pin SO-8 | LM7131BCMX | M08A | LM7131BCM | 2.5k units tape and reel |
| 5-Pin SOT 23-5 | LM7131ACM5 | MA05A | A02A | 250 units on tape and reel |
| 5-Pin SOT 23-5 | LM7131BCM5 | MA05A | A02B | 250 units on tape and reel |
| 5-Pin SOT 23-5 | LM7131ACM5X | MA05A | A02A | 3k units tape and reel |
| 5-Pin SOT 23-5 | LM7131BCM5X | MA05A | A02B | 3k units tape and reel |

| | |
|--------------------------------|------------------------------|
| ESD Tolerance (Note 2) | 2000V |
| Differential Input Voltage | ± 2.0 |
| Voltage at Input/Output Pin | $(V^+) + 0.1V, (V^-) - 0.3V$ |
| Supply Voltage ($V^+ - V^-$) | 12V |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin (Note 3) | ± 80 mA |
| Current at Power Supply Pin | ± 80 mA |

Operating Ratings

| | |
|--------------------------------------|---------------------------------------|
| Supply Voltage ($V^+ - V^-$) | $2.7V \leq V \leq 12V$ |
| Junction Temperature Range | $0^\circ C \leq T_J \leq +70^\circ C$ |
| LM7131AC, LM7131BC | |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 115°C/W |
| SO-8 Package, 8-Pin Surface Mount | 165°C/W |
| M05A Package, 5-Pin Surface Mount | 325°C/W |

3V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|------------|--|---|-----------------|---|---|----------------------|
| V_{OS} | Input Offset Voltage | | 0.02 | 2 4 | 7 10 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 10 | | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | | 20 | 30 40 | 30 40 | μA max |
| I_{OS} | Input Offset Current | | 0.35 | 3.5 5 | 3.5 5 | μA max |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 0.85V$ (Video Levels) | 75 | 60 55 | 60 55 | dB min |
| CMRR | Common Mode Rejection Ratio | $0.85V \leq V_{CM} \leq 1.7V$ (Mid-Range) | 70 | 55 50 | 55 50 | dB min |
| + PSRR | Positive Power Supply Rejection Ratio | $V^+ = 3V, V^- = 0V$ $V^+ = 3V$ to 6.5V | 75 | 65 60 | 65 60 | dB min |
| - PSRR | Negative Power Supply Rejection Ratio | $V^- = -3V, V^+ = 0V$ $V^- = -3V$ to -6.5V | 75 | 65 60 | 65 60 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 3V$ For CMRR ≥ 50 dB | 0.0 2.0 | 0.0 0.00 1.70 1.60 | 0.0 0.00 1.70 1.60 | V min V max |
| A_{VOL} | Voltage Gain | $R_L = 150\Omega, V_O = 0.250V$ to 1.250V | 60 | 55 50 | 55 50 | dB |
| C_{IN} | Common-Mode Input Capacitance | | 2 | | | pF |

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes. (Continued)

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|----------|------------------------------|--|-----------------|-------------------------------|-------------------------------|-----------|
| V_O | Output Swing High | $V^+ = 3\text{V}$, $R_L = 150\Omega$ terminated at 0V | 2.6 | 2.3 2.0 | 2.3 2.0 | V min |
| | Low | $V^+ = 3\text{V}$, $R_L = 150\Omega$ terminated at 0V | 0.05 | 0.15 0.20 | 0.15 0.20 | V max |
| | High | $V^+ = 3\text{V}$, $R_L = 150\Omega$ terminated at 1.5V | 2.6 | 2.3 2.0 | 2.3 2.0 | V min |
| | Low | $V^+ = 3\text{V}$, $R_L = 150\Omega$ terminated at 1.5V | 0.5 | 0.8 1.0 | 0.8 1.0 | V max |
| V_O | Output Swing High | $V^+ = 3\text{V}$, $R_L = 600\Omega$ terminated at 0V | 2.73 | | | V max |
| V_O | Output Swing Low | $V^+ = 3\text{V}$, $R_L = 600\Omega$ terminated at 0V | 0.06 | | | V max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 65 | 45 40 | 45 40 | mA min |
| | | Sinking, $V_O = 3\text{V}$ | 40 | 25 20 | 25 20 | mA min |
| I_S | Supply Current | $V^+ = +3\text{V}$ | 6.5 | 8.0 8.5 | 8.0 8.5 | mA max |

3V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|--------|------------------------------|--|-----------------|-------------------------------|-------------------------------|------------------|
| T.H.D. | Total Harmonic Distortion | $F = 4\text{ MHz}$, $A_V = +2$ $R_L = 150\Omega$, $V_O = 1.0V_{PP}$ | 0.1 | | | % |
| | Differential Gain | (Note 10) | 0.45 | | | % |
| | Differential Phase | (Note 10) | 0.6 | | | ° |
| SR | Slew Rate | $R_L = 150\Omega$, $C_L = 5\text{ pF}$ (Note 7) | 120 | | | V/ μS |
| SR | Slew Rate | $R_L = 150\Omega$, $C_L = 20\text{ pF}$ (Note 7) | 100 | | | V/ μS |
| GBW | Gain-Bandwidth Product | | 70 | | | MHz |
| | Closed-Loop - 3 dB Bandwidth | | 90 | | | MHz |

5V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = V_O = V^+/2$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|--------------------------|--|---|-----------------|-------------------------------|-------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.02 | 2 4 | 7 10 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 10 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 20 | 30 40 | 30 40 | μA max |
| I_{OS} | Input Offset Current | | 0.35 | 3.5 5 | 3.5 5 | μA max |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 1.85\text{V}$ (Video Levels) | 75 | 65 60 | 65 60 | dB min |
| CMRR | Common Mode Rejection Ratio | $1.85\text{V} \leq V_{\text{CM}} \leq 3.7\text{V}$ (Mid-Range) | 70 | 55 50 | 55 50 | dB min |
| + PSRR | Positive Power Supply Rejection Ratio | $V^+ = 5\text{V}$, $V^- = 0\text{V}$ $V^+ = 5\text{V}$ to 10V | 75 | 65 60 | 65 60 | dB min |
| - PSRR | Negative Power Supply Rejection Ratio | $V^- = -5\text{V}$, $V^+ = 0\text{V}$ $V^- = -5\text{V}$ to -10V | 75 | 65 60 | 65 60 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ For CMRR $\geq 50\text{ dB}$ | 0.0 | - 0.0 0.00 | - 0.0 0.00 | V min |
| | | | 4.0 | 3.70 3.60 | 3.70 3.60 | V max |
| A_{VOL} | Voltage Gain | $R_L = 150\Omega$, $V_O = 0.250\text{V}$ to 2.250V | 70 | 60 55 | 60 55 | dB min |
| C_{IN} | Common-Mode Input Capacitance | | 2 | | | pF |
| V_O | Output Swing High | $V^+ = 5\text{V}$, $R_L = 150\Omega$ terminated at 0V | 4.5 | 4.3 4.0 | 4.3 4.0 | V min |
| | Low | $V^+ = 5\text{V}$, $R_L = 150\Omega$ terminated at 0V | 0.08 | 0.15 0.20 | 0.15 0.20 | V max |
| | High | $V^+ = 5\text{V}$, $R_L = 150\Omega$ terminated at 2.5V | 4.5 | 4.3 4.0 | 4.3 4.0 | V min |
| | Low | $V^+ = 5\text{V}$, $R_L = 150\Omega$ terminated at 2.5V | 0.5 | 0.8 1.0 | 0.8 1.0 | V max |
| V_O | Output Swing High | $V^+ = 5\text{V}$, $R_L = 600\Omega$ terminated at 0V | 4.70 | | | V max |
| V_O | Output Swing Low | $V^+ = 5\text{V}$, $R_L = 600\Omega$ terminated at 0V | 0.07 | | | V max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 65 | 45 40 | 45 40 | mA min |
| | | Sinking, $V_O = 5\text{V}$ | 40 | 25 20 | 25 20 | mA min |
| I_S | Supply Current | $V^+ = +5\text{V}$ | 7.0 | 8.5 9.0 | 8.5 9.0 | mA max |

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|--------|--|---|-----------------|-------------------------------|-------------------------------|------------------------|
| T.H.D. | Total Harmonic Distortion | $F = 4 \text{ MHz}$, $A_V = +2$ $R_L = 150\Omega$, $V_O = 2.0V_{PP}$ | 0.1 | | | % |
| | Differential Gain | (Note 10) | 0.25 | | | % |
| | Differential Phase | (Note 10) | 0.75 | | | ° |
| SR | Slew Rate | $R_L = 150\Omega$, $C_L = 5 \text{ pF}$ (Note 8) | 150 | | | $V/\mu s$ |
| SR | Slew Rate | $R_L = 150\Omega$, $C_L = 20 \text{ pF}$ (Note 8) | 130 | | | $V/\mu s$ |
| GBW | Gain-Bandwidth Product | | 70 | | | MHz |
| | Closed-Loop -3 dB Bandwidth | | 90 | | | MHz |
| e_n | Input-Referred Voltage Noise | $f = 1 \text{ kHz}$ | 11 | | | $\frac{nV}{\sqrt{Hz}}$ |
| i_n | Input-Referred Current Noise | $f = 1 \text{ kHz}$ | 3.3 | | | $\frac{pA}{\sqrt{Hz}}$ |

$\pm 5V$ DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$, $V^+ = 5V$, $V^- = 5V$, $V_{CM} = V_O = 0V$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|------------|--|---|-----------------|--|--|----------------------|
| V_{OS} | Input Offset Voltage | | 0.02 | 2 4 | 7 10 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 10 | | | $\mu V/^\circ C$ |
| I_B | Input Bias Current | | 20 | 30 40 | 30 40 | μA max |
| I_{OS} | Input Offset Current | | 0.35 | 3.5 5 | 3.5 5 | μA max |
| CMRR | Common Mode Rejection Ratio | $-5V \leq V_{CM} \leq 3.7V$ | 75 | 65 60 | 65 60 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+ = 5V$, $V^- = 0V$ $V^+ = 5V$ to $10V$ | 75 | 65 60 | 65 60 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $V^- = -5V$, $V^+ = 0V$ $V^- = -5V$ to $-10V$ | 75 | 65 60 | 65 60 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5V$, $V^- = -5V$ For CMRR $\geq 60 \text{ dB}$ | -5.0 4.0 | -5.0 -5.0 3.70 3.60 | -5.0 -5.0 3.70 3.60 | V min V max |
| A_{VOL} | Voltage Gain | $R_L = 150\Omega$, $V_O = -2.0$ to $+2.0$ | 70 | 55 50 | 55 50 | dB |

± 5V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 5\text{V}$, $V_{CM} = V_O = 0\text{V}$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes. (Continued)

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|----------|----------------------------------|---|-----------------|-------------------------------|-------------------------------|-----------|
| C_{IN} | Common-Mode Input Capacitance | | 2 | | | pF |
| V_O | Output Swing High | $V^+ = 5\text{V}$, $V^- = -5\text{V}$ $R_L = 150\Omega$ terminated at 0V | 4.5 | 4.3 4.0 | 4.3 4.0 | V min |
| | Low | | -4.5 | -3.5 -2.5 | -3.5 -2.5 | V max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = -5\text{V}$ | 65 | 45 40 | 45 40 | mA min |
| | | Sinking, $V_O = 5\text{V}$ | 40 | 25 20 | 25 20 | mA min |
| I_S | Supply Current | $V^+ = +5\text{V}$, $V^- = -5\text{V}$ | 7.5 | 9 10 | 9 10 | mA max |

± 5V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 5\text{V}$, $V_{CM} = V_O = 0\text{V}$ and $R_L = 150\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LM7131AC Limit (Note 6) | LM7131BC Limit (Note 6) | Units |
|--------|--------------------------------|--|-----------------|-------------------------------|-------------------------------|------------------|
| T.H.D. | Total Harmonic Distortion | $F = 4\text{ MHz}$, $A_V = -2$ $R_L = 150\Omega$, $V_O = 4.0V_{PP}$ | 1.5 | | | % |
| | Differential Gain | (Note 10) | 0.25 | | | % |
| | Differential Phase | (Note 10) | 1.0 | | | ° |
| SR | Slew Rate | $R_L = 150\Omega$, $C_L = 5\text{ pF}$ (Note 9) | 150 | | | V/ μs |
| SR | Slew Rate | $R_L = 150\Omega$, $C_L = 20\text{ pF}$ (Note 9) | 130 | | | V/ μs |
| GBW | Gain-Bandwidth Product | | 70 | | | MHz |
| | Closed-Loop -3 dB Bandwidth | | 90 | | | MHz |

Note 1: Absolute maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: Connected as voltage follower with 1.5V step input. Number specified is the slower of the positive and negative slew rates. $V^+ = 3\text{V}$ and $R_L = 150\Omega$ connected to 1.5V. Amp excited with 1 kHz to produce $V_O = 1.5 V_{PP}$.

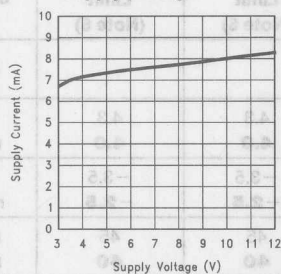
Note 8: Connected as Voltage Follower with 4.0V step input. Number specified is the slower of the positive and negative slew rates. $V^+ = 5\text{V}$ and $R_L = 150\Omega$ connected to 2.5V. Amp excited with 1 kHz to produce $V_O = 4 V_{PP}$.

Note 9: Connected as Voltage Follower with 4.0V step input. Number specified is the slower of the positive and negative slew rates. $V^+ = 5\text{V}$, $V^- = -5\text{V}$ and $R_L = 150\Omega$ connected to 0V. Amp excited with 1 kHz to produce $V_O = 4 V_{PP}$.

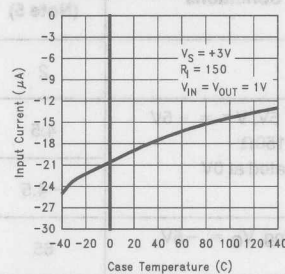
Note 10: Differential gain and phase measured with a 4.5 MHz signal into a 150 Ω load, Gain = +2.0, between 0.6V and 2.0V output.

Typical Performance Characteristics

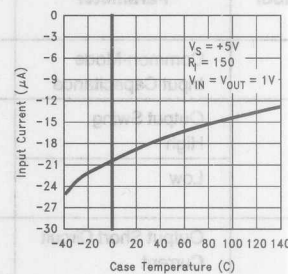
LM7131 Supply Current vs Supply Voltage



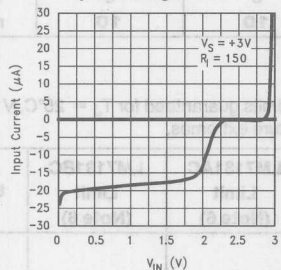
LM7131 Input Current vs Temperature @ 3V



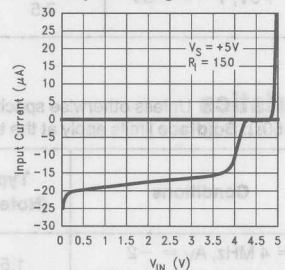
LM7131 Input Current vs Temperature @ 5V



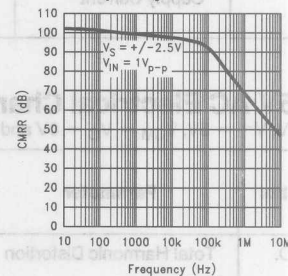
LM7131 Input Current vs Input Voltage @ 3V



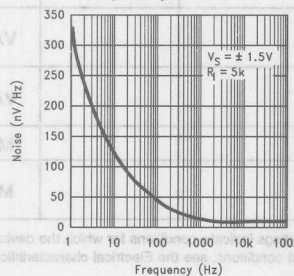
LM7131 Input Current vs Input Voltage @ 5V



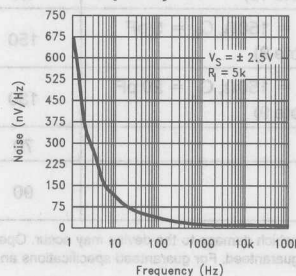
LM7131 CMRR vs Frequency @ 5V



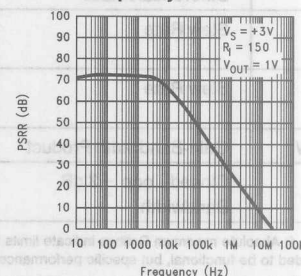
LM7131 Voltage Noise vs Frequency @ 3V



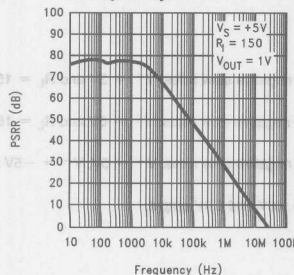
LM7131 Voltage Noise vs Frequency @ 5V



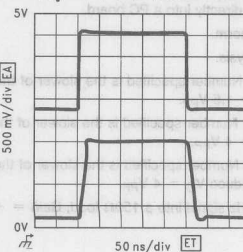
LM7131 PSRR vs Frequency @ 3V



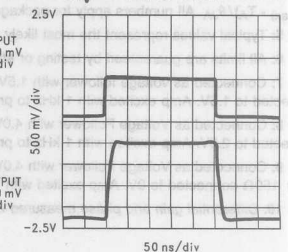
LM7131 PSRR vs Frequency @ 5V



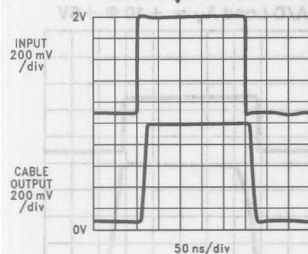
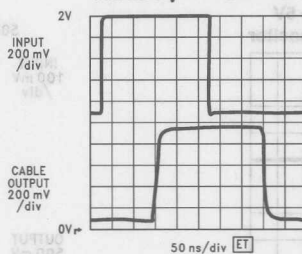
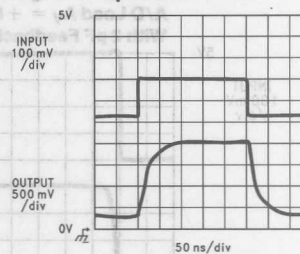
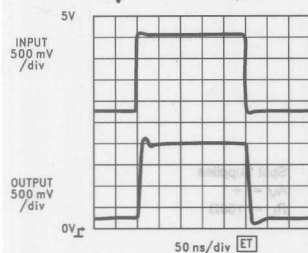
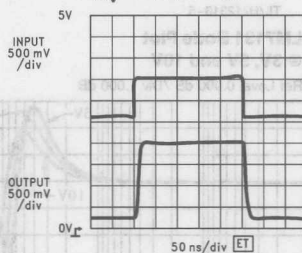
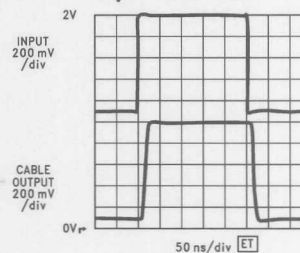
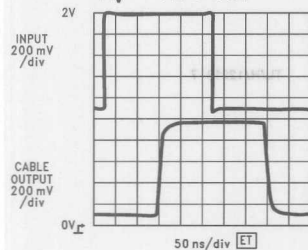
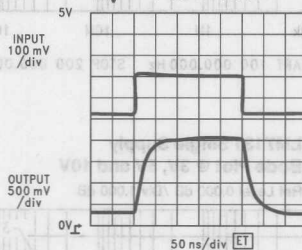
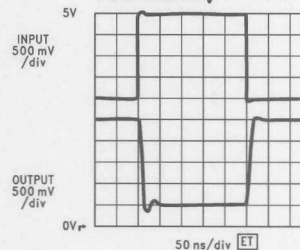
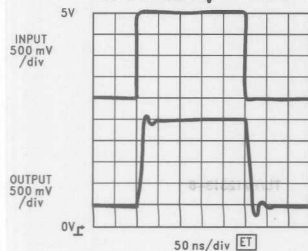
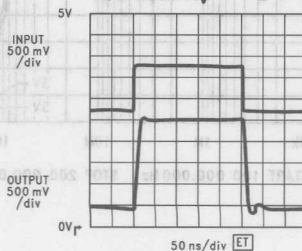
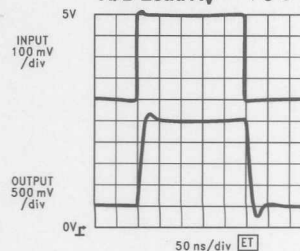
LM7131 Cable Driver A_y = +1 @ +3V



LM7131 Cable Driver A_y = +2 @ +3V



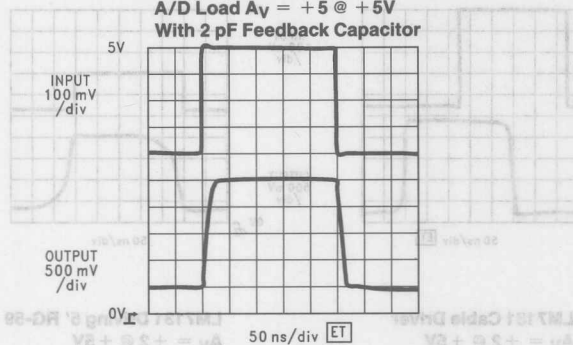
Typical Performance Characteristics (Continued)

LM7131 Driving 5'
RG-59 $A_V = +2 @ +3V$ LM7131 Driving 75'
RG-59 $A_V = +2 @ +3V$ LM7131 Cable Driver
 $A_V = +10 @ +3V$ LM7131 Cable Driver
 $A_V = +1 @ +5V$ LM7131 Cable Driver
 $A_V = +2 @ +5V$ LM7131 Driving 5' RG-59
 $A_V = +2 @ +5V$ LM7131 Driving 75' RG-59
 $A_V = +2 @ +5V$ LM7131 Cable Driver
 $A_V = +10 @ +5V$ LM7131 Driving Flash
A/D Load $A_V = -1 @ +5V$ LM7131 Driving Flash
A/D Load $A_V = +1 @ +5V$ LM7131 Driving Flash
A/D Load $A_V = +2 @ +5V$ LM7131 Driving Flash
A/D Load $A_V = +5 @ +5V$ 

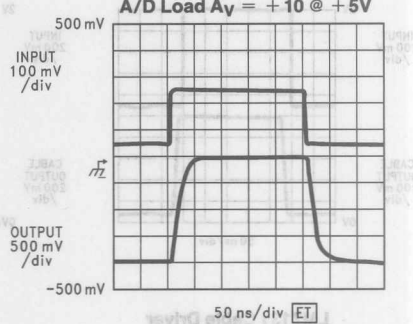
TL/H/12313-4

Typical Performance Characteristics (Continued)

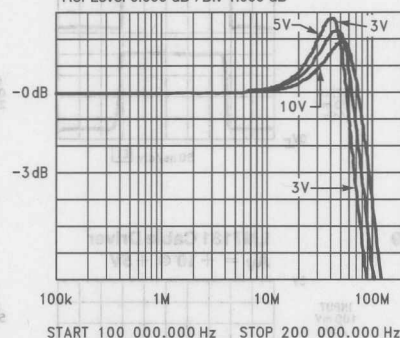
LM7131 Driving Flash
A/D Load $A_V = +5 @ +5V$
With 2 pF Feedback Capacitor



LM7131 Driving Flash
A/D Load $A_V = +10 @ +5V$

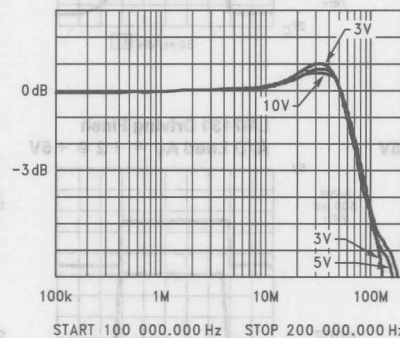


LM7131 Bode Plot
@ 3V, 5V and 10V
 Ref Level 0.000 dB / Div 1.000 dB



Split Supplies
 $A_V = +1$
 $R_L = 150\Omega$

LM7131 Single Supply
Bode Plot @ 3V, 5V and 10V
 Ref Level 0.000 dB / Div 1.000 dB



Single Supplies
 $A_V = +1$
 $R_L = 150\Omega$

Application Information

GENERAL INFORMATION

The LM7131 is a high speed complementary bipolar amplifier which provides high performance at single supply voltages. The LM7131 will operate at $\pm 5V$ split supplies, $+5V$ single supplies, and $+3V$ single supplies. It can provide improved performance for $\pm 5V$ designs with an easy transition to $+5V$ single supply. The LM7131 is a voltage feedback amplifier which can be used in most operational amplifier circuits.

The LM7131 is available in three package types: DIPs for through hole designs, SO-8 surface mount packages and the SOT23-5 Tiny package for space and weight savings.

The LM7131 has been designed to meet some of the most demanding requirements for single supply amplifiers—driving analog to digital converters and video cable driving. The output stage of the LM7131 has been specially designed for the dynamic load presented by analog to digital converters. The LM7131 is capable of a 4V output range with a $+5V$ single supply. The LM7131's drive capability and good differential gain and phase make quality video possible from a small package with only a $+5V$ supply.

BENEFITS OF THE LM7131

The LM7131 can make it possible to amplify high speed signals with a single $+5V$ or $+3V$ supply, saving the cost of split power supplies.

EASY DESIGN PATH FROM $\pm 5V$ to $+5V$ SYSTEMS

The DIP and SO-8 packages and similar $\pm 5V$ and single supply specifications means the LM7131 may be able to replace many more expensive or slower op amps, and then be used for an easy transition to $5V$ single supply systems. This could provide a migration path to lower voltages for the amplifiers in system designs, reducing the effort and expense of testing and re-qualifying different op amps for each new design.

In addition to providing a design migration path, the three packages types have other advantages.

The DIPs can be used for easy prototyping and through hole boards. The SO-8 for surface mount board designs, and using the SOT23-5 for a smaller surface mount package can save valuable board space.

SPECIFIC ADVANTAGES OF SOT23-5 (TINY PACKAGE)

The SOT23-5 (Tiny) package can save board space and allow tighter layouts. The low profile can help height limited designs, such as sub-notebook computers, consumer video equipment, personal digital assistants, and some of the thicker PCMCIA cards. The small size can improve signal integrity in noisy environments by placing the amplifier closer to the signal source. The tiny amp can fit into tight spaces and weighs little. This makes it possible to design the LM7131 into places where amplifiers could not previously fit.

The LM7131 can be used to drive coils and transformers referenced to virtual ground, such as magnetic tape heads

and disk drive write heads. The small size of the SOT23-5 package can allow it to be placed with a pre-amp inside of some rotating helical scan video head (VCR) assemblies. This avoids long cable runs for low level video signals, and can result in higher signal fidelity.

Additional space savings parts are available in tiny packages from National Semiconductor, including low power amplifiers, precision voltage references, and voltage regulators.

Notes on Performance Curves and Datasheet Limits

Important:

Performance curves represent an average of parts, and are not limits.

SUPPLY CURRENT vs SUPPLY VOLTAGE

Note that this curve is nearly straight, and rises slowly as the supply voltage increases.

INPUT CURRENT vs INPUT VOLTAGE

This curve is relatively flat in the 200 mV to 4V input range, where the LM7131 also has good common mode rejection.

COMMON MODE VOLTAGE REJECTION

Note that there are two parts to the CMRR specification of the datasheet for 3V and 5V. The common mode rejection ratio of the LM7131 has been maximized for signals near ground (typical of the active part of video signals, such as those which meet the RS-170 levels). This can help provide rejection of unwanted noise pick-up by cables when a balanced input is used with good input resistor matching. The mid-level CMRR is similar to that of other single supply op amps.

BODE PLOTS (GAIN vs FREQUENCY FOR $A_V = +1$)

The gain vs. frequency plots for a non-inverting gain of 1 show the three voltages with the 150 Ω load connected in two ways. For the single supply graphs, the load is connected to the most negative rail, which is ground. For the split supply graphs, the load is connected to a voltage halfway between the two supply rails.

DRIVING CABLES

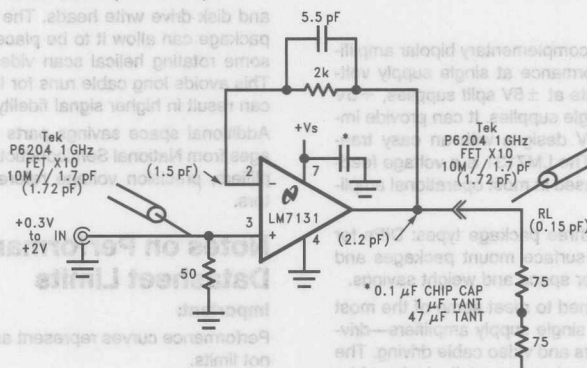
Pulse response curves for driving 75 Ω back terminate cables are shown for both 3V and 5V supplies. Note the good pulse fidelity with straight 150 loads, five foot (1.5 meter) and 75 foot (22 meter) cable runs. The bandwidth is reduced when used in a gain of ten ($A_V = +10$). Even in a gain of ten configuration, the output settles to $< 1\%$ in about 100 ns, making this useful for amplifying small signals at a sensor or signal source and driving a cable to the main electronics section which may be located away from the signal source. This will reduce noise pickup.

Please refer to *Figures 1-5* for schematics of test setups for cable driving.

Application Information (Continued)

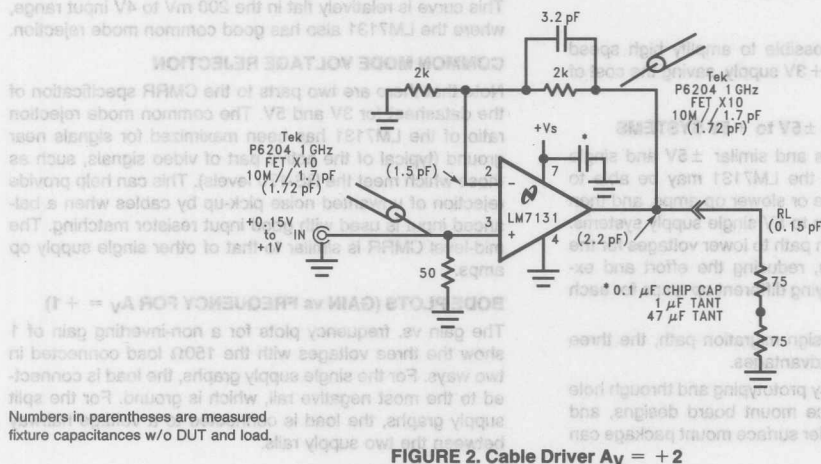
Numbers in parentheses are measured fixture capacitances w/o DUT and load

FIGURE 1. Cable Driver $A_V = +1$



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FIGURE 2. Cable Driver $A_V = +2$

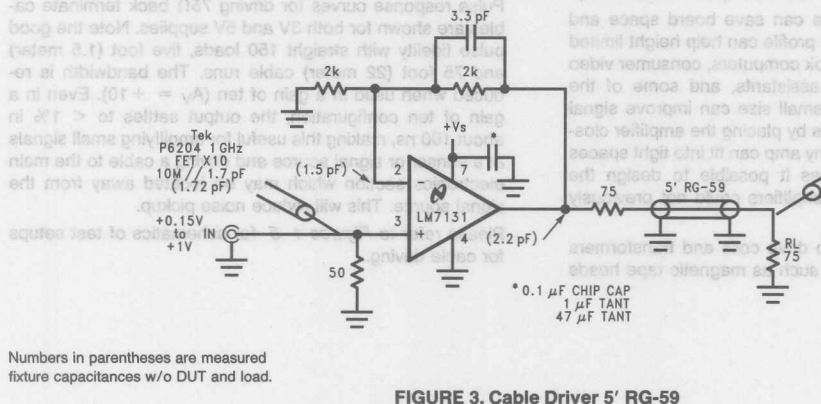


TI/H/12313-10

Numbers in parentheses are measured fixture capacitances w/o DUT and load

Numbers in parentheses are measured fixture capacitances w/o DUT and load

FIGURE 3. Cable Driver 5' RG-59



TL/H/12313-11

Application Information (Continued)

DRIVING TYPE 1175 FLASH A/D LOADS

The circuits in *Figures 6–11* show a LM7131 in a voltage follower configuration driving the passive equivalent of a typical flash A/D input. Note that there is a slight ringing on the output, which can affect accurate analog-to-digital conversion. In these graphs, we have adjusted the ringing to be a little larger than desirable in order to better show the settling time. Most settling times at low gain are about 75 ns to < 1% of final voltage. The ringing can be reduced by adding a low value (approximately 500Ω) feedback resistor from the output to the inverting input and placing a small (picofar-

ad range) capacitor across the feedback resistor. See *Figures 9 and 10* for schematics and respective performance curves for flash A/D driving at $A_V = +5$ with and without a 2 pF feedback capacitor.

See section on feedback compensation. Ringing can also be reduced by placing an isolation resistor between the output and the analog-to-digital converter input—see sections on driving capacitive loads and analog-to-digital converters.

Please refer to *Figures 6–11* for schematics of test setups for driving flash A/D converters.

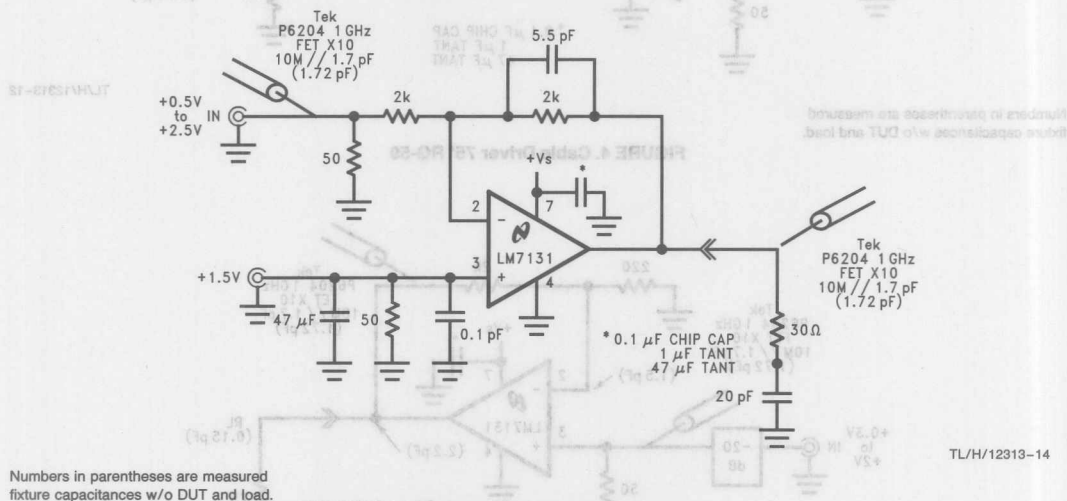


FIGURE 6. Flash A/D $A_V = -1$

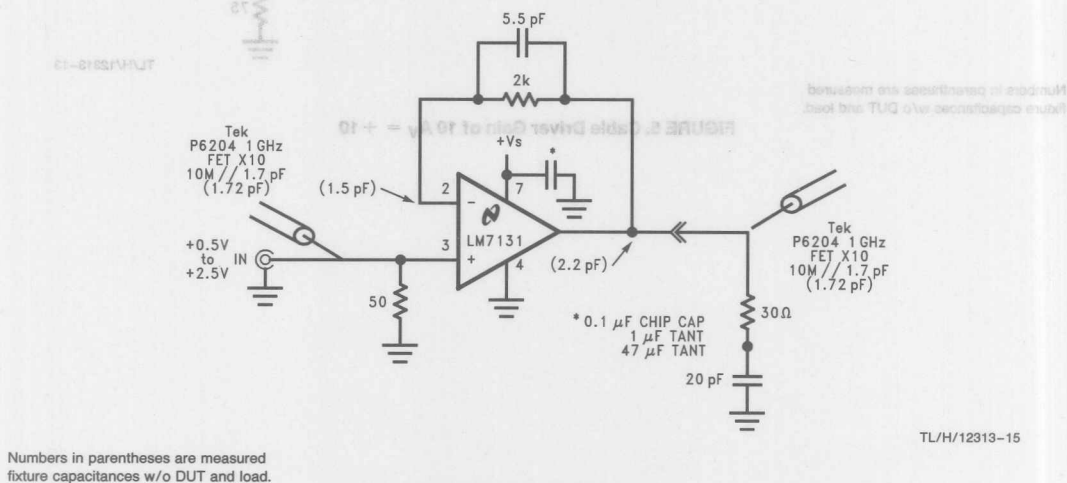
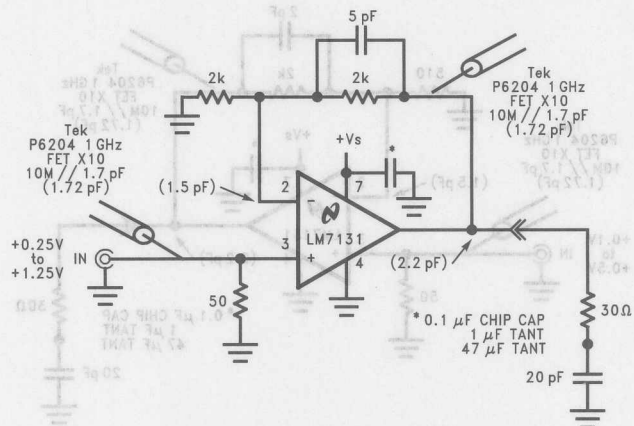


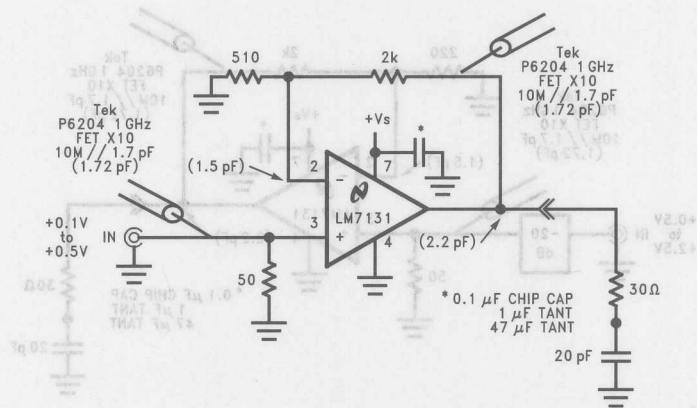
FIGURE 7. Flash A/D $A_V = +1$

Application Information (Continued)



TL/H/12313-16

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

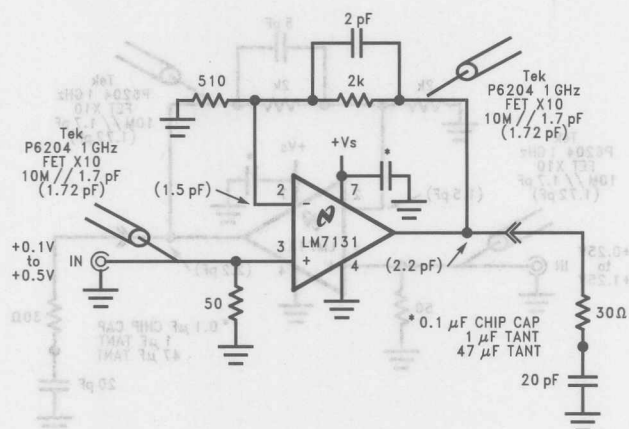
FIGURE 8. Flash A/D $A_v = +2$ 

TL/H/12313-17

Numbers in parentheses are measured fixture capacitances w/o DUT and load.

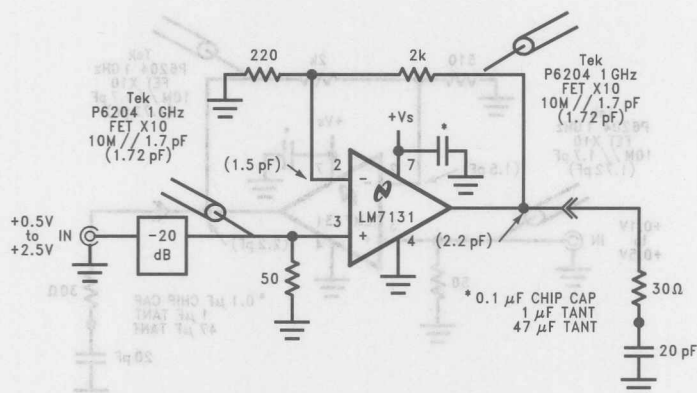
FIGURE 9. Flash A/D $A_v = +5$

Application Information (Continued)



TL/H/12313-18

Numbers in parentheses are measured
fixture capacitances w/o DUT and load.

FIGURE 10. Flash A/D $A_v = +5$ with Feedback Capacitor

TL/H/12313-19

Numbers in parentheses are measured
fixture capacitances w/o DUT and load.

FIGURE 11. Flash A/D $A_v = +10$

Using the LM7131

LIMITS AND PRECAUTIONS

Supply Voltage

The absolute maximum supply voltage which may be applied to the LM7131 is 12V. Designers should not design for more than 10V nominal, and carefully check supply tolerances under all conditions so that the voltages do not exceed the maximum.

Differential Input Voltage

Differential input voltage is the difference in voltage between the non-inverting (+) input and the inverting input (-) of the op amp. The absolute maximum differential input voltage is $\pm 2V$ across the inputs. This limit also applies when there is no power supplied to the op amp. This may not be a problem in most conventional op amp designs, however, designers should avoid using the LM7131 as comparator or forcing the inputs to different voltages. In some designs, diode protection may be needed between the inputs. See Figure 12.

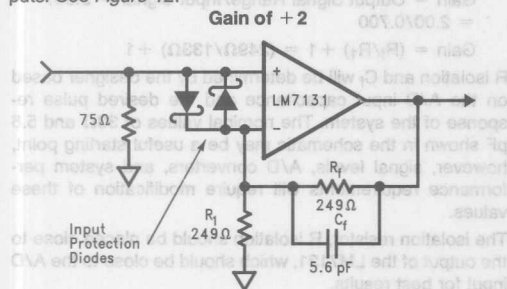


FIGURE 12

Output Short Circuits

The LM7131 has output short circuit protection, however, it is not designed to withstand continuous short circuits, very fast high energy transient voltage or current spikes, or shorts to any voltage beyond the power supply rails. Designs should reduce the number and energy level of any possible output shorts, especially when used with $\pm 5V$ supplies.

A resistor in series with the output, such as the 75Ω resistor used to back terminate 75Ω cables, will reduce the effects of shorts. For outputs which will send signals off the PC board additional protection devices, such as diodes to the power rails, zener-type surge suppressors, and varistors may be useful.

Thermal Management

Note that the SOT23-5 (Tiny) package has less power dissipation capability ($325^{\circ}/W$) than the S0-8 and DIP packages ($115^{\circ}/W$). This may cause overheating with $\pm 5V$ supplies and heavy loads at high ambient temps. This is less of a problem when using $+5V$ single supplies.

Example:

Driving a 150Ω load to 2.0V at a 40°C (104 °F) ambient temperature. (This is common external maximum temperature for office environments. Temperatures inside equipment may be higher.)

No load power-

No load LM7131 supply current - 9.0 mA

Supply voltage is 5.0V

No load LM7131 power - 9.0 mA x 5.0V = 45 mW

Power with load-

Current out is 2.0V/150 Ω = 13.33 mA

Voltage drop in LM7131 is 5.0V (supply) - 2.0V

(output) = 3.0V

Power dissipation 13.33 mA x 3.0V = 40 mW

Total Power = 45 mW + 40 mW = 85 mW =

0.085

Temperature Rise = 0.085 W x $325^{\circ}/W$ = 27.625 degrees

Junction temperature at 40° ambient = 40 + 27.625 = 67.625°.

This device is within the 0° to 70° specification limits.

The $325^{\circ}/W$ value is based on still air and the pc board land pattern shown in this datasheet. Actual power dissipation is sensitive to PC board connections and airflow.

SOT23-5 power dissipation may be increased by airflow or by increasing the metal connected to the pads, especially the center pin (pin number 2, V-) on the left side of the SOT23-5. This pin forms the mounting paddle for the die inside the SOT23-5, and can be used to conduct heat away from the die. The land pad for pin 2 can be made larger and/or connected to power planes in a multilayer board.

Additionally, it should be noted that difficulty in meeting performance specifications for the LM7131 is most common at cold temperatures. While excessively high junction temperatures will degrade LM7131 performance, testing has confirmed that most specifications are met at a junction temperature of 85°C.

See "Understanding Integrated Circuit Package Power Capabilities", Application Note AN-336, which may be found in the appendix of the Operational Amplifier Databook.

Layout and Power Supply Bypassing

Since the LM7131 is a high speed (over 50 MHz) device, good high speed circuit layout practices should be followed. This should include the use of ground planes, adequate power supply bypassing, removing metal from around the input pins to reduce capacitance, and careful routing of the output signal lines to keep them away from the input pins.

The power supply pins should be bypassed on both the negative and positive supply inputs with capacitors placed close to the pins. Surface mount capacitors should be used for best performance, and should be placed as close to the pins as possible. It is generally advisable to use two capacitors at each supply voltage pin. A small surface mount capacitor with a value of around 0.01 microfarad (10 nF), usually a ceramic type with good RF performance, should be placed closest to the pin. A larger capacitor, in usually in the range of 1.0 μF to 4.7 μF, should also be placed near the pin. The larger capacitor should be a device with good RF characteristics and low ESR (equivalent series resistance) for best results. Ceramic and tantalum capacitors generally work well as the larger capacitor.

For single supply operation, if continuous low impedance ground planes are available, it may be possible to use bypass capacitors between the +5V supply and ground only, and reduce or eliminate the bypass capacitors on the V- pin.

Using the LM7131 (Continued)

Capacitive Load Driving

The phase margin of the LM7131 is reduced by driving large capacitive loads. This can result in ringing and slower settling of pulse signals. This ringing can be reduced by placing a small value resistor (typically in the range of 22Ω – 100Ω) between the LM7131 output and the load. This resistor should be placed as close as practical to the LM7131 output. When driving cables, a resistor with the same value as the characteristic impedance of the cable may be used to isolate the cable capacitance from the output. This resistor will reduce reflections on the cable.

Input Current

The LM7131 has typical input bias currents in the $15\ \mu\text{A}$ to $25\ \mu\text{A}$ range. This will not present a problem with the low input impedances frequently used in high frequency and video circuits. For a typical 75Ω input termination, $20\ \mu\text{A}$ of input current will produce a voltage across the termination resistor of only $1.5\ \text{mV}$. An input impedance of $10\ \text{k}\Omega$, however, would produce a voltage of $200\ \text{mV}$, which may be large compared to the signal of interest. Using lower input impedances is recommended to reduce this error source.

Feedback Resistor Values and Feedback Compensation

Using large values of feedback resistances (roughly $2\text{k}\Omega$) with low gains (such gains of 2) will result in degraded pulse response and ringing. The large resistance will form a pole with the input capacitance of the inverting input, delaying feedback to the amplifier. This will produce overshoot and ringing. To avoid this, the gain setting resistors should be scaled to lower values (below $1\text{k}\Omega$). At higher gains (> 5) larger values of feedback resistors can be used.

Overshoot and ringing of the LM7131 can be reduced by adding a small compensation capacitor across the feedback resistor. For the LM7131 values in pF to tens of pF range are useful initial values. Too large a value will reduce the circuit bandwidth and degrade pulse response.

Since the small stray capacitance from the circuit layout, other components, and specific circuit bandwidth requirements will vary, it is often useful to select final values based on prototypes which are similar in layout to the production circuit boards.

Reflections

The output slew rate of the LM7131 is fast enough to produce reflected signals in many cables and long circuit traces. For best pulse performance, it may be necessary to terminate cables and long circuit traces with their characteristic impedance to reduce reflected signals.

Reflections should not be confused with overshoot. Reflections will depend on cable length, while overshoot will depend on load and feedback resistance and capacitance. When determining the type of problem, often removing or drastically shortening the cable will reduce or eliminate reflections. Overshoot can exist without a cable attached to the op amp output.

Driving Flash A/D Converters (Video Converters)

The LM7131 has been optimized to drive flash analog to digital converters in a $+5\text{V}$ only system. Different flash A/D converters have different voltage input ranges. The LM7131 has enough gain-bandwidth product to amplify standard video level signals to voltages which match the optimum input range of many types of A/D converters.

For example, the popular 1175 type 8-bit flash A/D converter has a preferred input range from 0.6V to 2.6V . If the input signal has an active video range (excluding sync levels) of approximately $700\ \text{mV}$, a circuit like the one in Figure 13 can be used to amplify and drive an A/D. The $10\ \mu\text{F}$ capacitor blocks the DC components, and allows the $+$ input of the LM7131 to be biased through R clamp so that the minimum output is equal to V_{RB} of the A/D converter. The gain of the circuit is determined as follows:

$$\text{Output Signal Range} = 2.6\text{V (V top)} - 0.6\text{V (V bot- tom)} = 2.0\text{V}$$

$$\text{Gain} = \text{Output Signal Range/Input Signal} = 2.857 = 2.00/0.700$$

$$\text{Gain} = (R_f/R_1) + 1 = (249\Omega/133\Omega) + 1$$

R isolation and C_f will be determined by the designer based on the A/D input capacitance and the desired pulse response of the system. The nominal values of 33Ω and $5.6\ \text{pF}$ shown in the schematic may be a useful starting point, however, signal levels, A/D converters, and system performance requirements will require modification of these values.

The isolation resistor, R isolation should be placed close to the output of the LM7131, which should be close to the A/D input for best results.

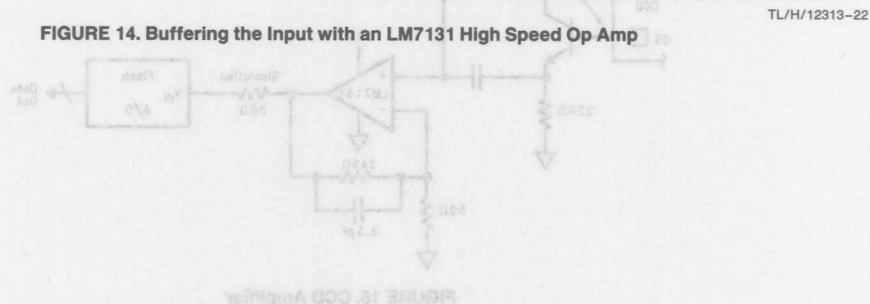
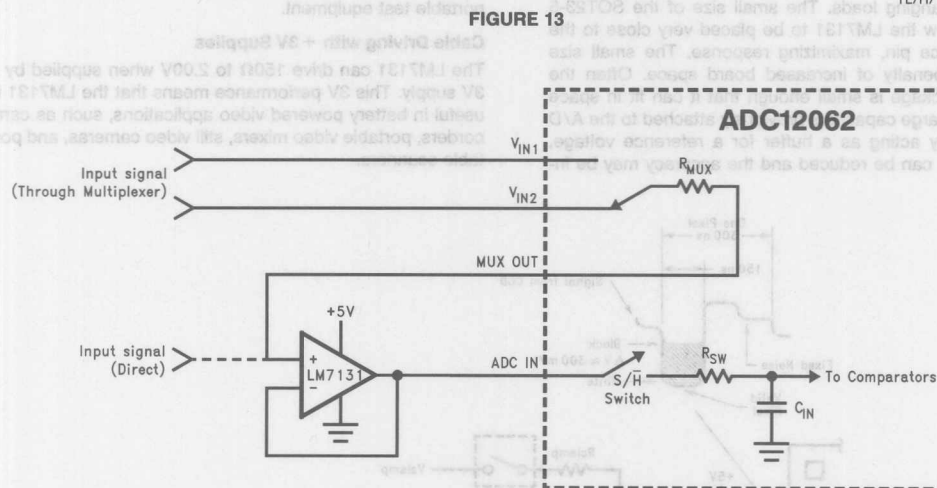
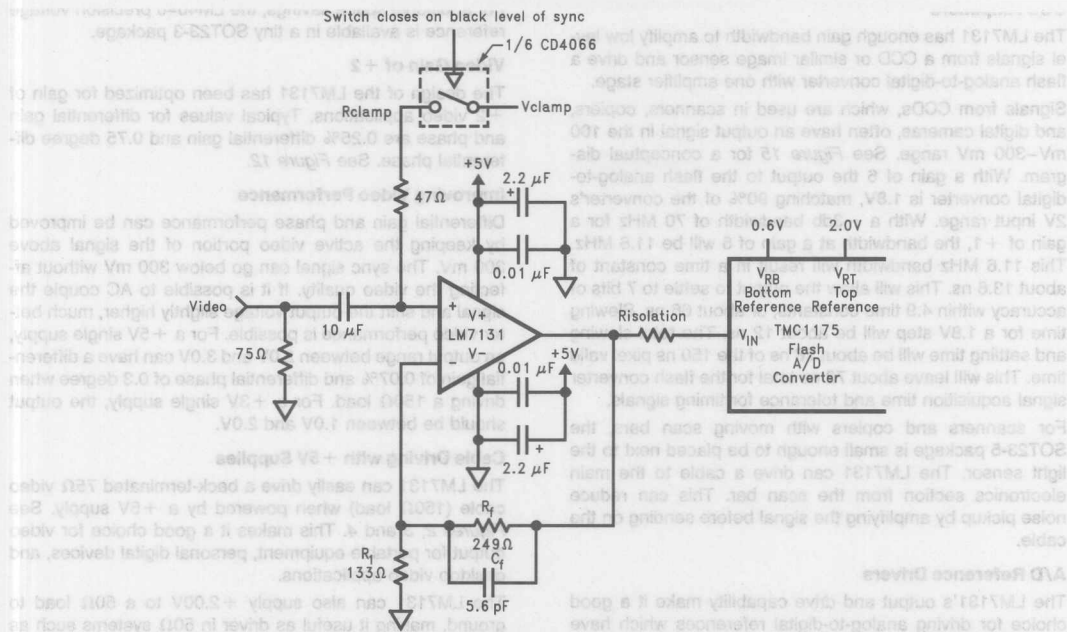
R clamp is connected to a voltage level which will result in the bottom of the video signal matching the V_{rb} level of the A/D converter. This level will need to be set by clamping the black level of the video signal. The clamp voltage will depend on the level and polarity of the video signal. Detecting the sync signal can be done by a circuit such as the LM1881 Video Sync Separator.

Important Note: This is an illustration of a conceptual use of the LM7131, not a complete design. The circuit designer will need to modify this for input protection, sync, and possibly some type of gain control for varying signal levels.

Some A/D converters have wide input ranges where the lower reference level can be adjusted. With these converters, best distortion results are obtained if the lower end of the output range is about $250\ \text{mV}$ or more above the V_{-} input of the LM7131 more. The upper limit can be as high as 4.0V with good results.

Driving the ADC12062 + 5V 12-BIT A/D Converter

Figure 14 shows the LM7131 driving a National ADC12062 12 bit analog to digital converter. Both devices can be powered from a single $+5\text{V}$ supply, lowering system complexity and cost. With the lowest signal voltage limited to $300\ \text{mV}$ and a 3.8V peak-to-peak $100\ \text{kHz}$ signal, bench tests have shown distortion less than $-75\ \text{db}$, signal to noise ratios greater than $66\ \text{db}$, and SINAD (signal to noise + distortion) values greater than $65\ \text{db}$. For information on the latest single supply analog-to-digital converters, please contact your National Semiconductor representative.



Using the LM7131 (Continued)

CCD Amplifiers

The LM7131 has enough gain bandwidth to amplify low level signals from a CCD or similar image sensor and drive a flash analog-to-digital converter with one amplifier stage.

Signals from CCDs, which are used in scanners, copiers, and digital cameras, often have an output signal in the 100 mV–300 mV range. See *Figure 15* for a conceptual diagram. With a gain of 6 the output to the flash analog-to-digital converter is 1.8V, matching 90% of the converter's 2V input range. With a -3db bandwidth of 70 MHz for a gain of +1, the bandwidth at a gain of 6 will be 11.6 MHz. This 11.6 MHz bandwidth will result in a time constant of about 13.6 ns. This will allow the output to settle to 7 bits of accuracy within 4.9 time constants, or about 66 ns. Slewing time for a 1.8V step will be about 12 ns. The total slewing and settling time will be about 78 ns of the 150 ns pixel valid time. This will leave about 72 ns total for the flash converter signal acquisition time and tolerance for timing signals.

For scanners and copiers with moving scan bars, the SOT23-5 package is small enough to be placed next to the light sensor. The LM7131 can drive a cable to the main electronics section from the scan bar. This can reduce noise pickup by amplifying the signal before sending on the cable.

A/D Reference Drivers

The LM7131's output and drive capability make it a good choice for driving analog-to-digital references which have suddenly changing loads. The small size of the SOT23-5 package allow the LM7131 to be placed very close to the A/D reference pin, maximizing response. The small size avoids the penalty of increased board space. Often the SOT23-5 package is small enough that it can fit in space used by the large capacitors previously attached to the A/D reference. By acting as a buffer for a reference voltage, noise pickup can be reduced and the accuracy may be increased.

For additional space savings, the LM4040 precision voltage reference is available in a tiny SOT23-3 package.

Video Gain of +2

The design of the LM7131 has been optimized for gain of +2 video applications. Typical values for differential gain and phase are 0.25% differential gain and 0.75 degree differential phase. See *Figure 12*.

Improving Video Performance

Differential gain and phase performance can be improved by keeping the active video portion of the signal above 300 mV. The sync signal can go below 300 mV without affecting the video quality. If it is possible to AC couple the signal and shift the output voltage slightly higher, much better video performance is possible. For a +5V single supply, an output range between 2.0V and 3.0V can have a differential gain of 0.07% and differential phase of 0.3 degree when driving a 150Ω load. For a +3V single supply, the output should be between 1.0V and 2.0V.

Cable Driving with +5V Supplies

The LM7131 can easily drive a back-terminated 75 Ω video cable (150 Ω load) when powered by a +5V supply. See *Figures 2, 3* and *4*. This makes it a good choice for video output for portable equipment, personal digital devices, and desktop video applications.

The LM7131 can also supply +2.00V to a 50Ω load to ground, making it useful as driver in 50Ω systems such as portable test equipment.

Cable Driving with +3V Supplies

The LM7131 can drive 150 Ω to 2.00V when supplied by a 3V supply. This 3V performance means that the LM7131 is useful in battery powered video applications, such as camcorders, portable video mixers, still video cameras, and portable scanners.

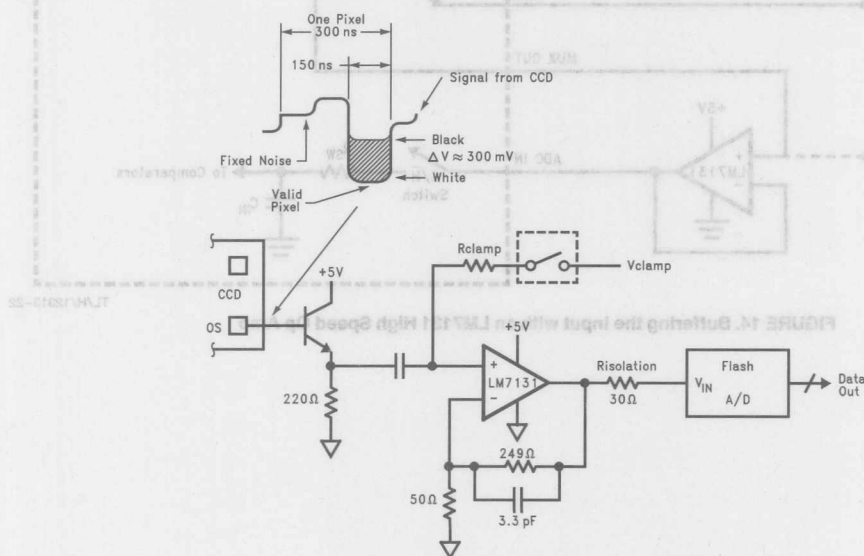


FIGURE 15. CCD Amplifier

TL/H/12313-23

Using the LM7131 (Continued)

Audio and High Frequency Signal Processing

The LM7131 is useful for high fidelity audio and signal processing. A typical LM7131 is capable of driving 2V across 150Ω (referenced to ground) at less than 0.1% distortion at 4 MHz when powered by a single 5V supply.

Use with 2.5V Virtual Ground Systems with +5V Single Supply Power

Many analog systems which must work on a single +5V supply use a 'virtual ground' - a reference voltage for the signal processing which is usually between +5V and 0V. This virtual ground is usually halfway between the top and bottom supply rails. This is usually +2.5V for +5V systems and +1.5V for +3V systems.

The LM7131 can be used in single supply/virtual ground systems driving loads referenced to 2.5V. The output swing specifications in the data sheet show the tested voltage limits for driving a 150Ω load to a virtual ground supply for +3V and +5V. A look at the output swing specifications shows that for heavy loads like 150 ohms, the output will swing as close as one diode drop (roughly, 0.7V) to the supply rail. This leaves a relatively wide range for +5V systems and a somewhat narrow range for +3V systems. One way to increase this output range is to have the output load referenced to ground—this will allow the output to swing lower. Another is to use higher load impedances. The output swing specifications show typical numbers for swing with loads of 600Ω to ground. Note that these typical numbers are similar to those for a 150Ω load. These typical numbers are an indication of the maximum DC performance of the LM7131.

The sinking output of the LM7131 is somewhat lower than the amplifier's sourcing capability. This means that the LM7131 will not drive as much current into a load tied to 2.5V as it will drive into a load tied to 0V.

Good AC performance will require keeping the output further away from the supply rails. For a +5V supply and relatively high impedance load (analog-to-digital converter input) the following are suggested as an initial starting range for achieving high (> 60 dB) AC accuracy

Upper output level—

Approximately 0.8V to 1V below the positive (V+) rail.

Lower output level—

Approximately 200 mV–300 mV above the negative rail.

The LM7131 very useful in virtual ground systems as an output device for output loads which are referenced to 0V or the lower rail. It is also useful as a driver for capacitive loads, such as sample and hold circuits, and audio analog to digital converters. If fast amplifiers with rail-to-rail output ranges are needed, please see the National Semiconductor LM6142 datasheet.

D/A Output Amplifier

The LM7131 can be used as an output amplifier for fast digital-to-analog converters. When using the LM7131 with converters with an output voltage range which may exceed the differential input voltage limit of $\pm 2V$, it may be necessary to add protection diodes to the inputs. See Figure 16. For high speed applications, it may be useful to consider low capacitance schottky diodes. Additional feedback capacitance may be needed to control ringing due to the additional input capacitance from the D/A and protection diodes. When used with current output D/As, the input bias currents may produce a DC offset in the output. This offset may be canceled by a resistor between the positive input and ground.

Spice Macromodel

A SPICE macromodel of the LM7131 and many other National Semiconductor op amps is available at no charge from your National Semiconductor representative.

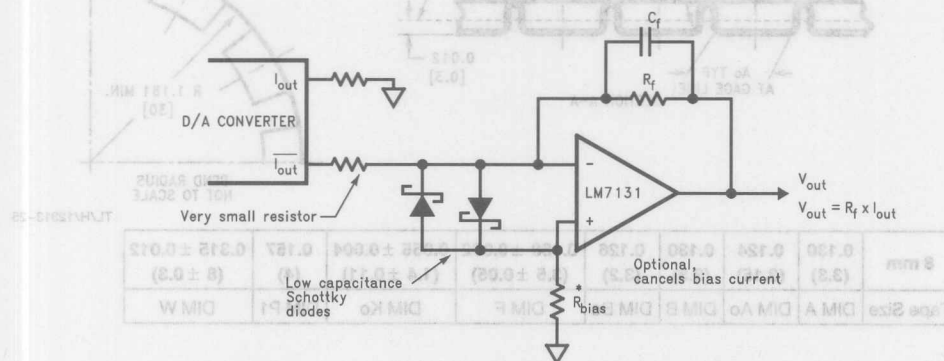


FIGURE 16. D/A Output Amplifier

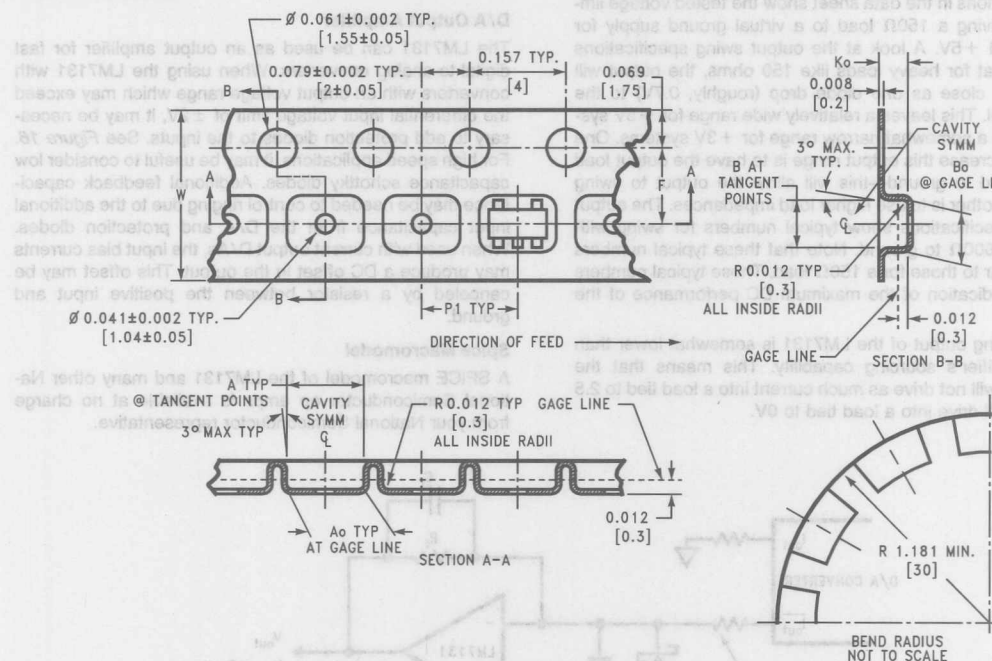
TL/H/12313-24

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

| Tape Section | # Cavaties | Cavity Status | Cover Tape Status |
|-----------------------|------------|---------------|-------------------|
| Leader (Start End) | 0 (min) | Empty | Sealed |
| | 75 (min) | Empty | Sealed |
| Carrier | 3000 | Filled | Sealed |
| | 250 | Filled | Sealed |
| Trailer (Hub End) | 125 (min) | Empty | Sealed |
| | 0 (min) | Empty | Sealed |

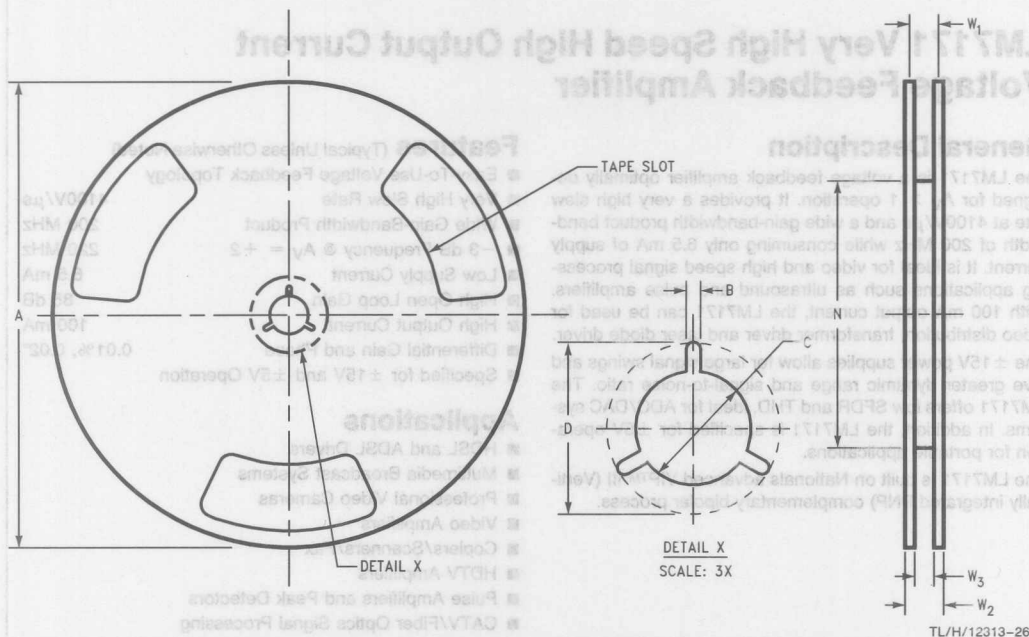
TAPE DIMENSIONS



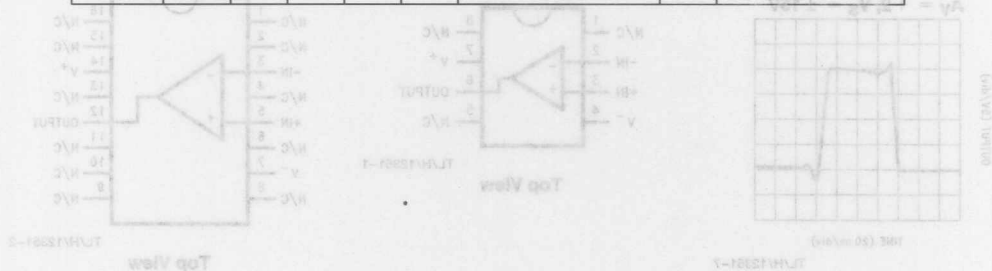
| | | | | | | | | |
|-----------|----------------|-----------------|----------------|----------------|-------------------------------|-------------------------------|--------------|----------------------------|
| 8 mm | 0.130 (3.3) | 0.124 (3.15) | 0.130 (3.3) | 0.126 (3.2) | 0.138 ± 0.002 (3.5 ± 0.05) | 0.055 ± 0.004 (1.4 ± 0.11) | 0.157 (4) | 0.315 ± 0.012 (8 ± 0.3) |
| Tape Size | DIM A | DIM Ao | DIM B | DIM Bo | DIM F | DIM Ko | DIM P1 | DIM W |

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



| 8 mm | 7.00 | 0.059 | 0.512 | 0.795 | 2.165 | 0.331 + 0.059/-0.000 | 0.567 | W1 + 0.078/-0.039 |
|-----------|--------|-------|-------|-------|-------|----------------------|-------|-------------------|
| | 330.00 | 1.50 | 13.00 | 20.20 | 55.00 | 8.4 + 1.50/-0.00 | 14.40 | W1 + 2.00/-1.00 |
| Tape Size | A | B | C | D | N | W1 | W2 | W3 |



Ordering Information

| Package | Military Drawing | Temperature Range | |
|---------------|------------------|-------------------|-----------------|
| | | Industrial | Military |
| 8-Pin DIP | LM7131M | -40°C to +85°C | -55°C to +125°C |
| 8-Pin CDIP | LM7131M | -40°C to +85°C | -55°C to +125°C |
| 8-Pin | LM7131M | -40°C to +85°C | -55°C to +125°C |
| Small Outline | LM7131M | -40°C to +85°C | -55°C to +125°C |
| 16-Pin | LM7131M | -40°C to +85°C | -55°C to +125°C |
| Small Outline | LM7131M | -40°C to +85°C | -55°C to +125°C |

*For the military temperature grade, please refer to the Military Drawing: MIL-M7131M/1.

LM7171 Very High Speed High Output Current Voltage Feedback Amplifier

General Description

The LM7171 is a voltage feedback amplifier optimally designed for $A_V > 1$ operation. It provides a very high slew rate at $4100\text{V}/\mu\text{s}$ and a wide gain-bandwidth product bandwidth of 200 MHz while consuming only 6.5 mA of supply current. It is ideal for video and high speed signal processing applications such as ultrasound and pulse amplifiers. With 100 mA output current, the LM7171 can be used for video distribution, transformer driver and laser diode driver.

The $\pm 15\text{V}$ power supplies allow for large signal swings and give greater dynamic range and signal-to-noise ratio. The LM7171 offers low SFDR and THD, ideal for ADC/DAC systems. In addition, the LM7171 is specified for $\pm 5\text{V}$ operation for portable applications.

The LM7171 is built on Nationals advanced VIPTM III (Vertically integrated PNP) complementary bipolar process.

Features (Typical Unless Otherwise Noted)

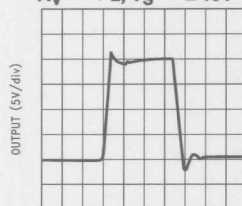
- Easy-To-Use Voltage Feedback Topology
- Very High Slew Rate $4100\text{V}/\mu\text{s}$
- Wide Gain-Bandwidth Product 200 MHz
- -3 dB Frequency @ $A_V = +2$ 220 MHz
- Low Supply Current 6.5 mA
- High Open Loop Gain 85 dB
- High Output Current 100 mA
- Differential Gain and Phase 0.01%, 0.02°
- Specified for $\pm 15\text{V}$ and $\pm 5\text{V}$ Operation

Applications

- HDSD and ADSL Drivers
- Multimedia Broadcast Systems
- Professional Video Cameras
- Video Amplifiers
- Copiers/Scanners/Fax
- HDTV Amplifiers
- Pulse Amplifiers and Peak Detectors
- CATV/Fiber Optics Signal Processing

Typical Performance

Large Signal Pulse Response
 $A_V = +2, V_S = \pm 15\text{V}$

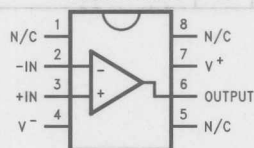


TIME (20 ns/div)

TL/H/12351-7

Connection Diagrams

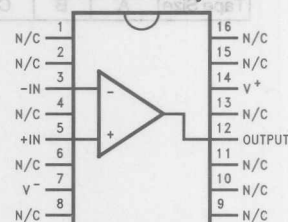
8-Pin DIP/SO



Top View

TL/H/12351-1

16-Pin Wide Body SO



Top View

TL/H/12351-2

Ordering Information

| Package | Temperature Range | | Transport Media | NSC Drawing |
|----------------------|------------------------------|-----------------------------|-----------------|-------------|
| | Industrial -40°C to +85°C | Military -55°C to +125°C | | |
| 8-Pin DIP | LM7171AIN, LM7171BIN | | Rails | N08E |
| 8-Pin CDIP | | | Rails | J08A |
| 8-Pin Small Outline | LM7171AIM, LM7171BIM | | Rails | M08A |
| | LM7171AIMX, LM7171BIMX | | Tape and Reel | |
| 16-Pin Small Outline | LM7171AIWM, LM7171BIWM | | Rails | M16B |
| | LM7171AWMX, LM7171BWMX | | Tape and Reel | |

*For the military temperature grade, please refer to the Military Datasheet: MNLM7171AMJ/883

LM13600 Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers which are especially designed to complement the dynamic range of the amplifiers are provided.

Features

- g_m adjustable over 6 decades
- Excellent g_m linearity

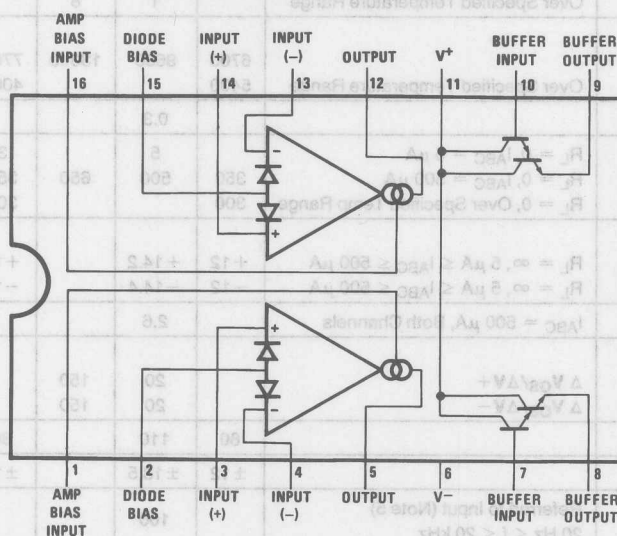
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal-to-noise ratio

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Connection Diagram

Dual-In-Line and Small Outline Packages



Top View

Order Number LM13600M, LM13600N or LM13600AN
See NS Package Number M16A or N16A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)

LM13600

36 V_{DC} or ± 18 V

LM13600A

44 V_{DC} or ± 22 V

Power Dissipation (Note 2) T_A = 25°C

570 mW

Differential Input Voltage

± 5 V

Diode Bias Current (I_D)

2 mA

Amplifier Bias Current (I_{ABC})

2 mA

Output Short Circuit Duration

Continuous

Buffer Output Current (Note 3)

20 mA

Operating Temperature Range

0°C to +70°C

DC Input Voltage

+V_S to -V_S

Storage Temperature Range

-65°C to +150°C

Soldering Information

Dual-In-Line Package

Soldering (10 seconds)

260°C

Small Outline Package

Vapor Phase (60 seconds)

215°C

Infrared (15 seconds)

220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

| Parameter | Conditions | LM13600 | | | LM13600A | | | Units |
|--|--|----------|------------|-------|----------|------------|-------|-----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (V _{OS}) | Over Specified Temperature Range | | 0.4 | 4 | | 0.4 | 1 | mV |
| | I _{ABC} = 5 μ A | | 0.3 | 4 | | 0.3 | 2 | mV |
| | | | | | | | 1 | mV |
| V _{OS} Including Diodes | Diode Bias Current (I _D) = 500 μ A | | 0.5 | 5 | | 0.5 | 2 | mV |
| Input Offset Change | 5 μ A \leq I _{ABC} \leq 500 μ A | | 0.1 | 3 | | 0.1 | 1 | mV |
| Input Offset Current | | | 0.1 | 0.6 | | 0.1 | 0.6 | μ A |
| Input Bias Current | Over Specified Temperature Range | | 0.4 | 5 | | 0.4 | 5 | μ A |
| | | | 1 | 8 | | 1 | 7 | μ A |
| Forward Transconductance (g _m) | | 6700 | 9600 | 13000 | 7700 | 9600 | 12000 | μ mho |
| | Over Specified Temperature Range | 5400 | | | 4000 | | | μ mho |
| g _m Tracking | | | 0.3 | | | 0.3 | | dB |
| Peak Output Current | R _L = 0, I _{ABC} = 5 μ A | | 5 | | 3 | 5 | 7 | μ A |
| | R _L = 0, I _{ABC} = 500 μ A | 350 | 500 | 650 | 350 | 500 | 650 | μ A |
| | R _L = 0, Over Specified Temp Range | 300 | | | 300 | | | μ A |
| Peak Output Voltage | R _L = ∞ , 5 μ A \leq I _{ABC} \leq 500 μ A | +12 | +14.2 | | +12 | +14.2 | | V |
| | R _L = ∞ , 5 μ A \leq I _{ABC} \leq 500 μ A | -12 | -14.4 | | -12 | -14.4 | | V |
| Supply Current | I _{ABC} = 500 μ A, Both Channels | | 2.6 | | | 2.6 | | mA |
| V _{OS} Sensitivity | $\Delta V_{OS}/\Delta V$ + | | 20 | 150 | | 20 | 150 | μ V/V |
| | $\Delta V_{OS}/\Delta V$ - | | 20 | 150 | | 20 | 150 | μ V/V |
| CMRR | | 80 | 110 | | 80 | 110 | | dB |
| Common Mode Range | | ± 12 | ± 13.5 | | ± 12 | ± 13.5 | | V |
| Crosstalk | Referred to Input (Note 5) 20 Hz $< f <$ 20 kHz | | 100 | | | 100 | | dB |
| Differential Input Current | I _{ABC} = 0, Input = ± 4 V | | 0.02 | 100 | | 0.02 | 10 | nA |
| Leakage Current | I _{ABC} = 0 (Refer to Test Circuit) | | 0.2 | 100 | | 0.2 | 5 | nA |

Electrical Characteristics (Note 4) (Continued)

| Parameter | Conditions | LM13600 | | | LM13600A | | | Units |
|----------------------------|--------------------------------------|---------|-----|-----|----------|-----|-----|------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Resistance | | 10 | 26 | | 10 | 26 | | k Ω |
| Open Loop Bandwidth | | | 2 | | | 2 | | MHz |
| Slew Rate | Unity Gain Compensated | | 50 | | | 50 | | V/ μ s |
| Buffer Input Current | (Note 5), Except $I_{ABC} = 0 \mu A$ | | 0.2 | 0.4 | | 0.2 | 0.4 | μA |
| Peak Buffer Output Voltage | (Note 5) | 10 | | | 10 | | | V |

Note 1: For selections to a supply voltage above $\pm 22V$, contact factory.

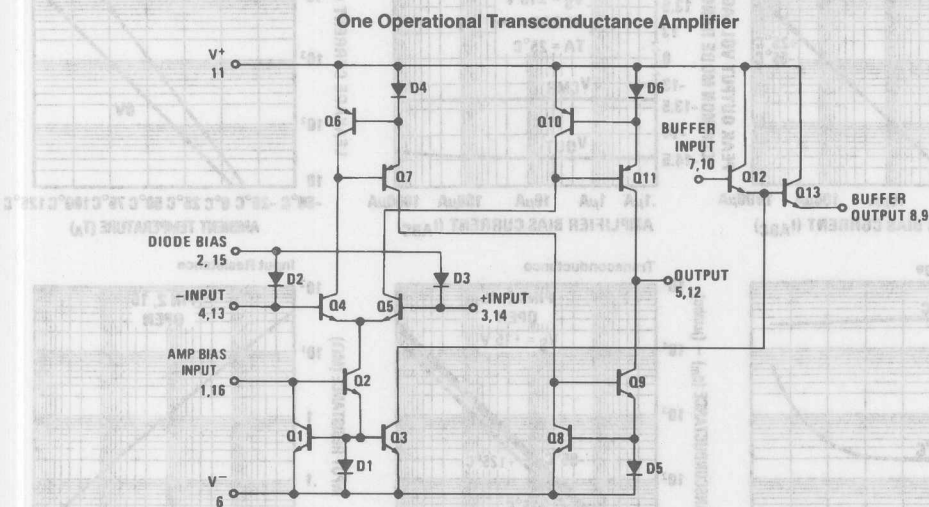
Note 2: For operating at high temperatures, the device must be derated based on a $150^{\circ}C$ maximum junction temperature and a thermal resistance of $175^{\circ}C/W$ which applies for the device soldered in a printed circuit board, operating in still air.

Note 3: Buffer output current should be limited so as to not exceed package dissipation.

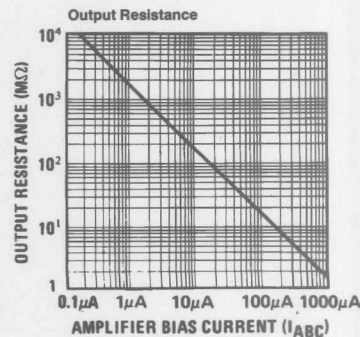
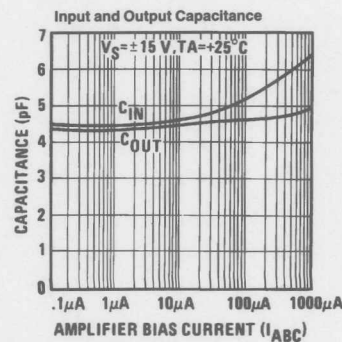
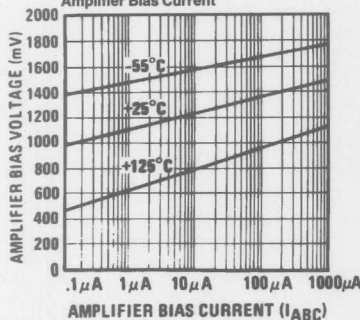
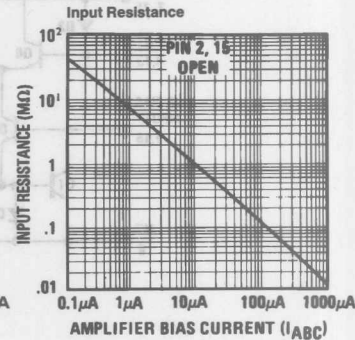
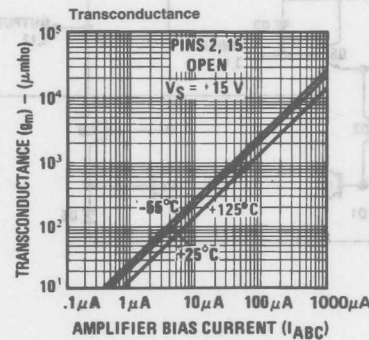
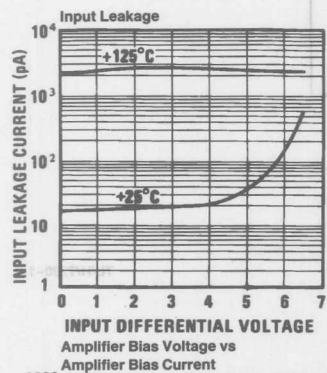
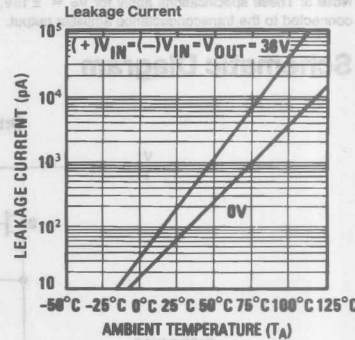
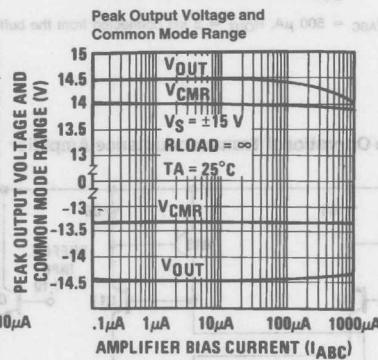
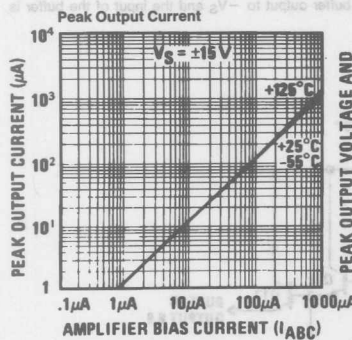
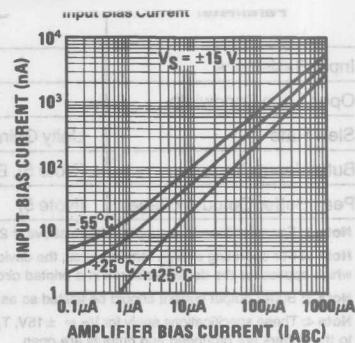
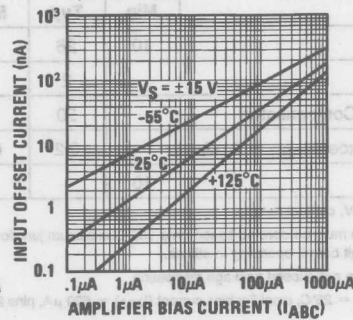
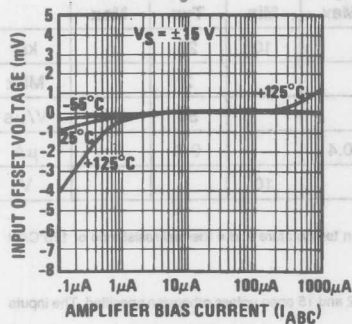
Note 4: These specifications apply for $V_S = \pm 15V$, $T_A = 25^{\circ}C$, amplifier bias current (I_{ABC}) = $500 \mu A$, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for $V_S = \pm 15V$, $I_{ABC} = 500 \mu A$, $R_{OUT} = 5 k\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

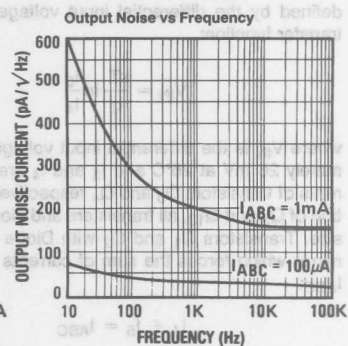
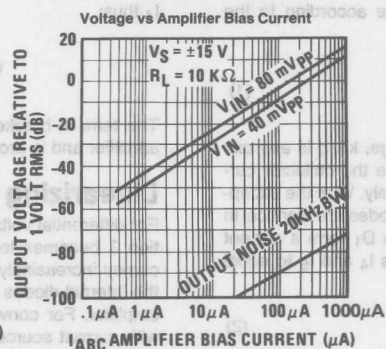
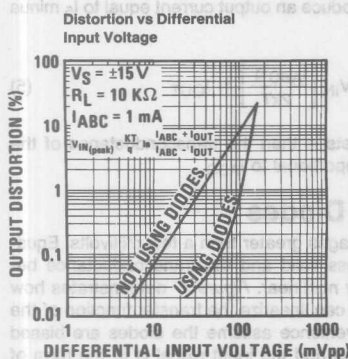
Schematic Diagram



TL/H/7980-1

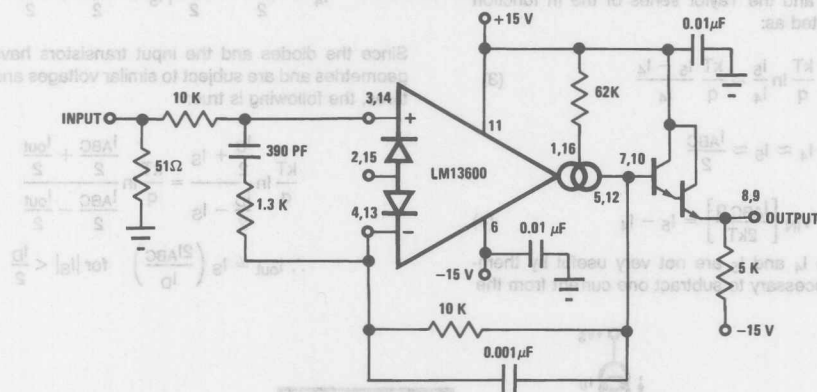


Typical Performance Characteristics (Continued)



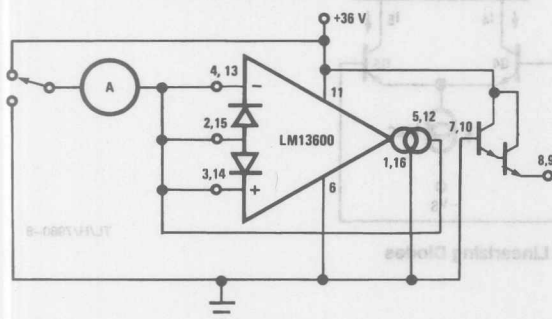
TL/H/7980-4

Unity Gain Follower



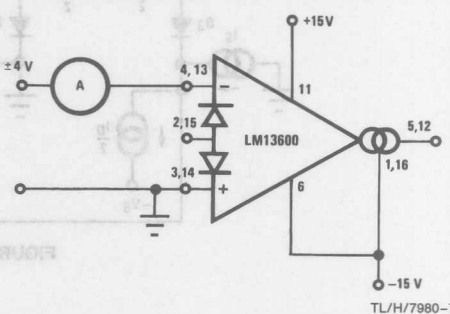
TL/H/7980-5

Leakage Current Test Circuit



TL/H/7980-6

Differential Input Current Test Circuit



TL/H/7980-7

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13} , all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC} :

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the \ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC} q}{2kT} \right] = I_5 - I_4 \quad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the

other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC} q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC} .

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S . Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT} , currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}}$$

$$\therefore I_{OUT} = I_S \left(\frac{2I_{ABC}}{I_D} \right) \quad \text{for } |I_S| < \frac{I_D}{2} \quad (6)$$

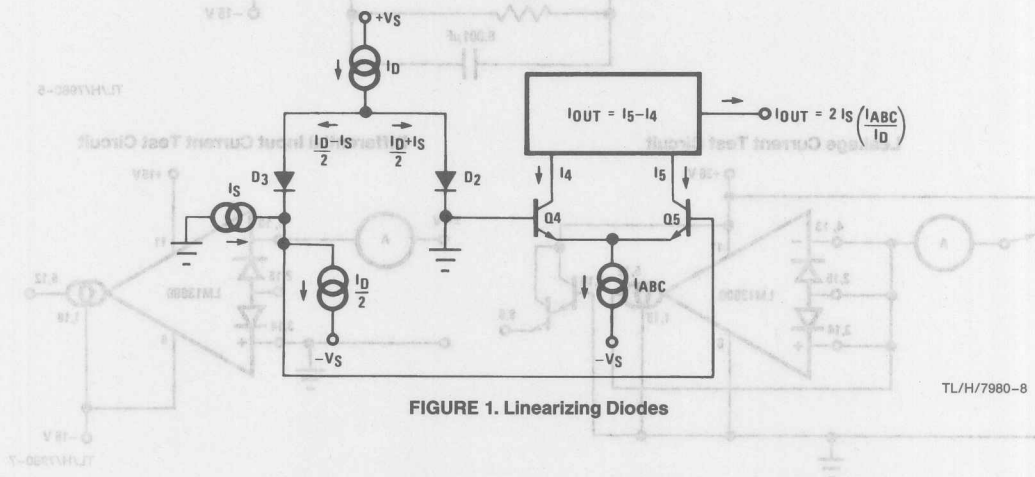


FIGURE 1. Linearizing Diodes

TL/H/7980-8

Linearizing Diodes (Continued)

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC} , a buffer which has very low input bias current is desirable. An FET follower satisfies the low input current requirement, but is somewhat non-linear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC} , the buffer's input current is minimal. At higher levels of I_{ABC} , transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate. When I_{ABC} is changed, the DC level of the Darlington output buffer will shift. In audio applications where I_{ABC} is changed suddenly, this shift may produce an audible "pop". For these applications the LM13700 may produce superior results.

Applications—Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 k Ω resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L .

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_d) and maximizes their linearizing action when balanced against R_{IN} . A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

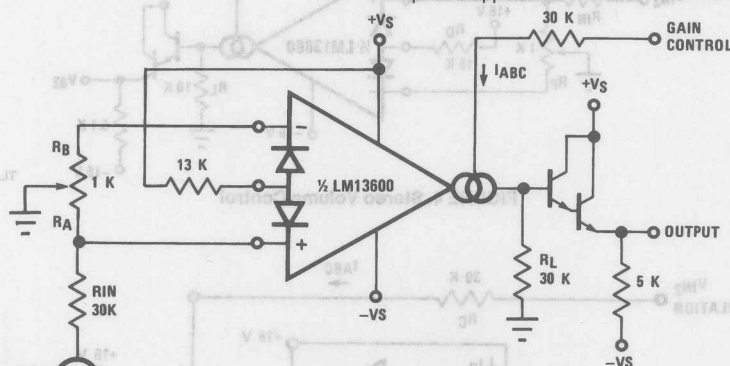


FIGURE 2. Voltage Controlled Amplifier

TL/H/7980-9

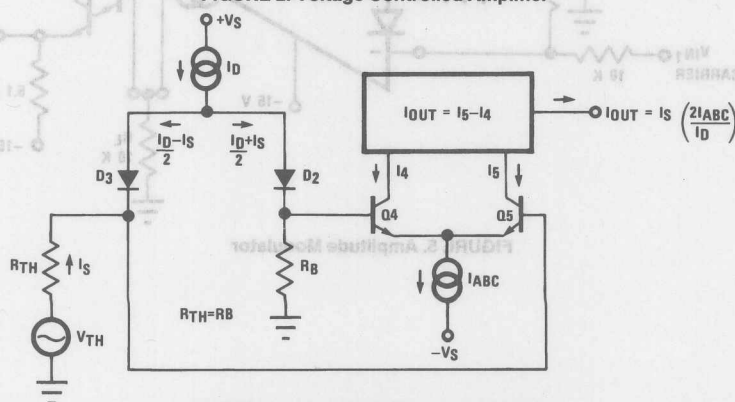


FIGURE 3. Equivalent VCA Input Circuit

TL/H/7980-10

Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_P is provided to minimize the output offset voltage and may be replaced with two 510 Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

For optimum signal-to-noise ratio, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current Graph. Larger amplitudes of input signal also improve the SNR ratio. The linearizing diodes help more by allowing larger input signals for the same output distortion as shown in the Distortion vs. Differential Input Voltage Graph. I_{ABC} can be adjusted by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output voltage is at the desired level. The output voltage can then be adjusted by selecting R_P .

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistor, it is as large as possible. This minimizes the dynamic range of the diodes (I_D and I_{ABC}) and maximizes their linearizing action when balanced against I_{ABC} . A value of 1 mA is recommended for I_{ABC} unless the application requires otherwise.

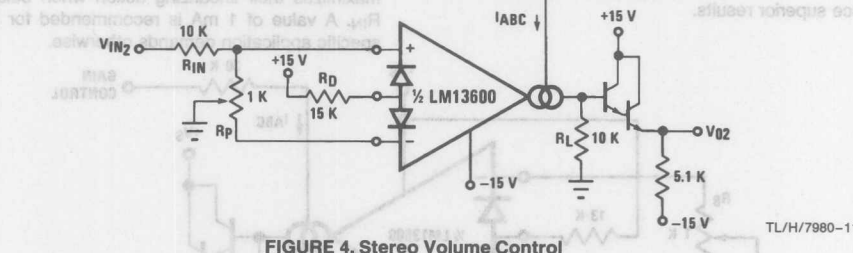


FIGURE 4. Stereo Volume Control

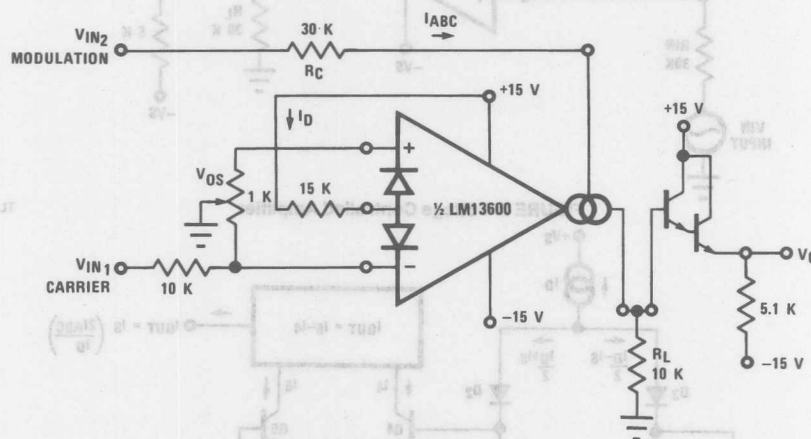


FIGURE 5. Amplitude Modulator

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D} (I_{ABC}) = \frac{-2I_S}{I_D} \frac{V_{IN2}}{R_C} = \frac{-2I_S}{I_D} \frac{(V_{IN2} + 1.4V)}{R_C}$$

Controlled Impedance Buffers

The upper limit of transconductance is defined by the minimum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC} , which has very low bias current is desirable. An amplifier that follows the low input current requirement, but is somewhat non-linear for large voltages. The output impedance buffer is a Darlington buffer. For low input current, the output current is not the same as the input current. The output current is biased up (with a constant level) for fast slew rate. When the input signal is small, the output current is small. When the input signal is large, the output current is large. This is the characteristic of a Darlington buffer. The output current is not the same as the input current. The output current is biased up (with a constant level) for fast slew rate. When the input signal is small, the output current is small. When the input signal is large, the output current is large. This is the characteristic of a Darlington buffer.

Stereo Volume Control (Continued)

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2$ ($V^- + 1.4V$) into I_O . The circuit of Figure 6 adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O .

Noting that the gain of the LM13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC} , Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3 V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown

in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at $25^\circ C$. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13600.

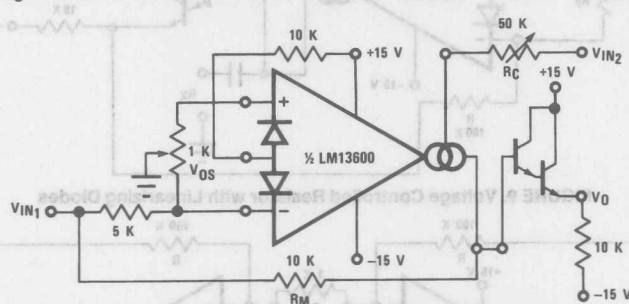


FIGURE 6. Four-Quadrant Multiplier

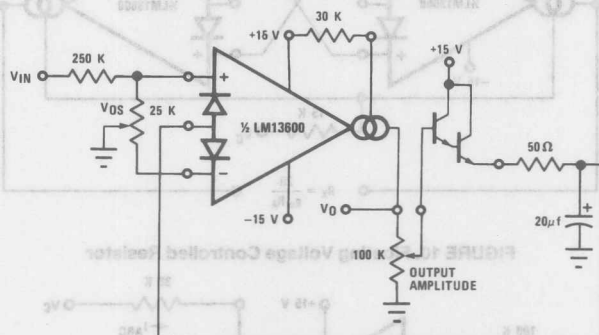


FIGURE 7. AGC Amplifier

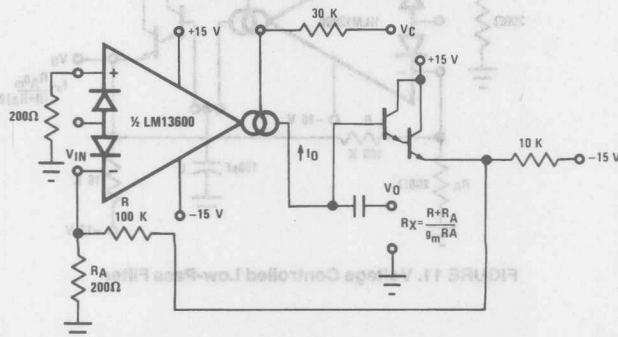


FIGURE 8. Voltage Controlled Resistor, Single-Ended

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A) . At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation,

where g_m is again $19.2 \times I_{ABC}$ at room temperature. Figure 12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent g_m tracking of the two amplifiers and the varied bias of the buffer Darlington's, these filters perform well over several decades of frequency.

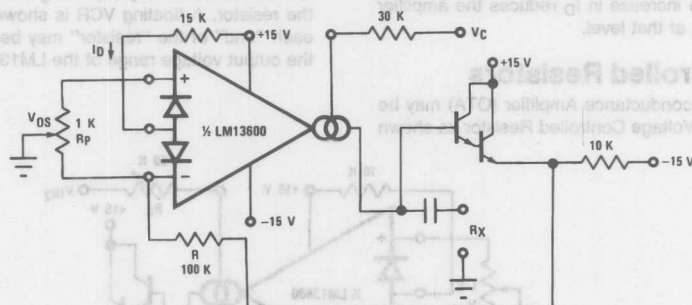


FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

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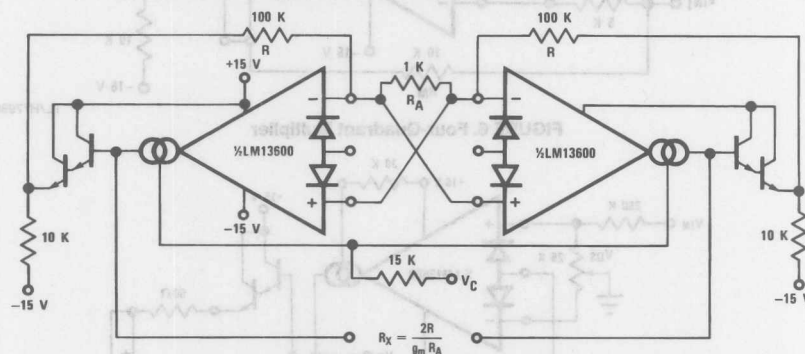


FIGURE 10. Floating Voltage Controlled Resistor

TL/H/7980-17

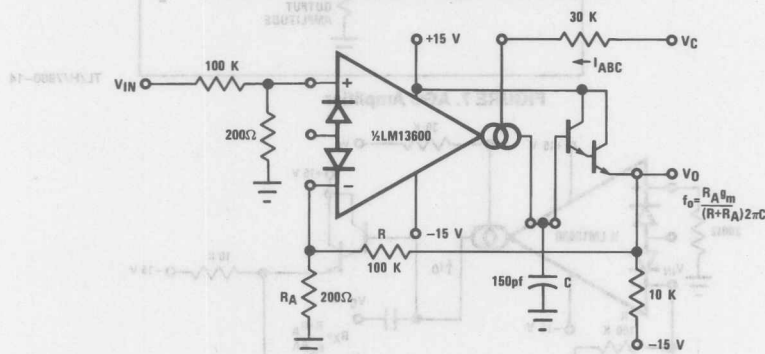


FIGURE 11. Voltage Controlled Low-Pass Filter

TL/H/7980-18

Voltage Controlled Filters (Continued)

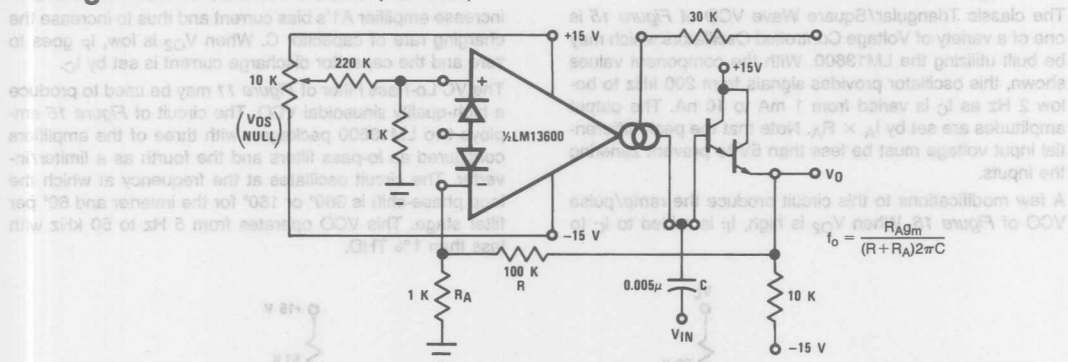


FIGURE 12. Voltage Controlled Hi-Pass Filter

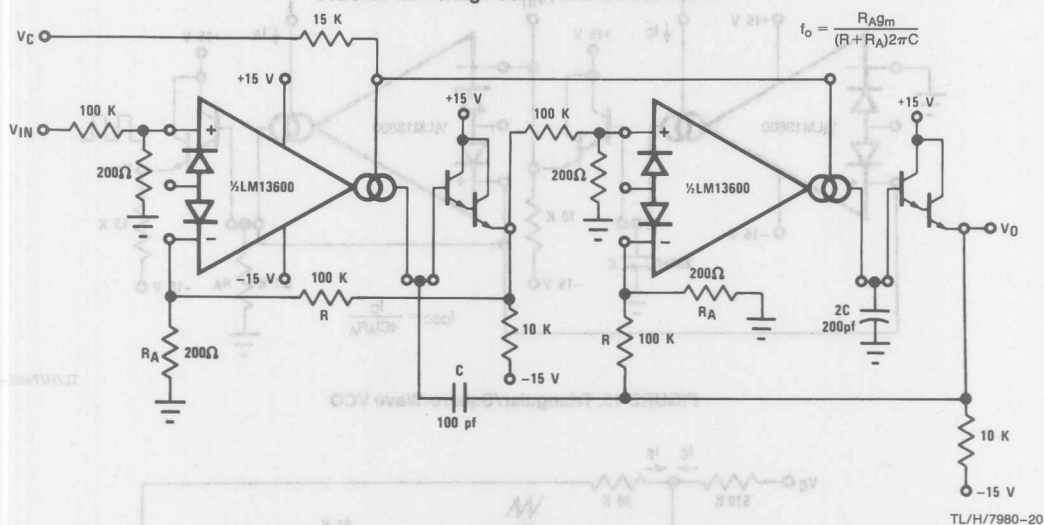


FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

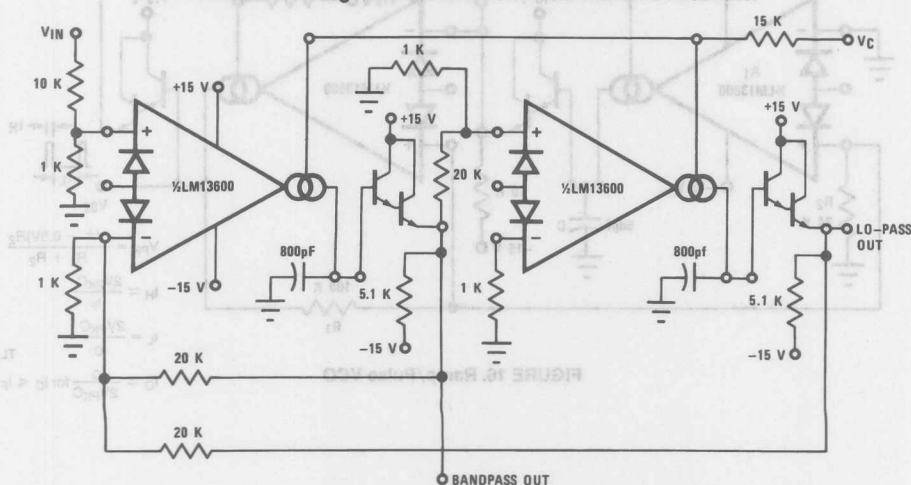


FIGURE 14. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of *Figure 15* is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to

increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C .

The VC Lo-Pass Filter of *Figure 11* may be used to produce a high-quality sinusoidal VCO. The circuit of *Figure 16* employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

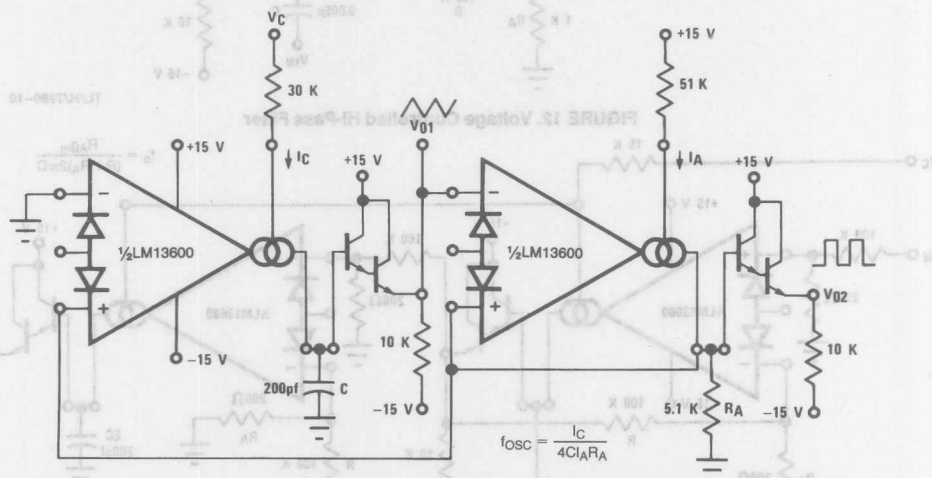


FIGURE 15. Triangular/Square-Wave VCO

TL/H/7980-22

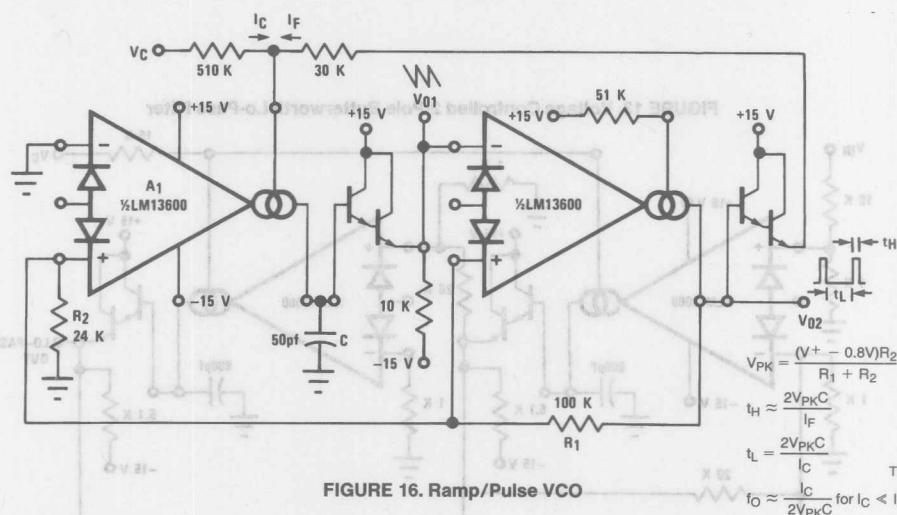


FIGURE 16. Ramp/Pulse VCO

TL/H/7980-23

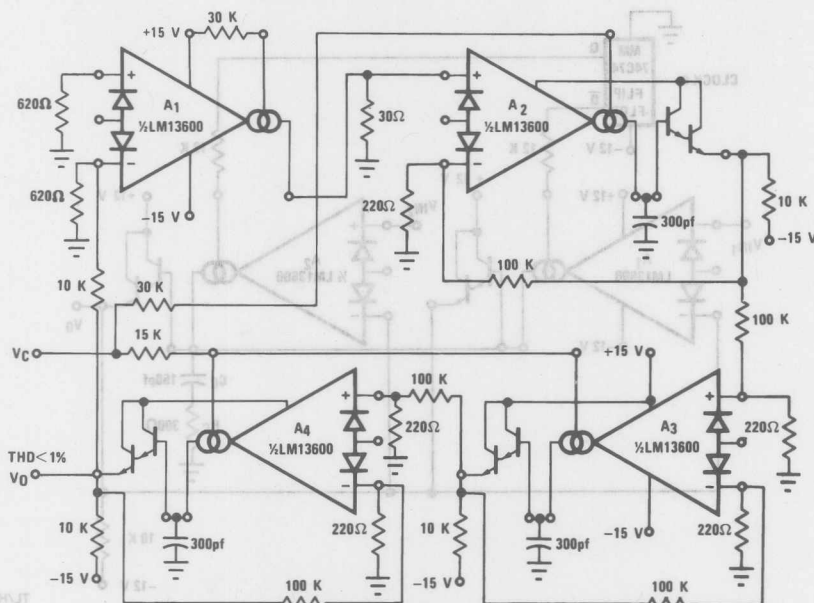


FIGURE 17. Sinusoidal VCO

TL/H/7980-24

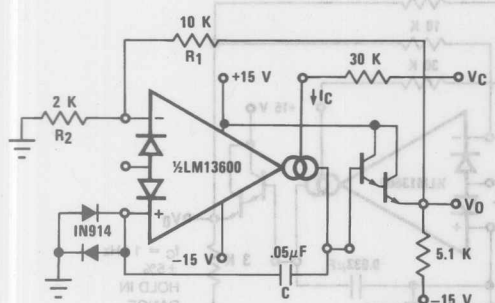


FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is increased by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O , can perform another function and draw zero stand-by power as well.

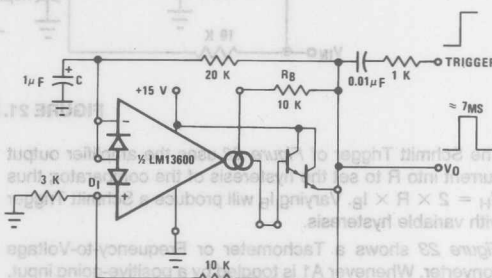


FIGURE 19. Zero Stand-By Power Timer

TL/H/7980-26

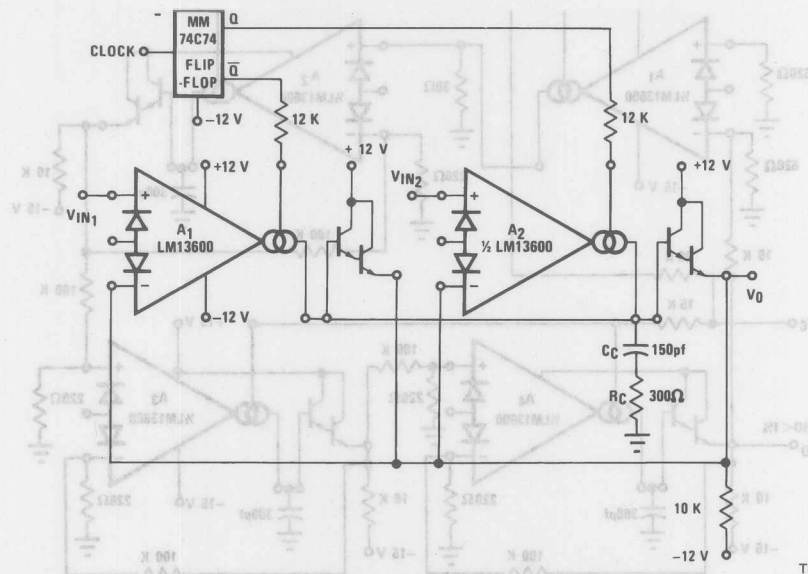


FIGURE 20. Multiplexer

TL/H/7980-27

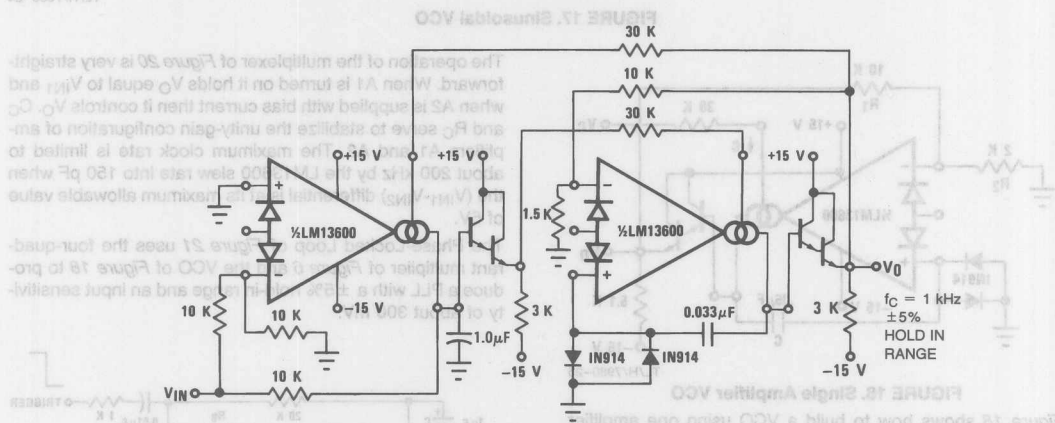


FIGURE 21. Phase Lock Loop

TL/H/7980-28

The Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L) C_t$ is sourced into C_t and R_t . This once-per-cycle charge is then balanced by the current of V_O/R_t . The maximum f_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B , where V_L and V_H represent the maximum low and maxi-

mum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_t when A1 switches low. The Peak Detector of Figure 24 uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O . A1 then charges storage capacitor C to hold V_O equal to V_{INPK} . One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

Additional Applications (Continued)

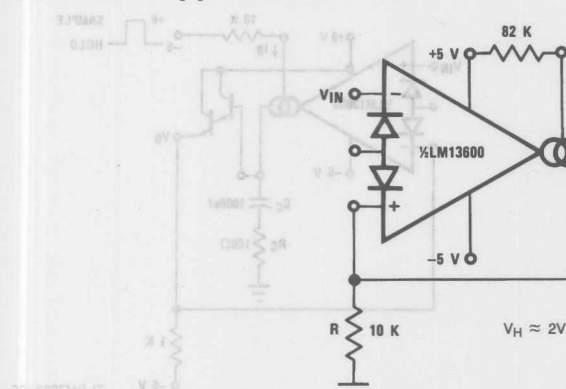


FIGURE 22. Schmitt Trigger

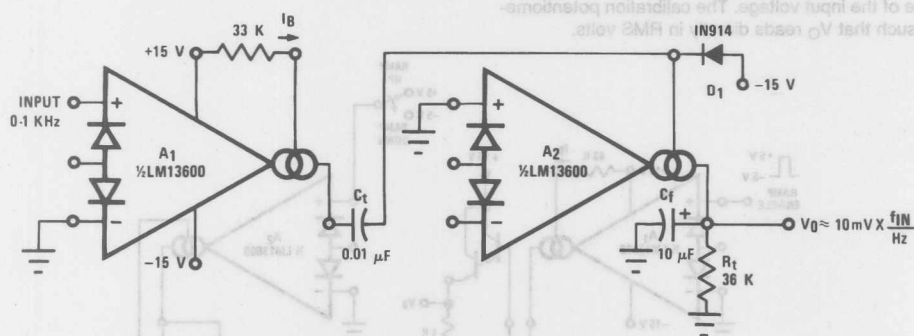


FIGURE 23. Tachometer

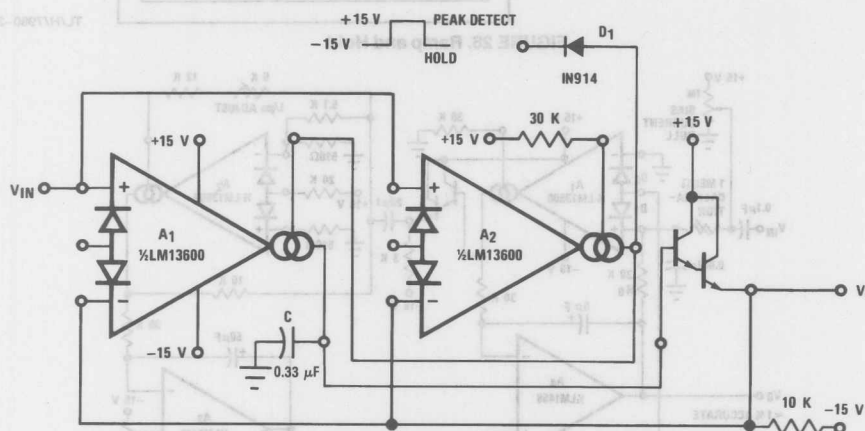


FIGURE 24. Peak Detector and Hold Circuit

Additional Applications (Continued)

The Sample-and-Hold circuit of *Figure 25* also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously. The Ramp-and-Hold of *Figure 26* sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1 V/ms for the component values shown.

The true-RMS converter of *Figure 27* is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

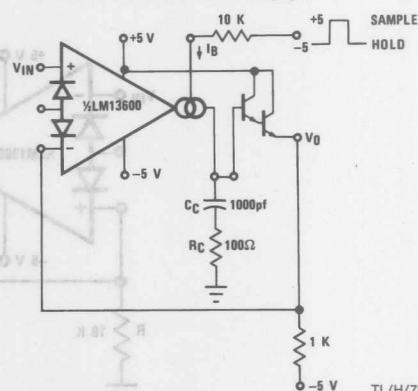


FIGURE 25. Sample-Hold Circuit

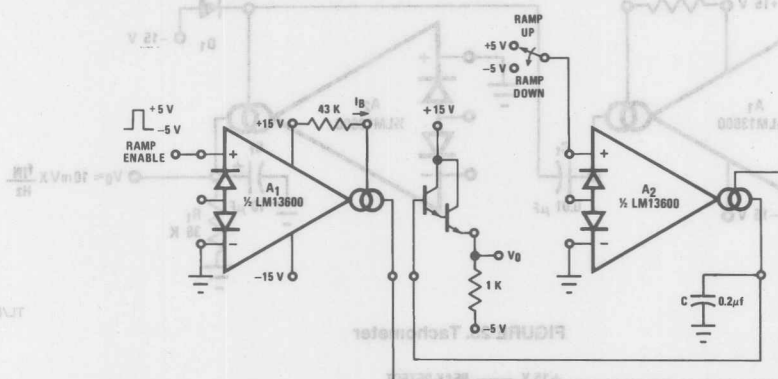


FIGURE 26. Ramp and Hold

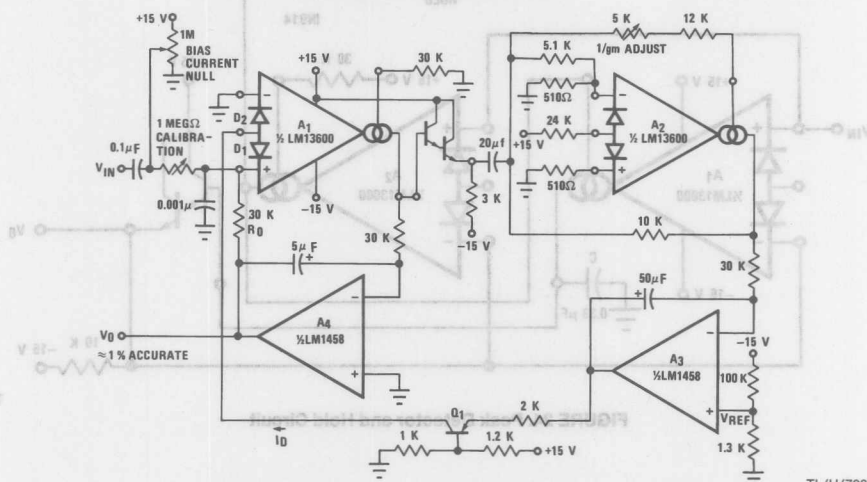


FIGURE 27. True RMS Converter

Additional Applications (Continued)

The circuit of Figure 28 is a voltage reference of variable temperature coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of Figure 29 responds to the ratio of currents through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured because the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 30.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1, R2 network so that A1 may be assumed to be

operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN1} = \frac{-2kT I_3}{q I_2} = \frac{2kT V_C}{q I_2 R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2) V_{IN1}}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_{B1} = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp \left[\frac{2(R_1 + R_2) V_C}{R_1 I_2 R_C} \right]$$

This logarithmic current can be used to bias the circuit of Figure 4 provide a temperature independent stereo attenuation characteristic.

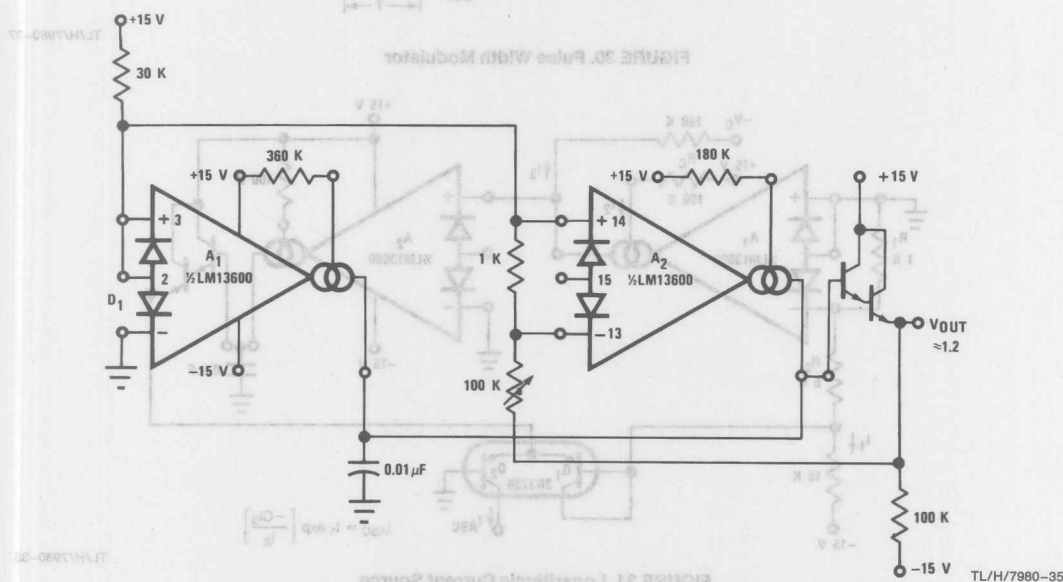


FIGURE 28. Delta VBE Reference

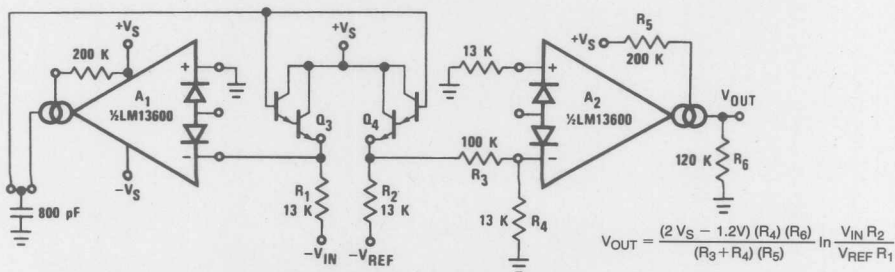


FIGURE 29. Log Amplifier

Additional Applications (Continued)

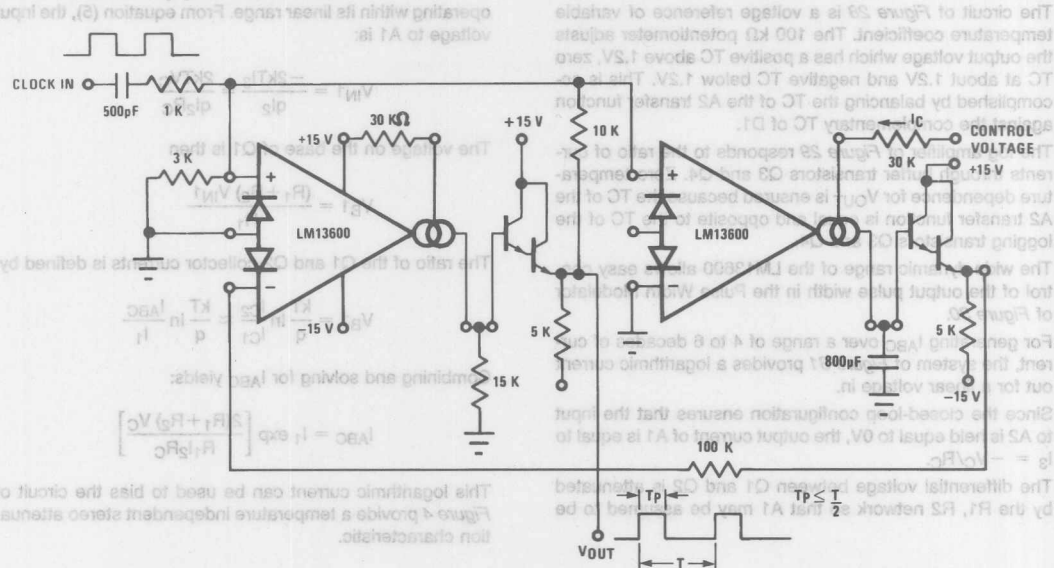


FIGURE 30. Pulse Width Modulator

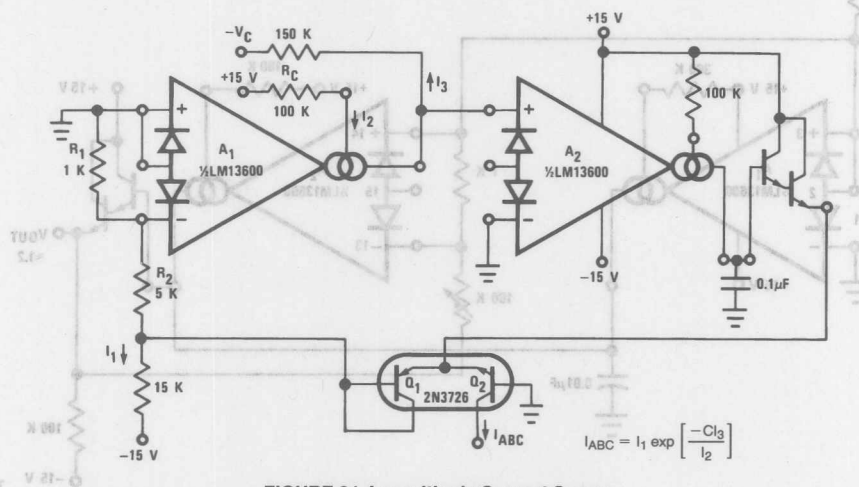


FIGURE 31. Logarithmic Current Source



LM13700/LM13700A

Dual Operational Transconductance Amplifiers with Linearizing Diodes and Buffers

General Description

The LM13700 series consists of two current controlled transconductance amplifiers, each with differential inputs and a push-pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The result is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. High impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers. The output buffers of the LM13700 differ from those of the LM13600 in that their input bias currents (and hence their output DC levels) are independent of I_{ABC} . This may result in performance superior to that of the LM13600 in audio applications.

Features

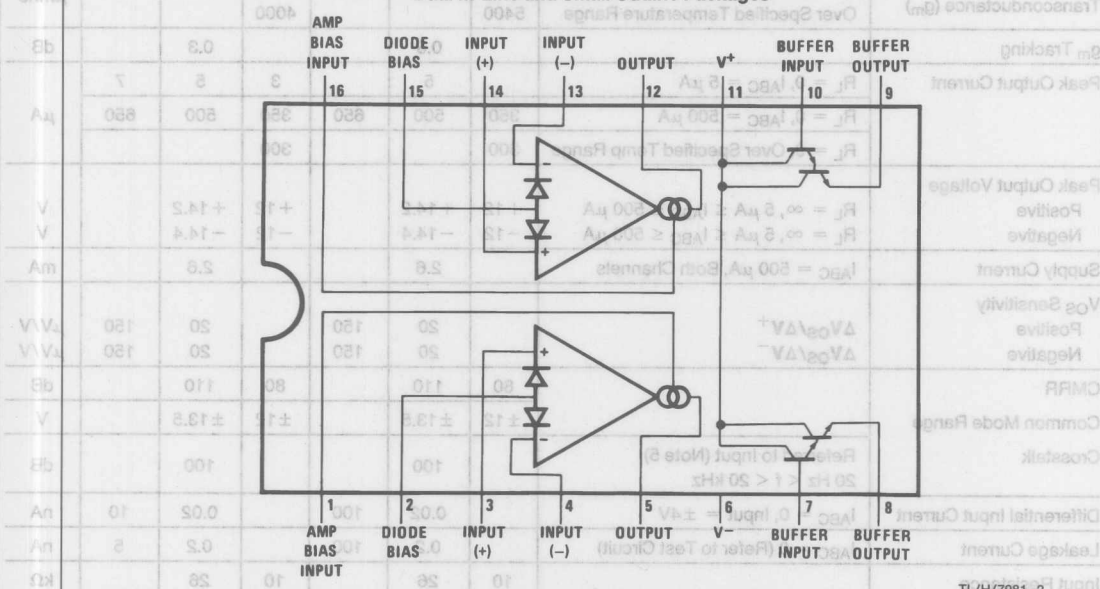
- g_m adjustable over 6 decades
- Excellent g_m linearity
- Excellent matching between amplifiers
- Linearizing diodes
- High impedance buffers
- High output signal-to-noise ratio

Applications

- Current-controlled amplifiers
- Current-controlled impedances
- Current-controlled filters
- Current-controlled oscillators
- Multiplexers
- Timers
- Sample-and-hold circuits

Connection Diagram

Dual In-Line and Small Outline Packages



Top View

Order Number LM13700M, LM13700N or LM13700AN
See NS Package Number M16A or N16A

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (Note 1)

LM13700

36 V_{DC} or $\pm 18V$

LM13700A

44 V_{DC} or $\pm 22V$ Power Dissipation (Note 2) T_A = 25°C

LM13700N, LM13700AN

570 mW

Differential Input Voltage

 $\pm 5V$ Diode Bias Current (I_D)

2 mA

Amplifier Bias Current (I_{ABC})

2 mA

Output Short Circuit Duration

Continuous

Buffer Output Current (Note 3)

20 mA

Operating Temperature Range

LM13700N, LM13700AN

0°C to +70°C

DC Input Voltage

 $+V_S$ to $-V_S$

Storage Temperature Range

-65°C to +150°C

Soldering Information

Dual-In-Line Package

Soldering (10 sec.)

260°C

Small Outline Package

Vapor Phase (60 sec.)

215°C

Infrared (15 sec.)

220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (Note 4)

| Parameter | Conditions | LM13700 | | | LM13700A | | | Units |
|--|--|----------|------------|-------|----------|------------|-------|------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (V _{OS}) | Over Specified Temperature Range | | 0.4 | 4 | | 0.4 | 1 | mV |
| | I _{ABC} = 5 μ A | | 0.3 | 4 | | 0.3 | 1 | |
| V _{OS} Including Diodes | Diode Bias Current (I _D) = 500 μ A | | 0.5 | 5 | | 0.5 | 2 | mV |
| Input Offset Change | 5 μ A \leq I _{ABC} \leq 500 μ A | | 0.1 | 3 | | 0.1 | 1 | mV |
| Input Offset Current | | | 0.1 | 0.6 | | 0.1 | 0.6 | μ A |
| Input Bias Current | Over Specified Temperature Range | | 0.4 | 5 | | 0.4 | 5 | μ A |
| | | | 1 | 8 | | 1 | 7 | |
| Forward Transconductance (g _m) | | 6700 | 9600 | 13000 | 7700 | 9600 | 12000 | μ mho |
| | Over Specified Temperature Range | 5400 | | | 4000 | | | |
| g _m Tracking | | | 0.3 | | | 0.3 | | dB |
| Peak Output Current | R _L = 0, I _{ABC} = 5 μ A | | 5 | | 3 | 5 | 7 | μ A |
| | R _L = 0, I _{ABC} = 500 μ A | 350 | 500 | 650 | 350 | 500 | 650 | |
| | R _L = 0, Over Specified Temp Range | 300 | | | 300 | | | |
| Peak Output Voltage | R _L = ∞ , 5 μ A \leq I _{ABC} \leq 500 μ A | +12 | +14.2 | | +12 | +14.2 | | V |
| | R _L = ∞ , 5 μ A \leq I _{ABC} \leq 500 μ A | -12 | -14.4 | | -12 | -14.4 | | |
| Supply Current | I _{ABC} = 500 μ A, Both Channels | | 2.6 | | | 2.6 | | mA |
| V _{OS} Sensitivity | Positive | | 20 | 150 | | 20 | 150 | μ V/V |
| | Negative | | 20 | 150 | | 20 | 150 | |
| CMRR | | 80 | 110 | | 80 | 110 | | dB |
| Common Mode Range | | ± 12 | ± 13.5 | | ± 12 | ± 13.5 | | V |
| Crosstalk | Referred to Input (Note 5) 20 Hz < f < 20 kHz | | 100 | | | 100 | | dB |
| Differential Input Current | I _{ABC} = 0, Input = $\pm 4V$ | | 0.02 | 100 | | 0.02 | 10 | nA |
| Leakage Current | I _{ABC} = 0 (Refer to Test Circuit) | | 0.2 | 100 | | 0.2 | 5 | nA |
| Input Resistance | | 10 | 26 | | 10 | 26 | | k Ω |

| Parameter | Conditions | LM13700 | | | LM13700A | | | Units |
|----------------------------|------------------------|---------|-----|-----|----------|-----|-----|------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Open Loop Bandwidth | | | 2 | | | 2 | | MHz |
| Slew Rate | Unity Gain Compensated | | 50 | | | 50 | | V/ μ s |
| Buffer Input Current | (Note 5) | | 0.5 | 2 | | 0.5 | 2 | μ A |
| Peak Buffer Output Voltage | (Note 5) | 10 | | | 10 | | | V |

Note 1: For selections to a supply voltage above ± 22 V, contact factory.

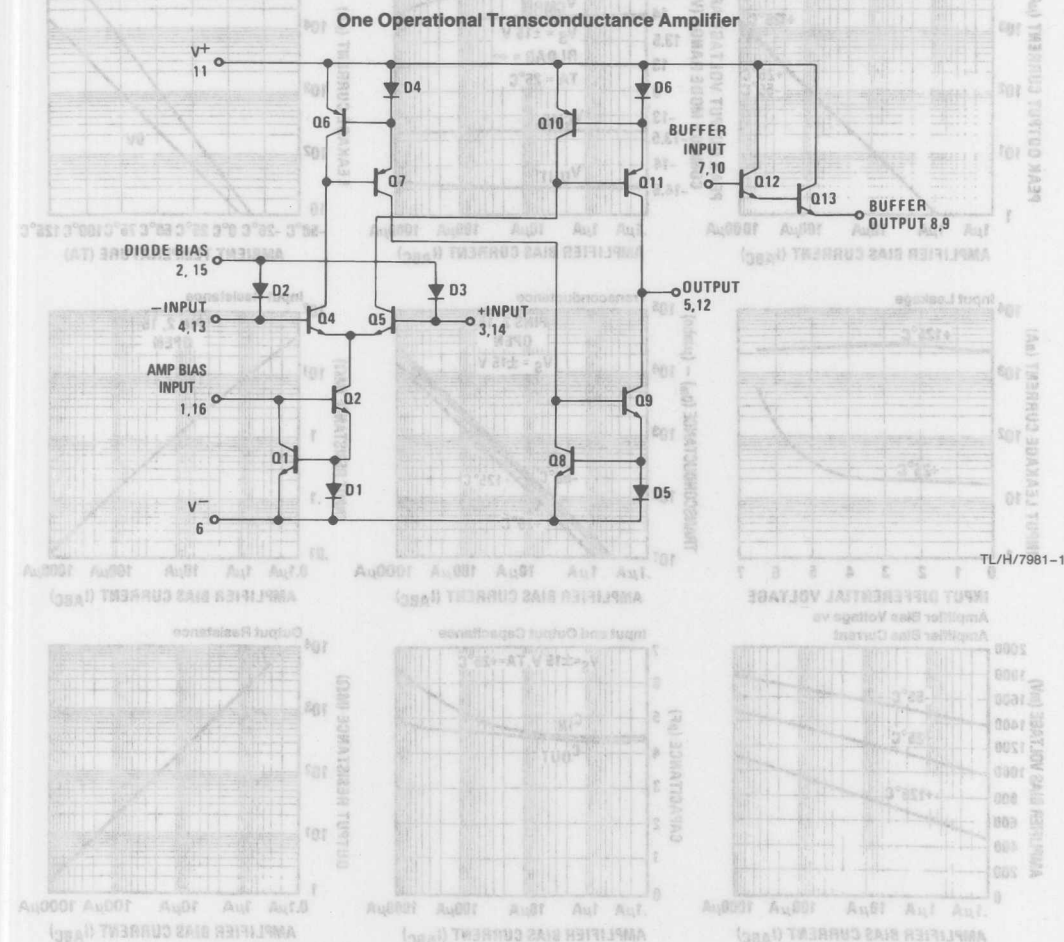
Note 2: For operation at ambient temperatures above 25°C , the device must be derated based on a 150°C maximum junction temperature and a thermal resistance, junction to ambient, as follows: LM13700N, 90°C/W ; LM13700M, 110°C/W .

Note 3: Buffer output current should be limited so as to not exceed package dissipation.

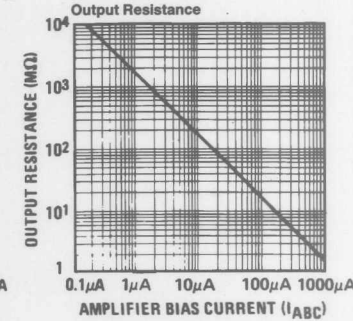
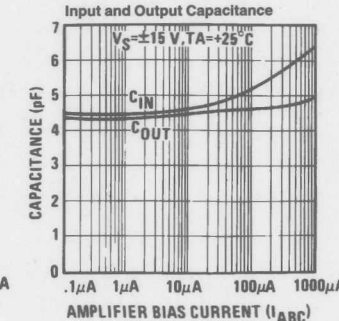
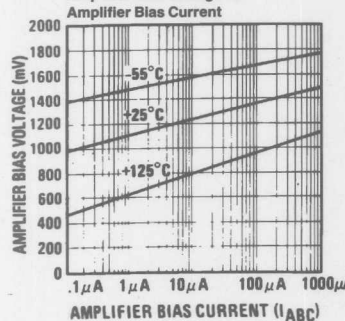
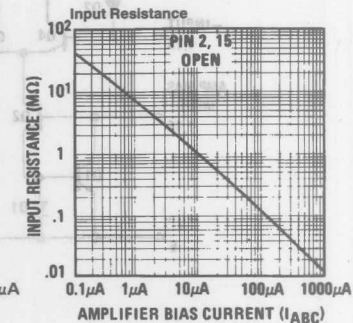
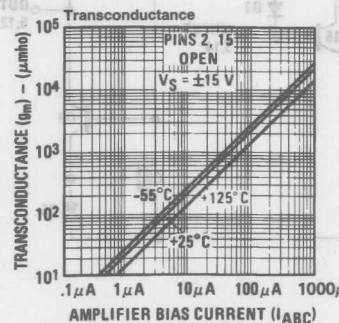
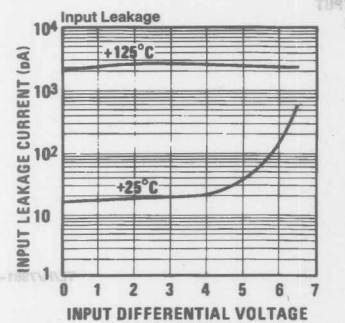
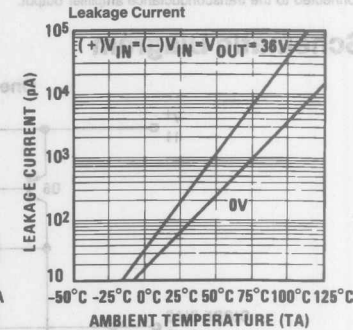
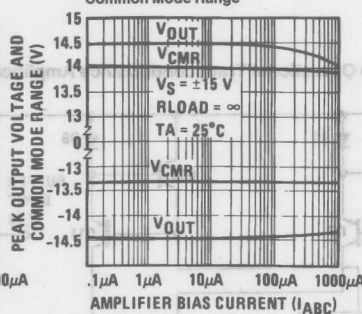
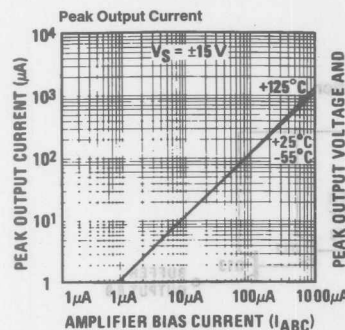
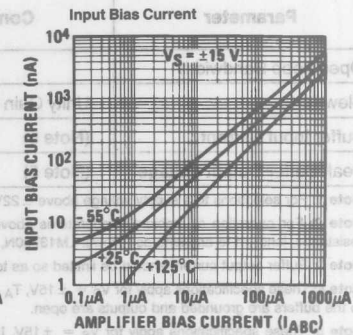
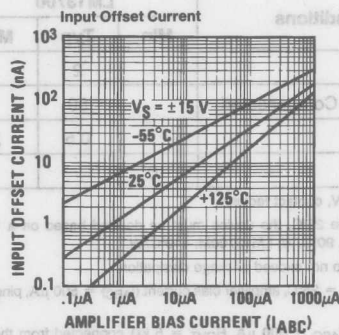
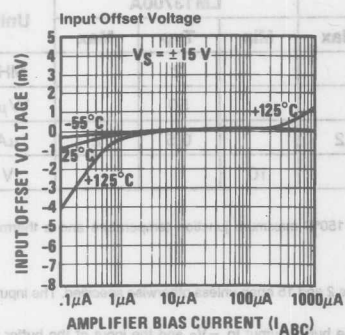
Note 4: These specifications apply for $V_S = \pm 15$ V, $T_A = 25^{\circ}\text{C}$, amplifier bias current (I_{ABC}) = $500\ \mu\text{A}$, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5: These specifications apply for $V_S = \pm 15$ V, $I_{ABC} = 500\ \mu\text{A}$, $R_{OUT} = 5\ \text{k}\Omega$ connected from the buffer output to $-V_S$ and the input of the buffer is connected to the transconductance amplifier output.

Schematic Diagram

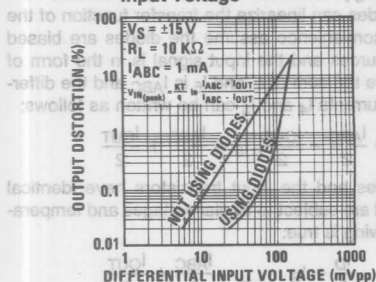


Typical Performance Characteristics

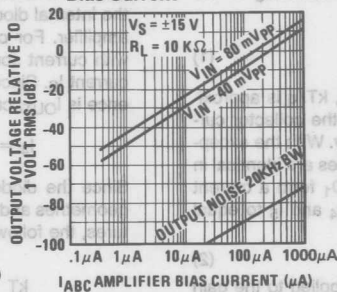


Typical Performance Characteristics (Continued)

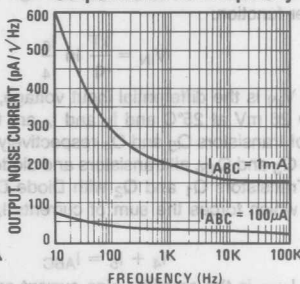
Distortion vs Differential Input Voltage



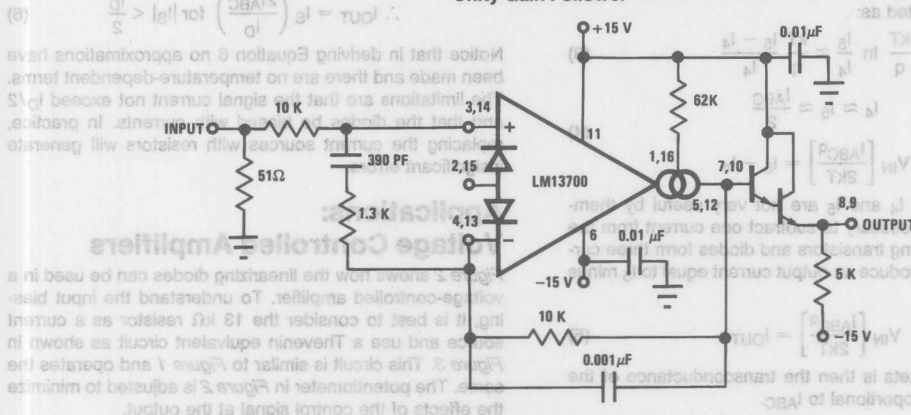
Voltage vs Amplifier Bias Current



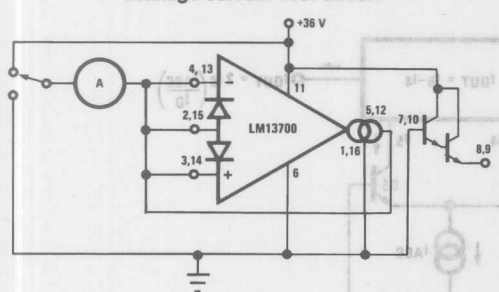
Output Noise vs Frequency



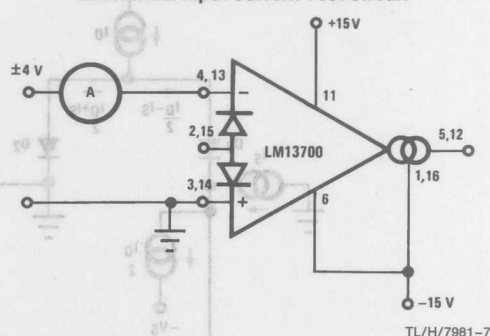
Unity Gain Follower



Leakage Current Test Circuit



Differential Input Current Test Circuit



Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{kT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, kT/q is approximately 26 mV at 25°C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13} , all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC} :

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{kT}{q} \ln \frac{I_5}{I_4} \approx \frac{kT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2} \quad (4)$$

$$V_{IN} \left[\frac{I_{ABC} q}{2kT} \right] = I_5 - I_4$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC} q}{2kT} \right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC} .

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S . Since the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT} , currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{kT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{kT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}}$$

$$\therefore I_{OUT} = I_S \left(\frac{2I_{ABC}}{I_D} \right) \text{ for } |I_S| < \frac{I_D}{2} \quad (6)$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature-dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Applications:

Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage-controlled amplifier. To understand the input biasing, it is best to consider the 13 kΩ resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

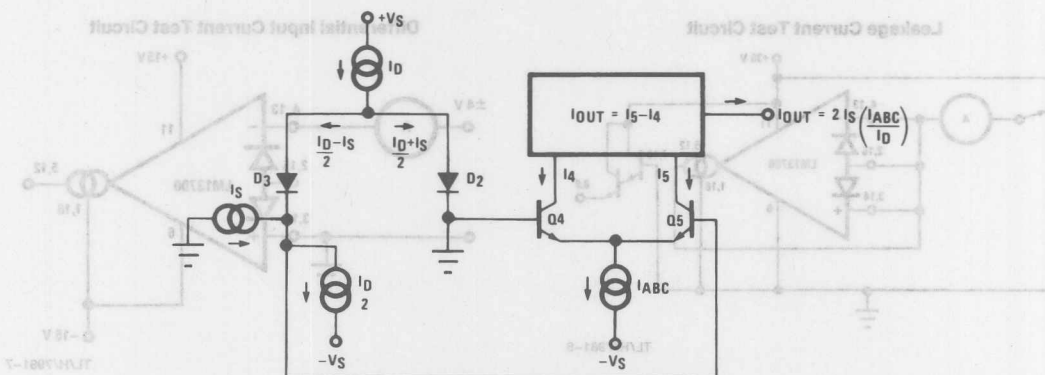


FIGURE 1. Linearizing Diodes

TL/H/7981-8

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2) until the output

distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L .

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_d) and maximizes their linearizing action when balanced against R_{IN} . A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

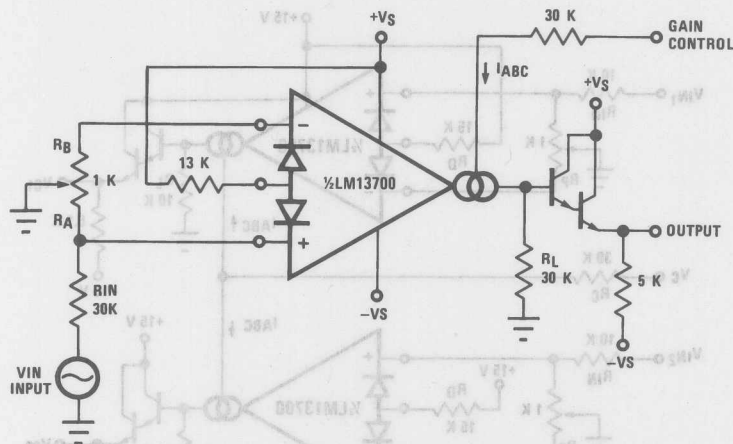


FIGURE 2. Voltage Controlled Amplifier

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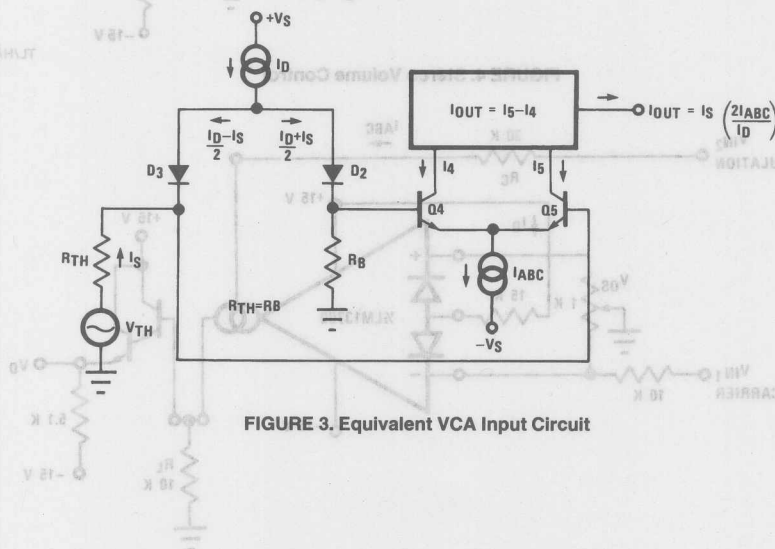


FIGURE 3. Equivalent VCA Input Circuit

TL/H/7981-10

Stereo Volume Control

The circuit of *Figure 4* uses the excellent matching of the two LM13700 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. R_p is provided to minimize the output offset voltage and may be replaced with two 510 Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived for *Figure 2* as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

If V_C is derived from a second signal source then the circuit becomes an amplitude modulator or two-quadrant multiplier as shown in *Figure 5*, where:

$$I_O = \frac{-2I_S}{I_D} (I_{ABC}) = \frac{-2I_S}{I_D} \frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D} \frac{(V^- + 1.4V)}{R_C}$$

The constant term in the above equation may be cancelled by feeding $I_S \times I_D R_C / 2(V^- + 1.4V)$ into I_O . The circuit of *Figure 6* adds R_M to provide this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O .

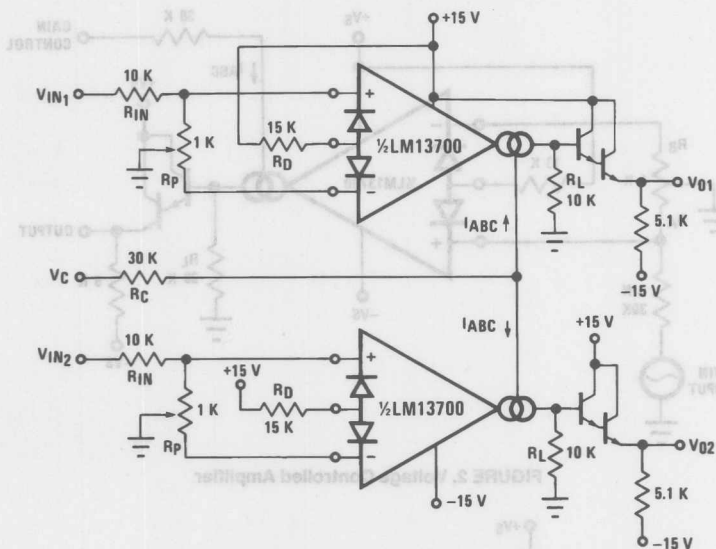


FIGURE 4. Stereo Volume Control

TL/H/7981-11

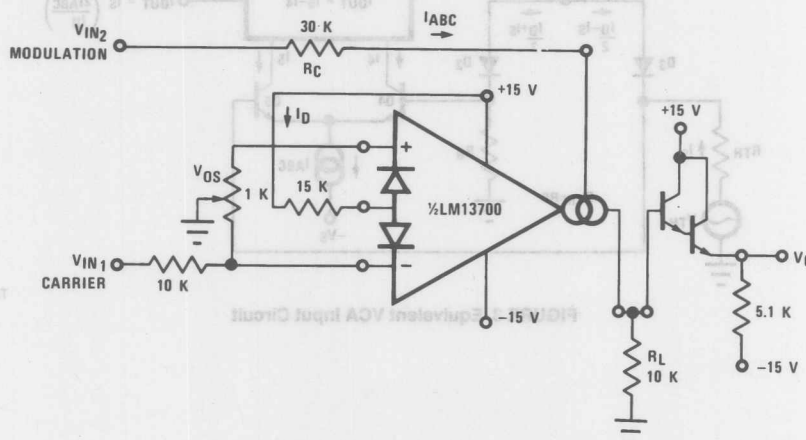


FIGURE 5. Amplitude Modulator

TL/H/7981-12

Stereo Volume Control (Continued)

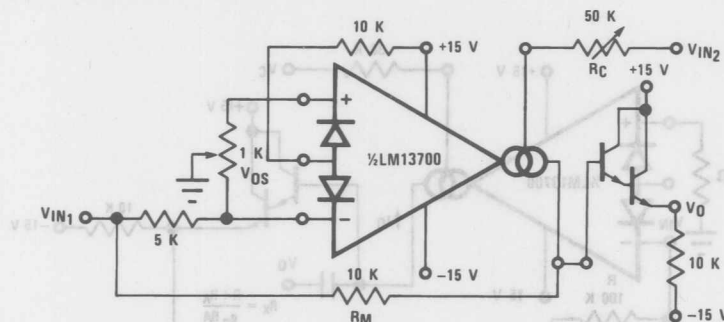


FIGURE 6. Four-Quadrant Multiplier

TL/H/7981-13

Noting that the gain of the LM13700 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC} , Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude (3 V_{BE}) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN}

to the LM13700 which is then multiplied by the g_m of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{g_m R_A}$$

where $g_m \approx 19.2 I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13700 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR is shown in Figure 10, where each "end" of the "resistor" may be at any voltage within the output voltage range of the LM13700.

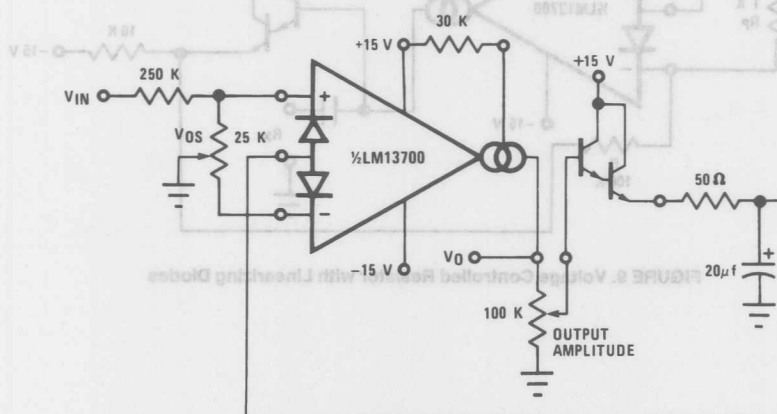


FIGURE 7. AGC Amplifier

TL/H/7981-14

Voltage Controlled Resistors (Continued)

Stereo Volume Control (Continued)

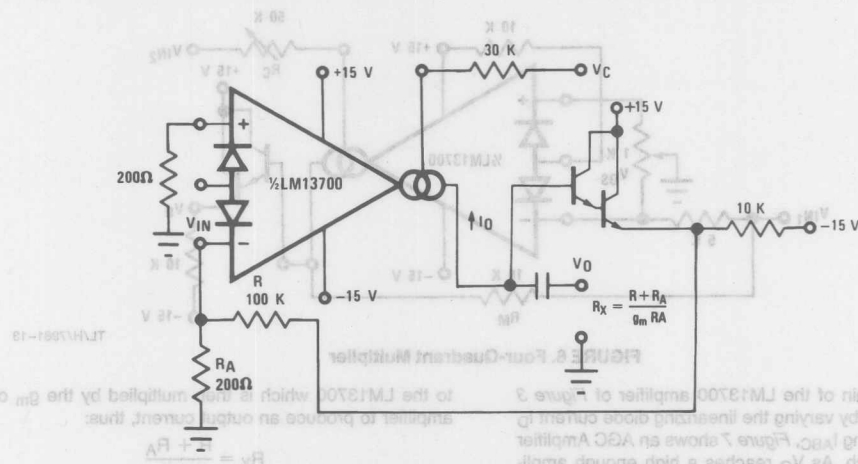


FIGURE 8. Voltage Controlled Resistor, Single-Ended

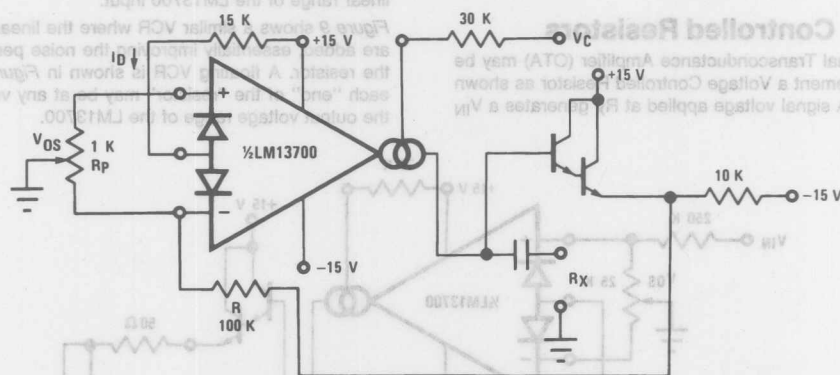


FIGURE 9. Voltage Controlled Resistor with Linearizing Diodes

TL/H/7981-16

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13700 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter of Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/g_m equals the closed-loop gain of (R/R_A) . At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation, where g_m is again $19.2 \times I_{ABC}$ at room temperature. Figure

12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent g_m tracking of the two amplifiers, these filters perform well over several decades of frequency.

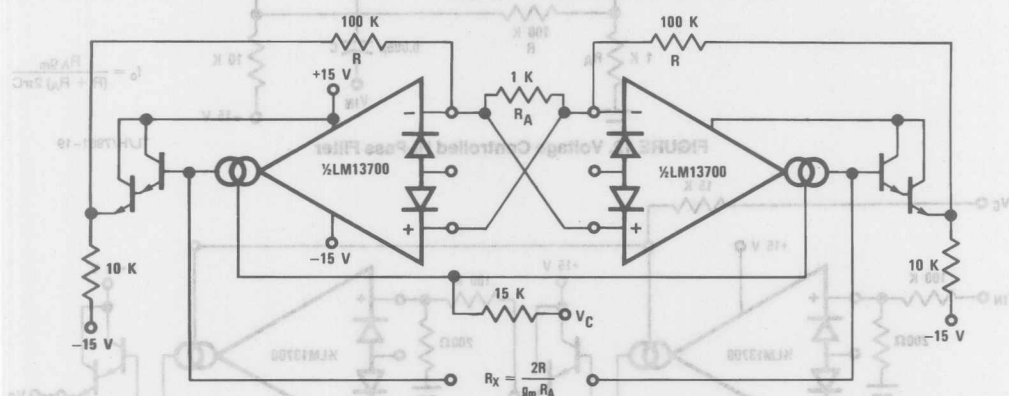


FIGURE 10. Floating Voltage Controlled Resistor

TL/H/7981-17

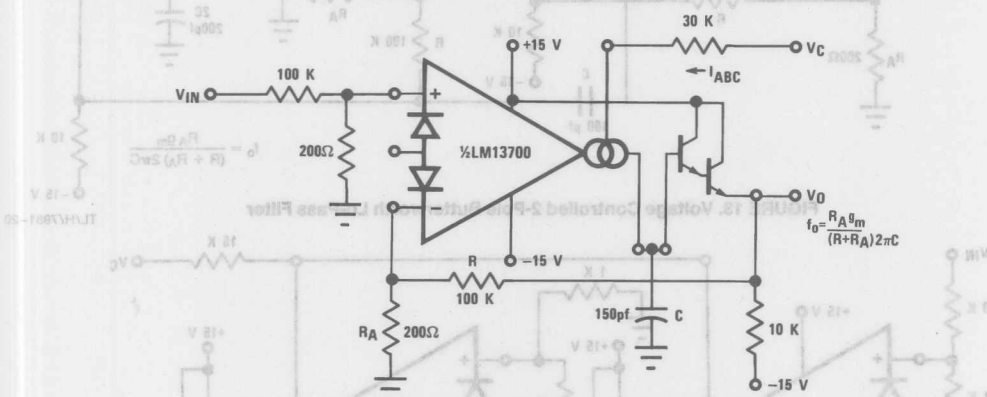


FIGURE 11. Voltage Controlled Low-Pass Filter

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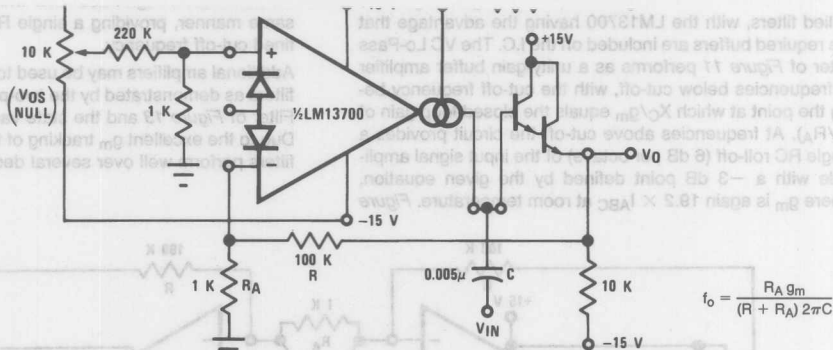


FIGURE 12. Voltage Controlled Hi-Pass Filter

TL/H/7981-19

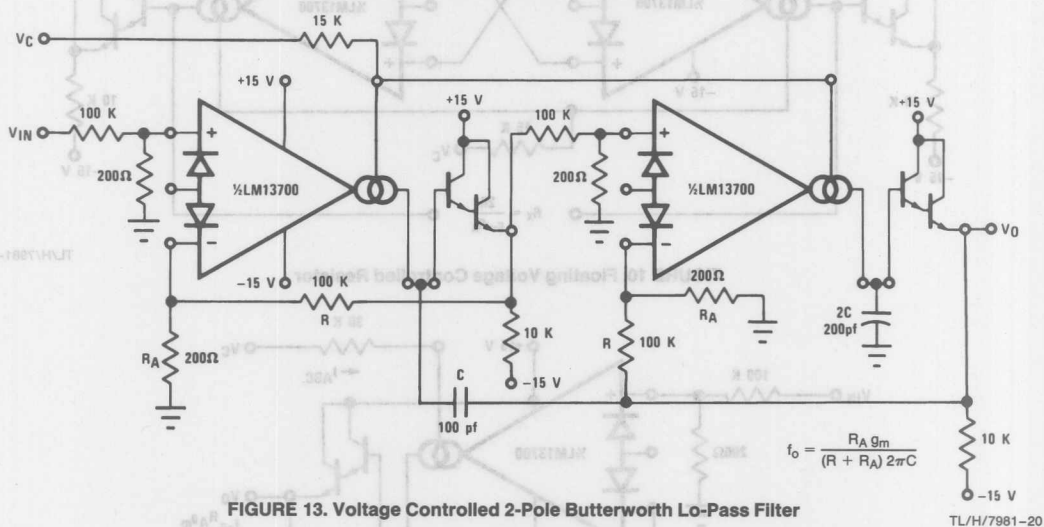


FIGURE 13. Voltage Controlled 2-Pole Butterworth Lo-Pass Filter

TL/H/7981-20

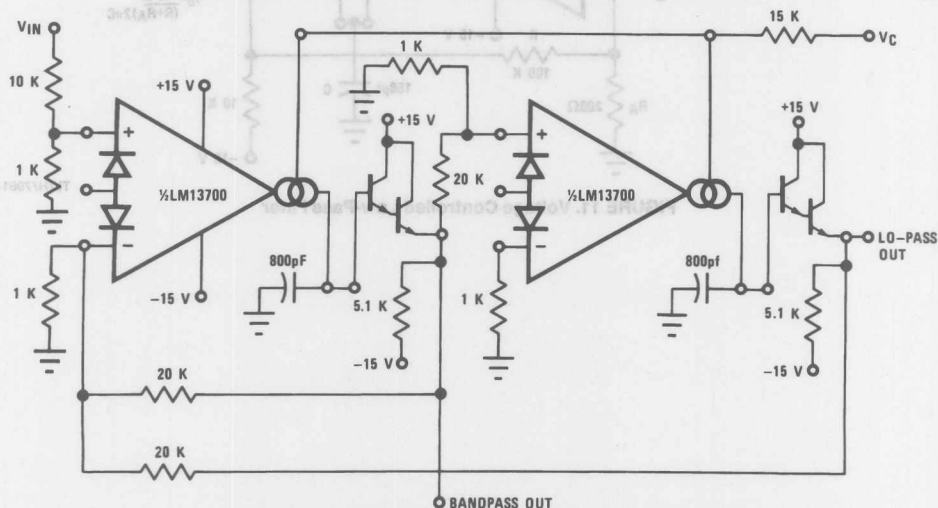


FIGURE 14. Voltage Controlled State Variable Filter

TL/H/7981-21

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13700. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1 mA to 10 nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5V to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to

increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C .

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two LM13700 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

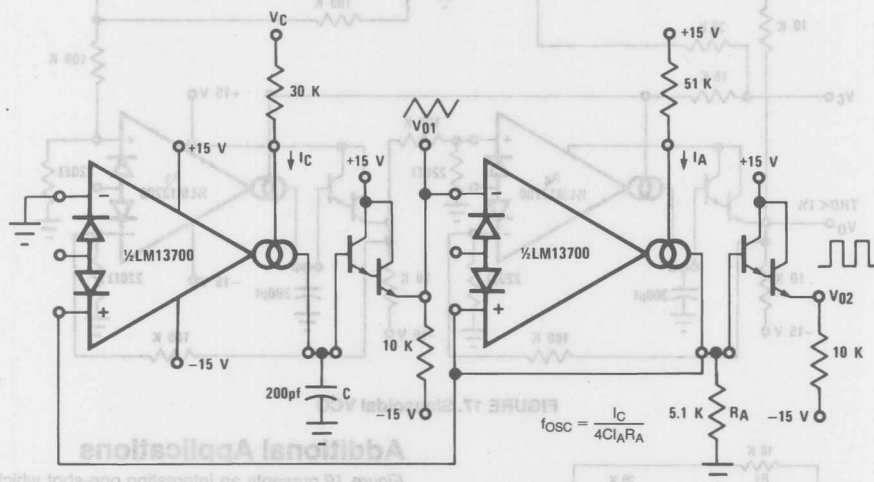


FIGURE 15. Triangular/Square-Wave VCO

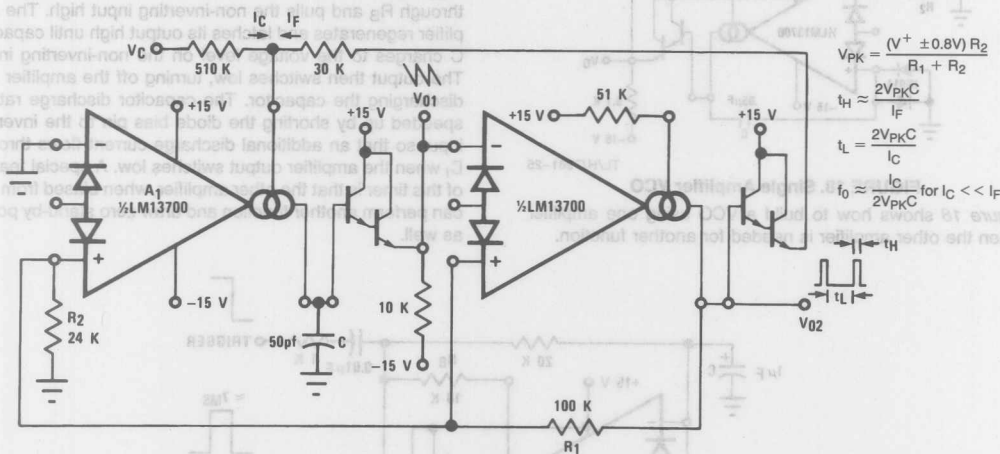


FIGURE 16. Ramp/Pulse VCO

Voltage Controlled Oscillators (Continued)

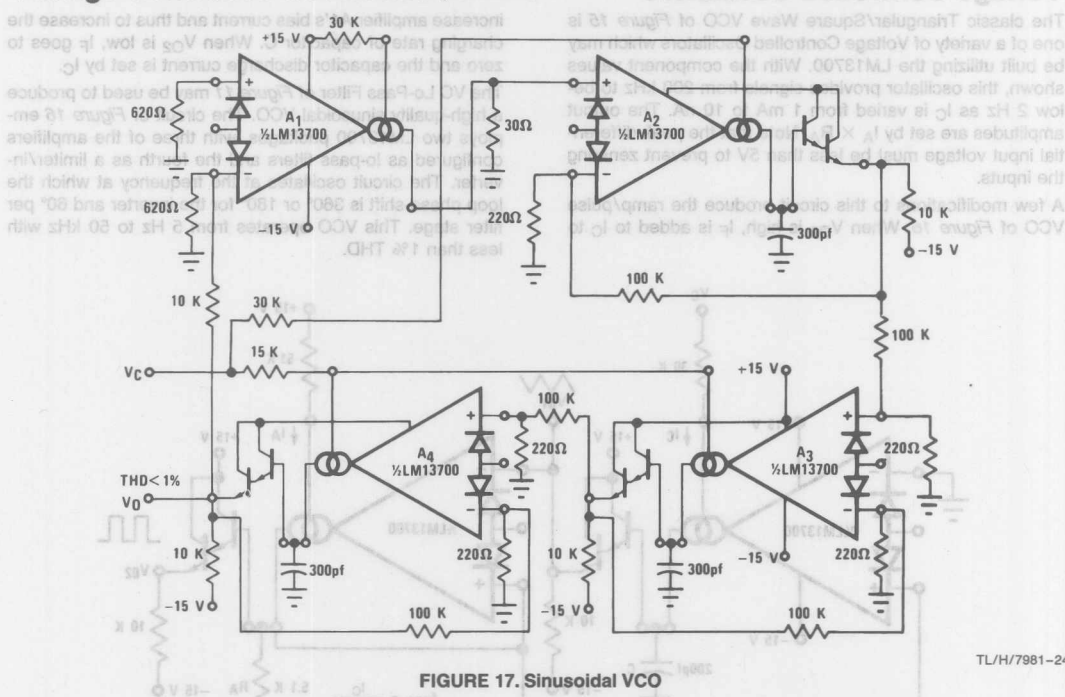


FIGURE 17. Sinusoidal VCO

TL/H/7981-24

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_0 , can perform another function and draw zero stand-by power as well.

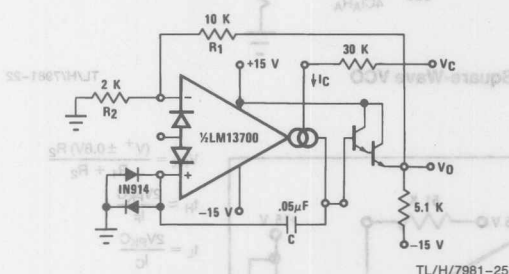


FIGURE 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

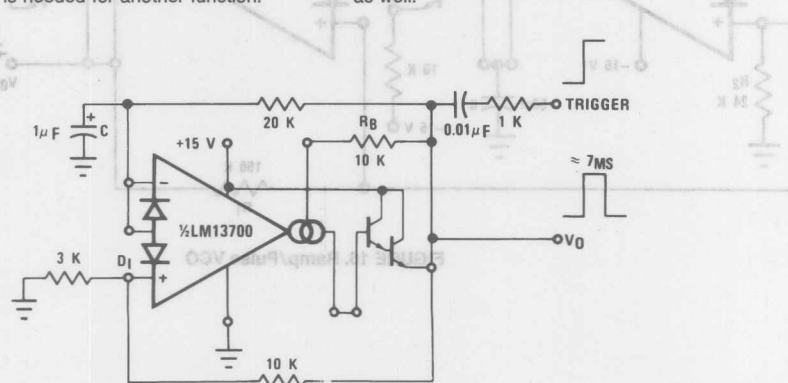


FIGURE 19. Zero Stand-By Power Timer

TL/H/7981-26

Additional Applications (Continued)

The operation of the multiplexer of Figure 20 is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O . C_C and R_C serve to stabilize the unity-gain configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 kHz by the LM13700 slew rate into 150 pF when the $(V_{IN1}-V_{IN2})$ differential is at its maximum allowable value of 5V.

The Peak Detector of Figure 21 uses the four-quadrant multiplier of Figure 6 and the VCO of Figure 18 to produce a PLL with a $\pm 5\%$ hold-in range and an input sensitivity of about 300 mV.

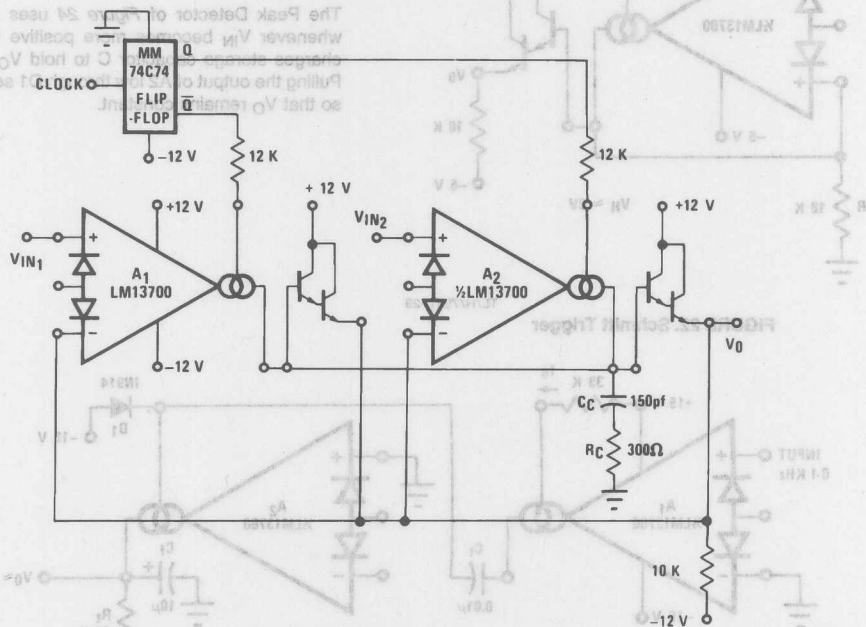


FIGURE 20. Multiplexer

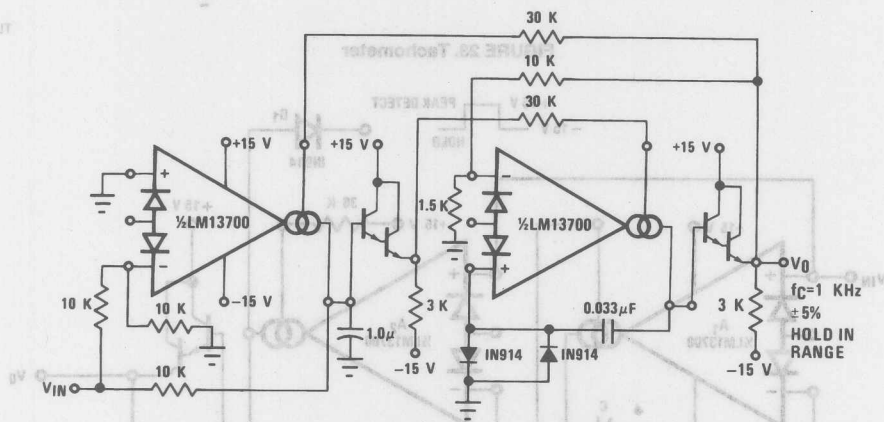


FIGURE 21. Phase Lock Loop

Additional Applications (Continued)

The Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

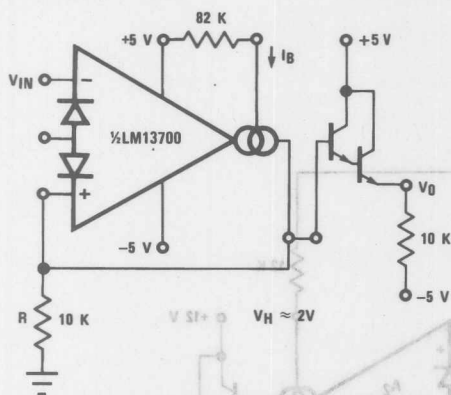


FIGURE 22. Schmitt Trigger

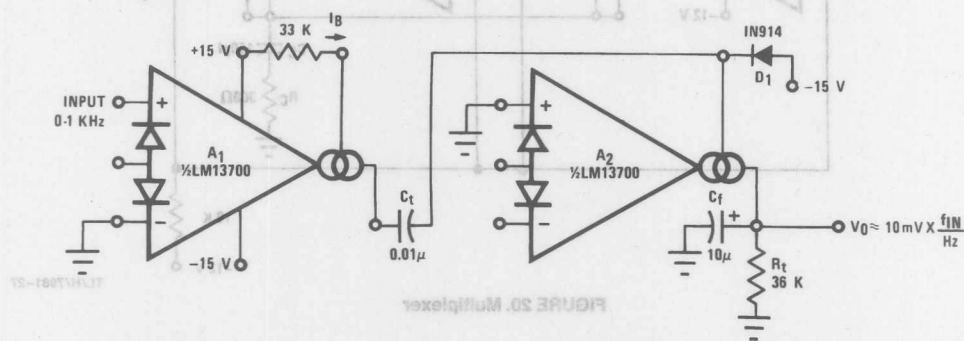


FIGURE 23. Tachometer

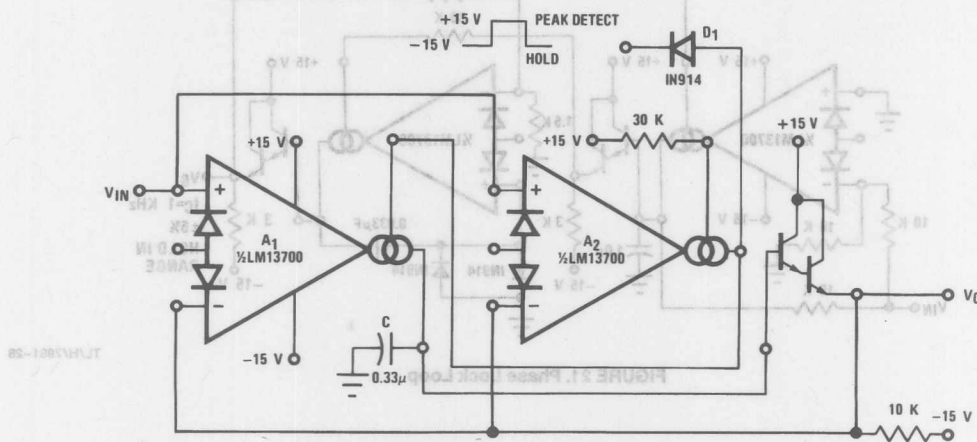


FIGURE 24. Peak Detector and Hold Circuit

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L) C_t$ is sourced into C_t and R_t . This once per cycle charge is then balanced by the current of V_O/R_t . The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B , where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13700. D1 is added to provide a discharge path for C_t when A1 switches low. The Peak Detector of Figure 24 uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O . A1 then charges storage capacitor C to hold V_O equal to V_{IN} PK. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

Additional Applications (Continued)

The Ramp-and-Hold of Figure 26 sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true-RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attenuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

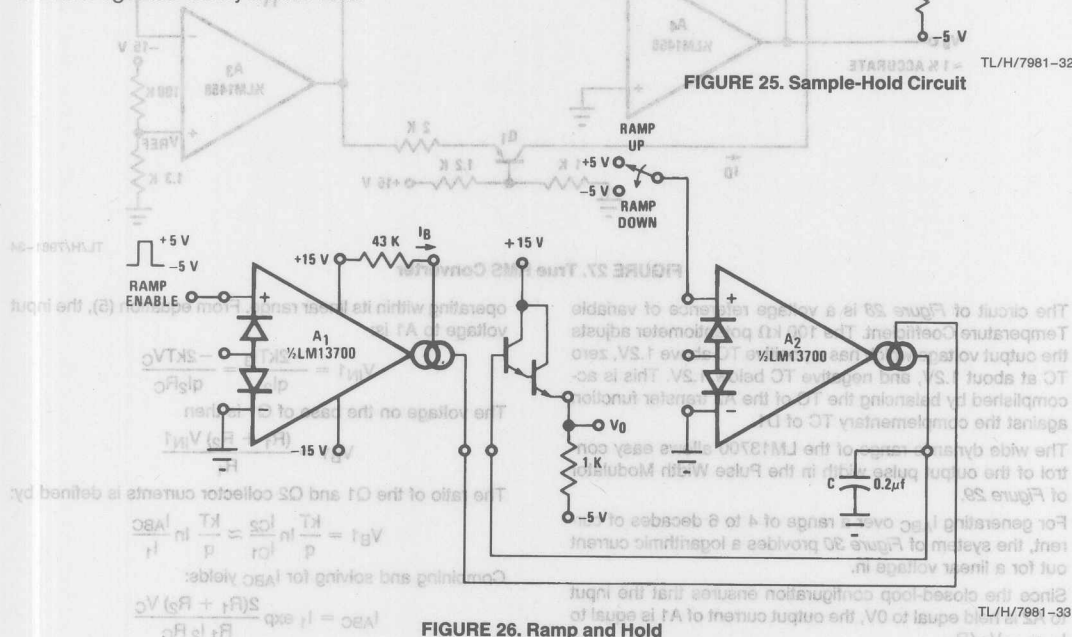


FIGURE 26. Ramp and Hold

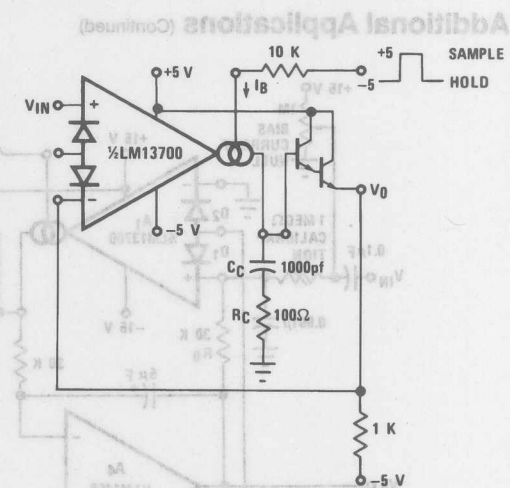


FIGURE 25. Sample-Hold Circuit

Additional Applications (Continued)

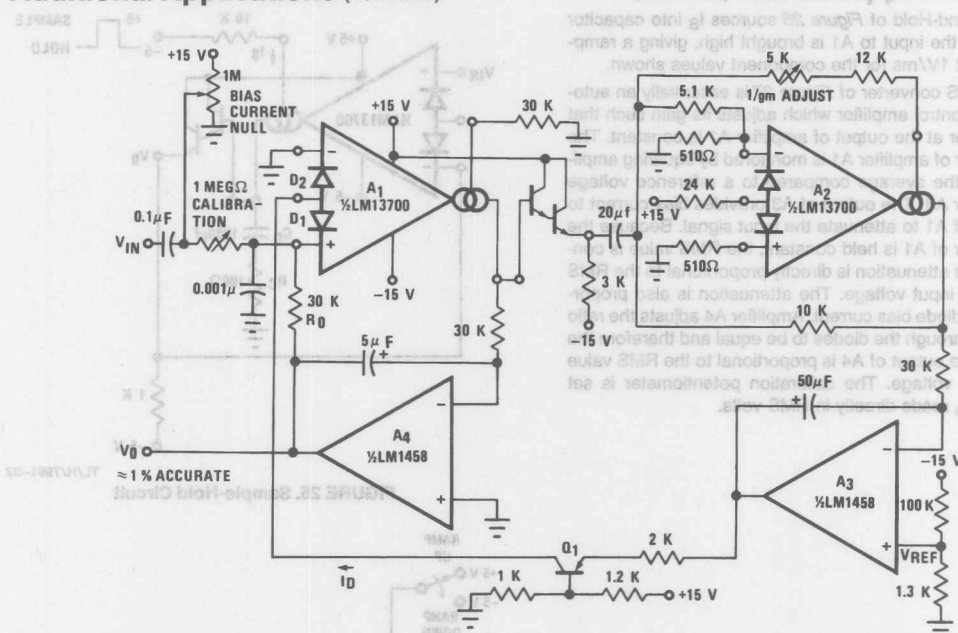


FIGURE 27. True RMS Converter

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The circuit of Figure 28 is a voltage reference of variable Temperature Coefficient. The 100 kΩ potentiometer adjusts the output voltage which has a positive TC above 1.2V, zero TC at about 1.2V, and negative TC below 1.2V. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The wide dynamic range of the LM13700 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 29.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 30 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be

operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN1} = \frac{-2kT I_3}{q I_2} = \frac{-2kT V_C}{q I_2 R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1 + R_2) V_{IN1}}{R_1}$$

The ratio of the Q1 and Q2 collector currents is defined by:

$$V_{B1} = \frac{kT}{q} \ln \frac{I_{C2}}{I_{C1}} \approx \frac{kT}{q} \ln \frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_1 \exp \frac{2(R_1 + R_2) V_C}{R_1 I_2 R_C}$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

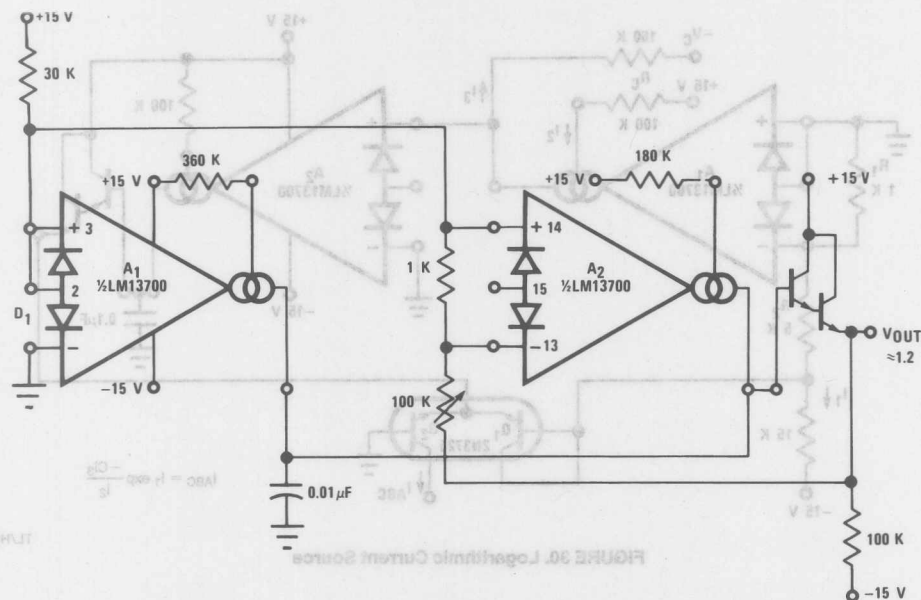


FIGURE 28. Delta VBE Reference

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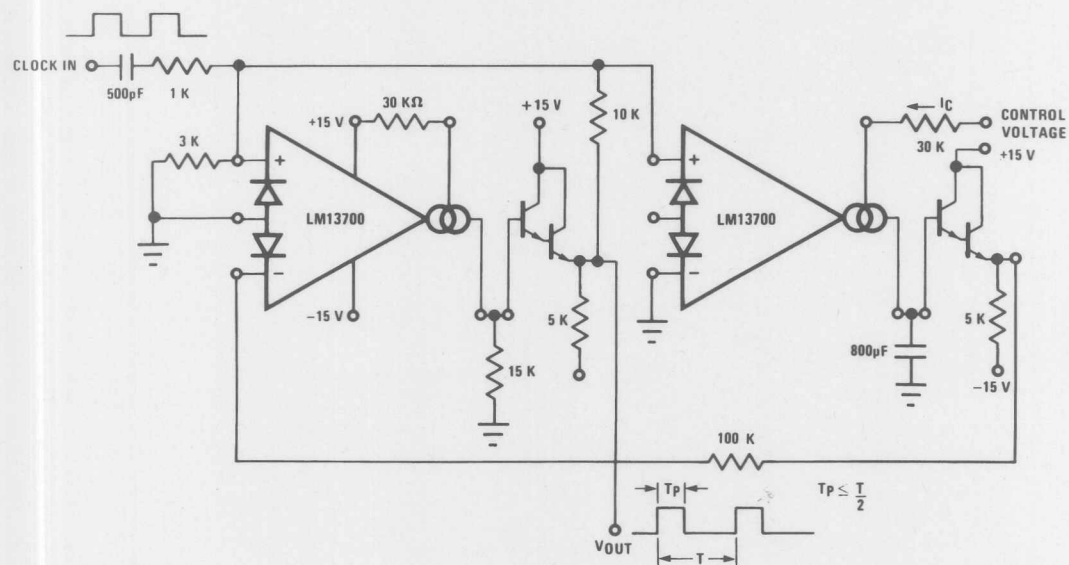


FIGURE 29. Pulse Width Modulator

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Additional Applications (Continued)

(Continued) Additional Applications

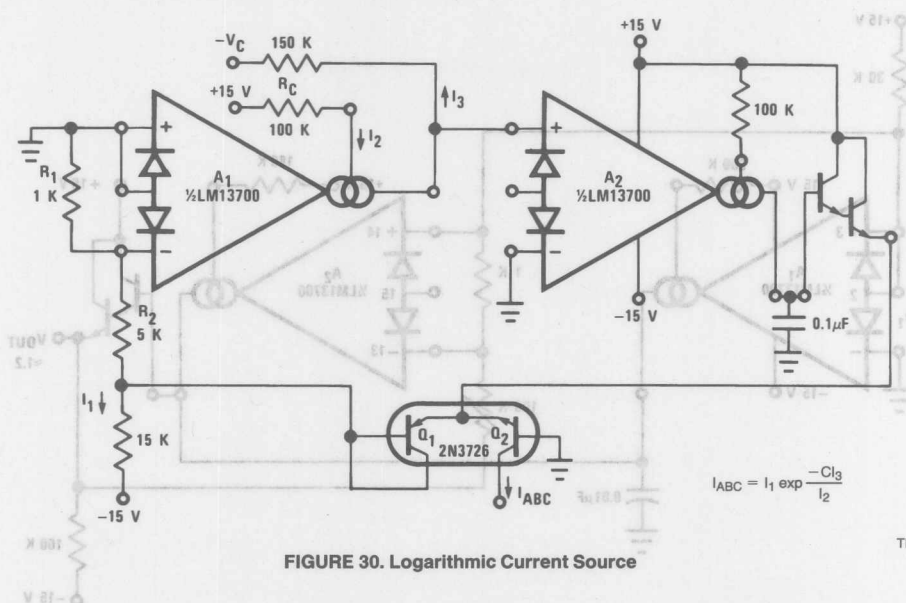


FIGURE 30. Logarithmic Current Source

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FIGURE 31. Delta VBE Reference

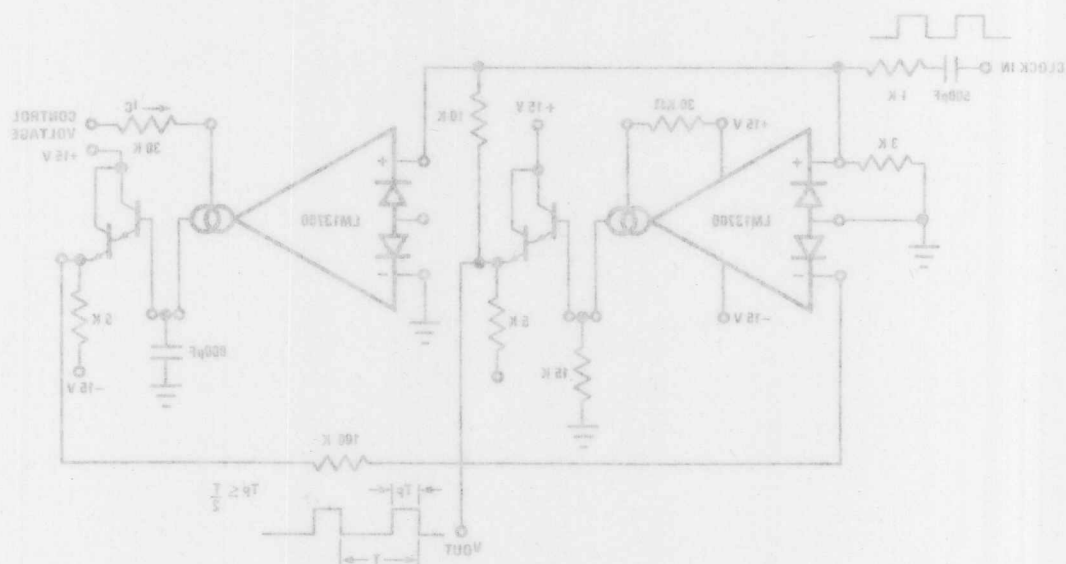
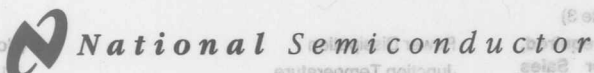


FIGURE 32. Pulse Width Modulator

TL/H/7981-39



LMC660 **CMOS Quad Operational Amplifier**

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS} , drift, and broadband noise as well as voltage gain into realistic loads (2 k Ω and 600 Ω) are all equal to, or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Features

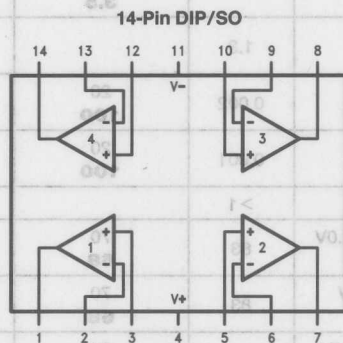
- Rail-to-rail output swing
- Specified for 2 k Ω and 600 Ω loads
- High voltage gain
- Low input offset voltage

- Low offset voltage drift
- Ultra low input bias current
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- $I_{SS} = 375 \mu A/\text{amplifier}$; independent of V^+
- Low distortion
- Slow rate
- Available in extended temperature range ($-40^\circ C$ to $+125^\circ C$); ideal for automotive applications
- Available to Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-Hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram



Ordering Information

| Package | Temperature Range | | | | NSC Drawing | Transport Media |
|---------------------------------|---|---|--|--|-------------|-----------------------|
| | Military $-55^\circ C$ to $+125^\circ C$ | Extended $-40^\circ C$ to $+125^\circ C$ | Industrial $-40^\circ C$ to $+85^\circ C$ | Commercial $0^\circ C$ to $+70^\circ C$ | | |
| 14-Pin Ceramic DIP | LMC660AMJ/883 | | | | J14A | Rail |
| 14-Pin Small Outline | | LMC660EM | LMC660AIM | LMC660CM | M14A | Rail Tape and Reel |
| 14-Pin Molded DIP | | LMC660ENS | LMC660AIN | LMC660CN | N14A | Rail |
| 14-Pin Side Braided Ceramic DIP | LMC660AMD | | | | D14E | Rail |

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--|
| Differential Input Voltage | ± Supply Voltage |
| Supply Voltage | 16V |
| Output Short Circuit to V ⁺ | (Note 12) |
| Output Short Circuit to V ⁻ | (Note 1) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Voltage at Input/Output Pins | (V ⁺) + 0.3V, (V ⁻) - 0.3V |
| Current at Output Pin | ± 18 mA |
| Current at Input Pin | ± 5 mA |
| Current at Power Supply Pin | 35 mA |

| | |
|------------------------|----------|
| Power Dissipation | (Note 2) |
| Junction Temperature | 150°C |
| ESD tolerance (Note 8) | 1000V |

Operating Ratings

| | |
|----------------------|---------------------------------|
| Temperature Range | |
| LMC660AMJ/883, | -55°C ≤ T _J ≤ +125°C |
| LMC660AMD | -40°C ≤ T _J ≤ +85°C |
| LMC660AI | 0°C ≤ T _J ≤ +70°C |
| LMC660C | -40°C ≤ T _J ≤ +125°C |
| LMC660E | |
| Supply Voltage Range | 4.75V to 15.5V |

Power Dissipation (Note 10)

| | |
|---|---------|
| Thermal Resistance (θ _{JA}) (Note 11) | |
| 14-Pin Ceramic DIP | 90°C/W |
| 14-Pin Molded DIP | 85°C/W |
| 14-Pin SO | 115°C/W |
| 14-Pin Side Brazed Ceramic DIP | 90°C/W |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L ≥ 1M unless otherwise specified.

| Parameter | Conditions | Typ (Note 4) | LMC660AMD LMC660AMJ/883 | LMC660AI | LMC660C | LMC660E | Units |
|--|--|----------------------|--|--|--|--|-------------|
| | | | Limit (Notes 4, 9) | Limit (Note 4) | Limit (Note 4) | Limit (Note 4) | |
| Input Offset Voltage | | 1 | 3 3.5 | 3 3.3 | 6 6.3 | 6 6.5 | mV max |
| Input Offset Voltage Average Drift | | 1.3 | | | | | μV/°C |
| Input Bias Current | | 0.002 | 20 100 | 4 | 2 | 60 | pA max |
| Input Offset Current | | 0.001 | 20 100 | 2 | 1 | 60 | pA max |
| Input Resistance | | > 1 | | | | | TeraΩ |
| Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 83 | 70 68 | 70 68 | 63 62 | 63 60 | dB min |
| Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 83 | 70 68 | 70 68 | 63 62 | 63 60 | dB min |
| Negative Power Supply Rejection Ratio | 0V ≤ V ⁻ ≤ -10V | 94 | 84 82 | 84 83 | 74 73 | 74 70 | dB min |
| Input Common-Mode Voltage Range | V ⁺ = 5V & 15V For CMRR ≥ 50 dB | -0.4 | -0.1 0 | -0.1 0 | -0.1 0 | -0.1 0 | V max |
| | | V ⁺ - 1.9 | V ⁺ - 2.3 V⁺ - 2.6 | V ⁺ - 2.3 V⁺ - 2.5 | V ⁺ - 2.3 V⁺ - 2.4 | V ⁺ - 2.3 V⁺ - 2.6 | V min |
| Large Signal Voltage Gain | R _L = 2 kΩ (Note 5) Sourcing | 2000 | 400 300 | 440 400 | 300 200 | 200 100 | V/mV min |
| | | 500 | 180 70 | 180 120 | 90 80 | 90 40 | V/mV min |
| | R _L = 600Ω (Note 5) Sourcing | 1000 | 200 150 | 220 200 | 150 100 | 100 75 | V/mV min |
| | | 250 | 100 35 | 100 60 | 50 40 | 50 20 | V/mV min |

| Parameter | Conditions | Typ (Note 4) | LMC660AMD LMC660AMJ/883 | LMC660AI | LMC660C | LMC660E | Units |
|-------------------------------|--|-----------------|----------------------------|-----------------------|-----------------------|-----------------------|-----------|
| | | | Limit (Notes 4, 9) | Limit (Note 4) | Limit (Note 4) | Limit (Note 4) | |
| Output Swing | $V^+ = 5V$ $R_L = 2\text{ k}\Omega$ to $V^+ / 2$ | 4.87 | 4.82 4.77 | 4.82 4.79 | 4.78 4.76 | 4.78 4.70 | V min |
| | | | 0.15 0.19 | 0.15 0.17 | 0.19 0.21 | 0.19 0.25 | V max |
| | $V^+ = 5V$ $R_L = 600\Omega$ to $V^+ / 2$ | 4.61 | 4.41 4.24 | 4.41 4.31 | 4.27 4.21 | 4.27 4.10 | V min |
| | | | 0.50 0.63 | 0.50 0.56 | 0.63 0.69 | 0.63 0.75 | V max |
| | $V^+ = 15V$ $R_L = 2\text{ k}\Omega$ to $V^+ / 2$ | 14.63 | 14.50 14.40 | 14.50 14.44 | 14.37 14.32 | 14.37 14.25 | V min |
| | | | 0.35 0.43 | 0.35 0.40 | 0.44 0.48 | 0.44 0.55 | V max |
| | | 13.90 | 13.35 13.02 | 13.35 13.15 | 12.92 12.76 | 12.92 12.60 | V min |
| | | | 1.16 1.42 | 1.16 1.32 | 1.45 1.58 | 1.45 1.75 | V max |
| Output Current $V^+ = 5V$ | Sourcing, $V_O = 0V$ | 22 | 16 12 | 16 14 | 13 11 | 13 9 | mA min |
| | | 21 | 16 12 | 16 14 | 13 11 | 13 9 | mA min |
| | Sinking, $V_O = 5V$ | 21 | 16 12 | 16 14 | 13 11 | 13 9 | mA min |
| | | 21 | 16 12 | 16 14 | 13 11 | 13 9 | mA min |
| Output Current $V^+ = 15V$ | Sourcing, $V_O = 0V$ | 40 | 19 19 | 28 25 | 23 21 | 23 15 | mA min |
| | | 39 | 19 19 | 28 24 | 23 20 | 23 15 | mA min |
| | Sinking, $V_O = 13V$ (Note 12) | 39 | 19 19 | 28 24 | 23 20 | 23 15 | mA min |
| | | 39 | 19 19 | 28 24 | 23 20 | 23 15 | mA min |
| Supply Current | All Four Amplifiers $V_O = 1.5V$ | 1.5 | 2.2 2.9 | 2.2 2.6 | 2.7 2.9 | 2.7 3.0 | mA max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Parameter | Conditions | Typ (Note 4) | LMC660AMD LMC660AMJ/883 | LMC660AI | LMC660C | LMC660E | Units |
|------------------------------|---|-----------------|----------------------------|-------------------|-------------------|-------------------|-------------------------------|
| | | | Limit (Notes 4, 9) | Limit (Note 4) | Limit (Note 4) | Limit (Note 4) | |
| Slew Rate | (Note 6) | 1.1 | 0.8 0.5 | 0.8 0.6 | 0.8 0.7 | 0.8 0.4 | $\text{V}/\mu\text{s}$ min |
| Gain-Bandwidth Product | | 1.4 | 0.5 | | | | MHz |
| Phase Margin | | 50 | | | | | Deg |
| Gain Margin | | 17 | | | | | dB |
| Amp-to-Amp Isolation | (Note 7) | 130 | | | | | dB |
| Input Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | | | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Input Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{PP}$ $V^+ = 15\text{V}$ | 0.01 | | | | | % |

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 6: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15\text{V}$ and $R_L = 10\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{PP}$.

Note 8: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

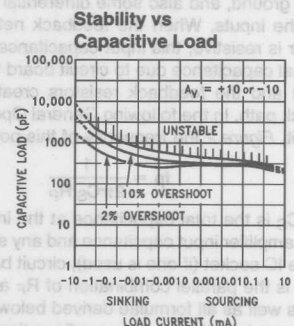
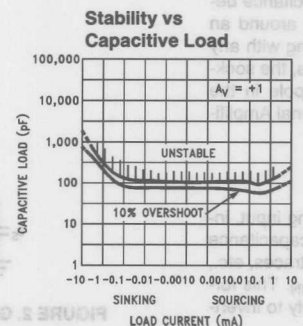
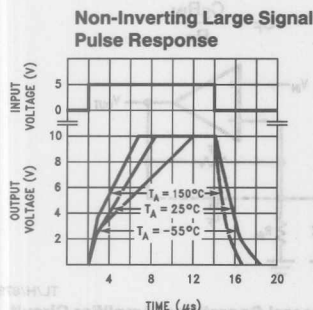
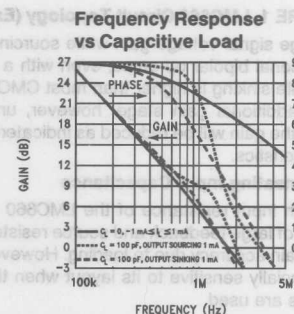
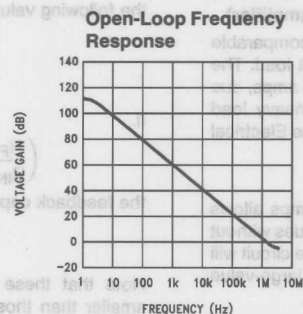
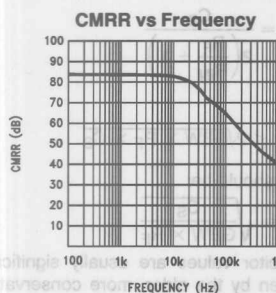
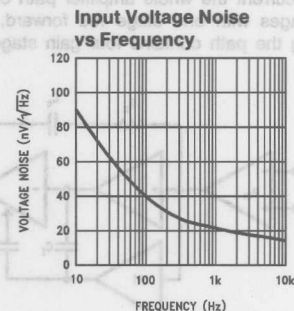
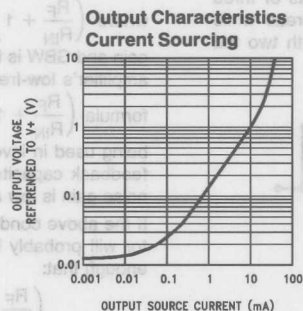
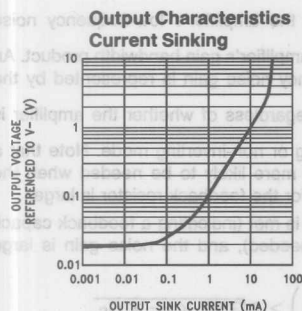
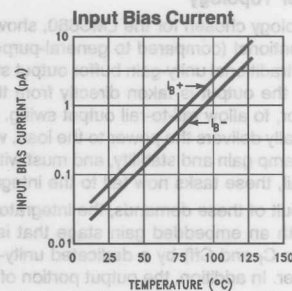
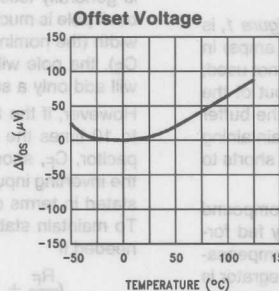
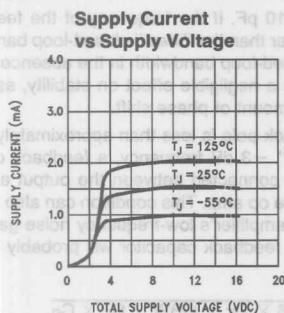
Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC660AMJ/883 RETS spec complied fully with the boldface limits in this column. The LMC660AMJ/883 may also be procured to a Standard Military Drawing specification.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified



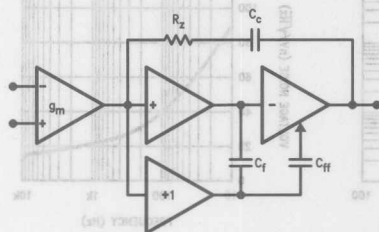
Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Application Hints

Amplifier Topology

The topology chosen for the LMC660, shown in Figure 1, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_F and C_{FF}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



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FIGURE 1. LMC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC660 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, Figure 2 the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN} . This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S

is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" -3 dB frequency, a feedback capacitor, C_F , should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times \text{GBW} \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{\text{GBW} \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

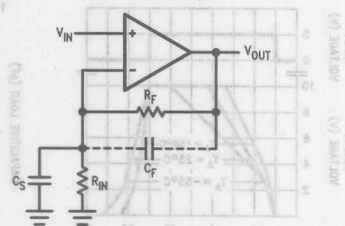
$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{\text{GBW} \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{\text{GBW} \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



TL/H/8767-6

FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

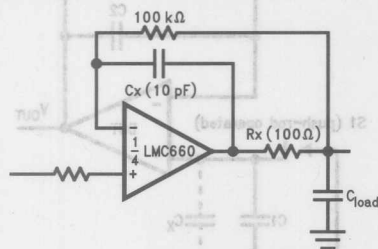
Application Hints (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

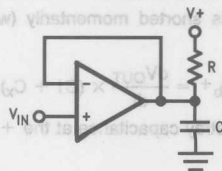
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 3a, the addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



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FIGURE 3a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 3b). Typically a pull up resistor conducting 500 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



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FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC660, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 4. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10¹² Ω , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10¹¹ Ω would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 5a, 5b, 5c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 5d.

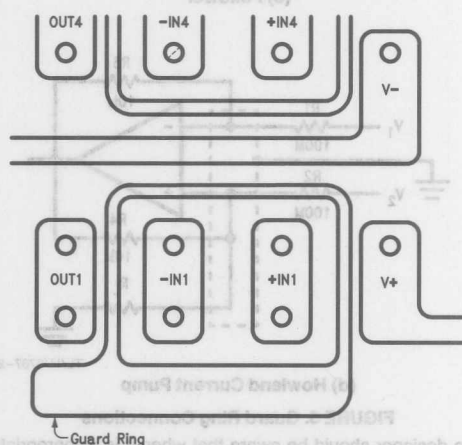
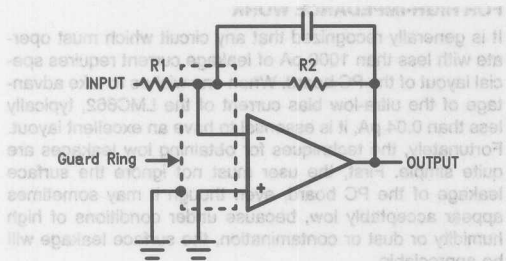


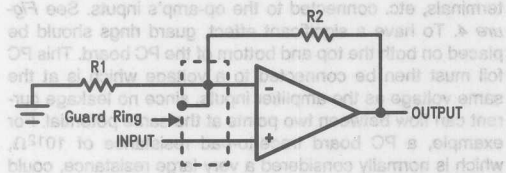
FIGURE 4. Example, using the LMC660, of Guard Ring in P.C. Board Layout

TL/H/8767-16



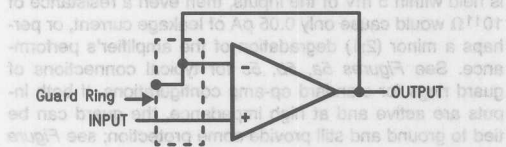
TL/H/8767-17

(a) Inverting Amplifier



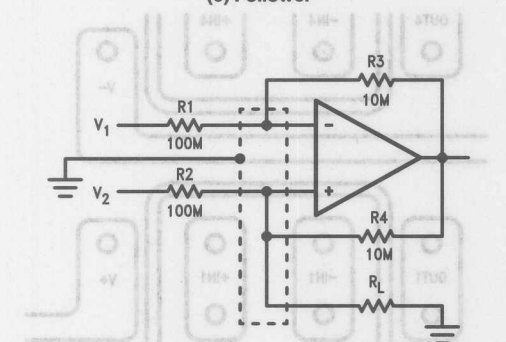
TL/H/8767-18

(b) Non-Inverting Amplifier



TL/H/8767-19

(c) Follower



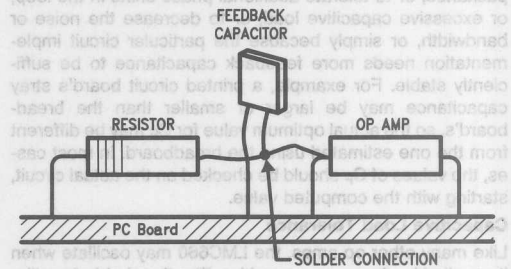
TL/H/8767-20

(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may

struction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 6.



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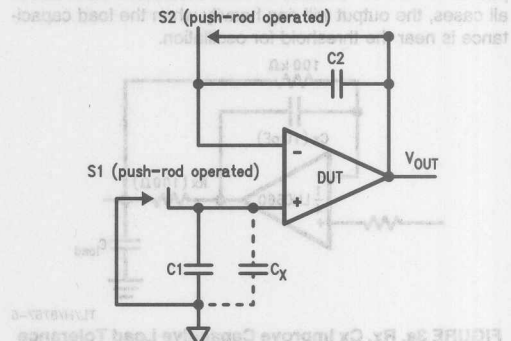
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 7 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b^- = \frac{dV_{OUT}}{dt} \times C_2$$



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FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b^- , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

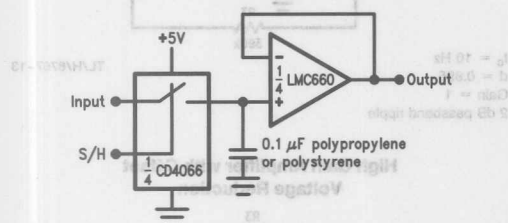
$$I_b^+ = \frac{dV_{OUT}}{dt} \times (C_1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0 \text{ VDC}$)

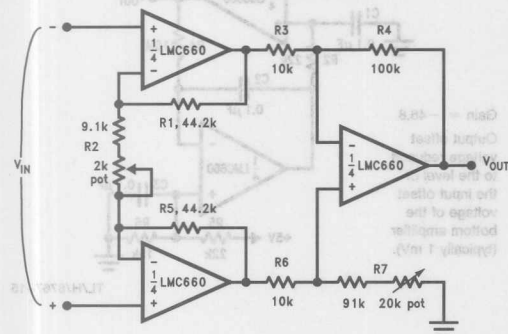
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



TL/H/8767-7

Instrumentation Amplifier



TL/H/8767-8

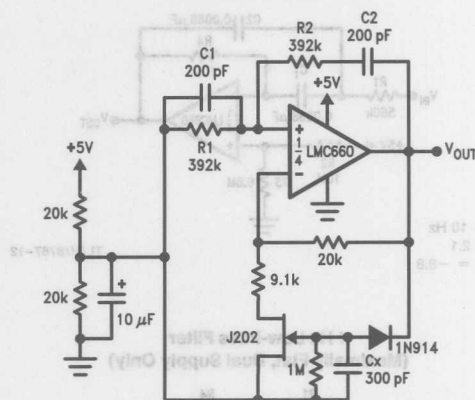
If $R1 = R5$, $R3 = R6$, and $R4 = R7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_v \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of $R3$ to $R6$ and $R4$ to $R7$ affect CMRR. Gain may be adjusted through $R2$. CMRR may be adjusted through $R7$.

Sine-Wave Oscillator



TL/H/8767-9

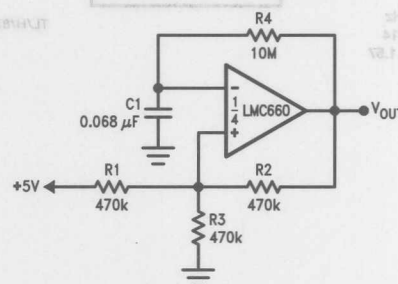
Oscillator frequency is determined by $R1$, $R2$, $C1$, and $C2$:

$$f_{osc} = 1/2\pi RC, \text{ where } R = R1 = R2 \text{ and}$$

$$C = C1 = C2.$$

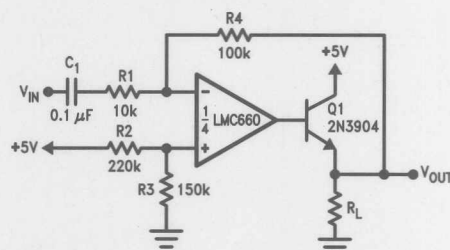
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



TL/H/8767-10

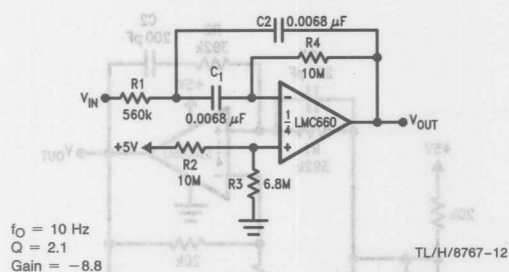
Power Amplifier



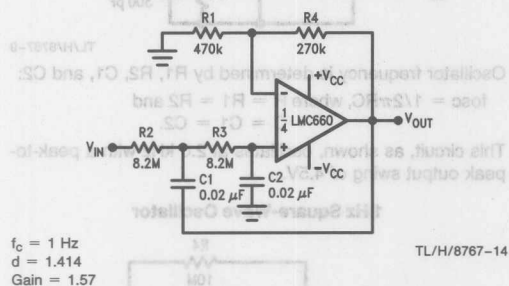
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Typical Single-Supply Applications ($V^+ = 5.0$ VDC) (Continued)

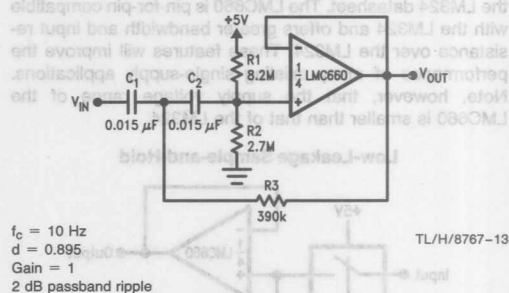
10 Hz Bandpass Filter



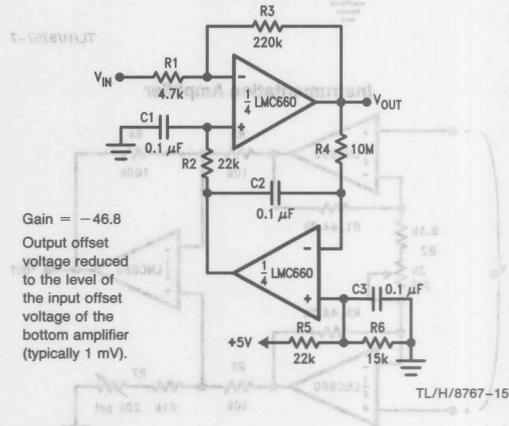
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



10 Hz High-Pass Filter



High Gain Amplifier with Offset Voltage Reduction



LMC662 **CMOS Dual Operational Amplifier**

General Description

The LMC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It operates from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS} , drift, and broadband noise as well as voltage gain into realistic loads (2 k Ω and 600 Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC660 datasheet for a Quad CMOS operational amplifier with these same features.

Features

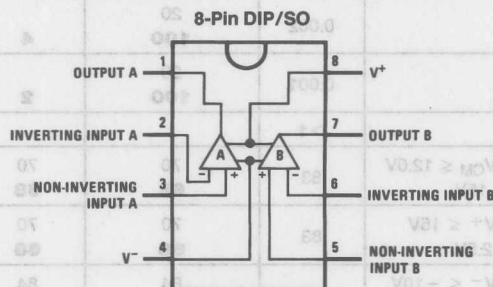
- Rail-to-rail output swing
- Specified for 2 k Ω and 600 Ω loads
- High voltage gain
- Low input offset voltage
- Low offset voltage drift

- Ultra low input bias current
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- $I_{SS} = 400 \mu A/\text{amplifier}$; independent of V^+
- Low distortion
- Slew rate
- Available in extended temperature range (-40°C to $+125^\circ\text{C}$); ideal for automotive applications
- Available to a Standard Military Drawing specification

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram



Ordering Information

| Package | Temperature Range | | | | NSC Drawing | Transport Media |
|-------------------------------|-------------------|----------|------------|------------|-------------|---------------------|
| | Military | Extended | Industrial | Commercial | | |
| 8-Pin Ceramic DIP | LMC662AMJ/883 | | | | J08A | Rail |
| 8-Pin Small Outline | | LMC662EM | LMC662AIM | LMC662CM | M08A | Rail, Tape and Reel |
| 8-Pin Molded DIP | | LMC662EN | LMC662AIN | LMC662CN | N08E | Rail |
| 8-Pin Side Brazed Ceramic DIP | LMC662AMD | | | | D08C | Rail |

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|------------------------------------|
| Differential Input Voltage | ± Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^+ | (Note 12) |
| Output Short Circuit to V^- | (Note 1) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temp. Range | −65°C to +150°C |
| Voltage at Input/Output Pins | (V^+) + 0.3V, (V^-) − 0.3V |
| Current at Output Pin | ± 18 mA |
| Current at Input Pin | ± 5 mA |
| Current at Power Supply Pin | 35 mA |
| Power Dissipation | (Note 2) |
| Junction Temperature | 150°C |
| ESD Tolerance (Note 8) | 1000V |

Operating Ratings (Note 3)

| | |
|--|------------------------|
| Temperature Range | |
| LMC662AMJ/883 | −55°C ≤ T_J ≤ +125°C |
| LMC662AMD | −40°C ≤ T_J ≤ +85°C |
| LMC662AI | 0°C ≤ T_J ≤ +70°C |
| LMC662C | −40°C ≤ T_J ≤ +125°C |
| LMC662E | |
| Supply Voltage Range | 4.75V to 15.5V |
| Power Dissipation | (Note 10) |
| Thermal Resistance (θ_{JA}) (Note 11) | |
| 8-Pin Ceramic DIP | 100°C/W |
| 8-Pin Molded DIP | 101°C/W |
| 8-Pin SO | 165°C/W |
| 8-Pin Side Braided Ceramic DIP | 100°C/W |

DC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Parameter | Conditions | Typ (Note 4) | LMC662AMJ/883 LMC662AMD | LMC662AI | LMC662C | LMC662E | Units |
|--|---|-----------------|--|--|--|--|------------------------------|
| | | | Limit (Note 4, 9) | Limit (Note 4) | Limit (Note 4) | Limit (Note 4) | |
| Input Offset Voltage | | 1 | 3 3.5 | 3 3.3 | 6 6.3 | 6 6.5 | mV max |
| Input Offset Voltage Average Drift | | 1.3 | | | | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | | 0.002 | 20 100 | 4 | 2 | 60 | pA max |
| Input Offset Current | | 0.001 | 20 100 | 2 | 1 | 60 | pA max |
| Input Resistance | | > 1 | | | | | Tera Ω |
| Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12.0\text{V}$ $V^+ = 15\text{V}$ | 83 | 70 68 | 70 68 | 63 62 | 63 60 | dB min |
| Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$ | 83 | 70 68 | 70 68 | 63 62 | 63 60 | dB min |
| Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 84 82 | 84 83 | 74 73 | 74 70 | dB min |
| Input Common-Mode Voltage Range | $V^+ = 5\text{V} \text{ \& } 15\text{V}$ For CMRR ≥ 50 dB | −0.4 | −0.1 0 | −0.1 0 | −0.1 0 | −0.1 0 | V max |
| | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.6$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.4$ | $V^+ - 2.3$ $V^+ - 2.6$ | V min |
| | | | | | | | |
| Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ (Note 5) Sourcing | 2000 | 400 300 | 440 400 | 300 200 | 200 100 | V/mV min |
| | Sinking | 500 | 180 70 | 180 120 | 90 80 | 90 40 | V/mV min |
| | $R_L = 600\Omega$ (Note 5) Sourcing | 1000 | 200 150 | 220 200 | 150 100 | 100 75 | V/mV min |
| | Sinking | 250 | 100 35 | 100 60 | 50 40 | 50 20 | V/mV min |

DC Electrical Characteristics (Continued)

unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = -5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Parameter | Conditions | Typ (Note 4) | LMC662AMJ/883 | LMC662AI | LMC662C | LMC662E | Units |
|--------------------------------------|---|-----------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------|
| | | | Limit (Note 4, 9) | Limit (Note 4) | Limit (Note 4) | Limit (Note 4) | |
| Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 4.87 | 4.82 4.77 | 4.82 4.79 | 4.78 4.76 | 4.78 4.70 | V min |
| | | | 0.15 0.19 | 0.15 0.17 | 0.19 0.21 | 0.19 0.25 | V max |
| | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to $V^+/2$ | 4.61 | 4.41 4.24 | 4.41 4.31 | 4.27 4.21 | 4.27 4.10 | V min |
| | | | 0.50 0.63 | 0.50 0.56 | 0.63 0.69 | 0.63 0.75 | V max |
| | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 14.63 | 14.50 14.40 | 14.50 14.44 | 14.37 14.32 | 14.37 14.25 | V min |
| | | | 0.35 0.43 | 0.35 0.40 | 0.44 0.48 | 0.44 0.55 | V max |
| | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to $V^+/2$ | 13.90 | 13.35 13.02 | 13.35 13.15 | 12.92 12.76 | 12.92 12.60 | V min |
| | | | 1.16 1.42 | 1.16 1.32 | 1.45 1.58 | 1.45 1.75 | V max |
| Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 12 | 16 14 | 13 11 | 13 9 | mA min |
| | Sinking, $V_O = 5\text{V}$ | 21 | 16 12 | 16 14 | 13 11 | 13 9 | mA min |
| Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 40 | 19 19 | 28 25 | 23 21 | 23 15 | mA min |
| | Sinking, $V_O = 13\text{V}$ (Note 12) | 39 | 19 19 | 28 24 | 23 20 | 23 15 | mA min |
| Supply Current | Both Amplifiers $V_O = 1.5\text{V}$ | 0.75 | 1.3 1.8 | 1.3 1.5 | 1.6 1.8 | 1.6 1.9 | mA max |

AC Electrical Characteristics

unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Parameter | Conditions | Typ (Note 4) | LMC662AMJ/883 LMC662AMD | LMC662AI | LMC662C | LMC662E | Units |
|------------------------------|---|-----------------|----------------------------|-------------------|-------------------|-------------------|-------------------------|
| | | | Limit (Note 4, 9) | Limit (Note 4) | Limit (Note 4) | Limit (Note 4) | |
| Slew Rate | (Note 6) | 1.1 | 0.8 0.5 | 0.8 0.6 | 0.8 0.7 | 0.8 0.4 | V/ μs min |
| Gain-Bandwidth Product | | 1.4 | | | | | MHz |
| Phase Margin | | 50 | | | | | Deg |
| Gain Margin | | 17 | | | | | dB |
| Amp-to-Amp Isolation | (Note 7) | 130 | | | | | dB |
| Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | | | | nV/ $\sqrt{\text{Hz}}$ |
| Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | | pA/ $\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{PP}$ $V^+ = 15\text{V}$ | 0.01 | | | | | % |

Note 1: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 6: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15\text{V}$ and $R_L = 10\text{ k}\Omega$ connected to $V^+ / 2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{PP}$.

Note 8: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 9: A military RETS electrical test specification is available on request. At the time of printing, the LMC662AMJ/883 RETS spec complied fully with the boldface limits in this column. The LMC662AMJ/883 may also be procured to a Standard Military Drawing specification.

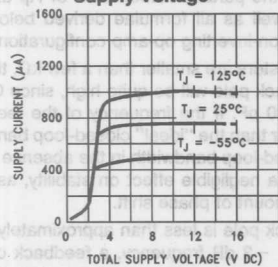
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

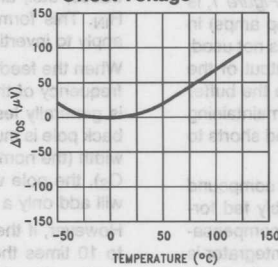
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified

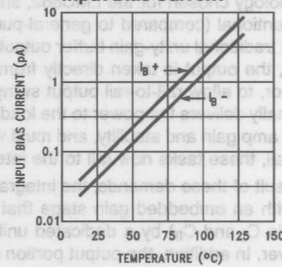
Supply Current vs Supply Voltage



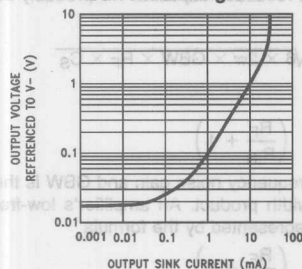
Offset Voltage



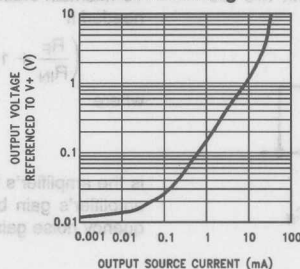
Input Bias Current



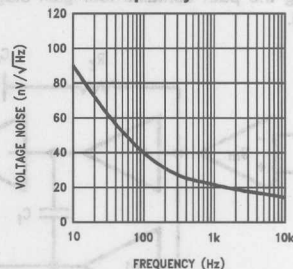
Output Characteristics Current Sinking



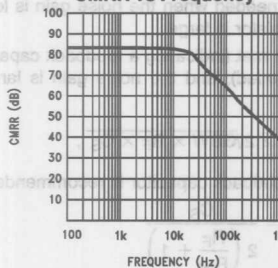
Output Characteristics Current Sourcing



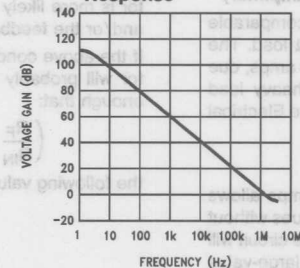
Input Voltage Noise vs Frequency



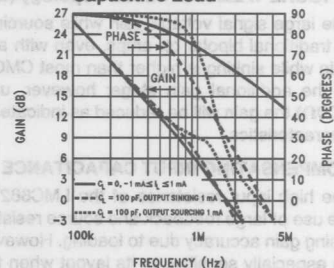
CMRR vs Frequency



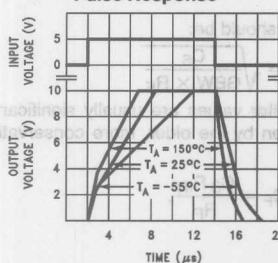
Open-Loop Frequency Response



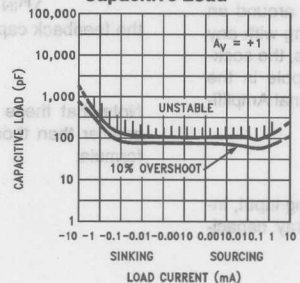
Frequency Response vs Capacitive Load



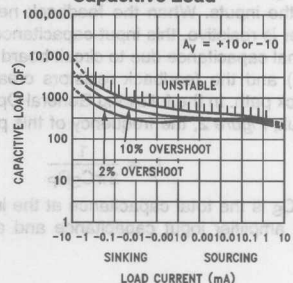
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

TL/H/9763-3

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC662, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

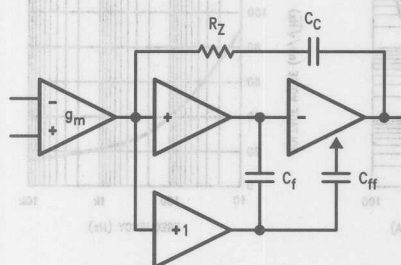


FIGURE 1. LMC662 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600 Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600 Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC662 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, *Figure 2*, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_s R_p}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capaci-

tance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN} . This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few $k\Omega$, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the “ideal” closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the “ideal” -3 dB frequency, a feedback capacitor, C_F , should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier’s low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \leq \sqrt{6 \times 2\pi \times \text{GBW} \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1 \right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula:

$$\left(\frac{R_F}{R_{IN}} + 1 \right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2 \left(\frac{R_F}{R_{IN}} + 1 \right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1 \right) < 2\sqrt{GBW \times R_F \times C_S},$$

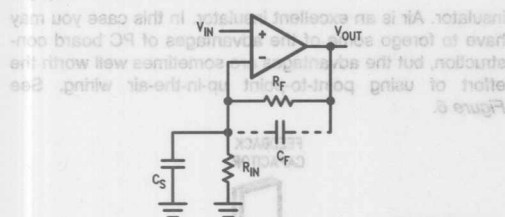
the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$

Application Hints (Continued)



TL/H/9763-6

FIGURE 2. General Operational Amplifier Circuit

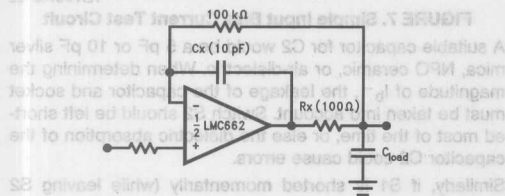
C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 3a, the addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

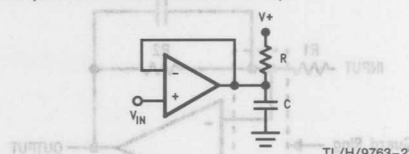


TL/H/9763-5

FIGURE 3a. R_X , C_X Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 3b). Typically a pull up resistor conducting 500 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open

loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



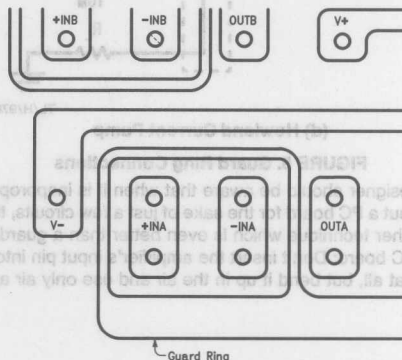
TL/H/9763-23

FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

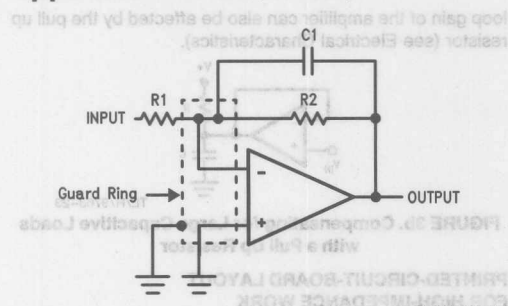
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC662's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 4. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10¹² Ω , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC662's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10¹¹ Ω would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 5a, 5b, 5c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 5d.



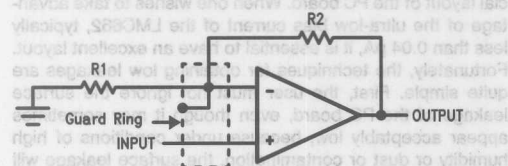
TL/H/9763-16

FIGURE 4. Example, using the LMC660, of Guard Ring in P.C. Board Layout

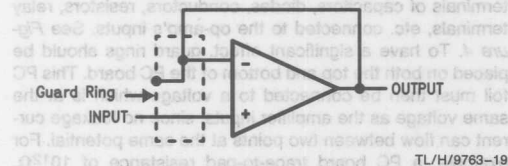
Application Hints (Continued)



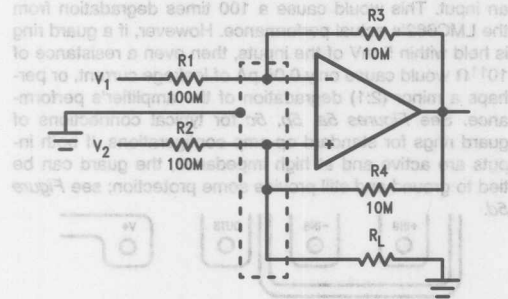
(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower



(d) Howland Current Pump

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an

insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 6.

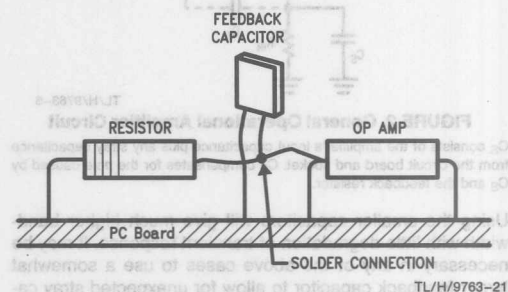


FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 7 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_{b-} = \frac{dV_{OUT}}{dt} \times C_2$$

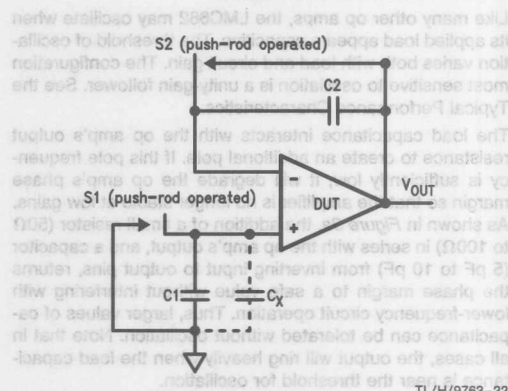


FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_{b-} , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

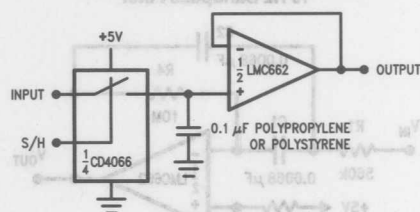
$$I_{b+} = \frac{dV_{OUT}}{dt} \times (C_1 + C_X)$$

where C_X is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

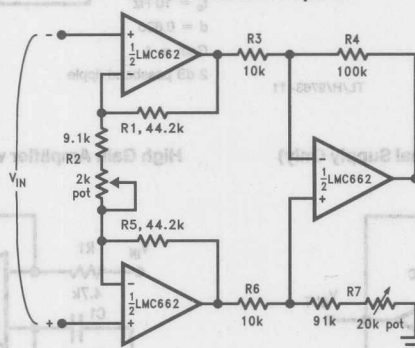
Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC662 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC662 is smaller than that of the LM358.

Low-Leakage Sample-and-Hold



TL/H/9763-15

Instrumentation Amplifier



TL/H/9763-7

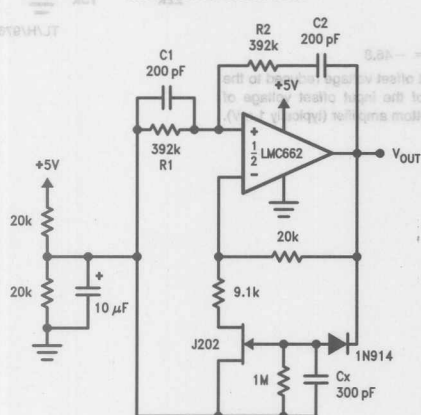
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$, then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R_3 to R_6 and R_4 to R_7 affects CMRR. Gain may be adjusted through R_2 . CMRR may be adjusted through R_7 .

Sine-Wave Oscillator



TL/H/9763-8

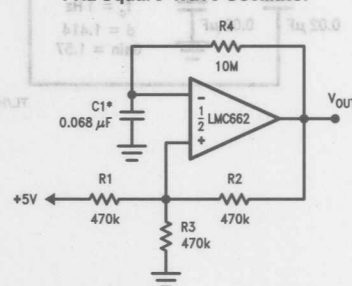
Oscillator frequency is determined by R_1 , R_2 , C_1 , and C_2 :

$$f_{OSC} = 1/2\pi RC$$

where $R = R_1 = R_2$ and $C = C_1 = C_2$.

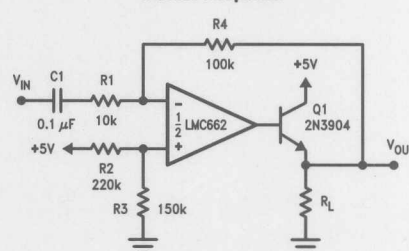
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



TL/H/9763-9

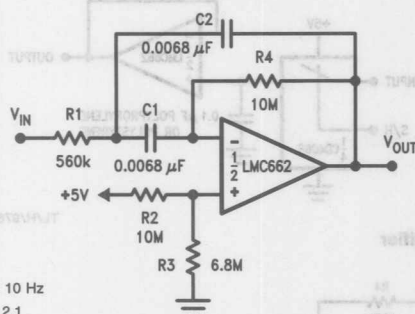
Power Amplifier



TL/H/9763-10

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

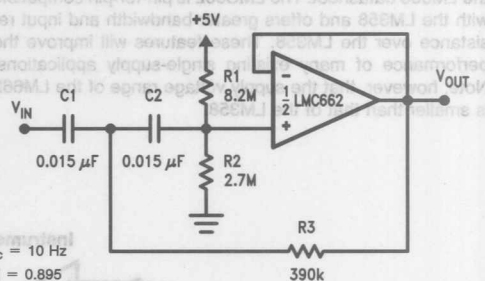
10 Hz Bandpass Filter



$f_O = 10 \text{ Hz}$
 $Q = 2.1$
 Gain = -8.8

TL/H/9763-11

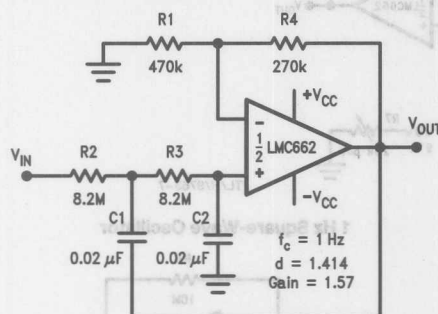
10 Hz High-Pass Filter



$f_c = 10 \text{ Hz}$
 $d = 0.895$
 Gain = 1
 2 dB passband ripple

TL/H/9763-12

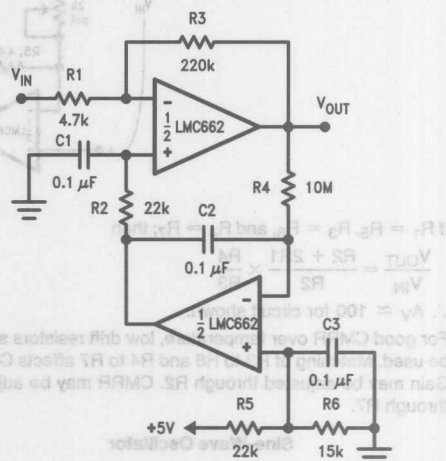
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



$f_c = 1 \text{ Hz}$
 $d = 1.414$
 Gain = 1.57

TL/H/9763-13

High Gain Amplifier with Offset Voltage Reduction



Gain = -46.8
 Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

TL/H/9763-14

LMC6001 Ultra Ultra-Low Input Current Amplifier

General Description

Featuring 100% tested input currents of 25 fA max., low operating power, and ESD protection of 2000V, the LMC6001 achieves a new industry benchmark for low input current operational amplifiers. By tightly controlling the molding compound, National is able to offer this ultra-low input current in a lower cost molded package.

To avoid long turn-on settling times common in other low input current opamps, the LMC6001A is tested 3 times in the first minute of operation. Even units that meet the 25 fA limit are rejected if they drift.

Because of the ultra-low input current noise of $0.13 \text{ fA}/\sqrt{\text{Hz}}$, the LMC6001 can provide almost noiseless amplification of high resistance signal sources. Adding only 1 dB at 100 k Ω , 0.1 dB at 1 M Ω and 0.01 dB or less from 10 M Ω to 2,000 M Ω , the LMC6001 is an almost noiseless amplifier.

The LMC6001 is ideally suited for electrometer applications requiring ultra-low input leakage such as sensitive photode-

tection transimpedance amplifiers and sensor amplifiers. Since input referred noise is only $22 \text{ nV}/\sqrt{\text{Hz}}$, the LMC6001 can achieve higher signal to noise ratio than JFET input type electrometer amplifiers. Other applications of the LMC6001 include long interval integrators, ultra-high input impedance instrumentation amplifiers, and sensitive electrical-field measurement circuits.

Features (Max limit, 25°C unless otherwise noted)

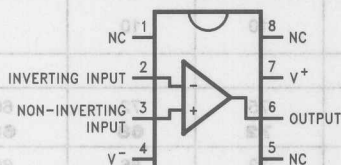
- Input current (100% tested) 25 fA
- Input current over temp. 2 pA
- Low power 750 μA
- Low V_{OS} 350 μV
- Low noise $22 \text{ nV}/\sqrt{\text{Hz}}$ @ 1 kHz Typ.

Applications

- Electrometer amplifier
- Photodiode preamplifier
- Ion detector
- A.T.E. leakage testing

Connection Diagrams

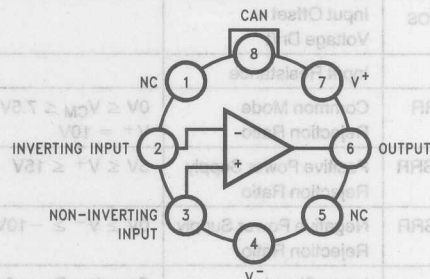
8-Pin DIP



Top View

TL/H/11887-1

8-Pin Metal Can



Top View

TL/H/11887-2

Ordering Information

| Package | Industrial Temperature Range -40°C to +85°C | NSC Package Drawing |
|---------------------|--|---------------------|
| 8-Pin Molded DIP | LMC6001AIN, LMC6001BIN, LMC6001CIN | N08E |
| 8-Pin Metal Can | LMC6001AIH, LMC6001BIH | H08C |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|---|
| Differential Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin | $(V^+) + 0.3V, (V^-) - 0.3V$ |
| Supply Voltage $(V^+ - V^-)$ | $-0.3V$ to $+16V$ |
| Output Short Circuit to V^+ | (Notes 2, 10) |
| Output Short Circuit to V^- | (Note 2) |
| Lead Temperature (Soldering, 10 Sec.) | 260°C |
| Storage Temperature | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature | 150°C |
| Current at Input Pin | $\pm 10\text{ mA}$ |

| | |
|-----------------------------|--------------------|
| Current at Output Pin | $\pm 30\text{ mA}$ |
| Current at Power Supply Pin | 40 mA |
| Power Dissipation | (Note 3) |
| ESD Tolerance (Note 9) | 2 kV |

Operating Ratings (Note 1)

| | |
|------------------------------|---|
| Temperature Range | LMC6001AI, LMC6001BI, LMC6001CI |
| | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Supply Voltage | $4.5V \leq V^+ \leq 15.5V$ |
| Thermal Resistance (Note 11) | |
| θ_{JA} , N Package | 100°C/W |
| θ_{JA} , H Package | 145°C/W |
| θ_{JC} , H Package | 45°C/W |
| Power Dissipation | (Note 8) |

DC Electrical Characteristics

Limits in standard typeface guaranteed for $T_J = 25^\circ\text{C}$ and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, and $R_L > 1M$.

| Symbol | Parameter | Conditions | Typical (Note 4) | Limits (Note 5) | | | Units |
|------------|---------------------------------------|---|---------------------|--------------------|--------------------|---------------------|------------------------------|
| | | | | LMC6001AI | LMC6001BI | LMC6001CI | |
| I_B | Input Current | Either Input, $V_{CM} = 0V$, $V_S = \pm 5V$ | 10 | 25 2000 | 100 4000 | 1000 4000 | fA |
| I_{OS} | Input Offset Current | | 5 | 1000 | 2000 | 2000 | |
| V_{OS} | Input Offset Voltage | | | 0.35 1.0 | 1.0 1.7 | 1.0 2.0 | mV |
| | | $V_S = \pm 5V, V_{CM} = 0V$ | | 0.7 1.35 | 1.35 2.0 | 1.35 | |
| TCV_{OS} | Input Offset Voltage Drift | | 2.5 | 10 | 10 | | $\mu\text{V}/^\circ\text{C}$ |
| R_{IN} | Input Resistance | | > 1 | | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 7.5V$ $V^+ = 10V$ | 83 | 75 72 | 72 68 | 66 63 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $5V \leq V^+ \leq 15V$ | 83 | 73 70 | 66 63 | 66 63 | |
| -PSRR | Negative Power Supply Rejection Ratio | $0V \geq V^- \geq -10V$ | 94 | 80 77 | 74 71 | 74 71 | |
| A_v | Large Signal Voltage Gain | Sourcing, $R_L = 2\text{ k}\Omega$ (Note 6) | 1400 | 400 300 | 300 200 | 300 200 | V/mV min |
| | | Sinking, $R_L = 2\text{ k}\Omega$ (Note 6) | 350 | 180 100 | 90 60 | 90 60 | |

| Package | Industrial Temperature Range -40°C to $+85^\circ\text{C}$ | NSC Package Drawing |
|---------------------|--|------------------------|
| 8-Pin Molded DIP | LMC6001AI, LMC6001BI, LMC6001CI | MOSE |
| 8-Pin Metal Can | LMC6001AI, LMC6001BI | HOBC |

DC Electrical Characteristics

Limits in standard typeface guaranteed for $T_J = 25^\circ\text{C}$ and limits in **boldface type** apply at the temperature extremes. Unless otherwise specified, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, and $R_L > 1\text{M}\Omega$. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 4) | Limits (Note 5) | | | Units |
|----------|---------------------------|---|---------------------|--|--|--|----------------------|
| | | | | LM6001AI | LM6001BI | LM6001CI | |
| V_{CM} | Input Common-Mode Voltage | $V^+ = 5\text{V}$ and 15V For $\text{CMRR} \geq 60\text{ dB}$ | -0.4 | -0.1 0 | -0.1 0 | -0.1 0 | V max |
| | | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.5$ | V min |
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.80 4.73 | 4.75 4.67 | 4.75 4.67 | V min |
| | | | 0.10 | 0.14 0.17 | 0.20 0.24 | 0.20 0.24 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 14.50 14.34 | 14.37 14.25 | 14.37 14.25 | V min |
| | | | 0.26 | 0.35 0.45 | 0.44 0.56 | 0.44 0.56 | V max |
| | | | | | | | |
| I_O | Output Current | Sourcing, $V^+ = 5\text{V}$, $V_O = 0\text{V}$ | 16 10 | 13 8 | 13 8 | 13 8 | mA min |
| | | | 22 | 10 | 8 | 8 | |
| | | Sinking, $V^+ = 5\text{V}$, $V_O = 5\text{V}$ | 21 13 | 16 10 | 13 10 | 13 10 | |
| | | Sourcing, $V^+ = 15\text{V}$, $V_O = 0\text{V}$ | 30 22 | 28 22 | 23 18 | 23 18 | |
| | | Sinking, $V^+ = 15\text{V}$, $V_O = 13\text{V}$ (Note 10) | 34 22 | 28 22 | 23 18 | 23 18 | |
| I_S | Supply Current | $V^+ = 5\text{V}$, $V_O = 1.5\text{V}$ | 450 900 | 750 900 | 750 900 | 750 900 | μA max |
| | | $V^+ = 15\text{V}$, $V_O = 7.5\text{V}$ | 550 950 | 850 950 | 850 950 | 850 950 | |

| Symbol | Parameter | Conditions | Typical (Note 4) | Limits (Note 5) | | | Units |
|-------------|------------------------------|---|---------------------|-----------------|------------|------------|------------------------|
| | | | | LM6001AI | LM6001BI | LM6001CI | |
| SR | Slew Rate | (Note 7) | 1.5 | 0.8 0.6 | 0.8 0.6 | 0.8 0.6 | V/ μ s min |
| GBW | Gain-Bandwidth Product | | 1.3 | | | | MHz |
| ϕ_{fm} | Phase Margin | | 50 | | | | Deg |
| G_M | Gain Margin | | 17 | | | | dB |
| e_n | Input-Referred Voltage Noise | F = 1 kHz | 22 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | F = 1 kHz | 0.13 | | | | fA/ $\sqrt{\text{Hz}}$ |
| THD | Total Harmonic Distortion | F = 10 kHz, $A_V = -10$, $R_L = 100 \text{ k}\Omega$, $V_O = 8 V_{PP}$ | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of $\pm 30 \text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 4: Typical values represent the most likely parametric norm.

Note 5: All limits are guaranteed by testing or statistical analysis.

Note 6: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V. For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 7: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Limit specified is the lower of the positive and negative slew rates.

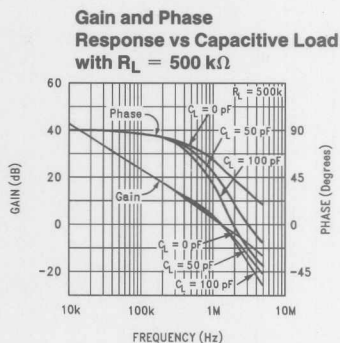
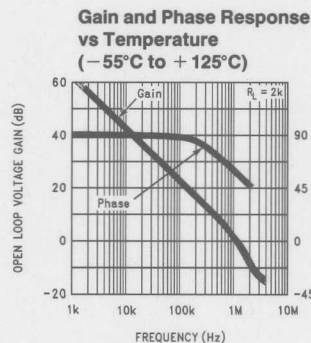
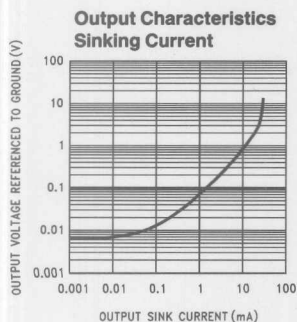
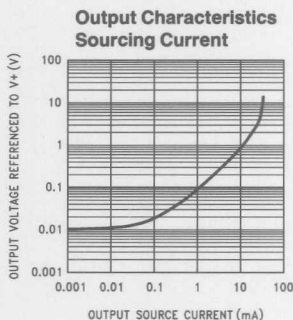
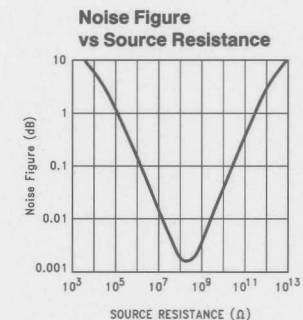
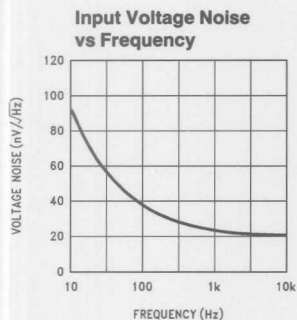
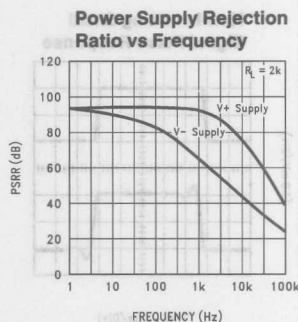
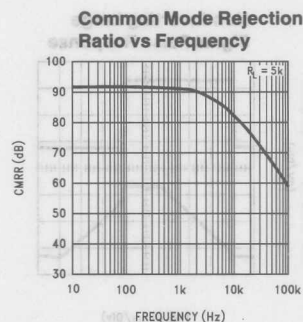
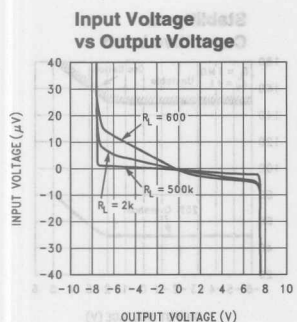
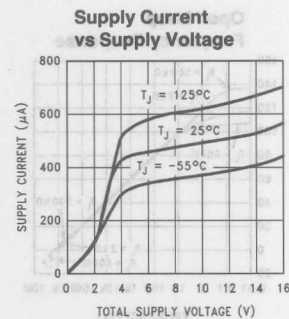
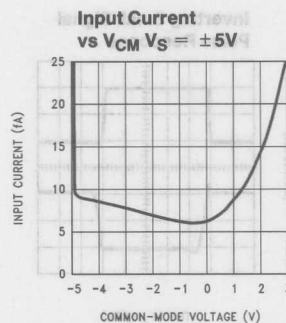
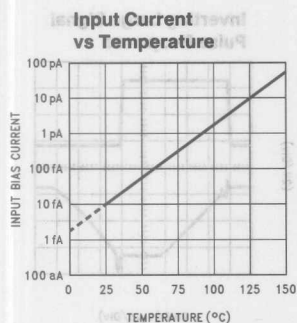
Note 8: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 9: Human body model, 1.5 k Ω in series with 100 pF.

Note 10: Do not connect the output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 11: All numbers apply for packages soldered directly into a printed circuit board.

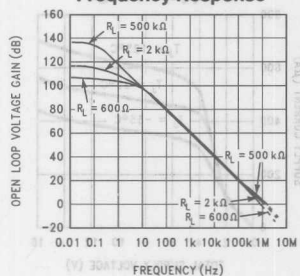
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, unless otherwise specified



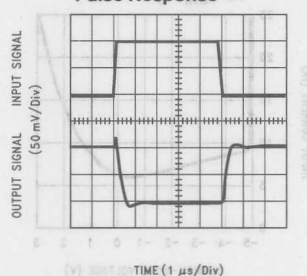
TL/H/11887-3

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, unless otherwise specified

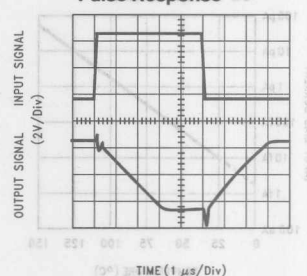
Open Loop Frequency Response



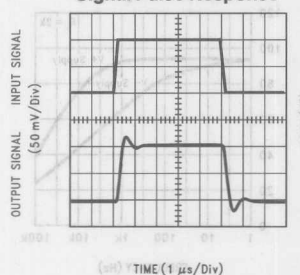
Inverting Small Signal Pulse Response



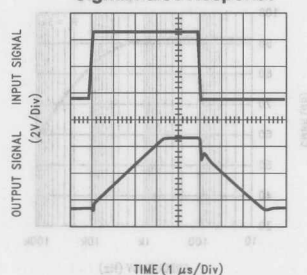
Inverting Large Signal Pulse Response



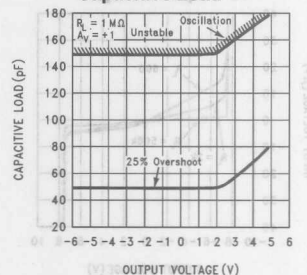
Non-Inverting Small Signal Pulse Response



Non-Inverting Large Signal Pulse Response

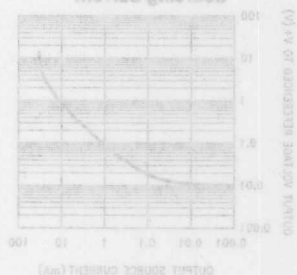


Stability vs Capacitive Load

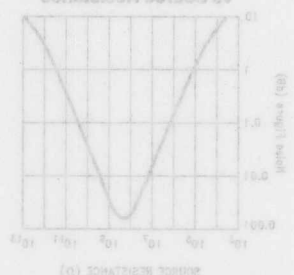


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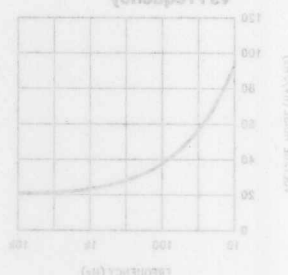
Output Characteristics



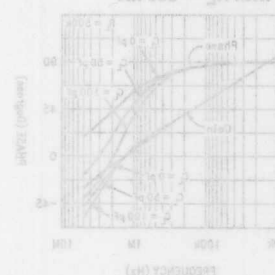
Noise Figure vs Source Resistance



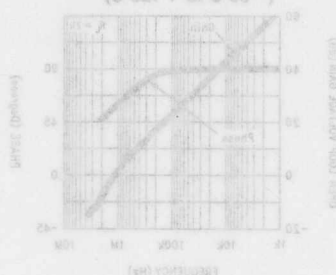
Input Voltage Noise vs Frequency



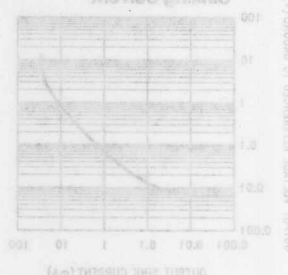
Gain and Phase Response vs Capacitive Load



Gain and Phase Response vs Temperature



Output Characteristics



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6001 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional op-amps. These features make the LMC6001 both easier to design with, and provide higher speed than products typically found in this low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6001.

Although the LMC6001 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6001 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in Figure 1) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

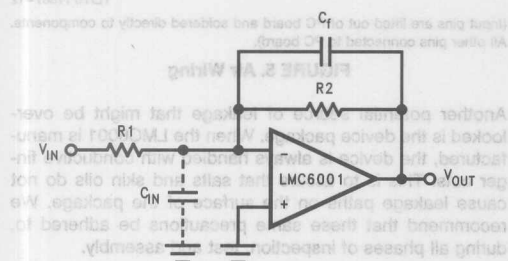


FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see Typical Curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2a.

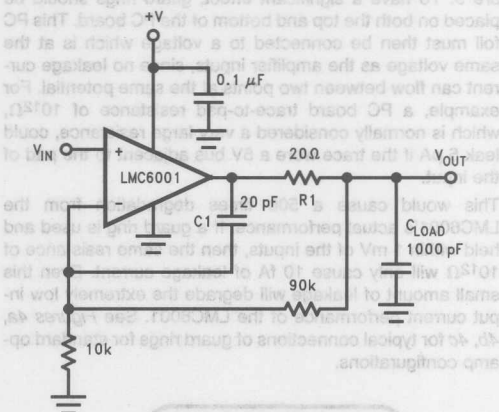


FIGURE 2a. LMC6001 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 2a, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pullup resistor to V^+ (Figure 2b). Typically a pullup resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pullup resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pullup resistor (see Electrical Characteristics).

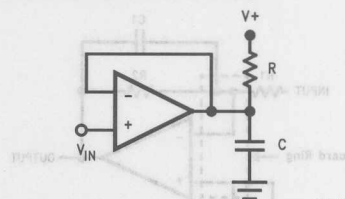


FIGURE 2b. Compensating for Large Capacitive Loads with a Pullup Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6001, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

Applications Hints (Continued)

leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6001's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc., connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input.

This would cause a 500 times degradation from the LMC6001's actual performance. If a guard ring is used and held within 1 mV of the inputs, then the same resistance of $10^{12}\Omega$ will only cause 10 fA of leakage current. Even this small amount of leakage will degrade the extremely low input current performance of the LMC6001. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

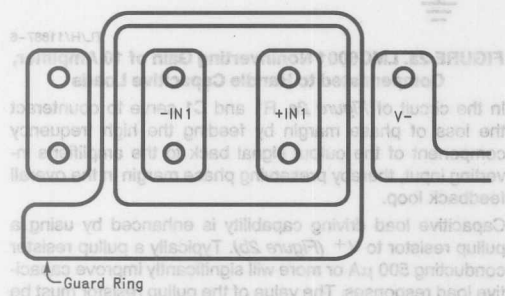
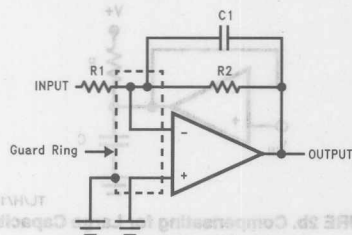
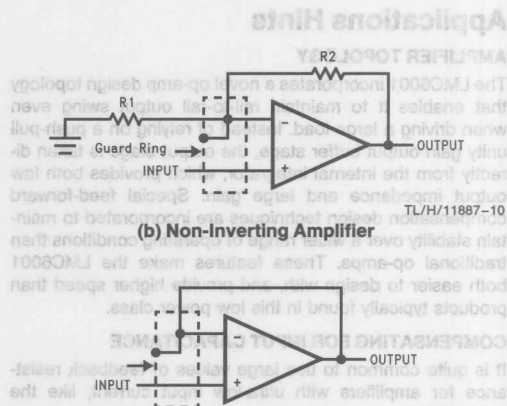


FIGURE 3. Examples of Guard Ring in PC Board Layout



(a) Inverting Amplifier



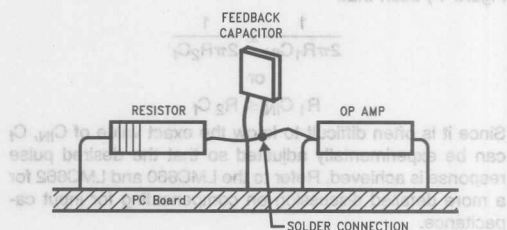
(b) Non-Inverting Amplifier



(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring

Another potential source of leakage that might be overlooked is the device package. When the LMC6001 is manufactured, the device is always handled with conductive finger cots. This is to assure that salts and skin oils do not cause leakage paths on the surface of the package. We recommend that these same precautions be adhered to, during all phases of inspection, test and assembly.

Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6001 is designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Applications

The extremely high input resistance, and low power consumption, of the LMC6001 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, electrostatic field detectors and gas chromatographs.

Two Opamp, Temperature Compensated pH Probe Amplifier

The signal from a pH probe has a typical resistance between 10 M Ω and 1000 M Ω . Because of this high value, it is very important that the amplifier input currents be as small as possible. The LMC6001 with less than 25 fA input current is an ideal choice for this application.

The theoretical output of the standard Ag/AgCl pH probe is 59.16 mV/pH at 25°C with 0V out at a pH of 7.00. This output is proportional to absolute temperature. To compensate for this, a temperature compensating resistor, R1, is

placed in the feedback loop. This cancels the temperature dependence of the probe. This resistor must be mounted where it will be at the same temperature as the liquid being measured.

The LMC6001 amplifies the probe output providing a scaled voltage of ± 100 mV/pH from a pH of 7. The second opamp, a micropower LMC6041 provides phase inversion and offset so that the output is directly proportional to pH, over the full range of the probe. The pH reading can now be directly displayed on a low cost, low power digital panel meter. Total current consumption will be about 1 mA for the whole system.

The micropower dual operational amplifier, LMC6042, would optimize power consumption but not offer these advantages:

1. The LMC6001A guarantees a 25 fA limit on input current at 25°C.
2. The input ESD protection diodes in the LMC6042 are only rated at 500V while the LMC6001 has much more robust protection that is rated at 2000V.

The setup and calibration is simple with no interactions to cause problems.

1. Disconnect the pH probe and with R3 set to about mid-range and the noninverting input of the LMC6001 grounded, adjust R8 until the output is 700 mV.
2. Apply -414.1 mV to the noninverting input of the LMC6001. Adjust R3 for an output of 1400 mV. This completes the calibration. As real pH probes may not perform exactly to theory, minor gain and offset adjustments should be made by trimming while measuring a precision buffer solution.

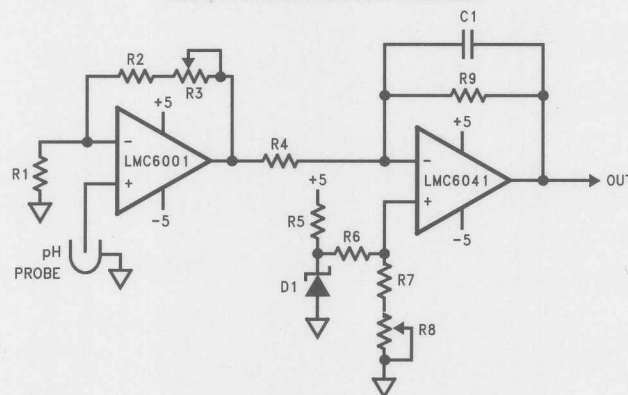


FIGURE 6. pH Probe Amplifier

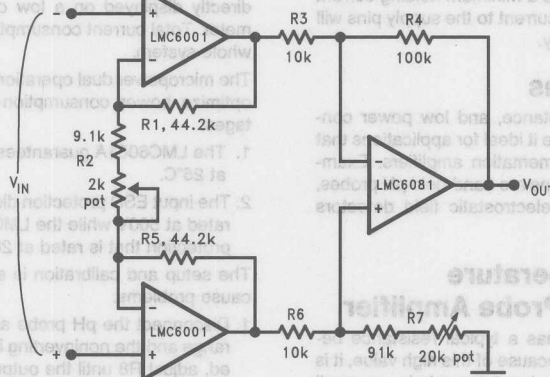
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- R1 100k + 3500 ppm/°C*
- R2 68.1k
- R3, 8 5k
- R4, 9 100k
- R5 36.5k
- R6 619k
- R7 97.6k
- D1 LM4040D1Z-2.5
- C1 2.2 μ F

*(Micro-ohm style 144 or similar)

Ultra-Low Input Current Instrumentation Amplifier

Figure 7 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 M Ω imbalance in source resistance. Input current is less than 20 fA and offset drift is less than $2.5 \mu\text{V}/^\circ\text{C}$.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.85\text{k}$).

FIGURE 7. Instrumentation Amplifier

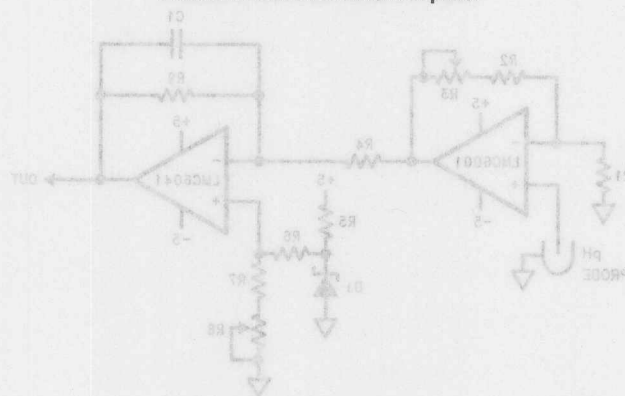


FIGURE 8. pH Probe Amplifier

quately

R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.

Typical Applications

The extremely high input resistance, and low power consumption of the LMC6001 make it ideal for applications that require battery-powered instrumentation in harsh environments. Examples of these types of applications include medical instrumentation, electrostatic discharge (ESD) protection, and gas chromatography.

Two Opamp, Temperature Compensated pH Probe Amplifier

The signal from a pH probe has a high impedance, typically between 10 M Ω and 1000 M Ω . Because the input impedance of the amplifier must be much higher than the probe impedance, the LMC6001 is an ideal choice for this application. The theoretical output of the standard Ag/AgCl pH probe is 59.16 mV/pH at 25°C with a pH of 7.00. This output is proportional to absolute temperature. To compensate for this, a temperature compensating resistor, R_1 , is

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TL/H/11887-13

R1 1.700k $\pm 300 \text{ ppm}/^\circ\text{C}$
R2 98.1k
R3 8.0k
R4 8.100k
R5 30.3k
R6 37.8k
R7 37.8k
D1 LMC6001:5.5
C1 5.5 μF

* (Values shown are for simulation)

LMC6022 **Low Power CMOS Dual Operational Amplifier**

General Description

The LMC6022 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^- , low input bias current, and voltage gain (into 100k and 5 k Ω loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6024 datasheet for a CMOS quad operational amplifier with these same features.

Features

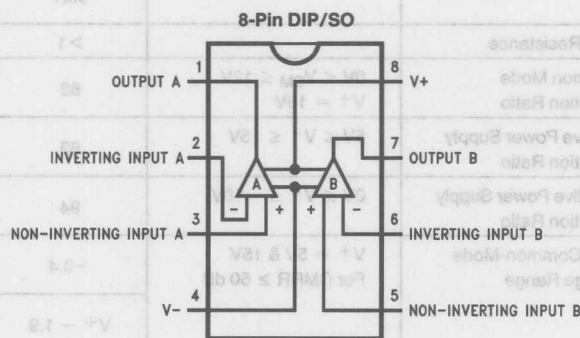
- Specified for 100 k Ω and 5 k Ω loads
- High voltage gain 120 dB
- Low offset voltage drift 2.5 μ V/ $^{\circ}$ C
- Ultra low input bias current 40 fA

- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/ μ s
- Micropower operation 0.5 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram



Top View

TL/H/11236-1

Ordering Information

| Temperature Range | Package | NSC Drawing | Transport Media |
|---|---------------------|-------------|-----------------------|
| Industrial $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$ | | | |
| LMC6022IN | 8-Pin Molded DIP | N08E | Rail |
| LMC6022IM | 8-Pin Small Outline | M08A | Rail Tape and Reel |

Absolute Maximum Ratings (Note 1)

| | |
|--|----------------------|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| ESD Tolerance (Note 4) | 1000V |
| Voltage at Output/Input Pin (V^+) + 0.3V, (V^-) - 0.3V | |
| Current at Output Pin | ± 18 mA |
| Current at Power Supply Pin | 35 mA |
| Power Dissipation | (Note 3) |

| | |
|-------------------------------|------------|
| Current at Input Pin | ± 5 mA |
| Output Short Circuit to V^- | (Note 2) |
| Output Short Circuit to V^+ | (Note 12) |

Operating Ratings

| | |
|---|---|
| Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Supply Voltage Range | 4.75V to 15.5V |
| Power Dissipation | (Note 10) |
| Thermal Resistance (θ_{JA}), (Note 11) | |
| 8-Pin DIP | 101°C/W |
| 8-Pin SO | 165°C/W |

DC Electrical Characteristics

The following specifications apply for $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$, and $R_L = 1\text{M}$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6022I Limit (Note 6) | Units |
|--------------------------|--|---|---------------------|--|------------------------------|
| V_{OS} | Input Offset Voltage | | 1 | 9 11 | mV max |
| $\Delta V_{OS}/\Delta T$ | Input Offset Voltage Average Drift | | 2.5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.04 | 200 | pA max |
| I_{OS} | Input Offset Current | | 0.01 | 100 | pA max |
| R_{IN} | Input Resistance | | > 1 | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12\text{V}$ $V^+ = 15\text{V}$ | 83 | 63 61 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ | 83 | 63 61 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 74 73 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V} \text{ \& } 15\text{V}$ For CMRR ≥ 50 dB | -0.4 | -0.1 0 | V max |
| | | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.5$ | V min |
| A_V | Large Signal Voltage Gain | $R_L = 100 \text{ k}\Omega$ (Note 7) Sourcing | 1000 | 200 100 | V/mV min |
| | | Sinking | 500 | 90 40 | V/mV min |
| | | $R_L = 5 \text{ k}\Omega$ (Note 7) Sourcing | 1000 | 100 75 | V/mV min |
| | | Sinking | 250 | 50 20 | V/mV min |

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted.

Boldface limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6022I Limit (Note 6) | Units |
|--------|----------------------|---|---------------------|-------------------------------|----------------|
| V_O | Output Voltage Swing | $V^+ = 5V$ $R_L = 100\text{ k}\Omega$ to $2.5V$ | 4.987 | 4.40 4.43 | V min |
| | | | 0.004 | 0.06 0.09 | V max |
| | | $V^+ = 5V$ $R_L = 5\text{ k}\Omega$ to $2.5V$ | 4.940 | 4.20 4.00 | V min |
| | | | 0.040 | 0.25 0.35 | V max |
| | | $V^+ = 15V$ $R_L = 100\text{ k}\Omega$ to $7.5V$ | 14.970 | 14.00 13.90 | V min |
| | | | 0.007 | 0.06 0.09 | V max |
| | | $V^+ = 15V$ $R_L = 5\text{ k}\Omega$ to $7.5V$ | 14.840 | 13.70 13.50 | V min |
| | | | 0.110 | 0.32 0.40 | V max |
| | | $V^+ = 5V$ Sourcing, $V_O = 0V$ | 22 | 13 9 | mA min |
| | | | 21 | 13 9 | mA min |
| I_O | Output Current | $V^+ = 15V$ Sourcing, $V_O = 0V$ | 40 | 23 15 | mA min |
| | | Sinking, $V_O = 13V$ (Note 12) | 39 | 23 15 | mA min |
| | | Both Amplifiers $V_O = 1.5V$ | 86 | 140 165 | μA max |

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6022I Limit (Note 6) | Units |
|----------|------------------------------|------------|---------------------|-------------------------------|-------------------|
| SR | Slew Rate | (Note 8) | 0.11 | 0.05 0.03 | V/ μs min |
| GBW | Gain-Bandwidth Product | | 0.35 | | MHz |
| ϕ_M | Phase Margin | | 50 | | Deg |
| G_M | Gain Margin | | 17 | | dB |
| | Amp-to-Amp Isolation | (Note 9) | 130 | | dB |
| e_n | Input-Referred Voltage Noise | F = 1 kHz | 42 | | nV/ \sqrt{Hz} |
| i_n | Input-Referred Current Noise | F = 1 kHz | 0.0002 | | pA/ \sqrt{Hz} |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of $150^\circ C$. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$, and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

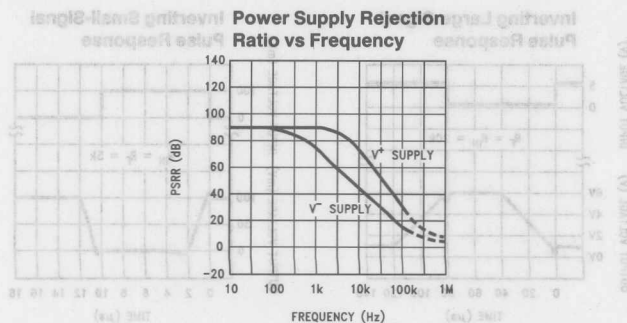
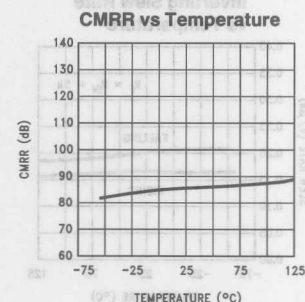
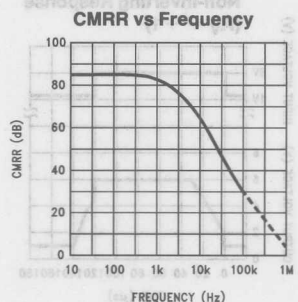
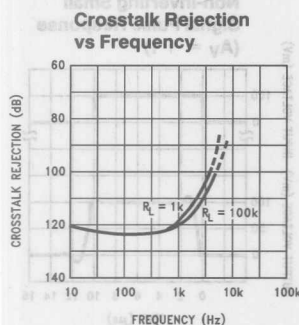
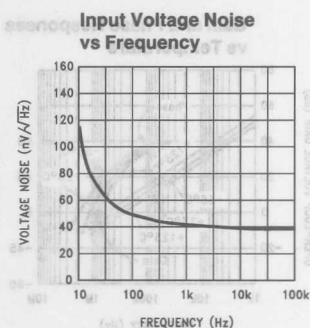
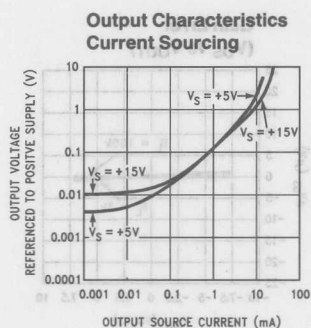
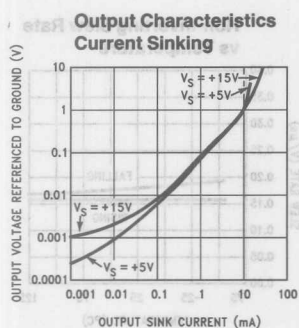
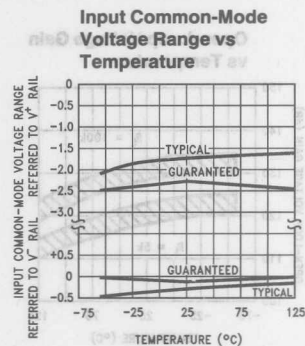
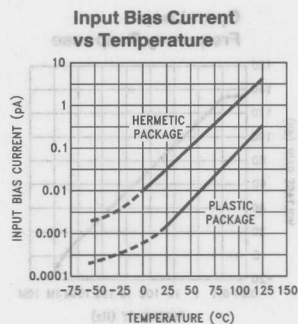
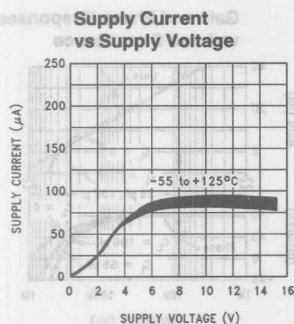
Note 9: Input referred. $V^+ = 15V$ and $R_L = 100$ k Ω connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13$ V_{pp}.

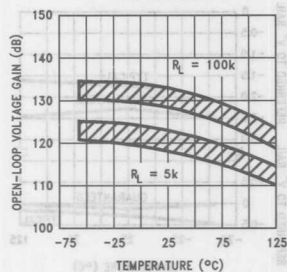
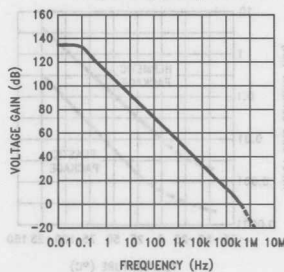
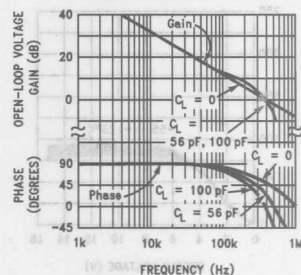
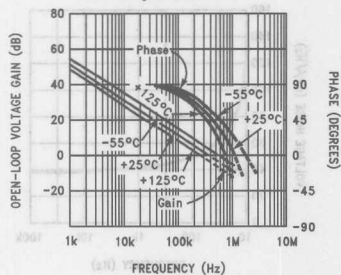
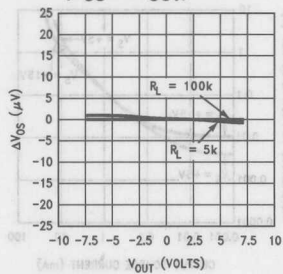
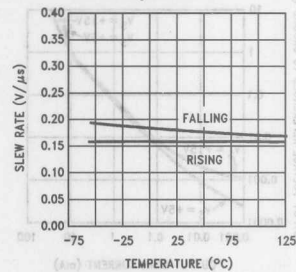
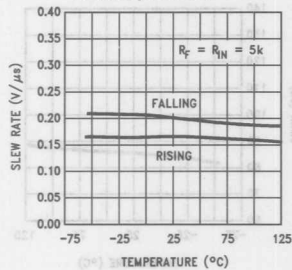
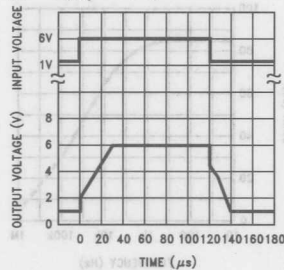
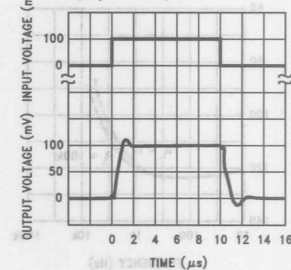
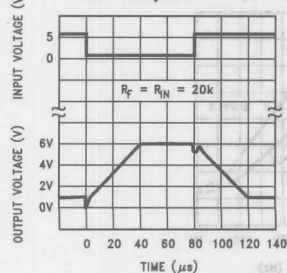
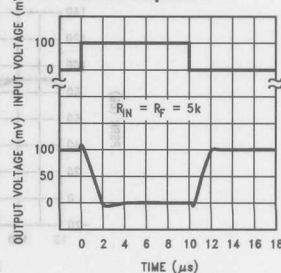
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

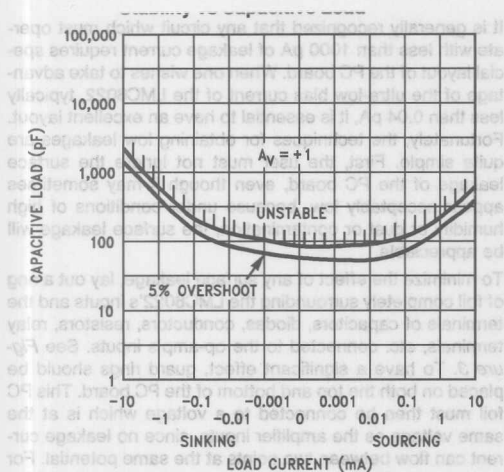
Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified



Open-Loop Voltage Gain vs Temperature

Open-Loop Frequency Response

Gain and Phase Responses vs Load Capacitance

Gain and Phase Responses vs Temperature

Gain Error (V_{OS} vs V_{OUT})

Non-Inverting Slew Rate vs Temperature

Inverting Slew Rate vs Temperature

Large-Signal Non-Inverting Response ($A_V = +1$)

Non-Inverting Small Signal Pulse Response ($A_V = +1$)

Inverting Large-Signal Pulse Response

Inverting Small-Signal Pulse Response




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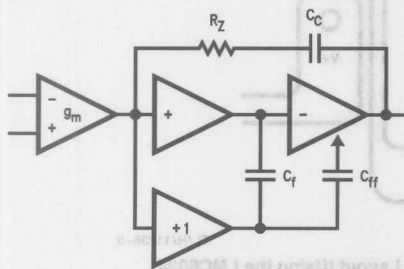
Note: Avoid resistive loads of less than 500 Ω , as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

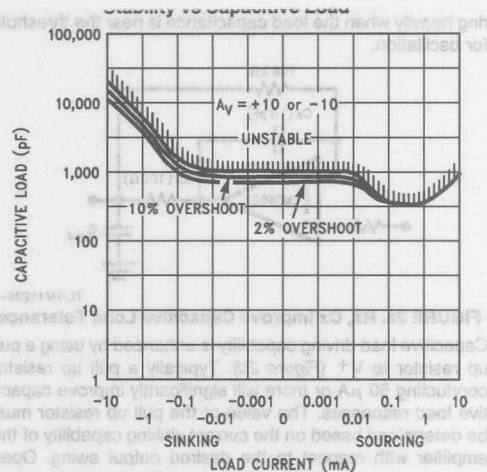
The topology chosen for the LMC6022 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



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FIGURE 1. LMC6022 Circuit Topology (Each Amplifier)



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The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 k Ω . The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 k Ω or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500 Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

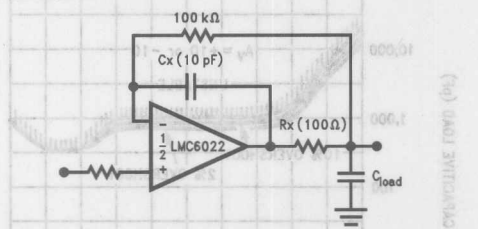
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6022 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

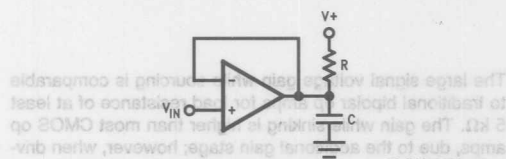
operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



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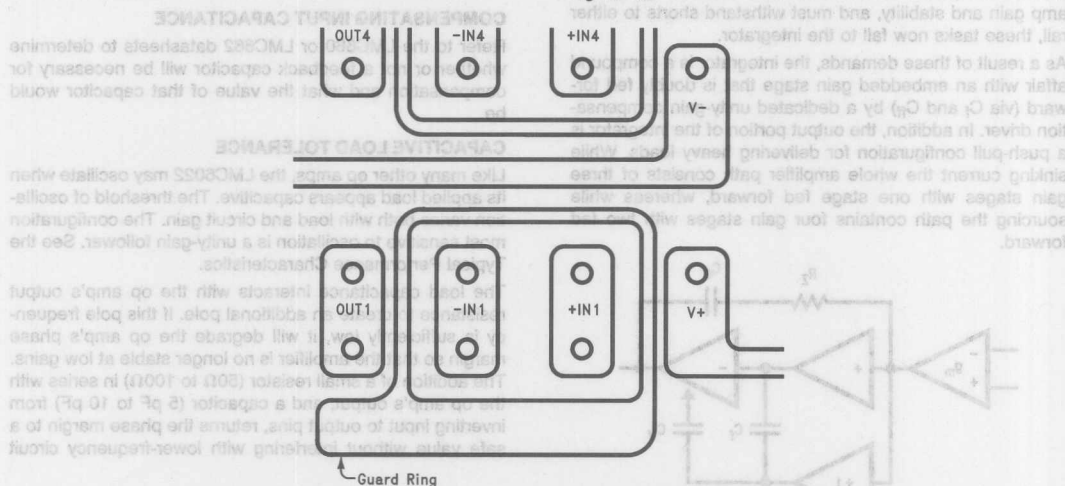
FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



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FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor



TL/H/11236-8

FIGURE 3. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6022, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6022's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6022's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11} \Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 4d.

Application Hints (Continued)

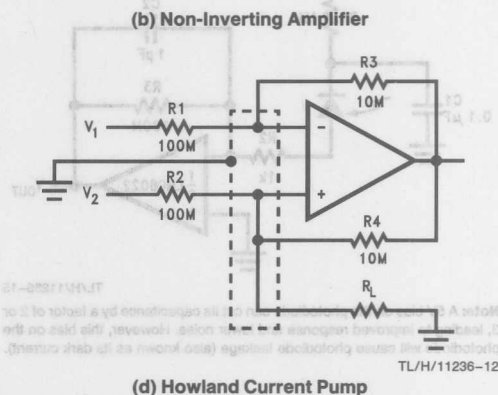
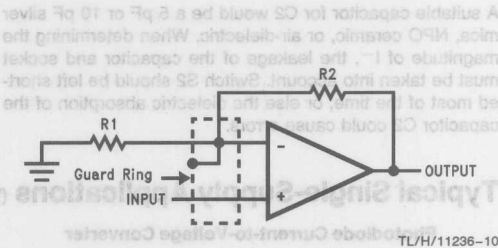
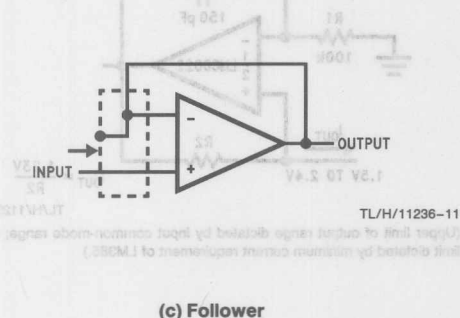
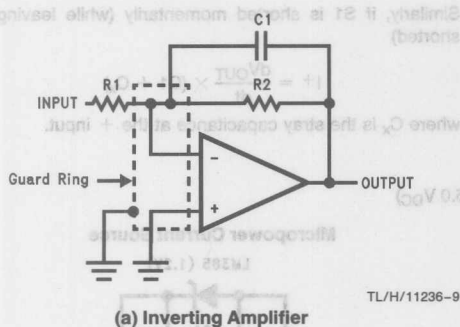


FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

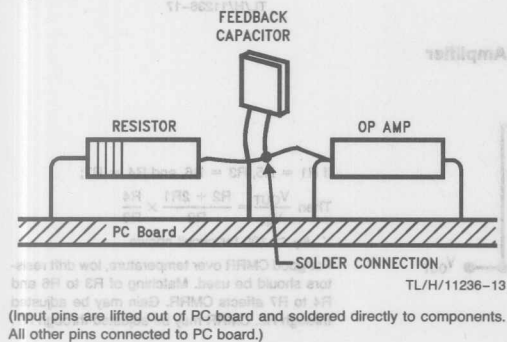


FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 6 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I = \frac{dV_{OUT}}{dt} \times C2$$

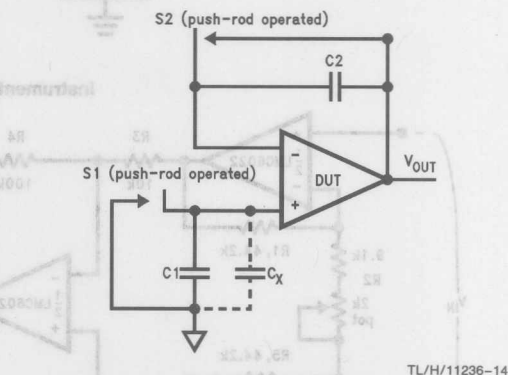
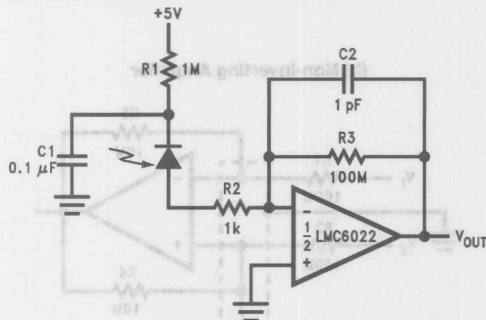


FIGURE 6. Simple Input Bias Current Test Circuit

mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^- , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

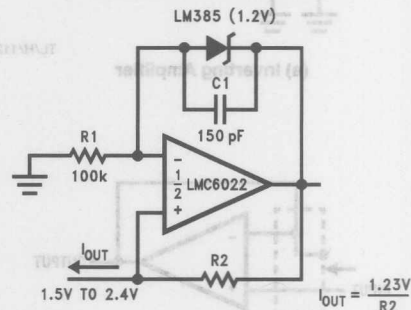
Photodiode Current-to-Voltage Converter



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Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

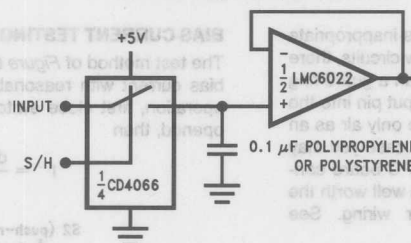
Micropower Current Source



TL/H/11236-16

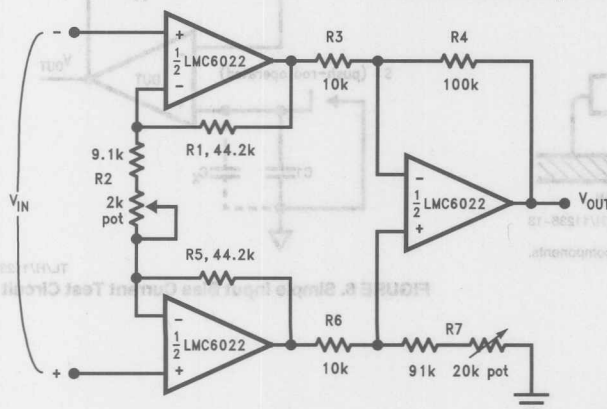
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



TL/H/11236-17

Instrumentation Amplifier



TL/H/11236-18

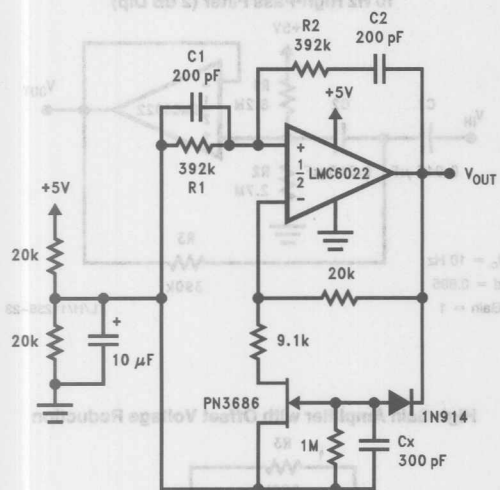
If $R1 = R5$, $R3 = R6$, and $R4 = R7$;

$$\text{Then } \frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_v \approx 100$ for circuit shown

For good CMRR over temperature, low drift resistors should be used. Matching of $R3$ to $R6$ and $R4$ to $R7$ affects CMRR. Gain may be adjusted through $R2$. CMRR may be adjusted through $R7$.

Sine-Wave Oscillator



TL/H/11236-19

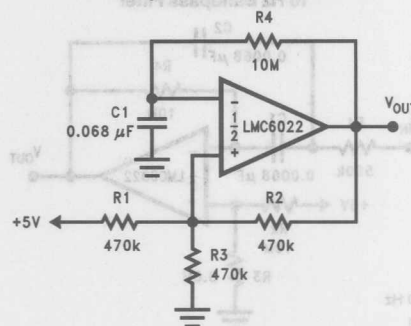
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{osc} = 1/2\pi RC$$

where $R = R1 = R2$ and $C = C1 = C2$.

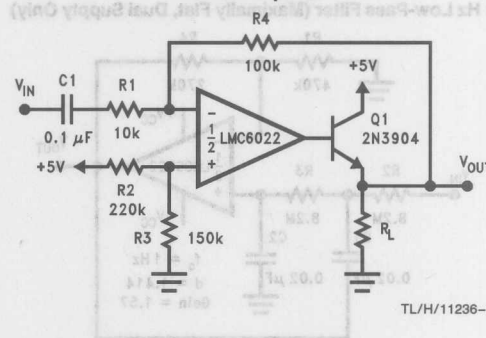
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



TL/H/11236-20

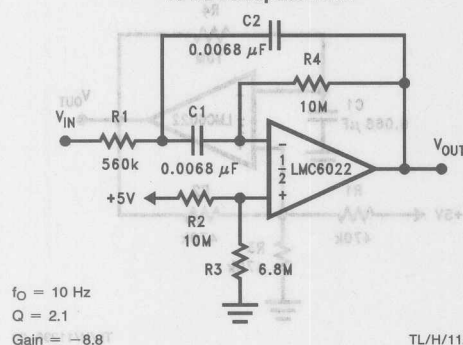
Power Amplifier



TL/H/11236-21

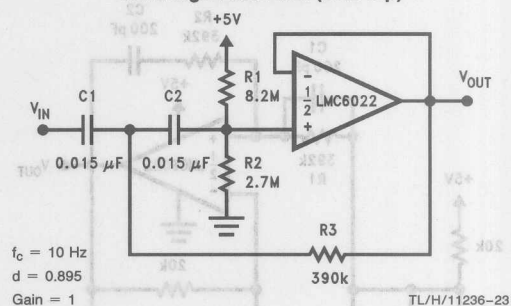
Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

10 Hz Bandpass Filter



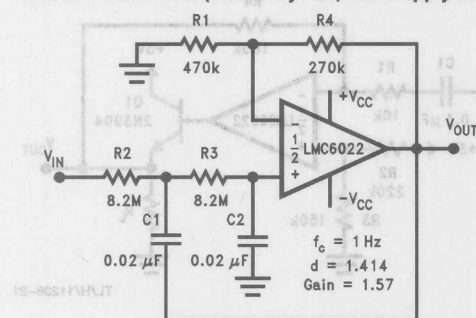
TL/H/11236-22

10 Hz High-Pass Filter (2 dB Dip)



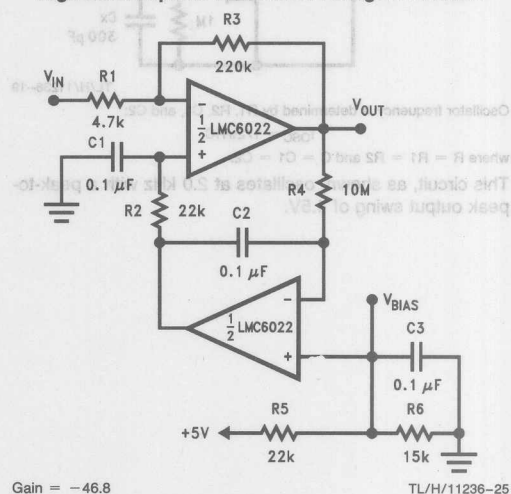
TL/H/11236-23

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



TL/H/11236-24

High Gain Amplifier with Offset Voltage Reduction



TL/H/11236-25

LMC6024 **Low Power CMOS Quad Operational Amplifier**

General Description

The LMC6024 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches V^- , low input bias current and voltage gain (into 100 k Ω and 5 k Ω loads) that is equal to or better than widely accepted bipolar equivalents, while the power supply requirement is less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6022 datasheet for a CMOS dual operational amplifier with these same features.

Features

- Specified for 100 k Ω and 5 k Ω loads
- High voltage gain

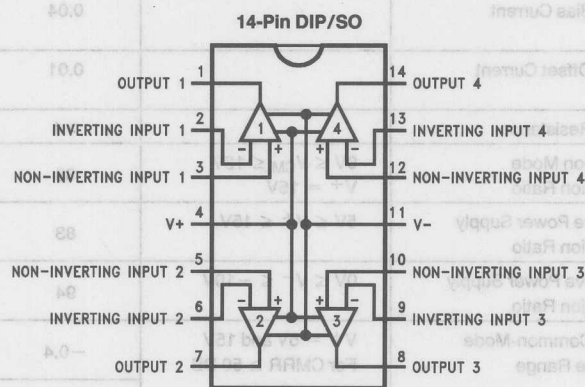
120 dB

- Low offset voltage drift 2.5 $\mu\text{V}/^\circ\text{C}$
- Ultra low input bias current 40 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15V supply
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/ μs
- Micropower operation 1 mW

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls

Connection Diagram



Top View

TL/H/11235-1

Ordering Information

| Temperature Range | Package | NSC Drawing | Transport Media |
|---|-------------------------|-------------|-----------------------|
| Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ | | | |
| LMC6024IN | 14-Pin Molded DIP | N14A | Rail |
| LMC6024IM | 14-Pin Small Outline | M14A | Rail Tape and Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|------------------------------------|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Voltage at Output/Input Pin | (V^+) + 0.3V, (V^-) - 0.3V |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin | ± 18 mA |
| Current at Power Supply Pin | 35 mA |
| Output Short Circuit to V^+ | (Note 12) |
| Output Short Circuit to V^- | (Note 2) |

| | |
|------------------------|----------|
| Junction Temperature | 150°C |
| ESD Tolerance (Note 4) | 1000V |
| Power Dissipation | (Note 3) |

Operating Ratings

| | |
|---|---|
| Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Supply Voltage Range | 4.75V to 15.5V |
| Power Dissipation | (Note 10) |
| Thermal Resistance (θ_{JA}), (Note 11) | |
| 14-Pin DIP | 85°C/W |
| 14-Pin SO | 115°C/W |

DC Electrical Characteristics

The following specifications apply for $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$, and $R_L = 1\text{M}$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6024I Limit (Note 6) | Units |
|--------------------------|--|---|---------------------|--|------------------------------|
| V_{OS} | Input Offset Voltage | | 1 | 9 11 | mV Max |
| $\Delta V_{OS}/\Delta T$ | Input Offset Voltage Average Drift | | 2.5 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.04 | 200 | pA Max |
| I_{OS} | Input Offset Current | | 0.01 | 100 | pA Max |
| R_{IN} | Input Resistance | | > 1 | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12\text{V}$ $V^+ = 15\text{V}$ | 83 | 63 61 | dB Min |
| +PSRR | Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ | 83 | 63 61 | dB Min |
| -PSRR | Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 74 73 | dB Min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ and 15V For CMRR ≥ 50 dB | -0.4 | -0.1 0 | V Max |
| | | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.5$ | V Min |
| A_V | Large Signal Voltage Gain | $R_L = 100\text{ k}\Omega$ (Note 7) Sourcing | 1000 | 200 100 | V/mV Min |
| | | Sinking | 500 | 90 40 | V/mV Min |
| | | $R_L = 5\text{ k}\Omega$ (Note 7) Sourcing | 1000 | 100 75 | V/mV Min |
| | | Sinking | 250 | 50 20 | V/mV Min |

DC Electrical Characteristics (Continued)

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6024 Limit (Note 6) | Units |
|-------------------|----------------------|---|---------------------|------------------------------|----------------|
| V_O V Min | Output Voltage Swing | $V^+ = 5V$ $R_L = 100\text{ k}\Omega$ to $2.5V$ | 4.987 | 4.40 4.43 | V Min |
| | | | 0.004 | 0.06 0.09 | V Max |
| | | $V^+ = 5V$ $R_L = 5\text{ k}\Omega$ to $2.5V$ | 4.940 | 4.20 4.00 | V Min |
| | | | 0.040 | 0.25 0.35 | V Max |
| | | $V^+ = 15V$ $R_L = 100\text{ k}\Omega$ to $7.5V$ | 14.970 | 14.00 13.90 | V Min |
| | | | 0.007 | 0.06 0.09 | V Max |
| | | $V^+ = 15V$ $R_L = 5\text{ k}\Omega$ to $7.5V$ | 14.840 | 13.70 13.50 | V Min |
| | | | 0.110 | 0.32 0.40 | V Max |
| I_O | Output Current | $V^+ = 5V$ Sourcing, $V_O = 0V$ | 22 | 13 9 | mA Min |
| | | Sinking $V_O = 5V$ (Note 2) | 21 | 13 9 | mA Min |
| | | $V^+ = 15V$ Sourcing, $V_O = 0V$ | 40 | 23 15 | mA Min |
| | | Sinking, $V_O = 13V$ (Note 12) | 39 | 23 15 | mA Min |
| | | All Four Amplifiers $V_O = 1.5V$ | 160 | 240 280 | μA Max |

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC60241 Limit (Note 6) | Units |
|------------|------------------------------|------------|---------------------|-------------------------------|------------------------|
| SR | Slew Rate | (Note 8) | 0.11 | 0.05 0.03 | V/ μ s/ Min |
| GBW | Gain-Bandwidth Product | | 0.35 | | MHz |
| θ_M | Phase Margin | | 50 | | Deg |
| G_M | Gain Margin | | 17 | | dB |
| | Amp-to-Amp Isolation | (Note 9) | 130 | | dB |
| e_n | Input-Referred Voltage Noise | F = 1 kHz | 42 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | F = 1 kHz | 0.0002 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharge through a 1.5 k Ω resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or correlation.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$, and R_L connected to 7.5V. For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

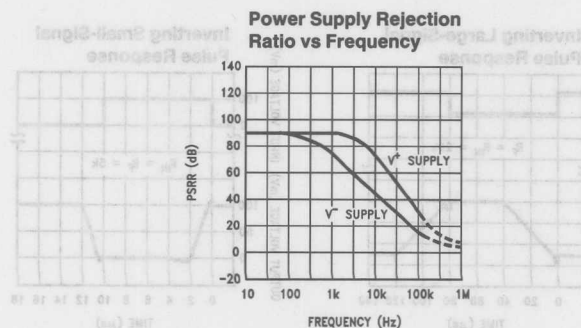
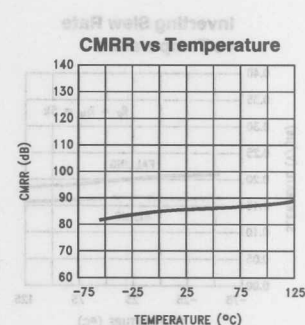
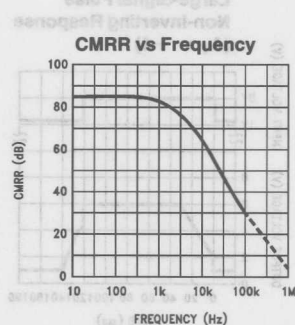
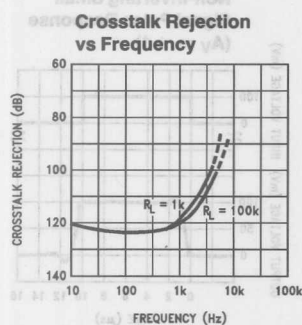
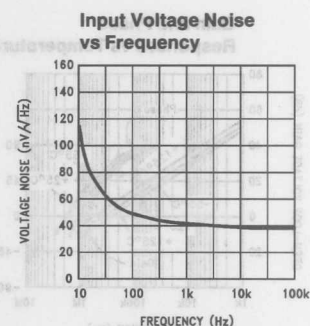
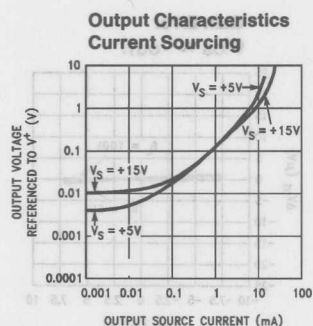
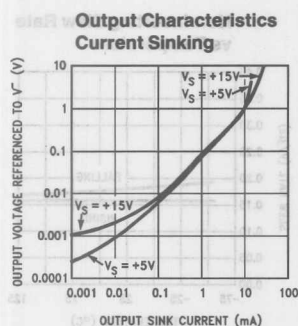
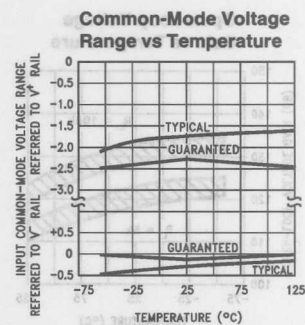
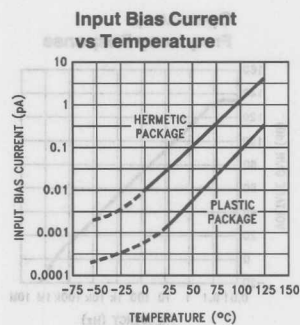
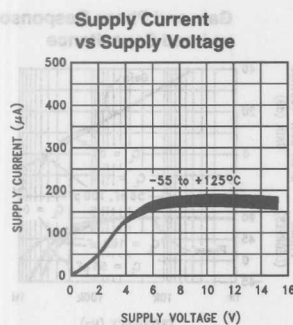
Note 9: Input referred, $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{pp}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

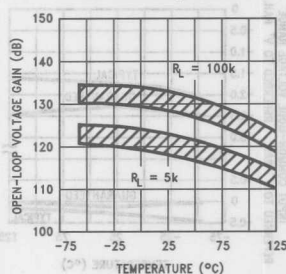
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified



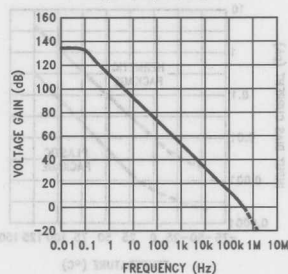
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Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

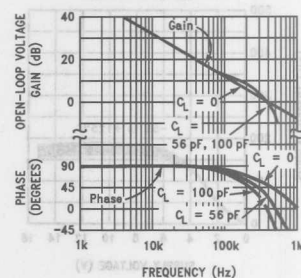
Open-Loop Voltage Gain vs Temperature



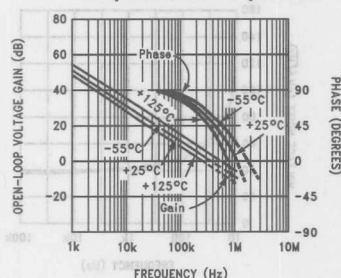
Open-Loop Frequency Response



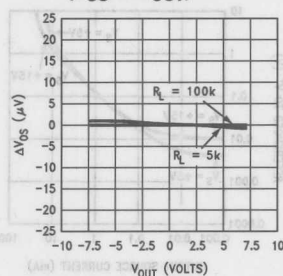
Gain and Phase Responses vs Load Capacitance



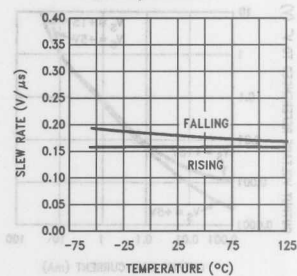
Gain and Phase Responses vs Temperature



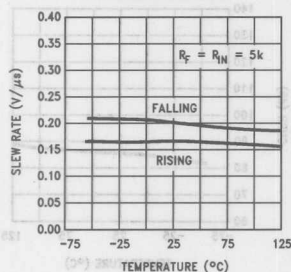
Gain Error (V_{OS} vs V_{OUT})



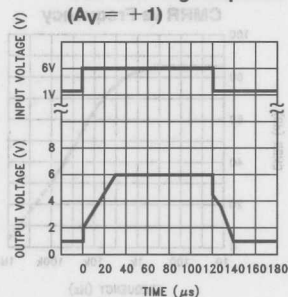
Non-Inverting Slew Rate vs Temperature



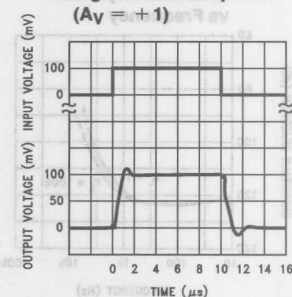
Inverting Slew Rate vs Temperature



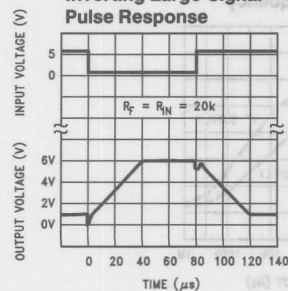
Large-Signal Pulse Non-Inverting Response ($A_v = +1$)



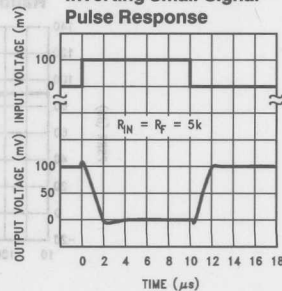
Non-Inverting Small Signal Pulse Response ($A_v = +1$)



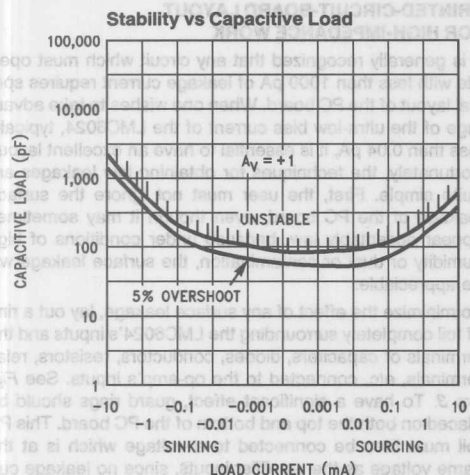
Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response



Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



Note: Avoid resistive loads of less than 500Ω , as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6024 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

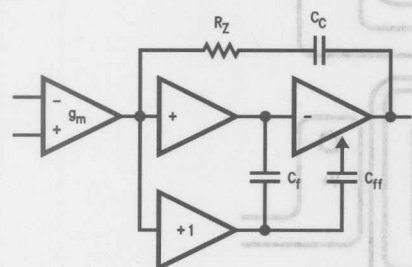
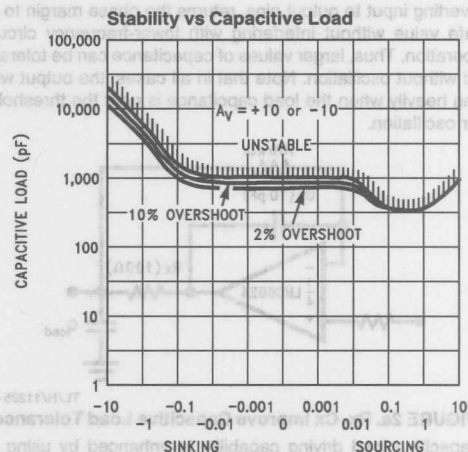


FIGURE 1. LMC6024 Circuit Topology (Each Amplifier)



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The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least $5k\Omega$. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of $5k\Omega$ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

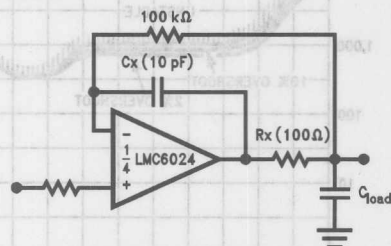
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6024 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor ($5pF$ to $10pF$) from

Application Hints (Continued)

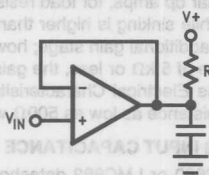
inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



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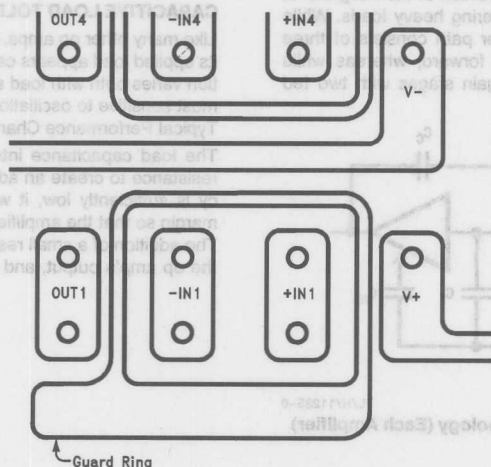
FIGURE 2a. R_x , C_x Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting $50\text{ }\mu\text{A}$ or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



TL/H/11235-26

FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor



TL/H/11235-8

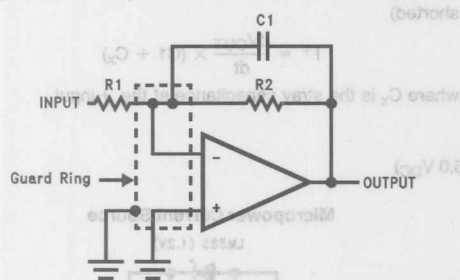
FIGURE 3. Example of Guard Ring in P.C. Board Layout (Using the LMC6024)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

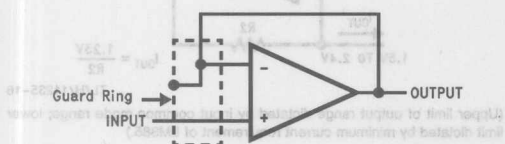
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6024, typically less than 0.04 pA , it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6024's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms , which is normally considered a very large resistance, could leak 5 pA if the trace were a 5 V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6024's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 4d.

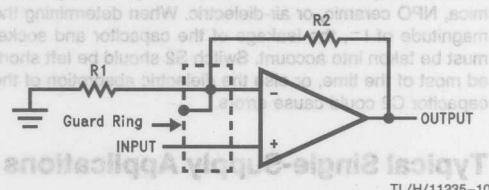
Application Hints (Continued)



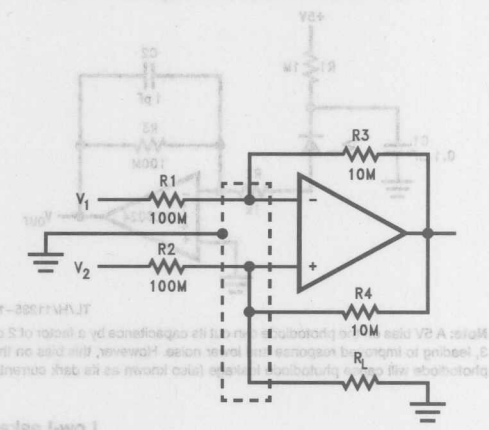
(a) Inverting Amplifier



(c) Follower



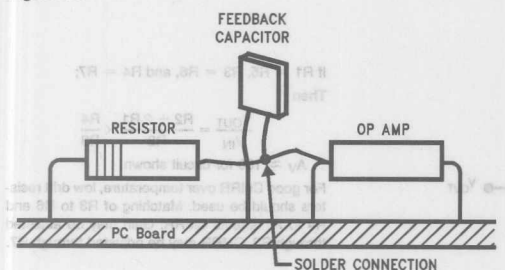
(b) Non-Inverting Amplifier



(d) Howland Current Pump

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-up-in-the-air wiring. See Figure 5.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 6 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

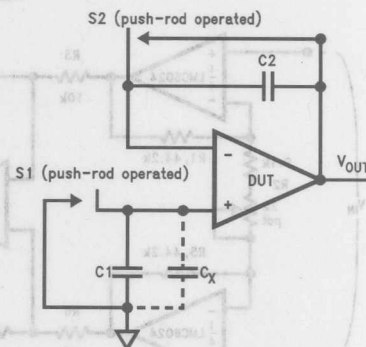
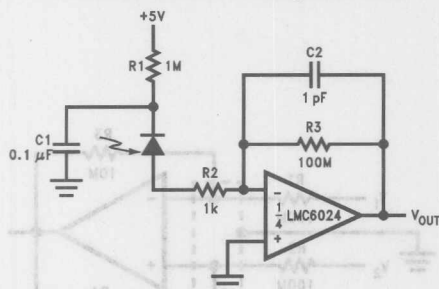


FIGURE 6. Simple Input Bias Current Test Circuit

mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_{-} , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Typical Single-Supply Applications ($V_{+} = 5.0 V_{DC}$)

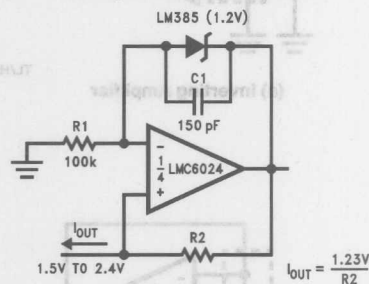
Photodiode Current-to-Voltage Converter



TL/H/11235-15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

Micropower Current Source

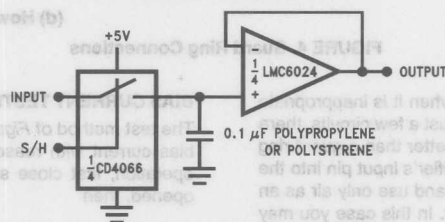


$$I_{OUT} = \frac{1.23V}{R2}$$

TL/H/11235-16

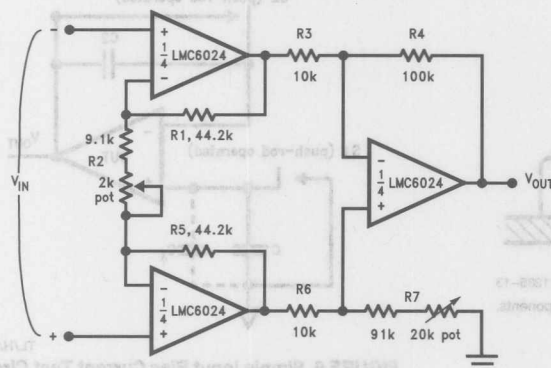
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



TL/H/11235-17

Instrumentation Amplifier



If $R1 = R5$, $R3 = R6$, and $R4 = R7$;

Then

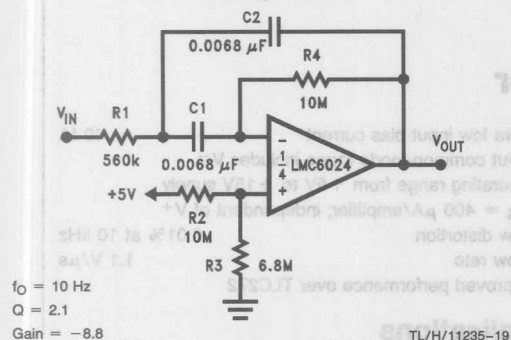
$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

$\therefore A_V \approx 100$ for circuit shown.

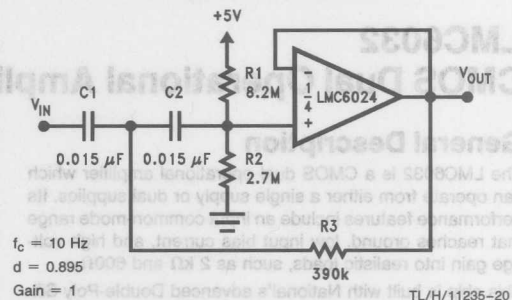
For good CMRR over temperature, low drift resistors should be used. Matching of $R3$ to $R6$ and $R4$ to $R7$ affects CMRR. Gain may be adjusted through $R2$. CMRR may be adjusted through $R7$.

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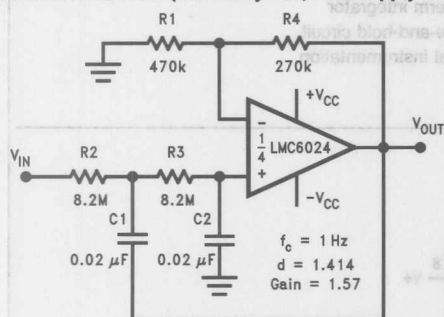
10 Hz Bandpass Filter



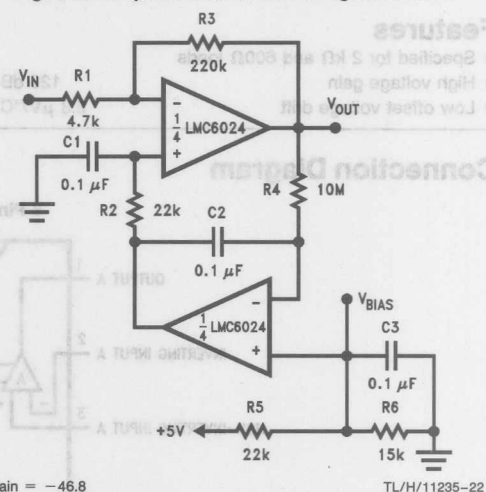
10 Hz High-Pass Filter (2 dB Dip)



1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



High Gain Amplifier with Offset Voltage Reduction



| Temperature Range | Industrial | Package | NWC Drawing | Transport Media |
|---|------------|---------------------|-------------|--------------------|
| | | | | |
| $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ | LMC6024M | 8-Pin Molded DIP | MOSE | Full |
| | LMC6024M | 8-Pin Small Outline | MOSE | Full Tape and Reel |



LMC6032 CMOS Dual Operational Amplifier

General Description

The LMC6032 is a CMOS dual operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 k Ω and 600 Ω .

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6034 datasheet for a CMOS quad operational amplifier with these same features. For higher performance characteristics refer to the LMC662.

Features

- Specified for 2 k Ω and 600 Ω loads
- High voltage gain
- Low offset voltage drift

126 dB
2.3 $\mu\text{V}/^\circ\text{C}$

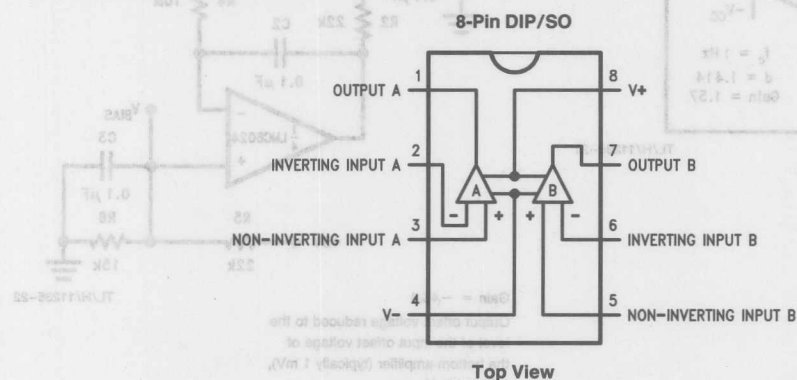
- Ultra low input bias current
- Input common-mode range includes V_{-}
- Operating range from +5V to +15V supply
- $I_{SS} = 400 \mu\text{A}/\text{amplifier}$; independent of V_{+}
- Low distortion
- Low rate
- Improved performance over TLC272

0.01% at 10 kHz
1.1 V/ μs

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

Connection Diagram



TL/H/11135-1

Ordering Information

| Temperature Range | Package | NSC Drawing | Transport Media |
|---|---------------------|-------------|--------------------|
| Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ | | | |
| LMC6032IN | 8-Pin Molded DIP | N08E | Rail |
| LMC6032IM | 8-Pin Small Outline | M08A | Rail Tape and Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|----------------------|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^+ | (Note 10) |
| Output Short Circuit to V^- | (Note 2) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| ESD Tolerance (Note 4) | 1000V |

Power Dissipation (Note 3)

Voltage at Output/Input Pin (V^+) + 0.3V,
(V^-) - 0.3V

| | |
|-----------------------------|-------------|
| Current at Output Pin | ± 18 mA |
| Current at Input Pin | ± 5 mA |
| Current at Power Supply Pin | 35 mA |

Operating Ratings (Note 1)

| | |
|---|-----------------------------|
| Temperature Range | -40°C $\leq T_J \leq$ +85°C |
| Supply Voltage Range | 4.75V to 15.5V |
| Power Dissipation | (Note 11) |
| Thermal Resistance (θ_{JA}), (Note 12) | |
| 8-Pin DIP | 101°C/W |
| 8-Pin SO | 165°C/W |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_{OUT} = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6032I Limit (Note 6) | Units |
|--------------------------|--|---|--|---|--|
| V_{OS} | Input Offset Voltage | | 1 | 9 11 | mV max |
| $\Delta V_{OS}/\Delta T$ | Input Offset Voltage Average Drift | | 2.3 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.04 | 200 | pA max |
| I_{OS} | Input Offset Current | | 0.01 | 100 | pA max |
| R_{IN} | Input Resistance | | > 1 | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12\text{V}$ $V^+ = 15\text{V}$ | 83 | 63 60 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$ | 83 | 63 60 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 74 70 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V} \text{ \& } 15\text{V}$ For CMRR ≥ 50 dB | -0.4 $V^+ - 1.9$ | -0.1 0 $V^+ - 2.3$ $V^+ - 2.6$ | V max V min |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ (Note 7) Sourcing Sinking $R_L = 600\Omega$ (Note 7) Sourcing Sinking | 2000 500 1000 250 | 200 100 90 40 100 75 50 20 | V/mV min V/mV min V/mV min V/mV min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_{\text{OUT}} = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6032 Limit (Note 6) | Units | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---------------------------------|---|---------------------|------------------------------|-----------|-----------------|---------------------------------|--|-------------|--------|---|-------|---------------------------|-----------------------------------|----------|-----|------|-----|------|----|------|----------------------------|---------|-----|------|-----|------|----|------|--|--|--|---------|----|------|----|------|
| V_O | Output Voltage Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.20 4.00 | V min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0.10 | 0.25 0.35 | V max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V | 4.61 | 4.00 3.80 | V min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0.30 | 0.63 0.75 | V max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 13.50 13.00 | V min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0.26 | 0.45 0.55 | V max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| V_m max | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V | 13.90 | 12.50 12.00 | V min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 0.79 | 1.45 1.75 | V max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | $V^+ = 5\text{V}$ Sourcing, $V_O = 0\text{V}$ | 22 | 13 9 | mA min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 21 | 13 9 | mA min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I_O | Output Current | $V^+ = 15\text{V}$ Sourcing, $V_O = 0\text{V}$ | 40 | 23 15 | mA min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | 39 | 23 15 | mA min | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | Sinking, $V_O = 13\text{V}$ (Note 10) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| I_S | Supply Current | Both Amplifiers $V_O = 1.5\text{V}$ | 0.75 | 1.6 1.9 | mA max | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1"> <tr> <td rowspan="2">V_{CM}</td> <td rowspan="2">Input Common-Mode Voltage Range</td> <td rowspan="2">$V^+ = 5\text{V}$ to 15V For CMRR $> 80\text{ dB}$</td> <td rowspan="2">$V^+ - 1.5$</td> <td rowspan="2">-0.4</td> <td rowspan="2">V</td> </tr> <tr> </tr> <tr> <td rowspan="6">A_V</td> <td rowspan="6">Large Signal Voltage Gain</td> <td rowspan="3">$R_L = 2\text{ k}\Omega$ (Note 7)</td> <td rowspan="3">Sourcing</td> <td>200</td> <td>V/mV</td> </tr> <tr> <td>100</td> <td>V/mV</td> </tr> <tr> <td>90</td> <td>V/mV</td> </tr> <tr> <td rowspan="3">$R_L = 800\Omega$ (Note 7)</td> <td rowspan="3">Sinking</td> <td>800</td> <td>V/mV</td> </tr> <tr> <td>100</td> <td>V/mV</td> </tr> <tr> <td>75</td> <td>V/mV</td> </tr> <tr> <td rowspan="2"></td> <td rowspan="2"></td> <td rowspan="2"></td> <td rowspan="2">Sinking</td> <td>50</td> <td>V/mV</td> </tr> <tr> <td>50</td> <td>V/mV</td> </tr> </table> | | | | | | V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ to 15V For CMRR $> 80\text{ dB}$ | $V^+ - 1.5$ | -0.4 | V | A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ (Note 7) | Sourcing | 200 | V/mV | 100 | V/mV | 90 | V/mV | $R_L = 800\Omega$ (Note 7) | Sinking | 800 | V/mV | 100 | V/mV | 75 | V/mV | | | | Sinking | 50 | V/mV | 50 | V/mV |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ to 15V For CMRR $> 80\text{ dB}$ | $V^+ - 1.5$ | -0.4 | V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ (Note 7) | Sourcing | 200 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 100 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 90 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | $R_L = 800\Omega$ (Note 7) | Sinking | 800 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 100 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 75 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | Sinking | 50 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | 50 | V/mV | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_{\text{OUT}} = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6032I Limit (Note 6) | Units |
|----------|------------------------------|--|---------------------|-------------------------------|-------------------------------|
| SR | Slew Rate | (Note 8) | 1.1 | 0.8 0.4 | $\text{V}/\mu\text{s}$ min |
| GBW | Gain-Bandwidth Product | | 1.4 | | MHz |
| ϕ_M | Phase Margin | | 50 | | Deg |
| G_M | Gain Margin | | 17 | | dB |
| | Amp-to-Amp Isolation | (Note 9) | 130 | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{\text{PP}}$ $\pm 5\text{V}$ Supply | 0.01 | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a $1.5\text{ k}\Omega$ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: $V^+ = 15\text{V}$, $V_{\text{CM}} = 7.5\text{V}$, and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

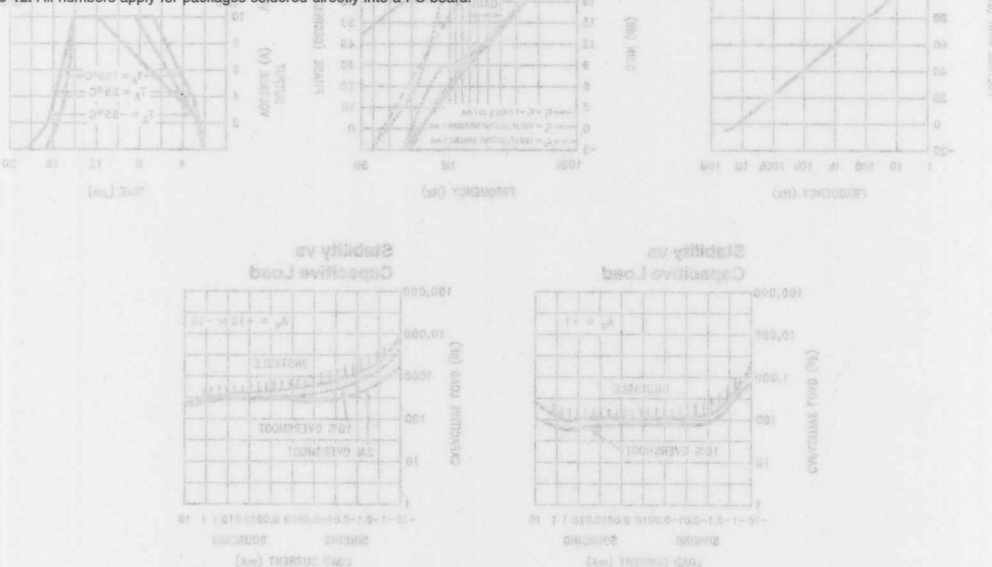
Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

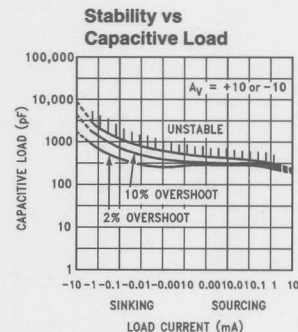
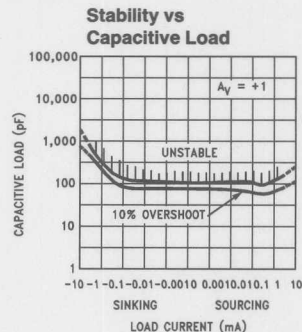
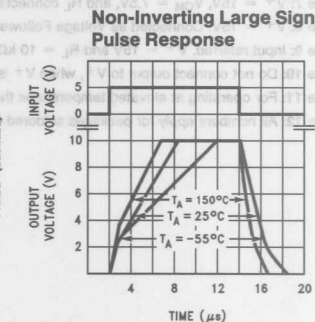
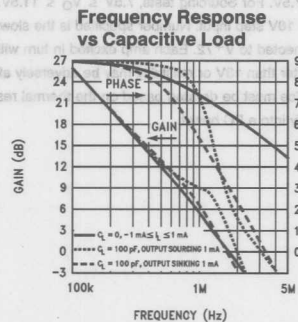
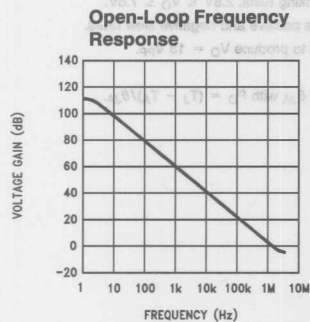
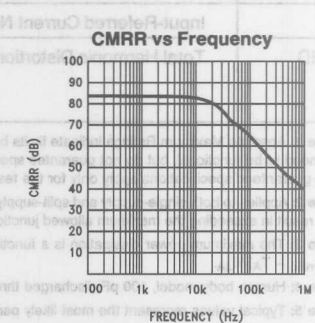
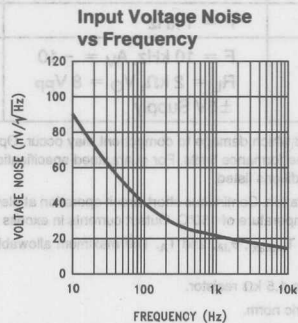
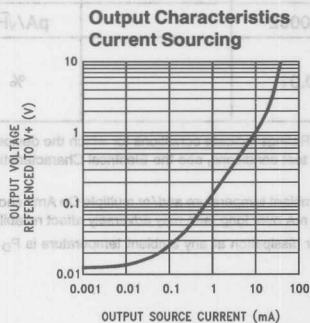
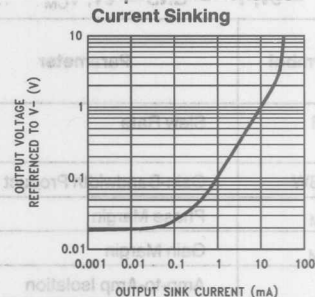
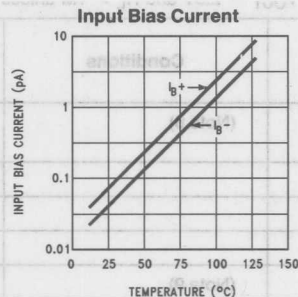
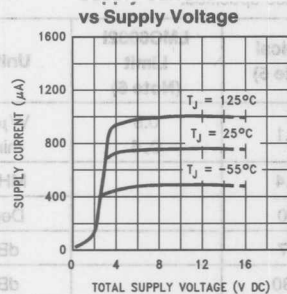
Note 9: Input referred. $V^+ = 15\text{V}$ and $R_L = 10\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{\text{PP}}$.

Note 10: Do not connect output to V^+ , when V^+ is greater than 13V or reliability may be adversely affected.

Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 12: All numbers apply for packages soldered directly into a PC board.





Note: Avoid resistive loads of less than 500Ω , as they may cause instability.

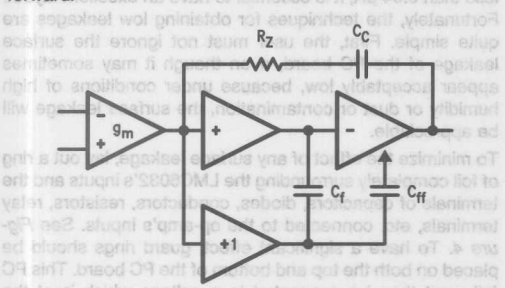
TL/H/11135-2

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC6032, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11135-3

FIGURE 1. LMC6032 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC6032 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier Circuit, *Figure 2*, the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_p}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capaci-

tance from the IC socket (if one is used), circuit board traces, etc., and R_p is the parallel combination of R_F and R_{IN} . This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" -3 dB frequency, a feedback capacitor, C_F , should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability, a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \leq \sqrt{6 \times 2\pi \times \text{GBW} \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1 \right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1 \right)$$

regardless of whether the amplifier is being used in an inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1 \right) \geq 2\sqrt{\text{GBW} \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2 \left(\frac{R_F}{R_{IN}} + 1 \right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1 \right) < 2\sqrt{\text{GBW} \times R_F \times C_S},$$

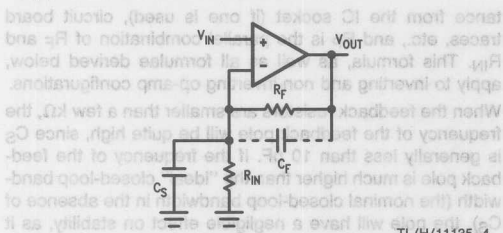
the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{\text{GBW} \times R_F}}$$

Note that these capacitor values are usually significantly smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$

Application Hints (Continued)



TL/H/11135-4

FIGURE 2. General Operational Amplifier Circuit

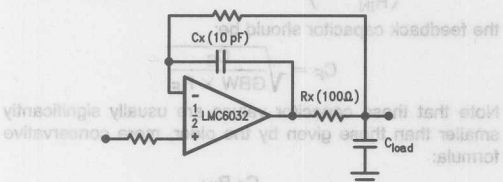
C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistor.

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the value of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC6032 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 3a, the addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

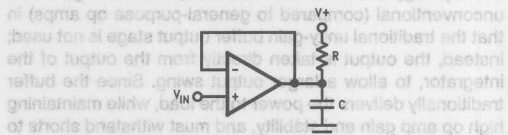


TL/H/11135-5

FIGURE 3a. R_x , C_x Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 3b). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open

loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



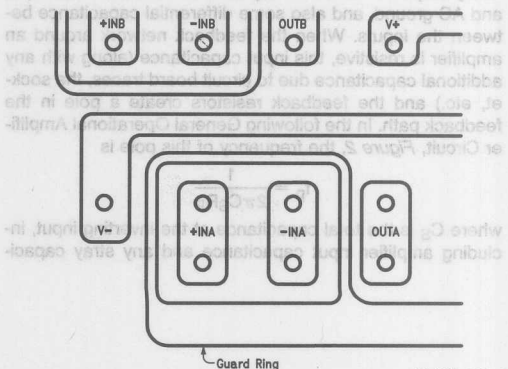
TL/H/11135-22

FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6032, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

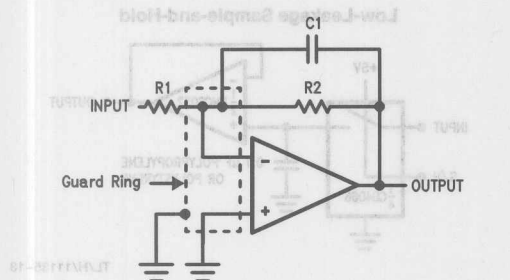
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6032's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 4. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6032's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11} \Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 5a, 5b, 5c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 5d.



TL/H/11135-6

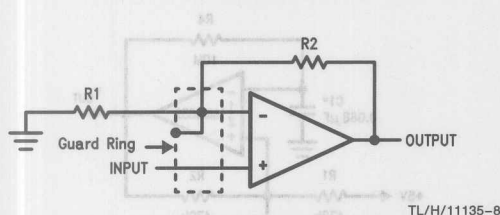
FIGURE 4. Example of Guard Ring in P.C. Board Layout

Application Hints (Continued)



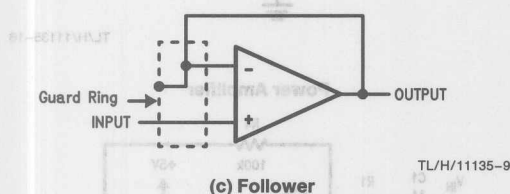
(a) Inverting Amplifier

TL/H/11135-7



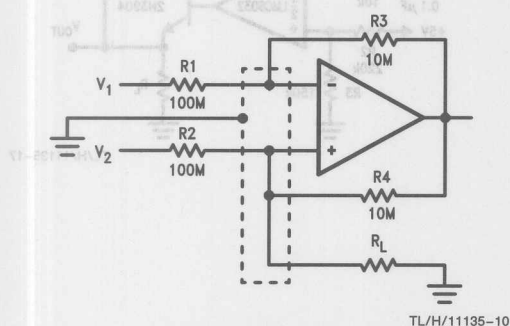
(b) Non-Inverting Amplifier

TL/H/11135-8



(c) Follower

TL/H/11135-9



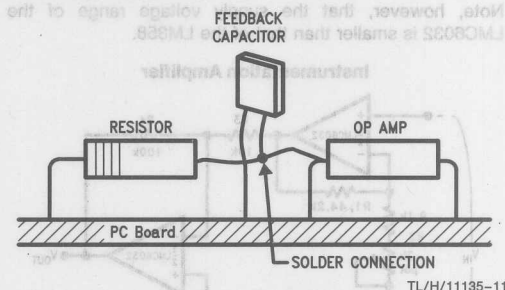
(d) Howland Current Pump

TL/H/11135-10

FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an

insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 6.



TL/H/11135-11

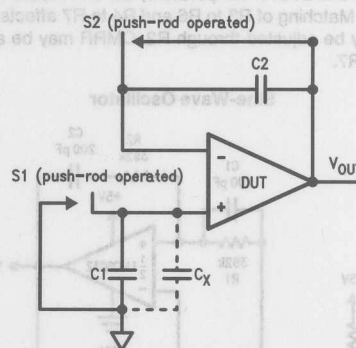
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 7 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_{b-} = \frac{dV_{OUT}}{dt} \times C2.$$



TL/H/11135-12

FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_{b-} , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

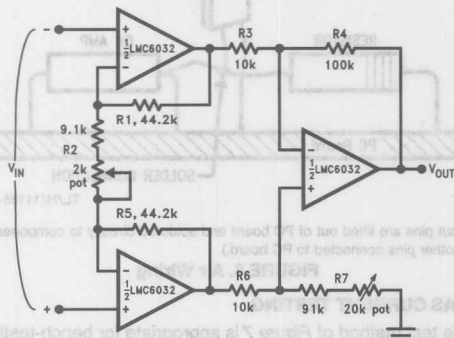
$$I_{b+} = \frac{dV_{OUT}}{dt} \times (C1 + Cx)$$

where Cx is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

Additional single-supply applications ideas can be found in the LM358 datasheet. The LMC6032 is pin-for-pin compatible with the LM358 and offers greater bandwidth and input resistance over the LM358. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6032 is smaller than that of the LM358.

Instrumentation Amplifier



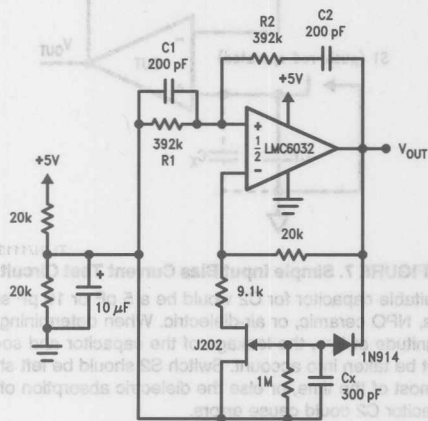
TL/H/11135-14

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3} \quad \text{if } R_1 = R_5; \\ R_3 = R_6, \text{ and } R_4 = R_7.$$

= 100 for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affects CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



TL/H/11135-15

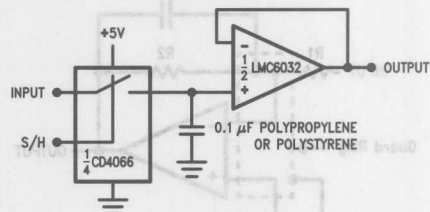
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{osc} = 1/2\pi RC$$

where $R = R_1 = R_2$ and $C = C_1 = C_2$.

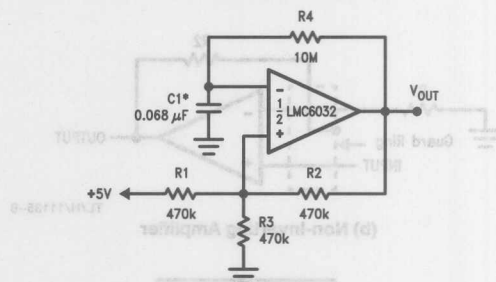
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

Low-Leakage Sample-and-Hold



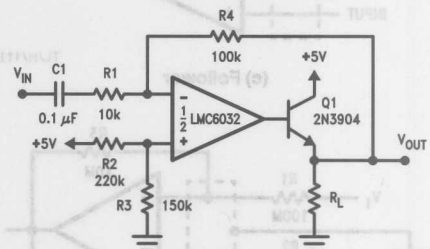
TL/H/11135-13

1 Hz Square-Wave Oscillator



TL/H/11135-16

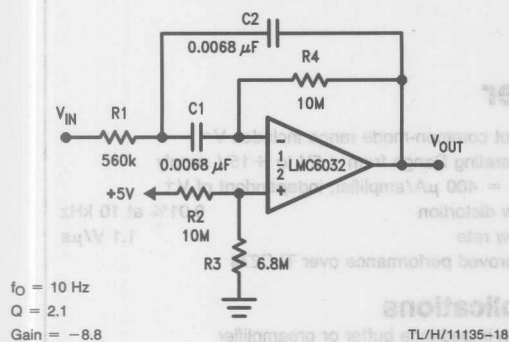
Power Amplifier



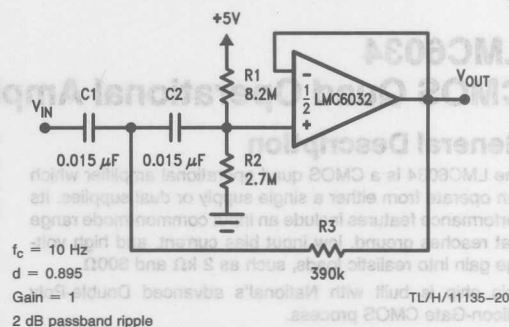
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Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

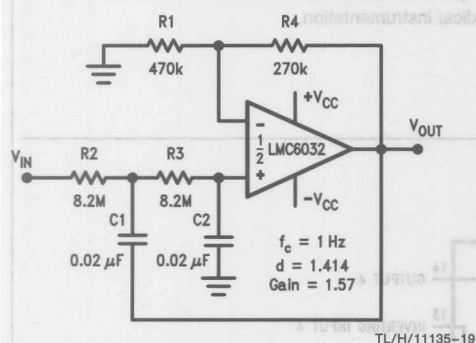
10 Hz Bandpass Filter



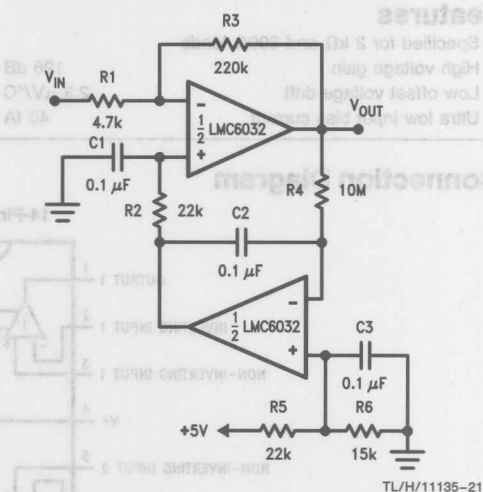
10 Hz High-Pass Filter



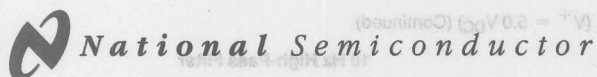
1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



High Gain Amplifier with Offset Voltage Reduction



| Temperature Range | Industrial | Package | NWC | Transport Media |
|-------------------|------------|---------------|------|-----------------|
| | | | | |
| -40°C to +85°C | LMC6032N | 14-Pin | MTAA | Roll |
| | | Molded DIP | | |
| | LMC6032M | 14-Pin | MTAA | Roll |
| | | Small Outline | | Tape and Reel |



LMC6034 CMOS Quad Operational Amplifier

General Description

The LMC6034 is a CMOS quad operational amplifier which can operate from either a single supply or dual supplies. Its performance features include an input common-mode range that reaches ground, low input bias current, and high voltage gain into realistic loads, such as 2 k Ω and 600 Ω .

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6032 datasheet for a CMOS dual operational amplifier with these same features. For higher performance characteristics refer to the LMC660.

Features

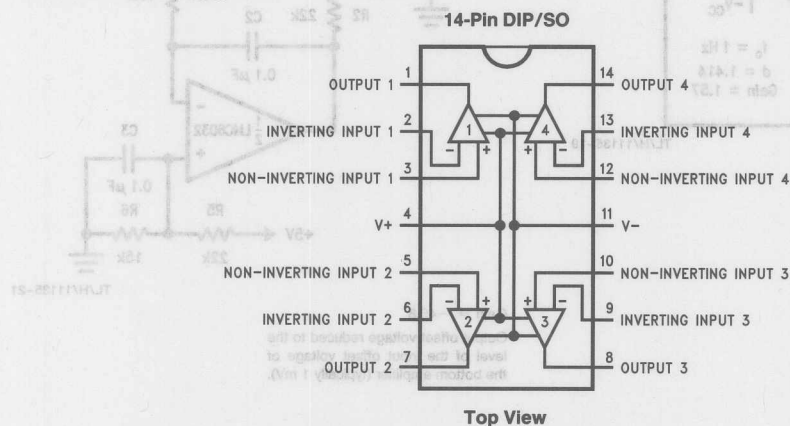
- Specified for 2 k Ω and 600 Ω loads
- High voltage gain 126 dB
- Low offset voltage drift 2.3 $\mu\text{V}/^\circ\text{C}$
- Ultra low input bias current 40 fA

- Input common-mode range includes V^-
- Operating Range from +5V to +15V supply
- $I_{SS} = 400 \mu\text{A}/\text{amplifier}$; independent of V^+
- Low distortion 0.01% at 10 kHz
- Slew rate 1.1 V/ μs
- Improved performance over TLC274

Applications

- High-impedance buffer or preamplifier
- Current-to-voltage converter
- Long-term integrator
- Sample-and-hold circuit
- Medical instrumentation

Connection Diagram



TL/H/11134-1

Ordering Information

| Temperature Range | Package | NSC Drawing | Transport Media |
|---|-------------------------|-------------|-----------------------|
| Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ | | | |
| LMC6034IN | 14-Pin Molded DIP | N14A | Rail |
| LMC6034IM | 14-Pin Small Outline | M14A | Rail Tape and Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|---|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^+ | (Note 10) |
| Output Short Circuit to V^- | (Note 2) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Power Dissipation | (Note 3) |
| Voltage at Output/Input Pin (V^+) | $+0.3\text{V}$, (V^-) -0.3V |
| Current at Output Pin | $\pm 18\text{ mA}$ |
| Current at Input Pin | $\pm 5\text{ mA}$ |

Current at Power Supply Pin

35 mA

Junction Temperature (Note 3)

150°C

ESD Tolerance (Note 4)

1000V

Operating Ratings (Note 1)

| | |
|---|---|
| Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Supply Voltage Range | 4.75V to 15.5V |
| Power Dissipation | (Note 11) |
| Thermal Resistance (θ_{JA}), (Note 12) | |
| 14-Pin DIP | 85°C/W |
| 14-Pin SO | 115°C/W |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_{OUT} = 2.5\text{V}$, and $R_L > 1\text{M}\Omega$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6034I Limit (Note 6) | Units |
|--------------------------|--|---|--|---|--|
| V_{OS} | Input Offset Voltage | | 1 | 9 11 | mV max |
| $\Delta V_{OS}/\Delta T$ | Input Offset Voltage Average Drift | | 2.3 | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.04 | 200 | pA max |
| I_{OS} | Input Offset Current | | 0.01 | 100 | pA max |
| R_{IN} | Input Resistance | | > 1 | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12\text{V}$ $V^+ = 15\text{V}$ | 83 | 63 60 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$ | 83 | 63 60 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 74 70 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V} \text{ \& } 15\text{V}$ For CMRR $\geq 50\text{ dB}$ | -0.4 $V^+ - 1.9$ | -0.1 0 $V^+ - 2.3$ $V^+ - 2.6$ | V max V min |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ (Note 7) Sourcing Sinking $R_L = 600\Omega$ (Note 7) Sourcing Sinking | 2000 500 1000 250 | 200 100 90 40 100 75 50 20 | V/mV min V/mV min V/mV min V/mV min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes, $V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_{\text{OUT}} = 2.5\text{V}$, and $R_L \geq 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6034 Limit (Note 6) | Units |
|-----------------|----------------------|--|---------------------|------------------------------|------------|
| V_O | Output Voltage Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.20 4.00 | V min |
| | | | 0.10 | 0.25 0.35 | V max |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V | 4.61 | 4.00 3.80 | V min |
| | | | 0.30 | 0.63 0.75 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 13.50 13.00 | V min |
| | | | 0.26 | 0.45 0.55 | V max |
| V_m max | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V | 13.90 | 12.50 12.00 | V min |
| | | | 0.79 | 1.45 1.75 | V max |
| | | | | | |
| | | | | | |
| I_O | Output Current | $V^+ = 5\text{V}$ Sourcing, $V_O = 0\text{V}$ | 22 | 13 9 | mA min |
| | | Sinking, $V_O = 5\text{V}$ | 21 | 13 9 | mA min |
| | | $V^+ = 15\text{V}$ Sourcing, $V_O = 0\text{V}$ | 40 | 23 15 | mA min |
| | | Sinking, $V_O = 13\text{V}$ (Note 10) | 39 | 23 15 | mA min |
| I_S | Supply Current | All Four Amplifiers $V_O = 1.5\text{V}$ | 1.5 | 2.7 3.0 | mA max |
| V_{CM} | | $V^+ = 5\text{V}$ & 15V For CMRR $\geq 50\text{ dB}$ | | | |
| A_V | | $R_L = 2\text{ k}\Omega$ (Note 7) | | | |
| | | Sourcing | | | |
| | | Sinking | | | |
| | | $R_L = 800\Omega$ (Note 7) | | | |
| | | Sourcing | | | |
| | | Sinking | | | |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_{\text{OUT}} = 2.5\text{V}$, and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6034I Limit (Note 6) | Units |
|----------|------------------------------|--|---------------------|-------------------------------|-------------------------------|
| SR | Slew Rate | (Note 8) | 1.1 | 0.8 0.4 | $\text{V}/\mu\text{s}$ min |
| GBW | Gain-Bandwidth Product | | 1.4 | | MHz |
| ϕ_M | Phase Margin | | 50 | | Deg |
| G_M | Gain Margin | | 17 | | dB |
| | Amp-to-Amp Isolation | (Note 9) | 130 | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{\text{PP}}$ $\pm 5\text{V Supply}$ | 0.01 | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, 100 pF discharged through a $1.5\text{ k}\Omega$ resistor.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 7: $V^+ = 15\text{V}$, $V_{\text{CM}} = 7.5\text{V}$, and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

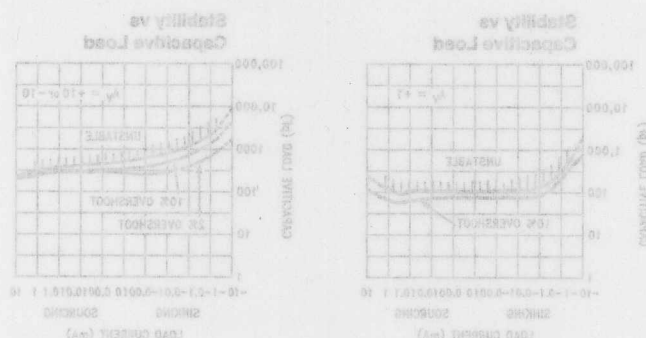
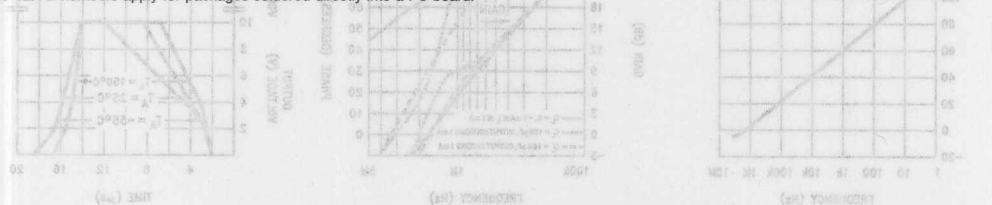
Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred. $V^+ = 15\text{V}$ and $R_L = 10\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{\text{PP}}$.

Note 10: Do not connect output to V^+ , when V^+ is greater than 13V or reliability may be adversely affected.

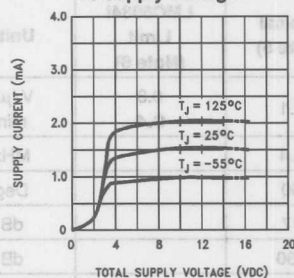
Note 11: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 12: All numbers apply for packages soldered directly into a PC board.

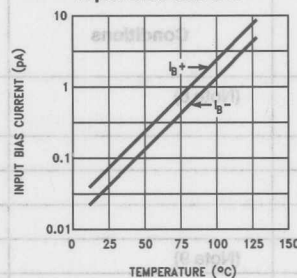


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified

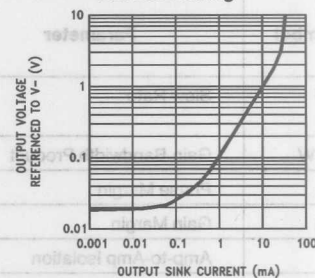
Supply Current vs Supply Voltage



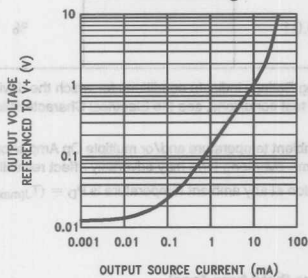
Input Bias Current



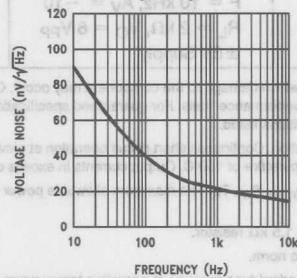
Output Characteristics Current Sinking



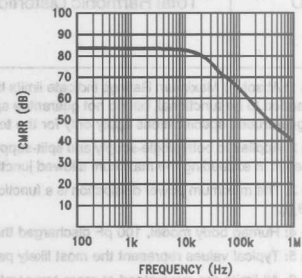
Output Characteristics Current Sourcing



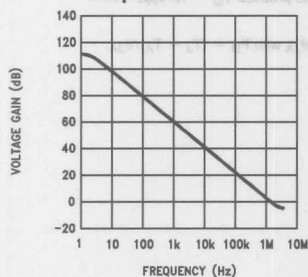
Input Voltage Noise vs Frequency



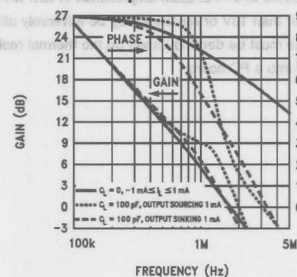
CMRR vs Frequency



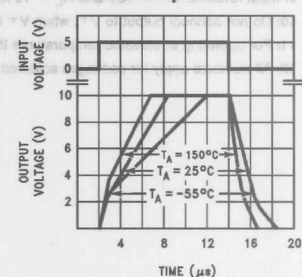
Open-Loop Frequency Response



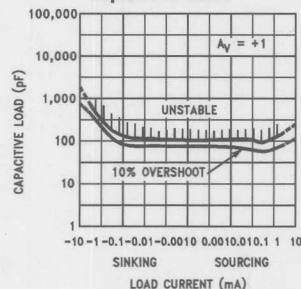
Frequency Response vs Capacitive Load



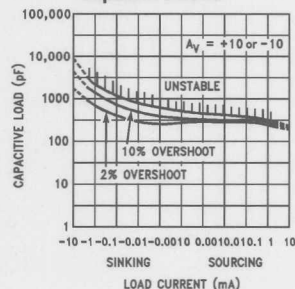
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load



Stability vs Capacitive Load



Note: Avoid resistive loads of less than 500Ω, as they may cause instability.

TL/H/11134-2

The topology chosen for the LMC6034, shown in Figure 1, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow a larger output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

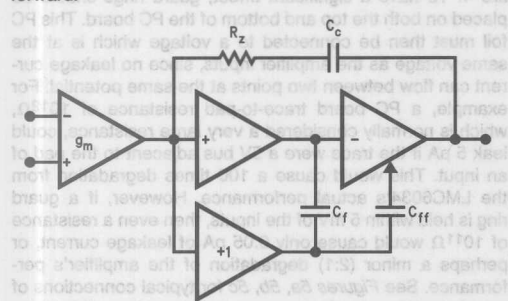


FIGURE 1. LMC6034 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics.

Compensating Input Capacitance

The high input resistance of the LMC6034 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit, Figure 2 the frequency of this pole is

$$f_p = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN} . This formula, as well as all formulae derived below, apply to inverting and non-inverting op-amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S

width (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" -3 dB frequency, a feedback capacitor, C_F , should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times \text{GBW} \times R_F \times C_S}$$

where $\left(\frac{R_F}{R_{IN}} + 1\right)$ is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the

formula $\left(\frac{R_F}{R_{IN}} + 1\right)$ regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{\text{GBW} \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{\text{GBW} \times R_F \times C_S}$$

the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{\text{GBW} \times R_F}}$$

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$

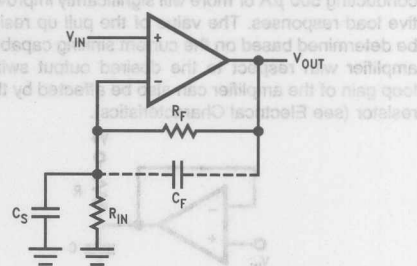


FIGURE 2. General Operational Amplifier Circuit

C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

Applications Hint (Continued)

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

Capacitive Load Tolerance

Like many other op amps, the LMC6034 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in Figure 3a, the addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

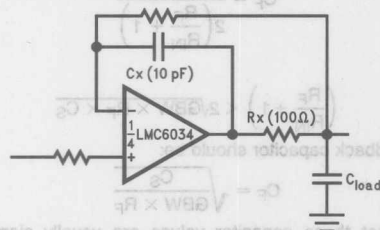


FIGURE 3a. R_x , C_x Improve Capacitive Load Tolerance
TL/H/11134-5

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 3b). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

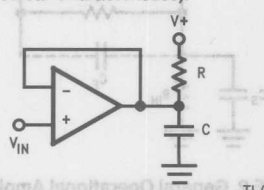


FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor
TL/H/11134-22

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6034, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6034's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 4. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC6034's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11} \Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 5a, 5b, 5c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 5d.

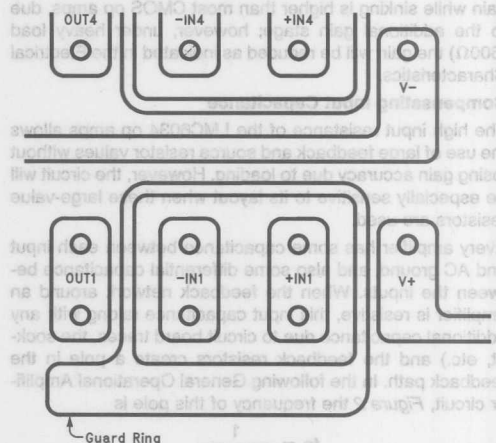


FIGURE 4. Example of Guard Ring in P.C. Board Layout
TL/H/11134-6

Application Hints (Continued)

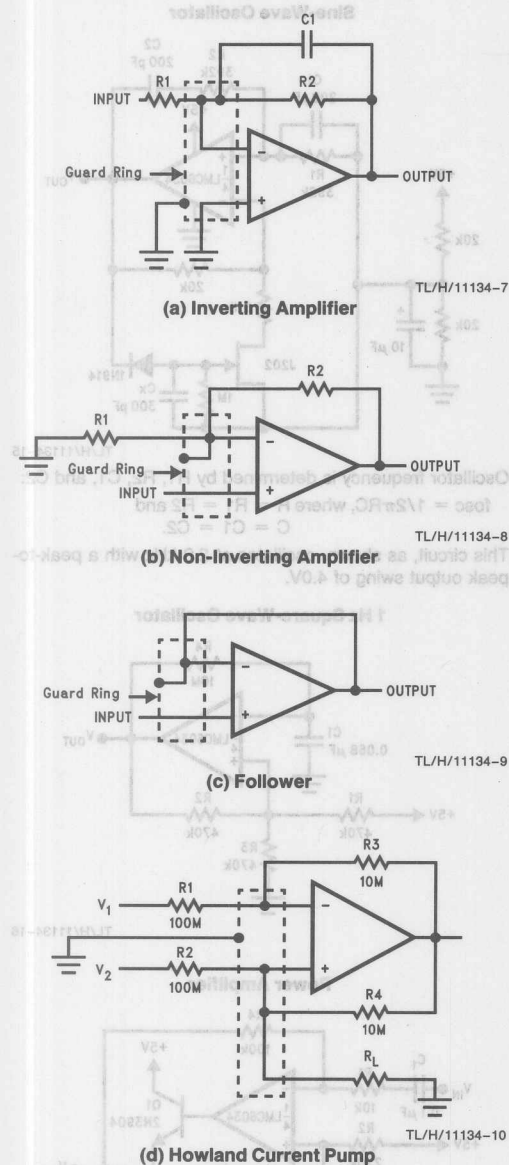
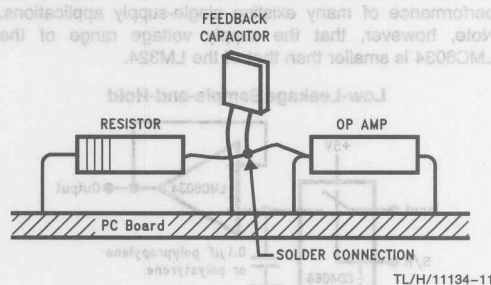


FIGURE 5. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may

have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 6.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 6. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 7 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_{b-} = \frac{dV_{OUT}}{dt} \times C_2$$

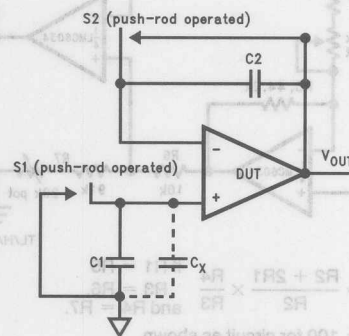


FIGURE 7. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_{b-} , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

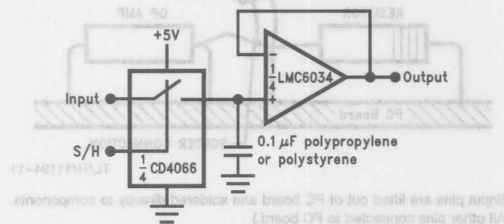
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I_{b+} = \frac{dV_{OUT}}{dt} \times (C_1 + C_x)$$

where C_x is the stray capacitance at the + input.

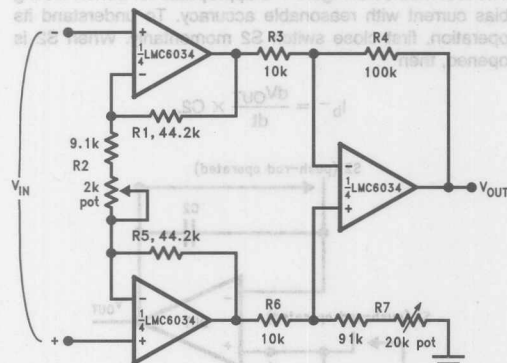
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC6034 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC6034 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



TL/H/11134-13

Instrumentation Amplifier



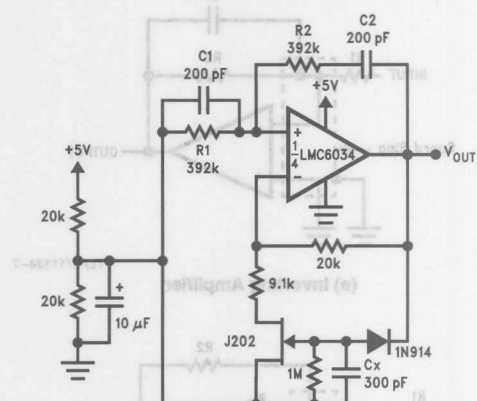
TL/H/11134-14

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3} \quad \begin{array}{l} \text{if } R_1 = R_5 \\ R_3 = R_6, \\ \text{and } R_4 = R_7. \end{array}$$

$$= 100 \text{ for circuit as shown.}$$

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-wave Oscillator



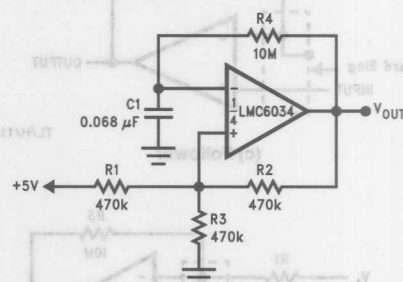
TL/H/11134-15

Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{osc} = 1/2\pi RC, \text{ where } R = R_1 = R_2 \text{ and } C = C_1 = C_2.$$

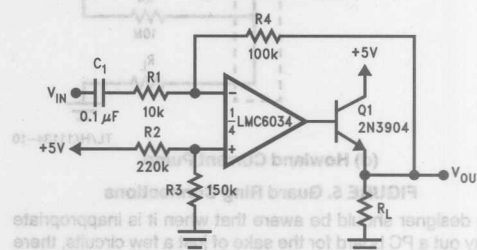
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.0V.

1 Hz Square-Wave Oscillator



TL/H/11134-16

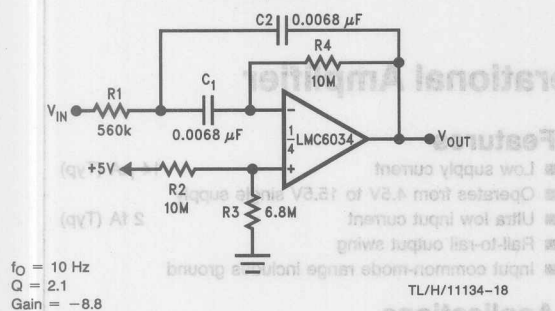
Power Amplifier



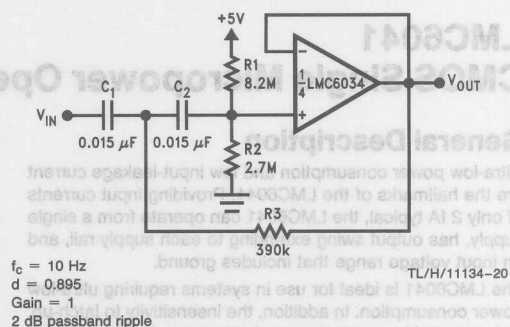
TL/H/11134-17

Typical Single-Supply Applications ($V^+ = 5.0 \text{ VDC}$) (Continued)

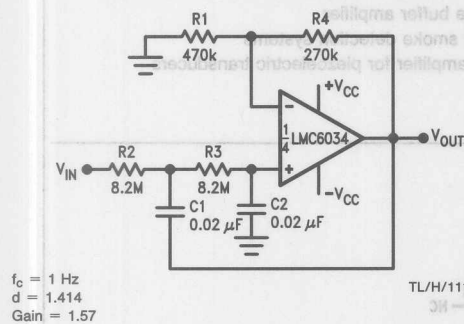
10 Hz Bandpass Filter



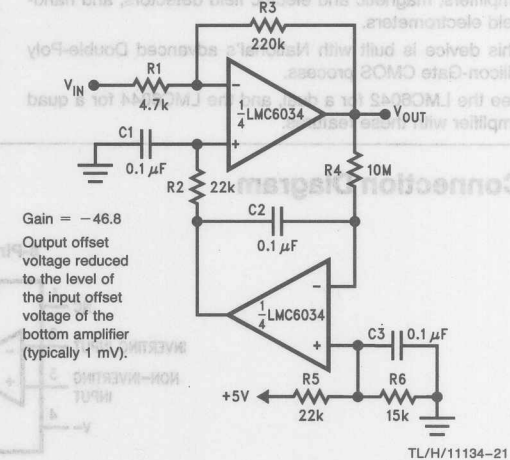
10 Hz High-Pass Filter



1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



High Gain Amplifier with Offset Voltage Reduction



| Package | Temperature Range | NSC Drawing | Transport Media |
|---------------------|--|-------------|-----------------|
| | | | |
| 8-Pin Small Outline | Industrial -40°C to $+85^\circ\text{C}$ | LMC6041M | Reel |
| 8-Pin Molded DIP | | LMC6041N | Reel |
| | | LMC6041 | |

LMC6041

CMOS Single Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6041. Providing input currents of only 2 fA typical, the LMC6041 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6041 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6041 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6042 for a dual, and the LMC6044 for a quad amplifier with these features.

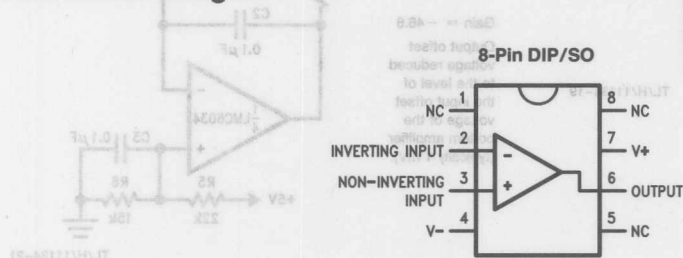
Features

- Low supply current 14 μ A (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram



8-Pin DIP/SO

TL/H/11136-1

Ordering Information

| Package | Temperature Range | NSC Drawing | Transport Media |
|------------------------|------------------------------|----------------|-----------------------|
| | Industrial −40°C to +85°C | | |
| 8-Pin Small Outline | LMC6041AIM LMC6041IM | M08A | Rail Tape and Reel |
| 8-Pin Molded DIP | LMC6041AIN LM6041IN | N08E | Rail |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|----------------------|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^- | (Note 2) |
| Output Short Circuit to V^+ | (Note 11) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature | 110°C |
| ESD Tolerance (Note 4) | 500V |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin | ± 18 mA |

| | |
|--|----------|
| Current at Power Supply Pin | 35 mA |
| Voltage at Input/Output Pin (V^+) + 0.3V, (V^-) - 0.3V | |
| Power Dissipation | (Note 3) |

Operating Ratings

| | |
|--|-----------------------------|
| Temperature Range | -40°C $\leq T_J \leq$ +85°C |
| LMC6041AI, LMC6041I | |
| Supply Voltage | 4.5V $\leq V^+ \leq$ 15.5V |
| Power Dissipation | (Note 9) |
| Thermal Resistance (θ_{JA}) (Note 10) | |
| 8-Pin DIP | 101°C/W |
| 8-Pin SO | 165°C/W |

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6041AI | LMC6041I | Units (Limit) | |
|-------------------|--|--|-----------------------|--|--|------------------|-------------|
| | | | | Limit (Note 6) | Limit (Note 6) | | |
| V _{OS} | Input Offset Voltage | | 1 | 3 3.3 | 6 6.3 | mV max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.3 | | | μV/°C | |
| I _B | Input Bias Current | | 0.002 | 4 | 4 | pA max | |
| I _{OS} | Input Offset Current | | 0.001 | 2 | 2 | pA max | |
| R _{IN} | Input Resistance | | > 10 | | | TeraΩ | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 75 | 68 66 | 62 60 | dB min | |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 75 | 68 66 | 62 60 | dB min | |
| −PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V V _O = 2.5V | 94 | 84 83 | 74 73 | dB min | |
| CMR | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V for CMRR ≥ 50 dB | −0.4 | −0.1 0 | −0.1 0 | V max | |
| | | | V ⁺ − 1.9V | V ⁺ − 2.3V V ⁺ − 2.5V | V ⁺ − 2.3V V ⁺ − 2.4V | V min | |
| A _V | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 1000 | 400 300 | 300 200 | V/mV min |
| | | | Sinking | 500 | 180 120 | 90 70 | V/mV min |
| | | R _L = 25 kΩ (Note 7) | Sourcing | 1000 | 200 160 | 100 80 | V/mV min |
| | | | Sinking | 250 | 100 60 | 50 40 | V/mV min |

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6041AI Limit (Note 6) | LMC6041I Limit (Note 6) | Units (Limit) |
|---|--------------------------------------|--|---------------------|-------------------------------------|-------------------------------|------------------------------|
| V_O (Note 9) $10\text{ } \mu\text{V}$ $100\text{ } \mu\text{V}$ 1 mV 10 mV 100 mV 1 V 10 V | Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 4.987 | 4.970 4.950 | 4.940 4.910 | V min |
| | | | 0.004 | 0.030 0.050 | 0.060 0.090 | V max |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | 4.980 | 4.920 4.870 | 4.870 4.820 | V min |
| | | | 0.010 | 0.080 0.130 | 0.130 0.180 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 14.970 | 14.920 14.880 | 14.880 14.820 | V min |
| | | | 0.007 | 0.030 0.050 | 0.060 0.090 | V max |
| V_m max | | $V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | 14.950 | 14.900 14.850 | 14.850 14.800 | V min |
| | | | 0.022 | 0.100 0.150 | 0.150 0.200 | V max |
| | | | | | | |
| | | | | | | |
| I_{SC} mA | Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 10 | 13 8 | mA min |
| | | Sinking, $V_O = 5\text{V}$ | 21 | 16 8 | 13 8 | mA min |
| I_{SC} mA | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 40 | 15 10 | 15 10 | mA min |
| | | Sinking, $V_O = 13\text{V}$ (Note 11) | 39 8 | 24 8 | 21 8 | mA min |
| I_S mA | Supply Current | $V_O = 1.5\text{V}$ | 14 | 20 24 | 26 30 | μA max |
| | | $V^+ = 15\text{V}$ | 18 31 | 26 31 | 34 39 | μA max |
| V max | | $V^+ = 5\text{V}$ and 15V for CMRR $\geq 80\text{ dB}$ | | | | |
| | | | | | | |
| V min | | | | | | |
| | | | | | | |
| V_m/V_m min | | Sourcing | 1000 | $R_L = 100\text{ k}\Omega$ (Note 7) | | Large Signal Voltage Gain |
| | | | | | | |
| V_m/V_m min | | Sinking | 500 | | | |
| | | | | | | |
| V_m/V_m min | | Sourcing | 1000 | $R_L = 50\text{ k}\Omega$ (Note 7) | | |
| | | | | | | |
| V_m/V_m min | | Sinking | 250 | | | |
| | | | | | | |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6041A Limit (Note 6) | LMC6041 Limit (Note 6) | Units (Limit) |
|----------|---------------------------------|---|-----------------|-------------------------------|------------------------------|-------------------------|
| SR | Slew Rate | (Note 8) | 0.02 | 0.015 0.010 | 0.010 0.007 | V/ μs min |
| GBW | Gain-Bandwidth Product | | 75 | | | kHz |
| ϕ_m | Phase Margin | | 60 | | | Deg |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 83 | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2V_{pp}$ $\pm 5\text{V}$ Supply | 0.01 | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

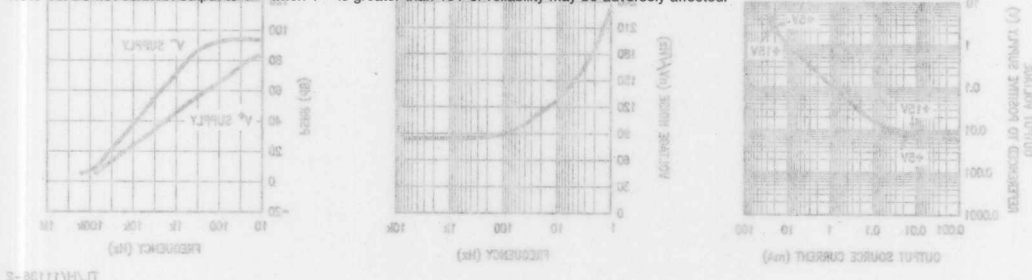
Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

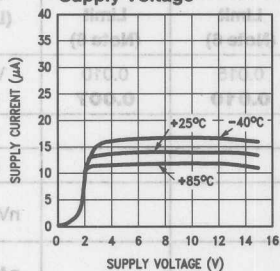
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

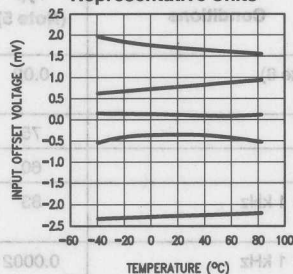
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.



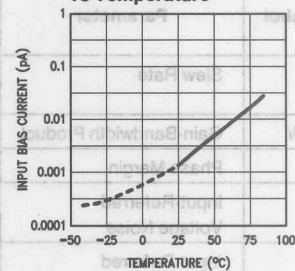
Supply Current vs Supply Voltage



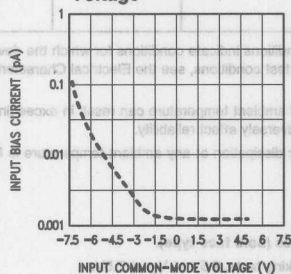
Offset Voltage vs Temperature of Five Representative Units



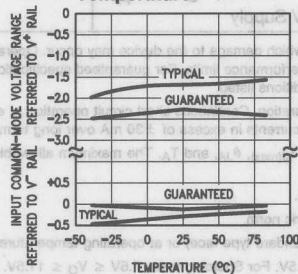
Input Bias Current vs Temperature



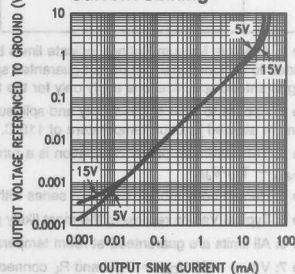
Input Bias Current vs Input Common-Mode Voltage



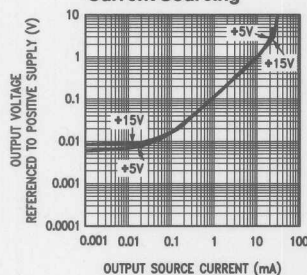
Input Common-Mode Voltage Range vs Temperature



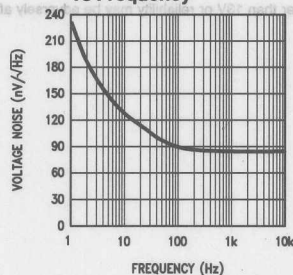
Output Characteristics Current Sinking



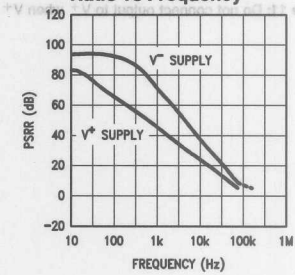
Output Characteristics Current Sourcing



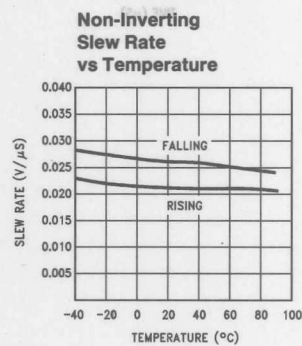
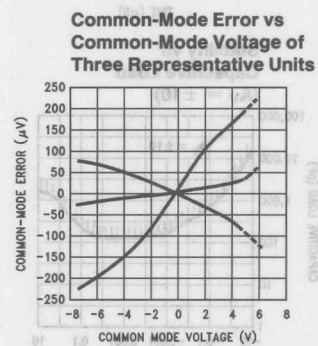
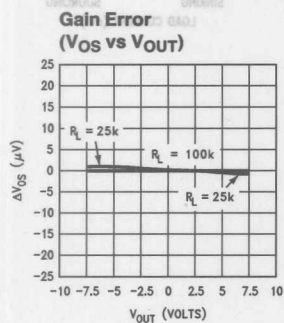
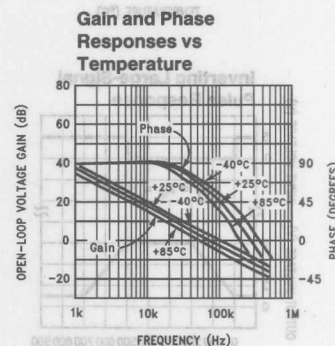
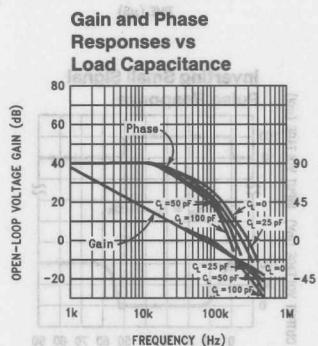
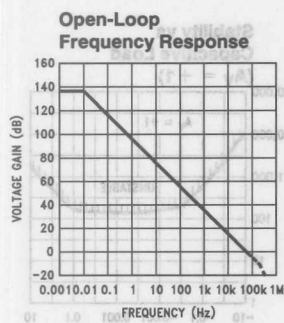
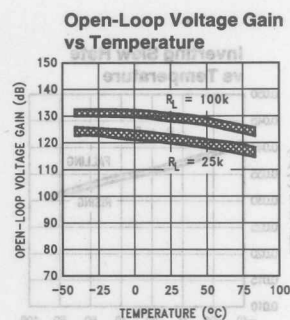
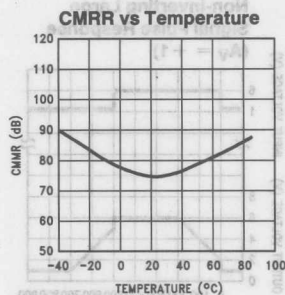
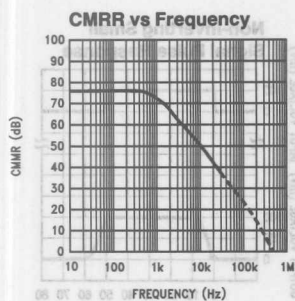
Input Voltage Noise vs Frequency



Power Supply Rejection Ratio vs Frequency

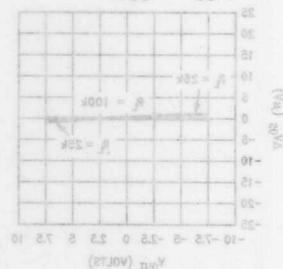
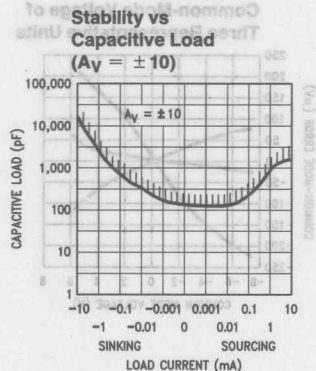
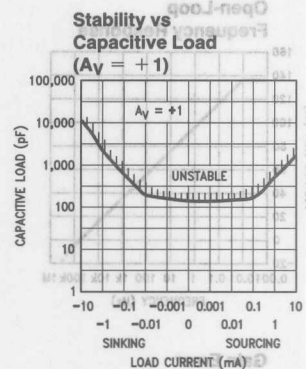
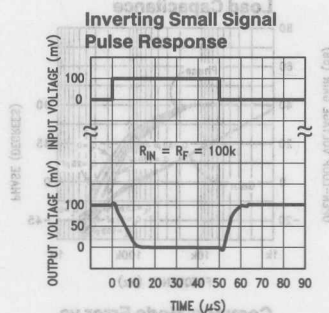
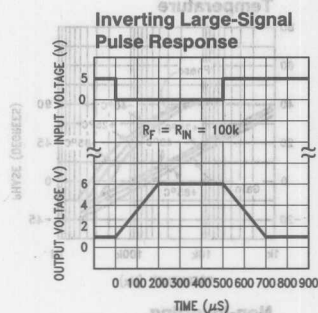
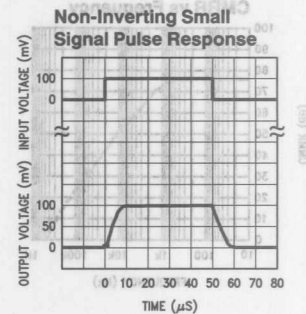
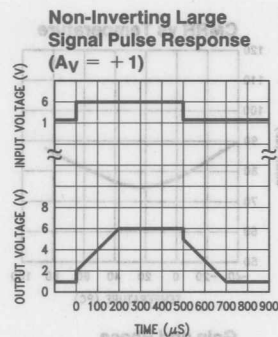
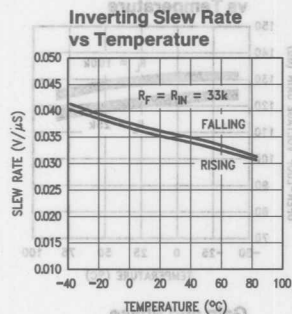


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



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Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6041 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6041 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6041.

Although the LMC6041 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6041 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

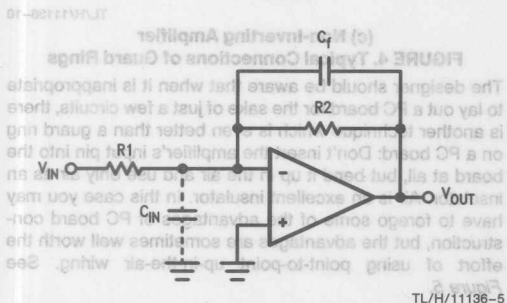


FIGURE 1. Cancelling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_f , around the feedback resistor (as in Figure 1) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad \text{or} \quad R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

Application Hints (Continued)

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2a.

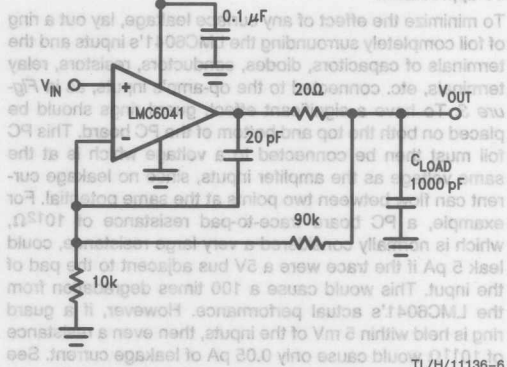


FIGURE 2a. LMC6041 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 2a, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

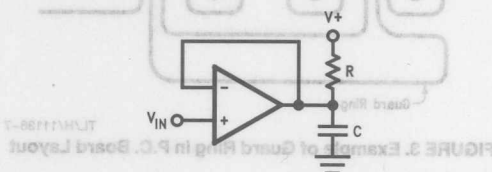


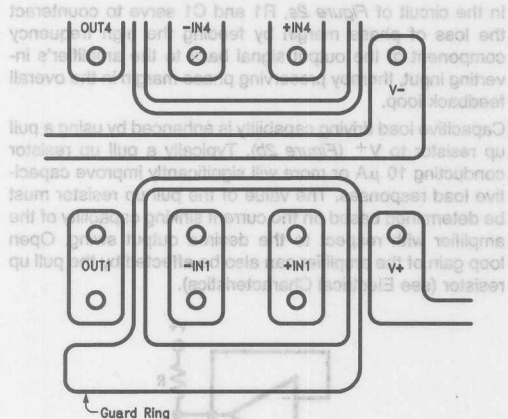
FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

Application Hints (Continued)

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6041, typically less than 2fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

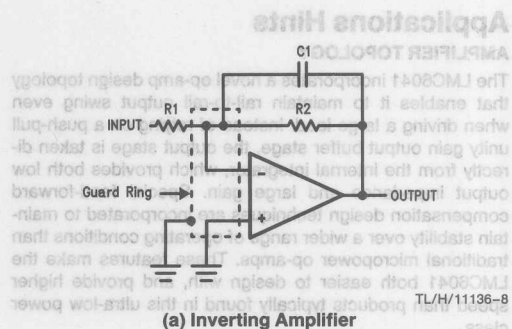
To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6041's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6041's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.



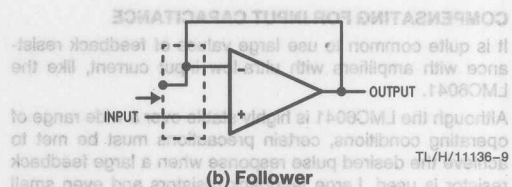
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FIGURE 3. Example of Guard Ring in P.C. Board Layout

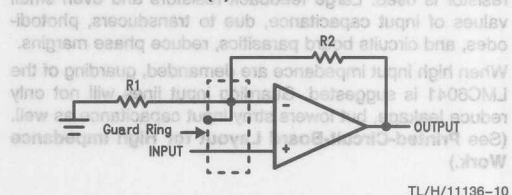
FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor



(a) Inverting Amplifier



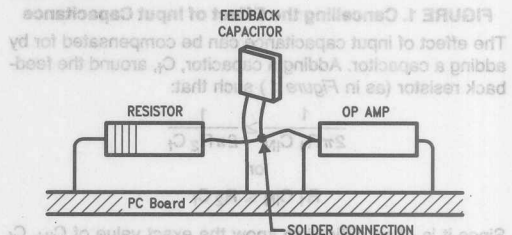
(b) Follower



(c) Non-Inverting Amplifier

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



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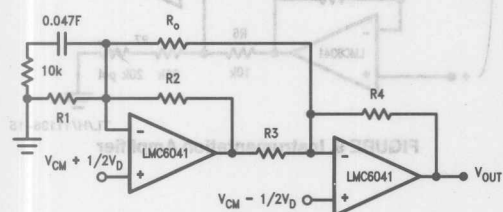
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6041 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.



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FIGURE 6. Two Op-Amp Instrumentation Amplifier

The circuit in Figure 6 is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 28 μA . To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to Figure 6, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D .

Rejection of the common-mode component of the input is accomplished by making the ratio of $R1/R2$ equal to $R3/R4$. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

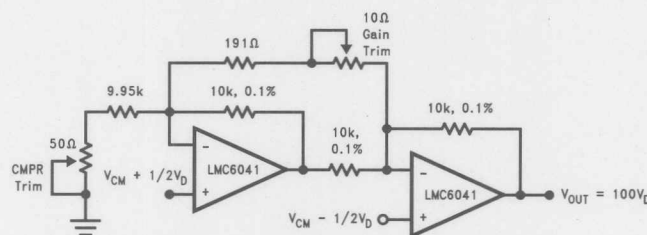
$$V_{OUT} = \frac{R4}{R3} \left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R_O} \right) V_D$$

A suggested design guideline is to minimize the difference of value between $R1$ through $R4$. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If $R_N = R1 = R2 = R3 = R4$ then the gain equation can be simplified:

$$V_{OUT} = 2 \left(1 + \frac{R_N}{R_O} \right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6041, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6041 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 7. Provisions have been made for low sensitivity trimming of CMRR and gain.



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FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

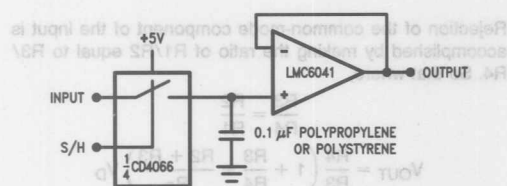


FIGURE 8. Low-Leakage Sample and Hold

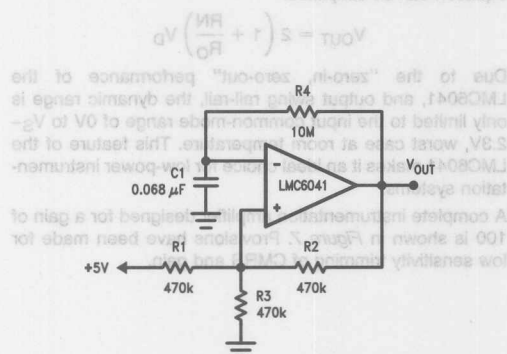


FIGURE 10. 1 Hz Square-Wave Oscillator

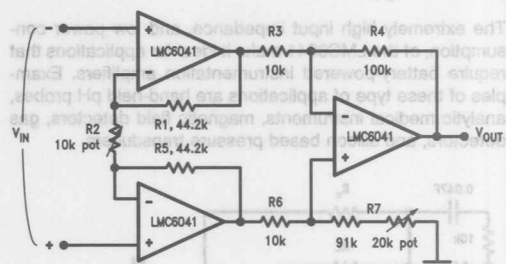


FIGURE 9. Instrumentation Amplifier

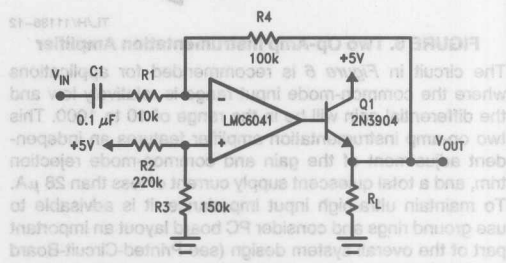


FIGURE 11. AC Coupled Power Amplifier

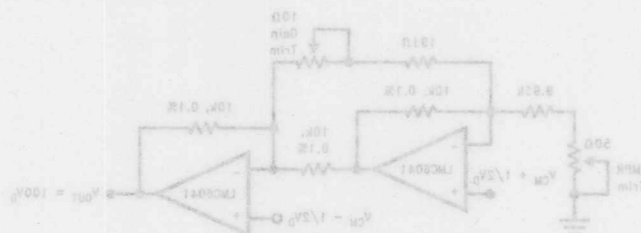


FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

LMC6042 CMOS Dual Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6042. Providing input currents of only 2 fA typical, the LMC6042 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6042 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6042 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6044 for a quad amplifier with these features.

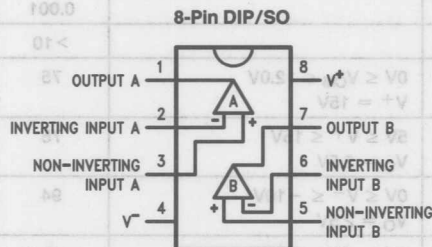
Features

- Low supply current 10 μ A/Amp (typ)
- Operates from 4.5V to 15V single supply
- Ultra low input current 2 fA (typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------|-------------------|----------------|---------------|-----------------|
| | Industrial | -40°C to +85°C | | |
| 8-Pin | LMC6042AIM | M08A | Rail | |
| Small Outline | LMC6042IM | | Tape and Reel | |
| 8-Pin | LMC6042AIN | N08E | Rail | |
| Molded DIP | LMC6042IN | | | |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|------------------|
| Differential Input Voltage | ± Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^+ | (Note 12) |
| Output Short Circuit to V^- | (Note 2) |
| Lead Temperature (Soldering, 10 seconds) | 260°C |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin | ± 18 mA |
| Current at Power Supply Pin | 35 mA |

| | |
|-------------------------------|------------------------------------|
| Power Dissipation | (Note 3) |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 3) | 110°C |
| ESD Tolerance (Note 4) | 500V |
| Voltage at Input/Output Pin | (V^+) + 0.3V, (V^-) - 0.3V |

Operating Ratings

| | |
|---|-----------------------|
| Temperature Range | -40°C ≤ T_J ≤ +85°C |
| LMC6042AI, LMC6042I | |
| Supply Voltage | 4.5V ≤ V^+ ≤ 15.5V |
| Power Dissipation | (Note 10) |
| Thermal Resistance (θ_{JA}), (Note 11) | |
| 8-Pin DIP | 101°C/W |
| 8-Pin SO | 165°C/W |

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6042AI | LMC6042I | Units (Limit) | | |
|-------------------|--|--|-----------------------|--|--|-------------------|-------------|--|
| | | | | Limit (Note 6) | Limit (Note 6) | | | |
| V _{OS} | Input Offset Voltage | | 1 | 3 3.3 | 6 6.3 | mV Max | | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.3 | | | μV/°C | | |
| I _B | Input Bias Current | | 0.002 | 4 | 4 | pA (Max) | | |
| I _{OS} | Input Offset Current | | 0.001 | 2 | 2 | pA (Max) | | |
| R _{IN} | Input Resistance | | > 10 | | | TeraΩ | | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ₊ = 15V | 75 | 68 66 | 62 60 | dB Min | | |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ₊ ≤ 15V V _O = 2.5V | 75 | 68 66 | 62 60 | dB Min | | |
| −PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V _− ≤ −10V V _O = 2.5V | 94 | 84 83 | 74 73 | dB Min | | |
| CMR | Input Common-Mode Voltage Range | V ₊ = 5V and 15V For CMRR ≥ 50 dB | −0.4 | −0.1 0 | −0.1 0 | V Max | | |
| | | | V ₊ − 1.9V | V ₊ − 2.3V V₊ − 2.5V | V ₊ − 2.3V V₊ − 2.4V | V Min | | |
| A _V | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 1000 | 400 300 | 300 200 | V/mV Min | |
| | | | Sinking | 500 | 180 120 | 90 70 | V/mV Min | |
| | | R _L = 25 kΩ (Note 7) | Sourcing | 1000 | 200 160 | 100 80 | V/mV Min | |
| | | | Sinking | 250 | 100 60 | 50 40 | V/mV Min | |
| | | | | | | | | |
| | | | | | | | | |

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L > 1\text{M}$ unless otherwise specified. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6042AI Limit (Note 6) | LMC6042I Limit (Note 6) | Units (Limit) |
|-----------------|--------------------------------------|---|---------------------|--------------------------------|-------------------------------|----------------------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 4.987 | 4.970 4.950 | 4.940 4.910 | V Min |
| | | | 0.004 | 0.030 0.050 | 0.060 0.090 | V Max |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | 4.980 | 4.920 4.870 | 4.870 4.820 | V Min |
| | | | 0.010 | 0.080 0.130 | 0.130 0.180 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 14.970 | 14.920 14.880 | 14.880 14.820 | V Min |
| | | | 0.007 | 0.030 0.050 | 0.060 0.090 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | 14.950 | 14.900 14.850 | 14.850 14.800 | V Min |
| | | | 0.022 | 0.100 0.150 | 0.150 0.200 | V Max |
| | | | | | | |
| | | | | | | |
| I_{SC} | Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 10 | 13 8 | mA Min |
| | | Sinking, $V_O = 5\text{V}$ | 21 | 16 8 | 13 8 | mA Min |
| I_{SC} | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 40 | 15 10 | 15 10 | mA Min |
| | | Sinking, $V_O = 13\text{V}$ (Note 12) | 39 | 24 8 | 21 8 | mA Min |
| I_S | Supply Current | Both Amplifiers $V_O = 1.5\text{V}$ | 20 | 34 39 | 45 50 | μA Max |
| | | Both Amplifiers $V^+ = 15\text{V}$ | 26 | 44 51 | 56 65 | μA Max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6042AI | LMC6042I | Units (Limit) |
|----------|------------------------------|---|-----------------|-----------------------|-----------------------|-------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | |
| SR | Slew Rate | (Note 8) | 0.02 | 0.015 0.010 | 0.010 0.007 | V/ μs Min |
| GBW | Gain-Bandwidth Product | | 100 | | | kHz |
| ϕ_m | Phase Margin | | 60 | | | Deg |
| | Amp-to-Amp Isolation | (Note 9) | 115 | | | dB |
| e_n | Input-Referred Voltage Noise | $f = 1\text{ kHz}$ | 83 | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $f = 1\text{ kHz}$ | 0.0002 | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $f = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{PP}$ $\pm 5\text{V}$ Supply | 0.01 | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{Max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{Max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$; For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

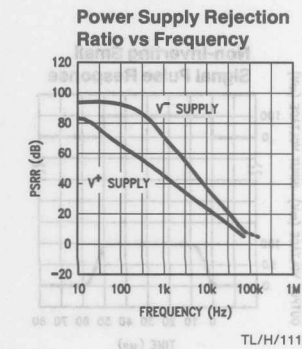
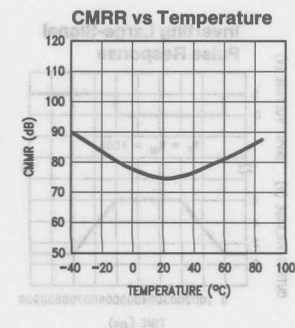
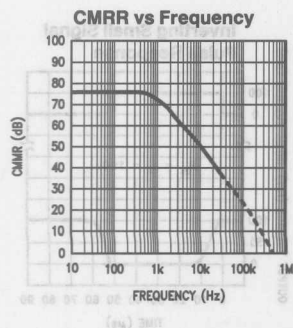
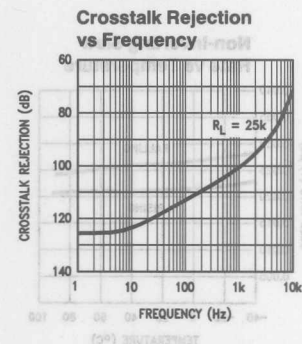
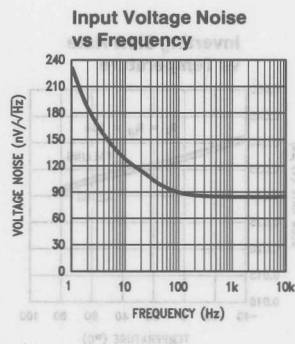
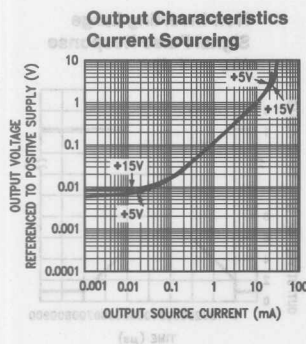
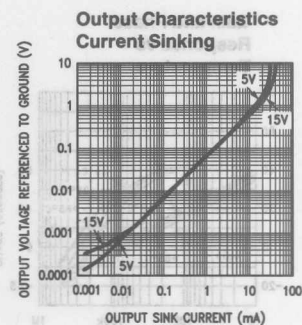
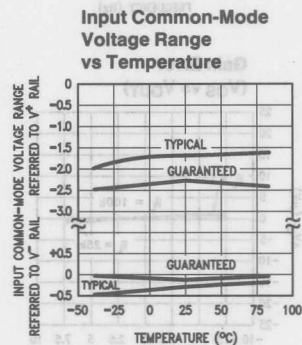
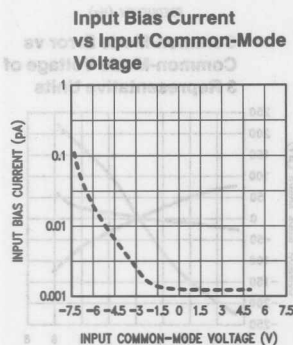
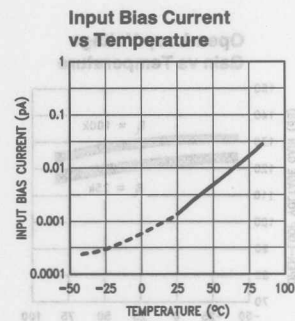
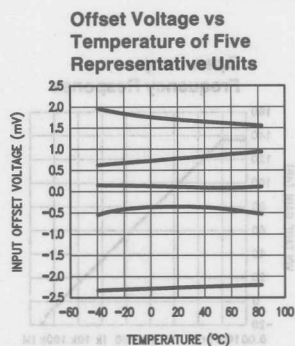
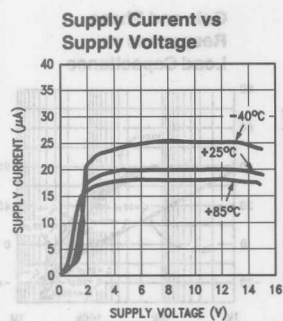
Note 9: Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12\text{ V}_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: All numbers apply for packages soldered directly into a PC board.

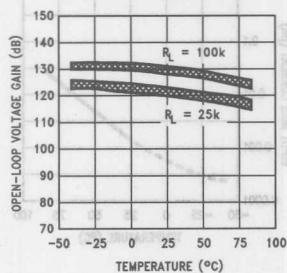
Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified

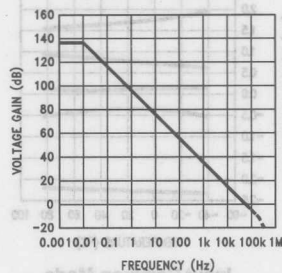


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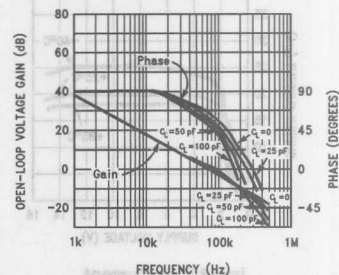
Open-Loop Voltage Gain vs Temperature



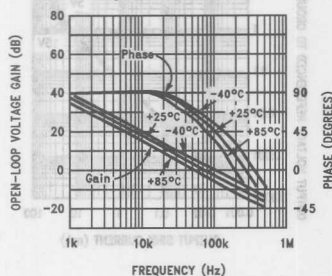
Open-Loop Frequency Response



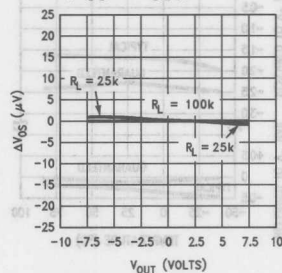
Gain and Phase Responses vs Load Capacitance



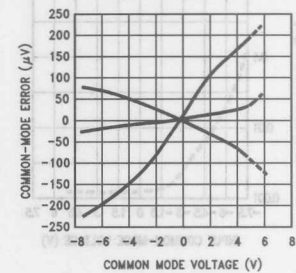
Gain and Phase Response vs Temperature



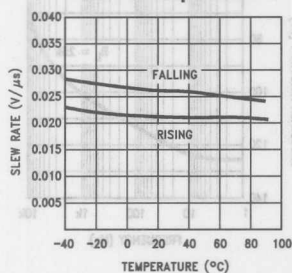
Gain Error (V_{OS} vs V_{OUT})



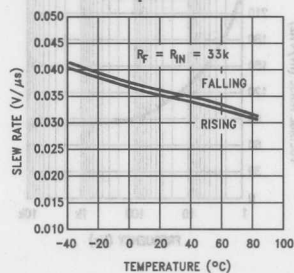
Common-Mode Error vs Common-Mode Voltage of 3 Representative Units



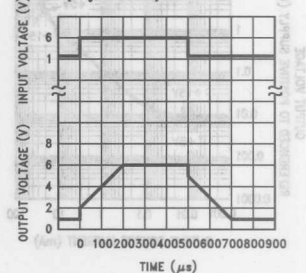
Non-Inverting Slew Rate vs Temperature



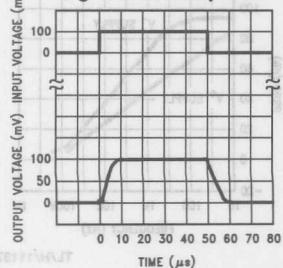
Inverting Slew Rate vs Temperature



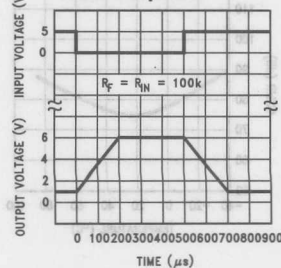
Non-Inverting Large Signal Pulse Response ($A_v = +1$)



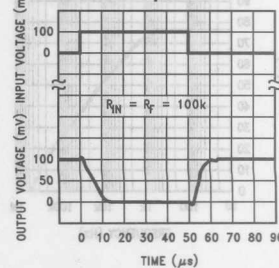
Non-Inverting Small Signal Pulse Response



Inverting Large-Signal Pulse Response



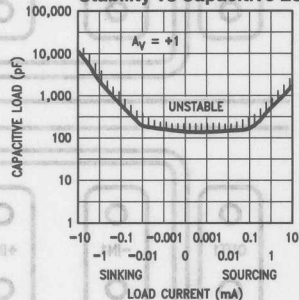
Inverting Small Signal Pulse Response



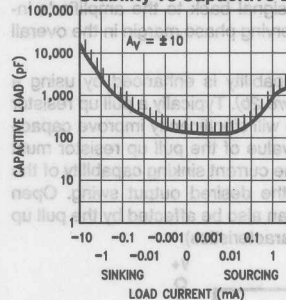
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

Stability vs Capacitive Load



Stability vs Capacitive Load



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6042 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6042 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistors with amplifiers with ultra-low input current, like the LMC6042.

Although the LMC6042 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6042 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work**).

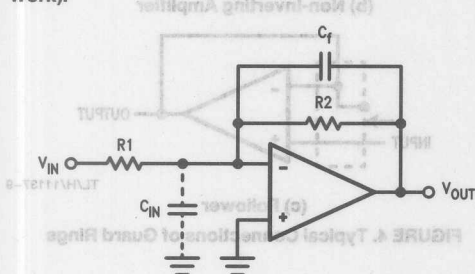


FIGURE 1. Cancelling the Effect of Input Capacitance

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The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f , around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

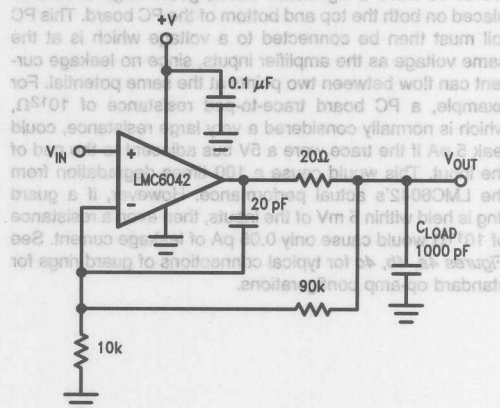


FIGURE 2a. LMC6042 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

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Applications Hints (Continued)

In the circuit of *Figure 2a*, R1 and C1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

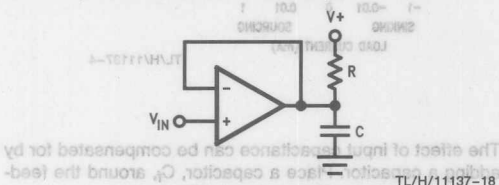


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6042, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6042's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100-times degradation from the LMC6042's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

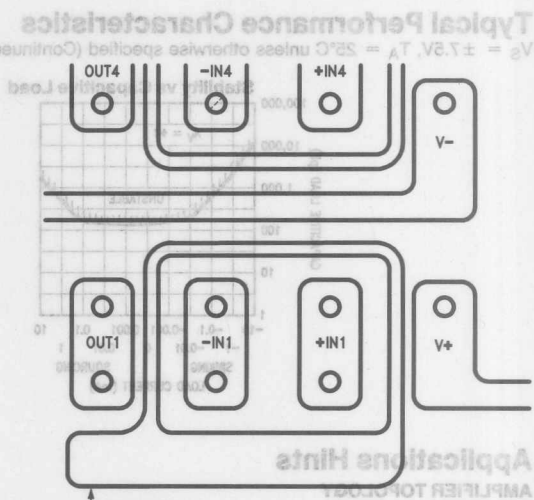
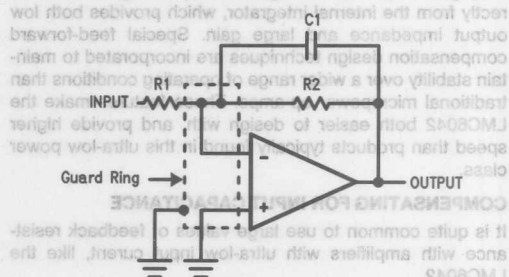
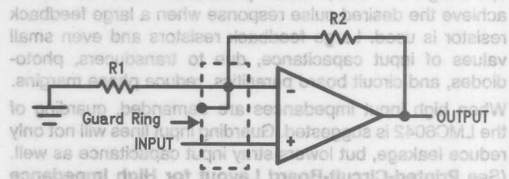


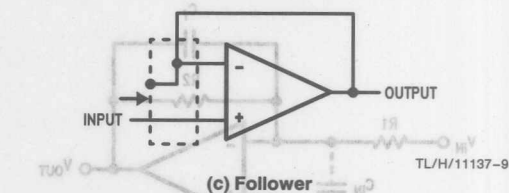
FIGURE 3. Example of Guard Ring in P.C. Board Layout



(a) Inverting Amplifier



(b) Non-Inverting Amplifier

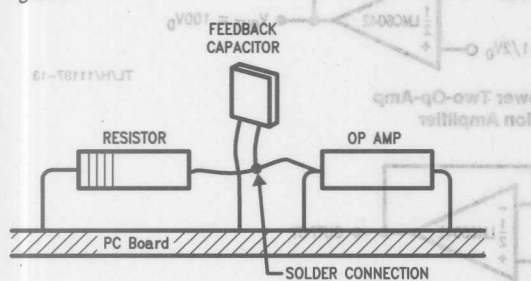


(c) Follower

FIGURE 4. Typical Connections of Guard Rings

Application Hints (Continued)

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6042 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in Figure 6 is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 20 μA . To maintain ultra-high input impedance, it is advisable to use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to Figure 6, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D .

Rejection of the common-mode component of the input is accomplished by making the ratio of $R1/R2$ equal to $R3/R4$. So that where,

$$\frac{R3}{R4} = \frac{R2}{R1}$$

$$V_{OUT} = \frac{R4}{R3} \left(1 + \frac{R3}{R4} + \frac{R2 + R3}{R0} \right) V_D$$

A suggested design guideline is to minimize the difference of value between $R1$ through $R4$. This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If $R_N = R1 = R2 = R3 = R4$ then the gain equation can be simplified:

$$V_{OUT} = 2 \left(1 + \frac{R_N}{R0} \right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6042, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6042 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 7. Provisions have been made for low sensitivity trimming of CMRR and gain.

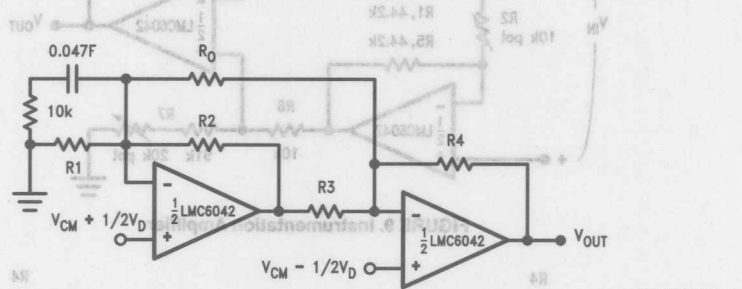


FIGURE 6. Two Op-Amp Instrumentation Amplifier

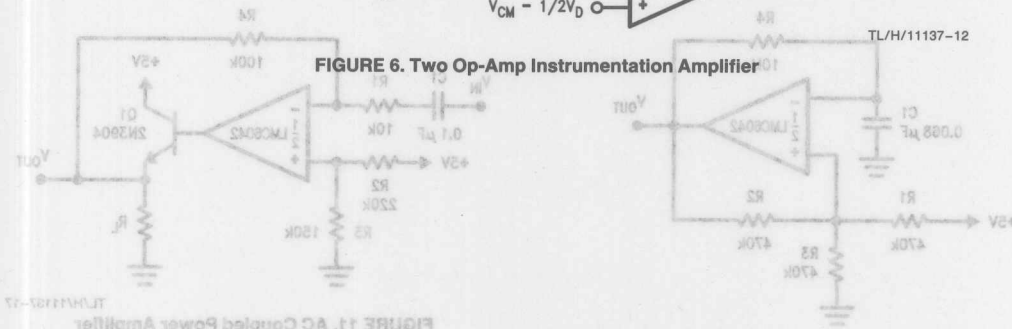


FIGURE 7. AC Coupled Power Amplifier

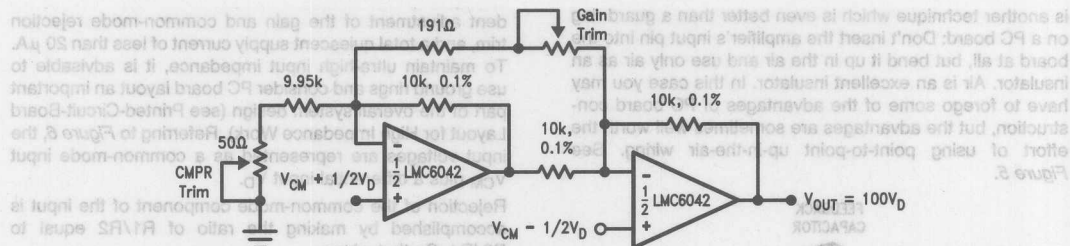


FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

TL/H/11137-13

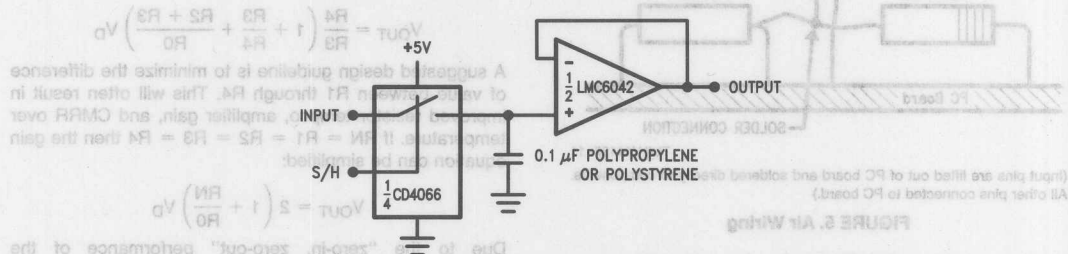


FIGURE 8. Low-Leakage Sample and Hold

TL/H/11137-14

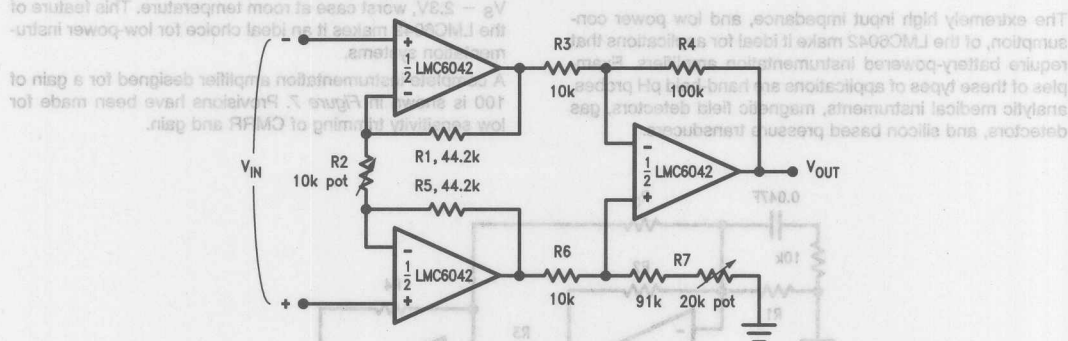


FIGURE 9. Instrumentation Amplifier

TL/H/11137-15

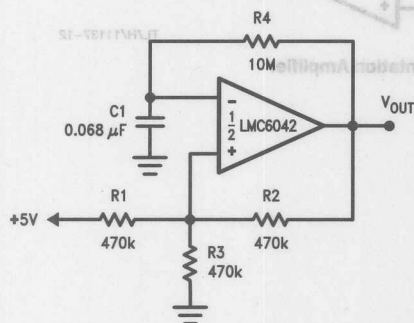


FIGURE 10. 1 Hz Square Wave Oscillator

TL/H/11137-16

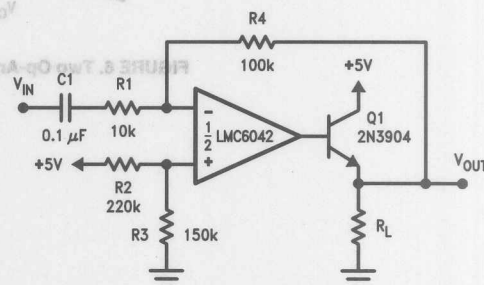


FIGURE 11. AC Coupled Power Amplifier

TL/H/11137-17

LMC6044 CMOS Quad Micropower Operational Amplifier

General Description

Ultra-low power consumption and low input-leakage current are the hallmarks of the LMC6044. Providing input currents of only 2 fA typical, the LMC6044 can operate from a single supply, has output swing extending to each supply rail, and an input voltage range that includes ground.

The LMC6044 is ideal for use in systems requiring ultra-low power consumption. In addition, the insensitivity to latch-up, high output drive, and output swing to ground without requiring external pull-down resistors make it ideal for single-supply battery-powered systems.

Other applications for the LMC6044 include bar code reader amplifiers, magnetic and electric field detectors, and hand-held electrometers.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC6041 for a single, and the LMC6042 for a dual amplifier with these features.

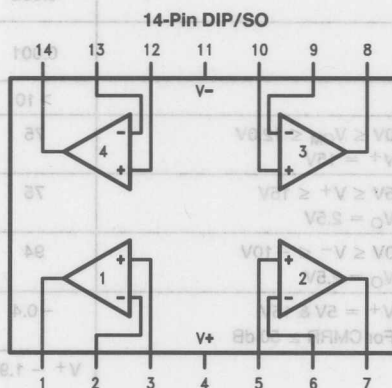
Features

- Low supply current $10 \mu\text{A}/\text{Amp}$ (Typ)
- Operates from 4.5V to 15.5V single supply
- Ultra low input current 2 fA (Typ)
- Rail-to-rail output swing
- Input common-mode range includes ground

Applications

- Battery monitoring and power conditioning
- Photodiode and infrared detector preamplifier
- Silicon based transducer systems
- Hand-held analytic instruments
- pH probe buffer amplifier
- Fire and smoke detection systems
- Charge amplifier for piezoelectric transducers

Connection Diagram



TL/H/11138-1

Ordering Information

| Package | Temperature Range | NSC Drawing | Transport Media |
|-------------------------|--------------------------------|-------------|-----------------------|
| | Industrial - 40°C to + 85°C | | |
| 14-Pin Small Outline | LMC6044AIM LMC6044IM | M14A | Rail Tape and Reel |
| 14-Pin Molded DIP | LMC6044AIN LMC6044IN | N14A | Rail |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|------------------|
| Differential Input Voltage | ± Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^+ | (Note 12) |
| Output Short Circuit to V^- | (Note 2) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin | ± 18 mA |
| Current at Power Supply Pin | 35 mA |
| Power Dissipation | (Note 3) |
| Storage Temperature Range | -65°C to +150°C |

Junction Temperature (Note 3)

110°C

ESD Tolerance (Note 4)

500V

Voltage at I/O Pin (V^+)+0.3V, (V^-) -0.3V**Operating Ratings**

| | |
|---|-----------------------|
| Temperature Range | -40°C ≤ T_J ≤ +85°C |
| LMC6044AI, LMC6044I | |
| Supply Voltage | 4.5V ≤ V^+ ≤ 15.5V |
| Power Dissipation | (Note 10) |
| Thermal Resistance (θ_{JA}), (Note 11) | |
| 14-Pin DIP | 85°C/W |
| 14-Pin SO | 115°C/W |

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6044AI Limit (Note 6) | LMC6044I Limit (Note 6) | Units (Limit) | |
|-------------------|--|--|-----------------------|--|--|------------------|-------------|
| V _{OS} | Input Offset Voltage | | 1 | 3 3.3 | 6 6.3 | mV max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.3 | | | μV/°C | |
| I _B | Input Bias Current | | 0.002 | 4 | 4 | pA max | |
| I _{OS} | Input Offset Current | | 0.001 | 2 | 2 | pA max | |
| R _{IN} | Input Resistance | | > 10 | | | TeraΩ | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 75 | 68 66 | 62 60 | dB min | |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 75 | 68 66 | 62 60 | dB min | |
| −PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V V _O = 2.5V | 94 | 84 83 | 74 73 | dB min | |
| CMR | Input Common-Mode Voltage Range | V ⁺ = 5V & 15V For CMRR ≥ 50 dB | −0.4 | −0.1 0 | −0.1 0 | V max | |
| | | | V ⁺ − 1.9V | V ⁺ − 2.3V V ⁺ − 2.5V | V ⁺ − 2.3V V ⁺ − 2.4V | V min | |
| A _V | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 1000 | 400 300 | 300 200 | V/mV min |
| | | | Sinking | 500 | 180 120 | 90 70 | V/mV min |
| | | R _L = 25 kΩ (Note 7) | Sourcing | 1000 | 200 160 | 100 80 | V/mV min |
| | | | Sinking | 250 | 100 60 | 50 40 | V/mV min |

Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_A = T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$, and $R_L > 1\text{M}$ unless otherwise specified. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 5) | LMC6044AI Limit (Note 6) | LMC6044I Limit (Note 6) | Units (Limit) |
|----------|--------------------------------------|--|------------------|--------------------------|-------------------------|----------------------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to 2.5V | 4.987 | 4.970 4.950 | 4.940 4.910 | V min |
| | | | 0.004 | 0.030 0.050 | 0.060 0.090 | V max |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to 2.5V | 4.980 | 4.920 4.870 | 4.870 4.820 | V min |
| | | | 0.010 | 0.080 0.130 | 0.130 0.180 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 14.970 | 14.920 14.880 | 14.880 14.820 | V min |
| | | | 0.007 | 0.030 0.050 | 0.060 0.090 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | 14.950 | 14.900 14.850 | 14.850 14.800 | V min |
| | | | 0.022 | 0.100 0.150 | 0.150 0.200 | V max |
| I_{SC} | Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 10 | 13 8 | mA min |
| | | Sinking, $V_O = 5\text{V}$ | 21 | 16 8 | 13 8 | mA min |
| I_{SC} | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 40 | 15 10 | 15 10 | mA min |
| | | Sinking, $V_O = 13\text{V}$ (Note 12) | 39 | 24 8 | 21 8 | mA min |
| I_S | Supply Current | Four Amplifiers $V_O = 1.5\text{V}$ | 40 | 65 72 | 75 82 | μA max |
| | | Four Amplifiers $V^+ = 15\text{V}$ | 52 | 85 94 | 98 107 | μA max |

specified.

| Units Symbol | Parameter | Typical Conditions | Typical (Note 5) | LMC6044AI | LMC6044I | Units (Limit) |
|-----------------|---------------------------------|--|---------------------|-------------------|-------------------|------------------------|
| | | | | Limit (Note 6) | Limit (Note 6) | |
| SR V min | Slew Rate | (Note 8) | 0.02 | 0.015 | 0.010 | V/ μ s/ min |
| GBW | Gain-Bandwidth Product | | 0.10 | | | MHz |
| ϕ_m | Phase Margin | | 60 | | | Deg |
| | Amp-to-Amp Isolation | (Note 9) | 115 | | | dB |
| e_n | Input-Referred Voltage Noise | F = 1 kHz | 83 | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | F = 1 kHz | 0.0002 | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | F = 1 kHz, $A_V = -5$ $R_L = 100 \text{ k}\Omega$, $V_O = 2 V_{pp}$ $\pm 5V$ Supply | 0.01 | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 110°C. Output currents in excess of $\pm 30 \text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, 1.5 k Ω in series with 100 pF.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified in the slower of the positive and negative slew rates.

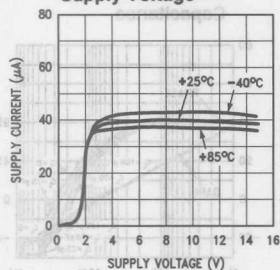
Note 9: Input referred $V^+ = 15V$ and $R_L = 100 \text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 100 Hz to produce $V_O = 12 V_{pp}$.

Note 10: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

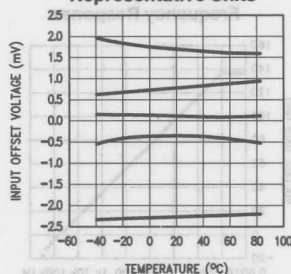
Note 11: All numbers apply for packages soldered directly into a PC board.

Note 12: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

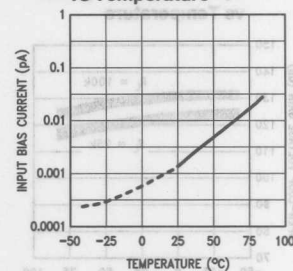
**Supply Current vs
Supply Voltage**



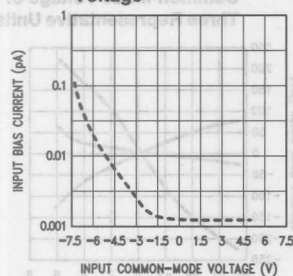
**Offset Voltage vs
Temperature of Five
Representative Units**



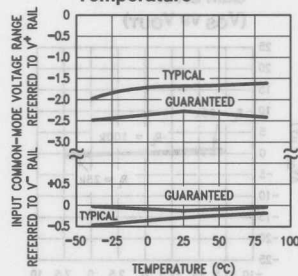
**Input Bias Current
vs Temperature**



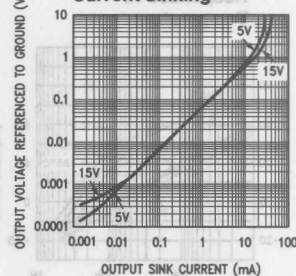
**Input Bias Current vs
Input Common-Mode
Voltage**



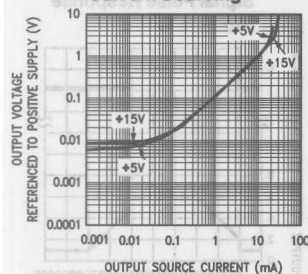
**Input Common-Mode
Voltage Range vs
Temperature**



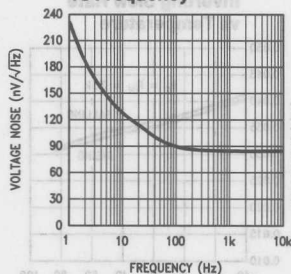
**Output Characteristics
Current Sinking**



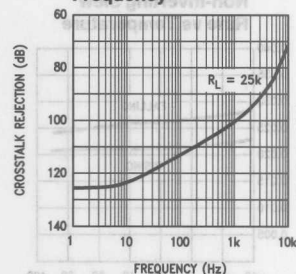
**Output Characteristics
Current Sourcing**



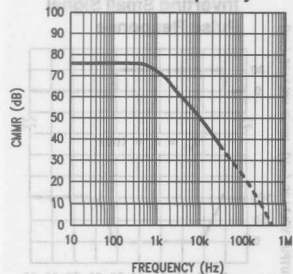
**Input Voltage Noise
vs Frequency**



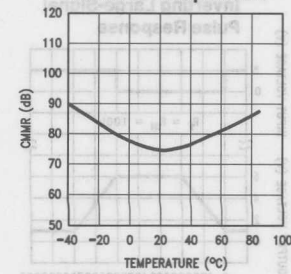
**Crosstalk Rejection vs
Frequency**



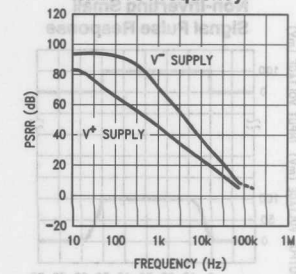
CMRR vs Frequency



CMRR vs Temperature



**Power Supply Rejection
Ratio vs Frequency**

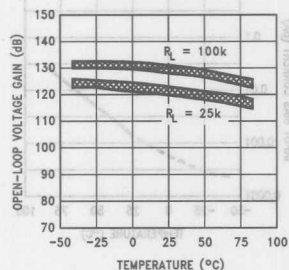


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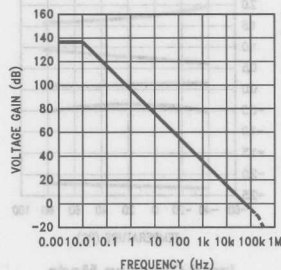
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

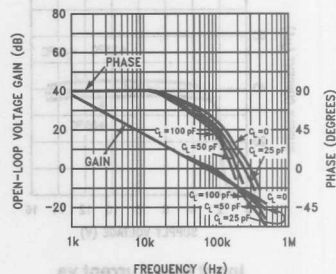
Open-Loop Voltage Gain vs Temperature



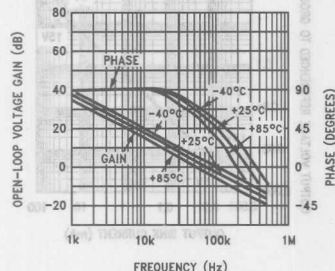
Open-Loop Frequency Response



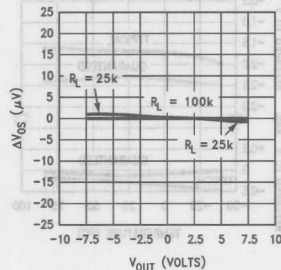
Gain and Phase Responses vs Load Capacitance



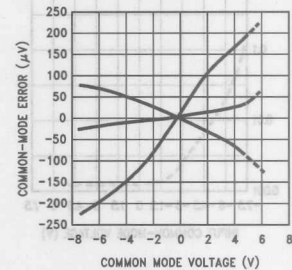
Gain and Phase Responses vs Temperature



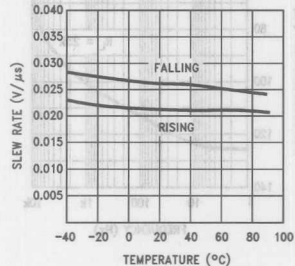
Gain Error (V_{OS} vs V_{OUT})



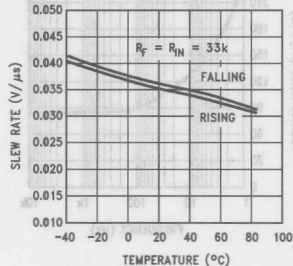
Common-Mode Error vs Common-Mode Voltage of Three Representative Units



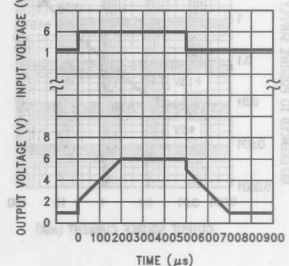
Non-Inverting Slew Rate vs Temperature



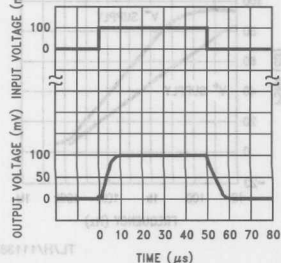
Inverting Slew Rate vs Temperature



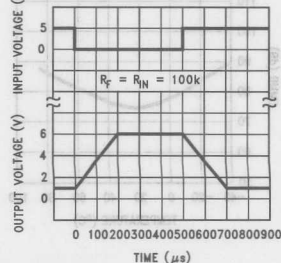
Non-Inverting Large Signal Pulse Response ($A_V = +1$)



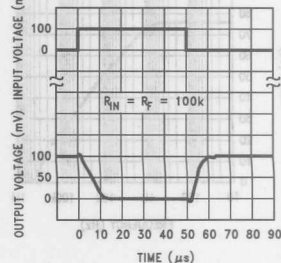
Non-Inverting Small Signal Pulse Response



Inverting Large-Signal Pulse Response

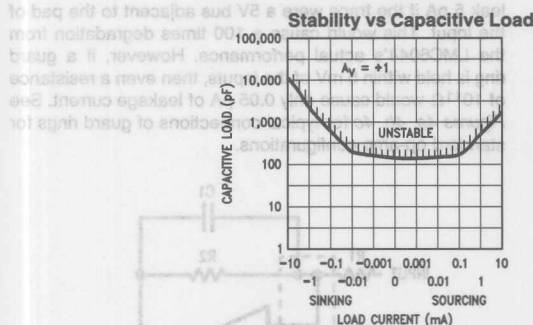


Inverting Small Signal Pulse Response



Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)



Application Hints

AMPLIFIER TOPOLOGY

The LMC6044 incorporates a novel op-amp design topology that enables it to maintain rail to rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6044 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance with amplifiers with ultra-low input current, like the LMC6044.

Although the LMC6044 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuits board parasitics, reduce phase margins.

When high input impedance are demanded, guarding of the LMC6044 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See **Printed-Circuit-Board Layout for High Impedance Work.**)

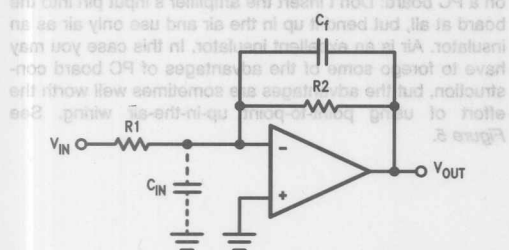
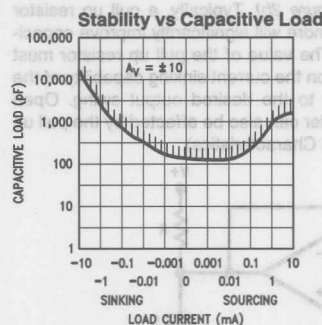


FIGURE 1. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a capacitor. Adding a capacitor, C_F , around the feedback resistor (as in Figure 1) such that:



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$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F}$$

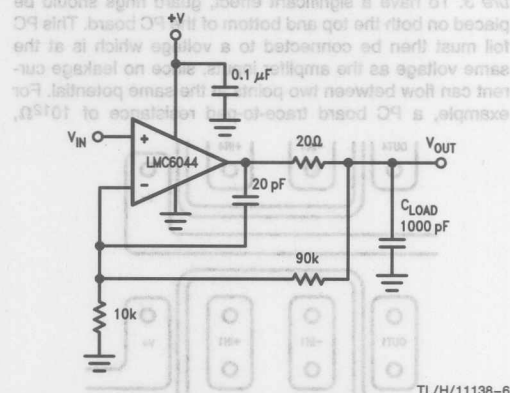
$$\text{or}$$

$$R_1 C_{IN} \leq R_2 C_F$$

Since it is often difficult to know the exact value of C_{IN} , C_F can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2a.



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FIGURE 2a. LMC6044 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 2a, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Application Hints (Continued)

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically, a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

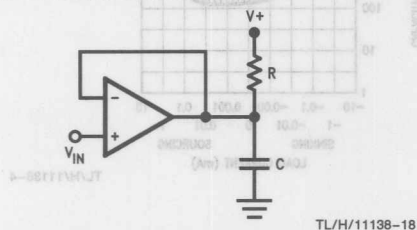


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6044, typically less than 2 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6044's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$,

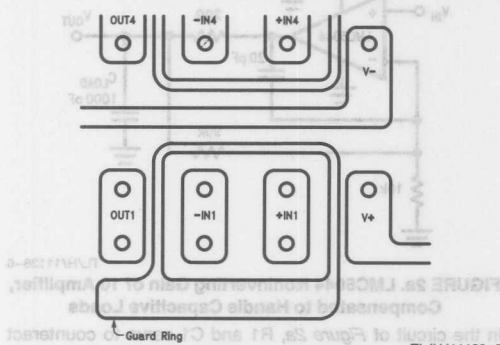
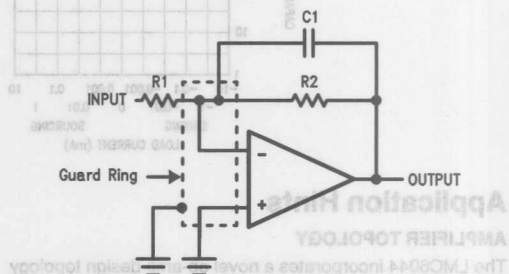
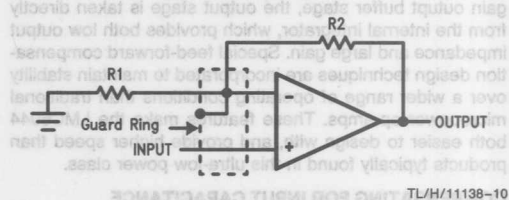


FIGURE 3. Example of Guard Ring in P.C. Board Layout

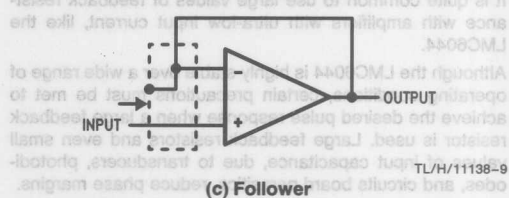
which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6044's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.



(a) Inverting Amplifier



(b) Non-Inverting Amplifier



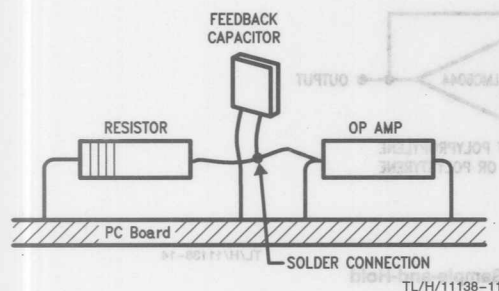
(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



Typical Single-Supply Applications ($V^+ = 5.0 V_{DD}$)



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

The extremely high input impedance, and low power consumption, of the LMC6044 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these type of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

The circuit in Figure 6 is recommended for applications where the common-mode input range is relatively low and the differential gain will be in the range of 10 to 1000. This two op-amp instrumentation amplifier features an independent adjustment of the gain and common-mode rejection trim, and a total quiescent supply current of less than 40 μA . To maintain ultra-high input impedance, it is advisable to

use ground rings and consider PC board layout an important part of the overall system design (see Printed-Circuit-Board Layout for High Impedance Work). Referring to Figure 6, the input voltages are represented as a common-mode input V_{CM} plus a differential input V_D . Rejection of the common-mode component of the input is accomplished by making the ratio of R_1/R_2 equal to R_3/R_4 . So that where,

$$\frac{R_3}{R_4} = \frac{R_2}{R_1}$$

$$V_{OUT} = \frac{R_4}{R_3} \left(1 + \frac{R_3}{R_4} + \frac{R_2 + R_3}{R_O} \right) V_D$$

A suggested design guideline is to minimize the difference of value between R_1 through R_4 . This will often result in improved resistor tempco, amplifier gain, and CMRR over temperature. If $R_N = R_1 = R_2 = R_3 = R_4$ then the gain equation can be simplified:

$$V_{OUT} = 2 \left(1 + \frac{R_N}{R_O} \right) V_D$$

Due to the "zero-in, zero-out" performance of the LMC6044, and output swing rail-rail, the dynamic range is only limited to the input common-mode range of 0V to $V_S - 2.3V$, worst case at room temperature. This feature of the LMC6044 makes it an ideal choice for low-power instrumentation systems.

A complete instrumentation amplifier designed for a gain of 100 is shown in Figure 7. Provisions have been made for low sensitivity trimming of CMRR and gain.

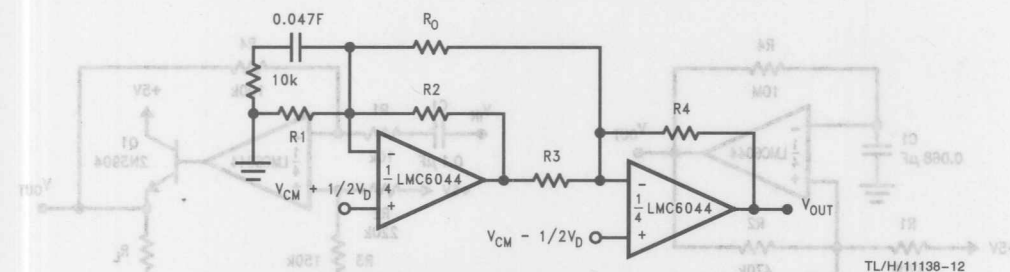


FIGURE 6. Two Op-Amp Instrumentation Amplifier

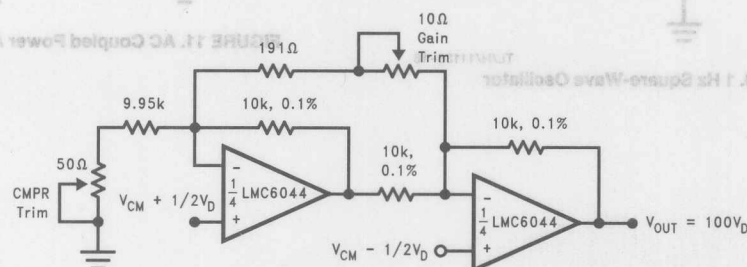


FIGURE 7. Low-Power Two-Op-Amp Instrumentation Amplifier

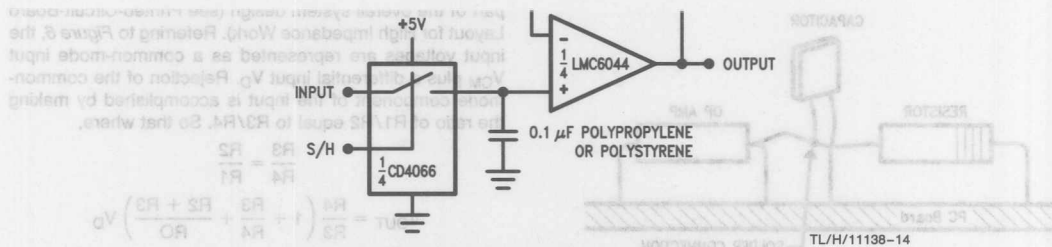


FIGURE 8. Low-Leakage Sample-and-Hold

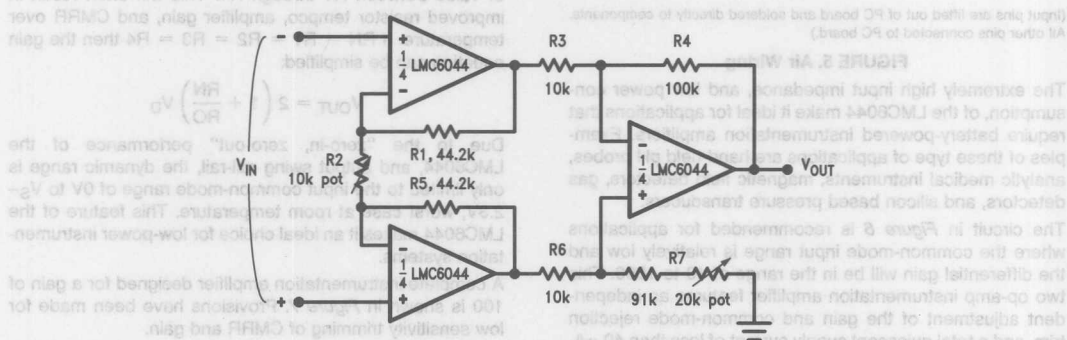


FIGURE 9. Instrumentation Amplifier

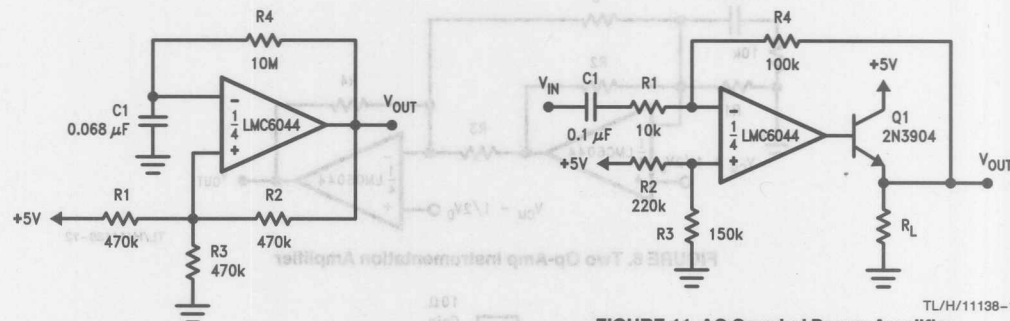
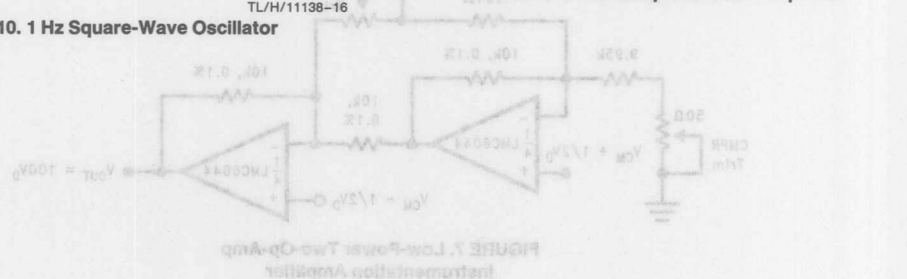
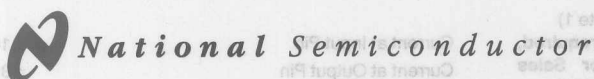


FIGURE 10. 1 Hz Square-Wave Oscillator

FIGURE 11. AC Coupled Power Amplifier





LMC6061

LMC6061 Precision CMOS Single Micropower Operational Amplifier

General Description

The LMC6061 is a precision single low offset voltage, micro-power operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6061 ideally suited for battery powered applications.

Other applications using the LMC6061 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

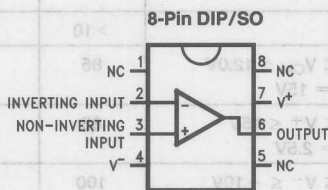
This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6081 precision single operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6062 or LMC6064 respectively.

PATENT PENDING

Connection Diagram



Top View

Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 8-Pin Molded DIP | LMC6061AMN | LMC6061AIN LMC6061IN | N08E | Rail |
| 8-Pin Small Outline | | LMC6061AIM LMC6061IM | M08A | Rail Tape and Reel |
| 8-Pin Ceramic DIP | LMC6061AMJ/883 | | J08A | Rail |

Features (Typical Unless Otherwise Noted)

- Low offset voltage 100 μ V
- Ultra low supply current 20 μ A
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V-
- High voltage gain 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage \pm Supply Voltage
 Voltage at Input/Output Pin (V⁺) +0.3V,
 (V⁻) -0.3V

Supply Voltage (V⁺ - V⁻) 16V

Output Short Circuit to V⁺ (Note 10)

Output Short Circuit to V⁻ (Note 2)

Lead Temperature (Soldering, 10 sec.) 260°C

Storage Temp. Range -65°C to +150°C

Junction Temperature 150°C

ESD Tolerance (Note 4) 2 kV

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

Current at Input Pin \pm 10 mA
 Current at Output Pin \pm 30 mA
 Current at Power Supply Pin 40 mA
 Power Dissipation (Note 3)

Operating Ratings (Note 1)

Temperature Range
 LMC6061AM -55°C ≤ T_J ≤ +125°C
 LMC6061AI, LMC6082I -40°C ≤ T_J ≤ +85°C

Supply Voltage 4.5V ≤ V⁺ ≤ 15.5V

Thermal Resistance (θ_{JA}) (Note 11)

N Package, 8-Pin Molded DIP 115°C/W

M Package, 8-Pin Surface Mount 193°C/W

Power Dissipation (Note 9)

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6061AM Limit (Note 6) | LMC6061AI Limit (Note 6) | LMC6061I Limit (Note 6) | Units | |
|-------------------|--|--|----------------------|--|--|--|------------|-------------|
| V _{OS} | Input Offset Voltage | | 100 | 350 1200 | 350 900 | 800 1300 | μV Max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C | |
| I _B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max | |
| I _{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max | |
| R _{IN} | Input Resistance | | > 10 | | | | Tera Ω | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 85 | 75 70 | 75 72 | 66 63 | dB Min | |
| + PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 85 | 75 70 | 75 72 | 66 63 | dB Min | |
| − PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V | 100 | 84 70 | 84 81 | 74 71 | dB Min | |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V for CMRR ≥ 60 dB | −0.4 | −0.1 0 | −0.1 0 | −0.1 0 | V Max | |
| | | | V ⁺ − 1.9 | V ⁺ − 2.3 V ⁺ − 2.6 | V ⁺ − 2.3 V ⁺ − 2.5 | V ⁺ − 2.3 V ⁺ − 2.5 | V Min | |
| A _V | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 4000 | 400 200 | 400 300 | 300 200 | V/mV Min |
| | | | Sinking | 3000 | 180 70 | 180 100 | 90 60 | V/mV Min |
| | | R _L = 25 kΩ (Note 7) | Sourcing | 3000 | 400 150 | 400 150 | 200 80 | V/mV Min |
| | | | Sinking | 2000 | 100 35 | 100 50 | 70 35 | V/mV Min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6061AM Limit (Note 6) | LMC6061AI Limit (Note 6) | LMC6061I Limit (Note 6) | Units |
|--------|--------------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|----------------------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to 2.5V | 4.995 | 4.990 4.970 | 4.990 4.980 | 4.950 4.925 | V Min |
| | | | 0.005 | 0.010 0.030 | 0.010 0.020 | 0.050 0.075 | V Max |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to 2.5V | 4.990 | 4.975 4.955 | 4.975 4.965 | 4.950 4.850 | V Min |
| | | | 0.010 | 0.020 0.045 | 0.020 0.035 | 0.050 0.150 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to 7.5V | 14.990 | 14.975 14.955 | 14.975 14.965 | 14.950 14.925 | V Min |
| | | | 0.010 | 0.025 0.050 | 0.025 0.035 | 0.050 0.075 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 25\text{ k}\Omega$ to 7.5V | 14.965 | 14.900 14.800 | 14.900 14.850 | 14.850 14.800 | V Min |
| | | | 0.025 | 0.050 0.200 | 0.050 0.150 | 0.100 0.200 | V Max |
| | Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | Sinking, $V_O = 5\text{V}$ | 21 | 16 7 | 16 8 | 16 8 | mA Min |
| I_O | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 25 | 15 9 | 15 10 | 15 10 | mA Min |
| | | Sinking, $V_O = 13\text{V}$ (Note 10) | 35 | 24 7 | 24 8 | 24 8 | mA Min |
| I_S | Supply Current | $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | 20 | 24 35 | 24 32 | 32 40 | μA Max |
| | | $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | 24 | 30 40 | 30 38 | 40 48 | μA Max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6061AM Limit (Note 6) | LMC6061AI Limit (Note 6) | LMC6061I Limit (Note 6) | Units |
|------------|------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|------------------------|
| SRV | Slew Rate | (Note 8) | 35 | 20 | 20 | 15 | V/ms Min |
| GBW | Gain-Bandwidth Product | | 100 | | | | kHz |
| θ_m | Phase Margin | | 50 | | | | Deg |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 83 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{PP}$ $\pm 5\text{V}$ Supply | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{Max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{Max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

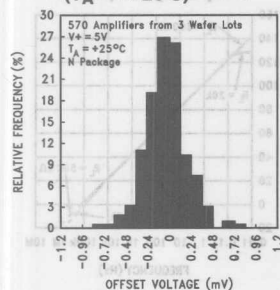
Note 10: Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 11: All numbers apply for packages soldered directly into a PC board.

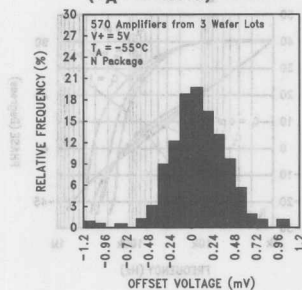
Note 12: For guaranteed Military Temperature Range parameters see RETSMC6061X.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

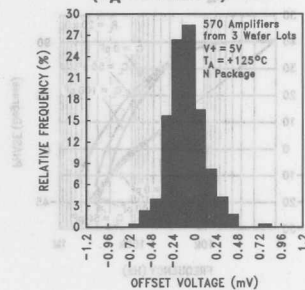
**Distribution of LMC6061
Input Offset Voltage
($T_A = +25^\circ C$)**



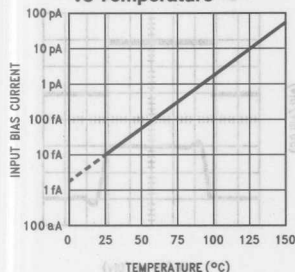
**Distribution of LMC6061
Input Offset Voltage
($T_A = -55^\circ C$)**



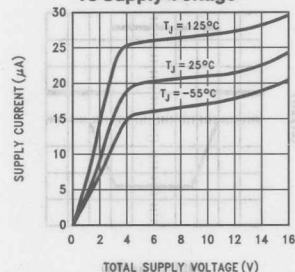
**Distribution of LMC6061
Input Offset Voltage
($T_A = +125^\circ C$)**



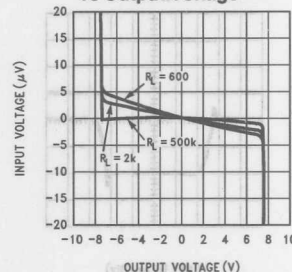
**Input Bias Current
vs Temperature**



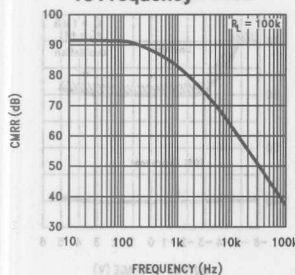
**Supply Current
vs Supply Voltage**



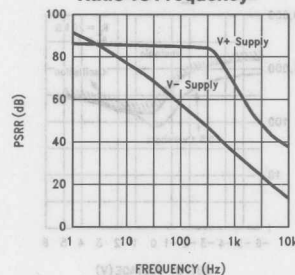
**Input Voltage
vs Output Voltage**



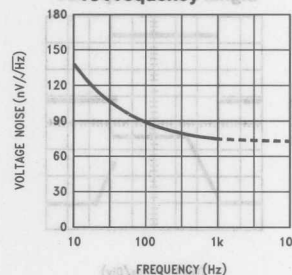
**Common Mode
Rejection Ratio
vs Frequency**



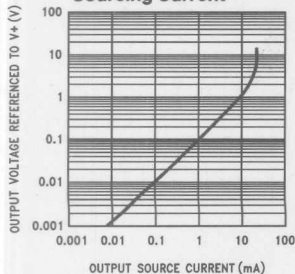
**Power Supply Rejection
Ratio vs Frequency**



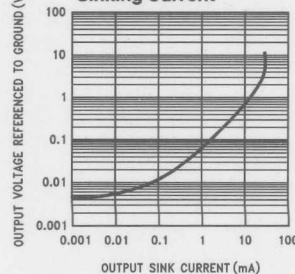
**Input Voltage Noise
vs Frequency**



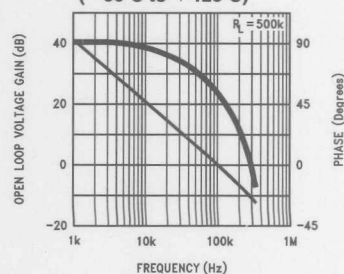
**Output Characteristics
Sourcing Current**



**Output Characteristics
Sinking Current**



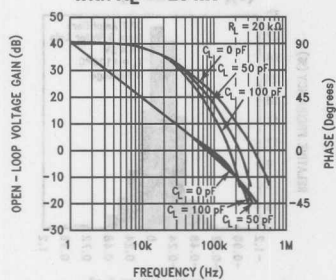
**Gain and Phase Response
vs Temperature
($-55^\circ C$ to $+125^\circ C$)**



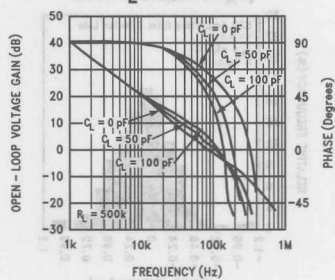
TL/H/11422-2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

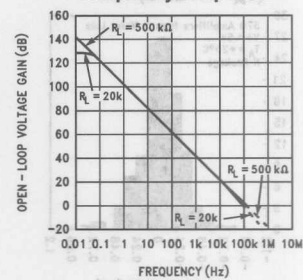
Gain and Phase Response vs Capacitive Load with $R_L = 20\text{ k}\Omega$



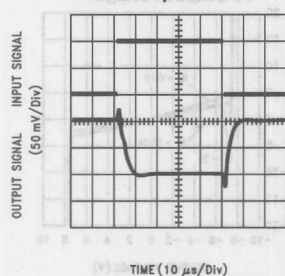
Gain and Phase Response vs Capacitive Load with $R_L = 500\text{ k}\Omega$



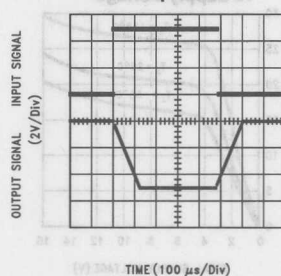
Open Loop Frequency Response



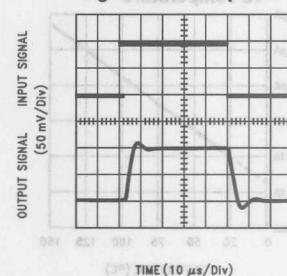
Inverting Small Signal Pulse Response



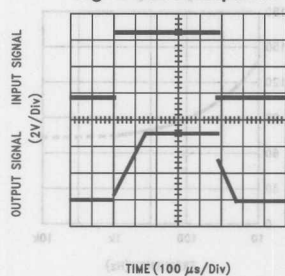
Inverting Large Signal Pulse Response



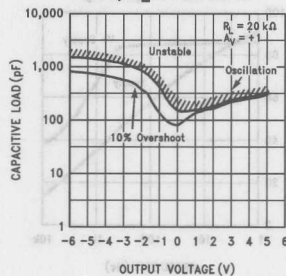
Non-Inverting Small Signal Pulse Response



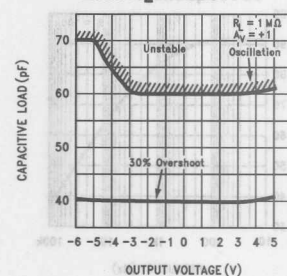
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load, $R_L = 20\text{ k}\Omega$



Stability vs Capacitive Load, $R_L = 1\text{ M}\Omega$



TL/H/11422-3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6061 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6061 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6061.

Although the LMC6061 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6061 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_i , around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

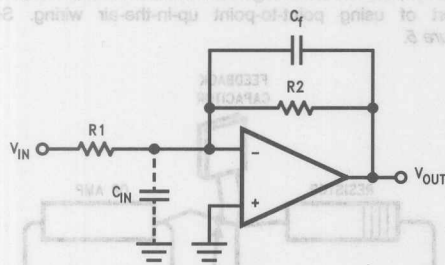


FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

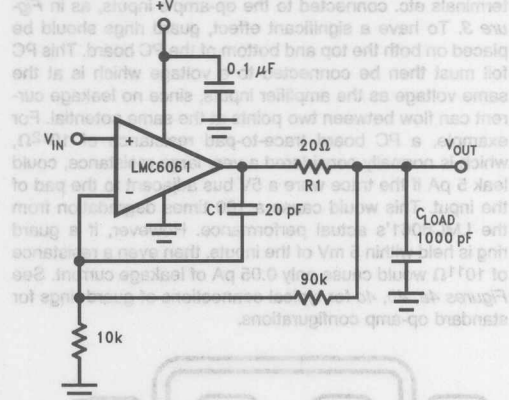


FIGURE 2a. LMC6061 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

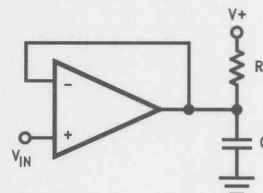


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6061, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6061's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6061's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

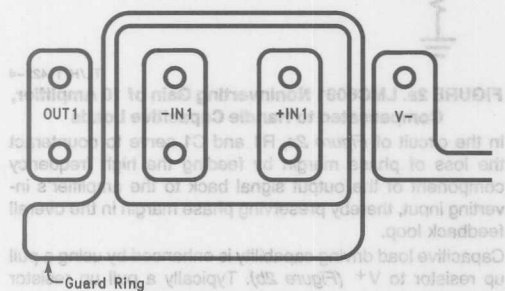


FIGURE 3. Example of Guard Ring in P.C. Board Layout

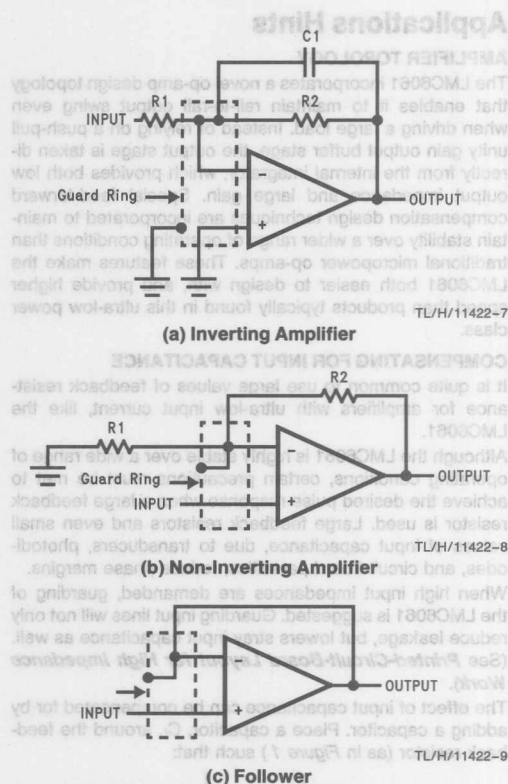
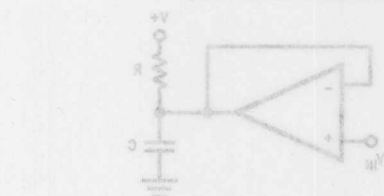


FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

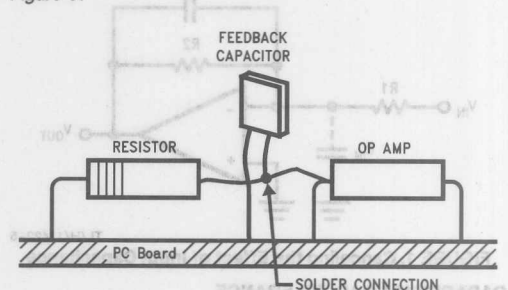


FIGURE 5. Air Wiring

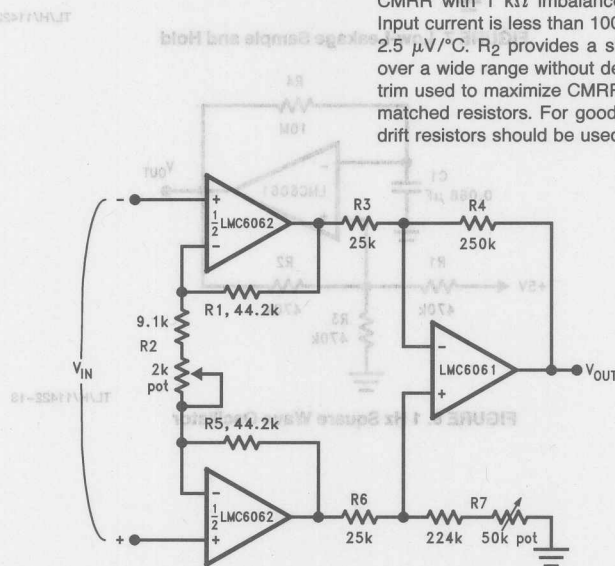
Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6061 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than $2.5 \mu V/^{\circ}C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

TL/H/11422-11

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

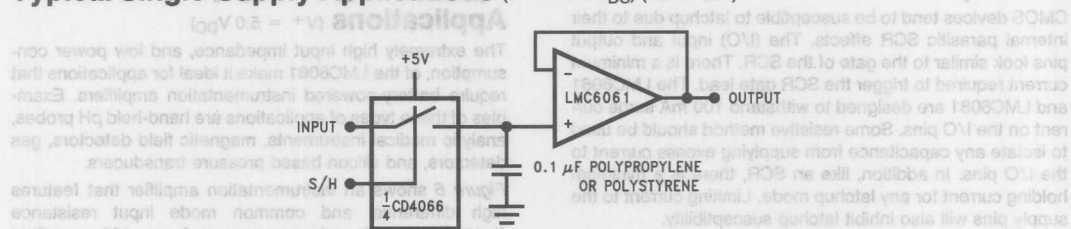


FIGURE 7. Low-Leakage Sample and Hold

TL/H/11422-12

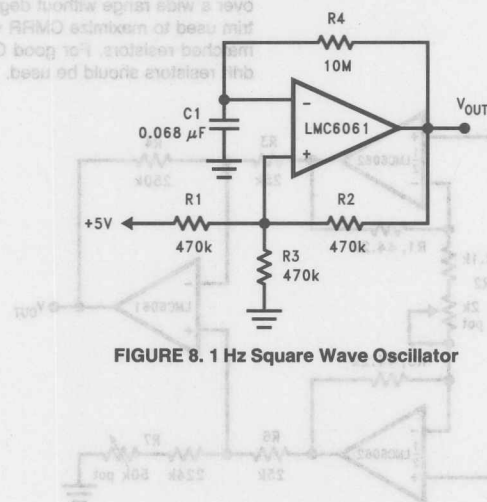


FIGURE 8. 1 Hz Square Wave Oscillator

TL/H/11422-13

LMC6062 Precision CMOS Dual Micropower Operational Amplifier

General Description

The LMC6062 is a precision dual low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption, make the LMC6062 ideally suited for battery powered applications.

Other applications using the LMC6062 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6082 precision dual operational amplifier.

Features (Typical Unless Otherwise Noted)

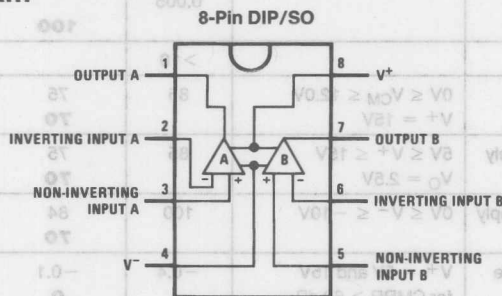
- Low offset voltage 100 μ V
- Ultra low supply current 16 μ A/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

PATENT PENDING

Connection Diagram



Top View

Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 8-Pin Molded DIP | LMC6062AMN | LMC6062AIN LMC6062IN | N08E | Rail |
| 8-Pin Small Outline | | LMC6062AIM LMC6062IM | M08A | Rail Tape and Reel |
| 8-Pin Ceramic DIP | LMC6062AMJ/883 | | J08A | Rail |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage \pm Supply Voltage
Voltage at Input/Output Pin $(V^+ + 0.3V, V^- - 0.3V)$

Supply Voltage $(V^+ - V^-)$ 16V

Output Short Circuit to V^+ (Note 11)

Output Short Circuit to V^- (Note 12)

Lead Temperature (Soldering, 10 sec.) 260°C

Storage Temp. Range -65°C to $+150^\circ\text{C}$

Junction Temperature 150°C

ESD Tolerance (Note 4) 2 kV

Current at Input Pin $\pm 10\text{ mA}$

Current at Output Pin $\pm 30\text{ mA}$

Current at Power Supply Pin 40 mA

Power Dissipation (Note 3)

Operating Ratings (Note 1)

Temperature Range

LMC6062AM $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

LMC6062AI, LMC6062I $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$

Supply Voltage $4.5\text{V} \leq V^+ \leq 15.5\text{V}$

Thermal Resistance (θ_{JA}) (Note 12)

8-Pin Molded DIP 115°C/W

8-Pin SO 193°C/W

Power Dissipation (Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6062AM Limit (Note 6) | LMC6062AI Limit (Note 6) | LMC6062I Limit (Note 6) | Units | |
|-------------------|--|--|----------------------|--|--|--|------------|-------------|
| V _{OS} | Input Offset Voltage | | 100 | 350 1200 | 350 900 | 800 1300 | μV Max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C | |
| I _B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max | |
| I _{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max | |
| R _{IN} | Input Resistance | | > 10 | | | | Tera Ω | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 85 | 75 70 | 75 72 | 66 63 | dB Min | |
| + PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 85 | 75 70 | 75 72 | 66 63 | dB Min | |
| − PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V | 100 | 84 70 | 84 81 | 74 71 | dB Min | |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V for CMRR ≥ 60 dB | −0.4 | −0.1 0 | −0.1 0 | −0.1 0 | V Max | |
| | | | V ⁺ − 1.9 | V ⁺ − 2.3 V ⁺ − 2.6 | V ⁺ − 2.3 V ⁺ − 2.5 | V ⁺ − 2.3 V ⁺ − 2.5 | V Min | |
| A _V | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 4000 | 400 200 | 400 300 | 300 200 | V/mV Min |
| | | | Sinking | 3000 | 180 70 | 180 100 | 90 60 | V/mV Min |
| | | R _L = 25 kΩ (Note 7) | Sourcing | 3000 | 400 150 | 400 150 | 200 80 | V/mV Min |
| | | | Sinking | 2000 | 100 35 | 100 50 | 70 35 | V/mV Min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6062AM Limit (Note 6) | LMC6062AI Limit (Note 6) | LMC6062I Limit (Note 6) | Units |
|--------|--------------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|----------------------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to 2.5V | 4.995 | 4.990 4.970 | 4.990 4.980 | 4.950 4.925 | V Min |
| | | | 0.005 | 0.010 0.030 | 0.010 0.020 | 0.050 0.075 | V Max |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to 2.5V | 4.990 | 4.975 4.955 | 4.975 4.965 | 4.950 4.850 | V Min |
| | | | 0.010 | 0.020 0.045 | 0.020 0.035 | 0.050 0.150 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to 7.5V | 14.990 | 14.975 14.955 | 14.975 14.965 | 14.950 14.925 | V Min |
| | | | 0.010 | 0.025 0.050 | 0.025 0.035 | 0.050 0.075 | V Max |
| | | | 14.965 | 14.900 14.800 | 14.900 14.850 | 14.850 14.800 | V Min |
| | | | 0.025 | 0.050 0.200 | 0.050 0.150 | 0.100 0.200 | V Max |
| | | Sourcing, $V_O = 0\text{V}$ | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | | 21 | 16 7 | 16 8 | 16 8 | mA Min |
| I_O | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 25 | 15 9 | 15 10 | 15 10 | mA Min |
| | | Sinking, $V_O = 13\text{V}$ (Note 11) | 35 | 24 7 | 24 8 | 24 8 | mA Min |
| | | | | | | | |
| I_S | Supply Current | Both Amplifiers $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | 32 | 38 60 | 38 46 | 46 56 | μA Max |
| | | Both Amplifiers $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | 40 | 47 70 | 47 55 | 57 66 | μA Max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

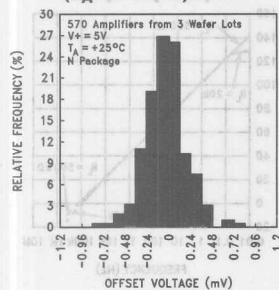
| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6062AM Limit (Note 6) | LMC6062AI Limit (Note 6) | LMC6062I Limit (Note 6) | Units |
|------------|------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|------------------------|
| SR | Slew Rate | (Note 8) | 35 | 20 | 20 | 15 | V/ms Min |
| GBW | Gain-Bandwidth Product | | 100 | | | | kHz |
| θ_m | Phase Margin | | 50 | | | | Deg |
| | Amp-to-Amp Isolation | (Note 9) | 155 | | | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 83 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{pp}$ $\pm 5\text{V Supply}$ | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.
Note 3: The maximum power dissipation is a function of $T_{J(\text{Max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{Max})} - T_A)/\theta_{JA}$.
Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .
Note 5: Typical values represent the most likely parametric norm.
Note 6: All limits are guaranteed by testing or statistical analysis.
Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.
Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.
Note 9: Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 100 Hz to produce $V_O = 12\text{ V}_{pp}$.
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.
Note 11: Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.
Note 12: All numbers apply for packages soldered directly into a PC board.
Note 13: For guaranteed Military Temperature Range parameters, see RETSMC6062X.

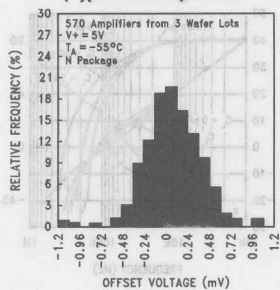
| | | | | | | | |
|-----------------|----|----|----|----|--|----------------|----|
| I_{AQ} Max | 64 | 38 | 38 | 32 | Both Amplifiers $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | Supply Current | 12 |
| I_{AQ} Max | 57 | 47 | 47 | 40 | Both Amplifiers $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | | |

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

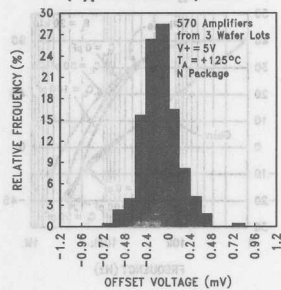
**Distribution of LMC6062
Input Offset Voltage
($T_A = +25^\circ C$)**



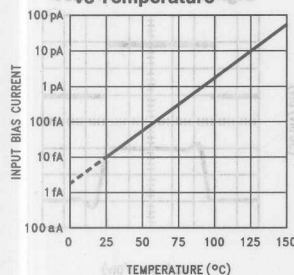
**Distribution of LMC6062
Input Offset Voltage
($T_A = -55^\circ C$)**



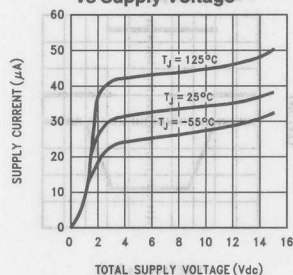
**Distribution of LMC6062
Input Offset Voltage
($T_A = +125^\circ C$)**



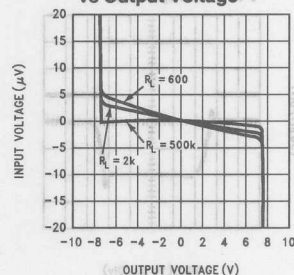
**Input Bias Current
vs Temperature**



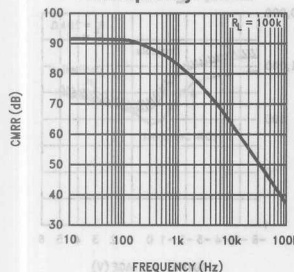
**Supply Current
vs Supply Voltage**



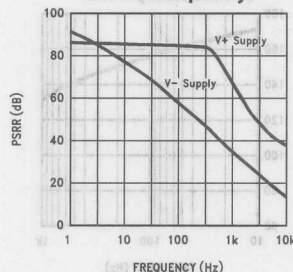
**Input Voltage
vs Output Voltage**



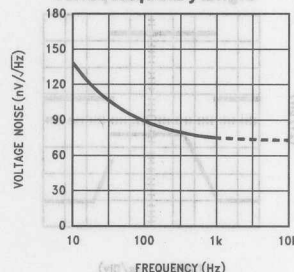
**Common Mode
Rejection Ratio
vs Frequency**



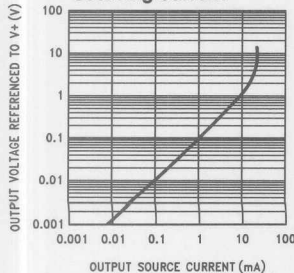
**Power Supply Rejection
Ratio vs Frequency**



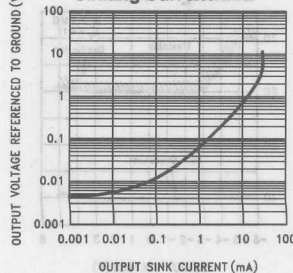
**Input Voltage Noise
vs Frequency**



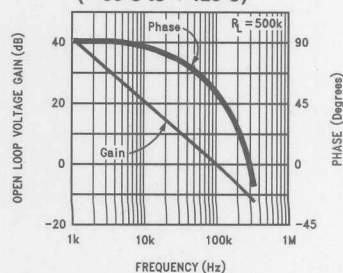
**Output Characteristics
Sourcing Current**



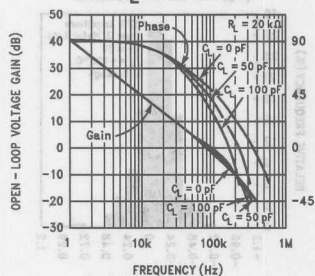
**Output Characteristics
Sinking Current**



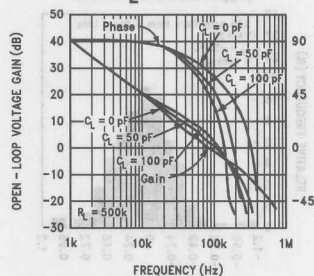
**Gain and Phase Response
vs Temperature
($-55^\circ C$ to $+125^\circ C$)**



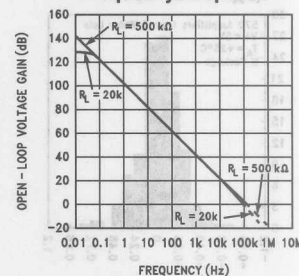
Gain and Phase Response vs Capacitive Load with $R_L = 20\text{ k}\Omega$



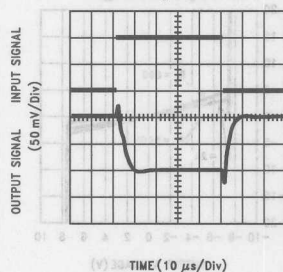
Gain and Phase Response vs Capacitive Load with $R_L = 500\text{ k}\Omega$



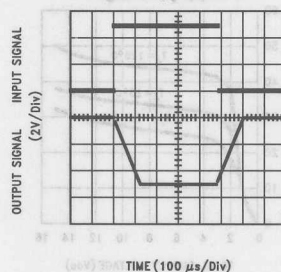
Open Loop Frequency Response



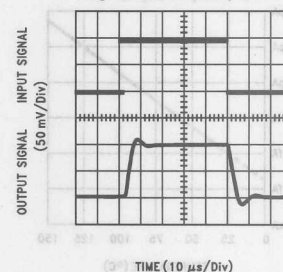
Inverting Small Signal Pulse Response



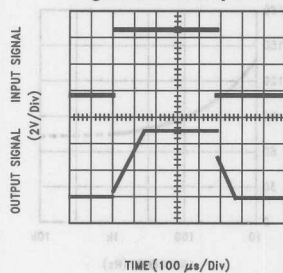
Inverting Large Signal Pulse Response



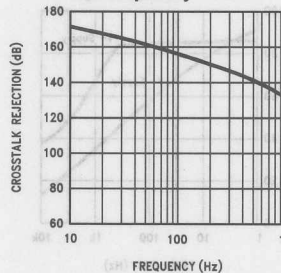
Non-Inverting Small Signal Pulse Response



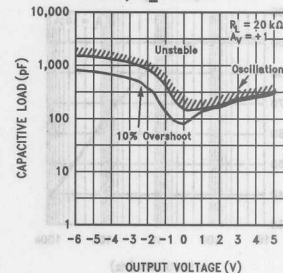
Non-Inverting Large Signal Pulse Response



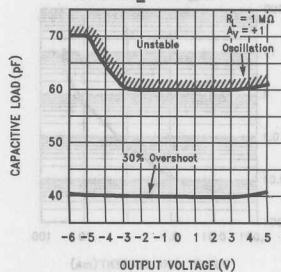
Crosstalk Rejection vs Frequency



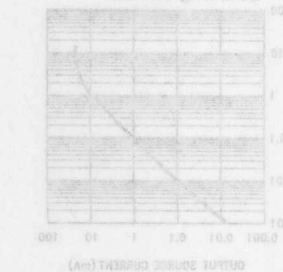
Stability vs Capacitive Load, $R_L = 20\text{ k}\Omega$



Stability vs Capacitive Load $R_L = 1\text{ M}\Omega$



Output Characteristics



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6062 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6062 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6062.

Although the LMC6062 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6062 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f , around the feedback resistor (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad \text{or} \quad R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

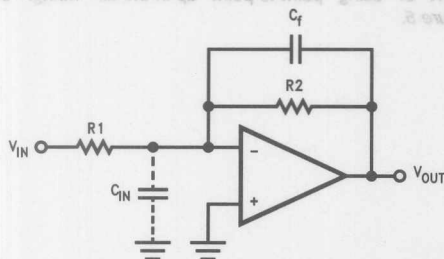


FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

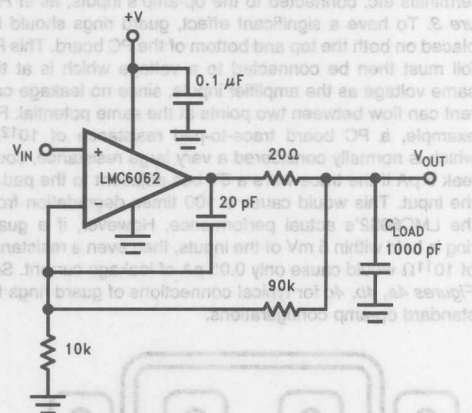


FIGURE 2a. LMC6062 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

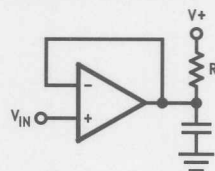


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6062, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6062's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in *Figure 3*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6062's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See *Figures 4a, 4b, 4c* for typical connections of guard rings for standard op-amp configurations.

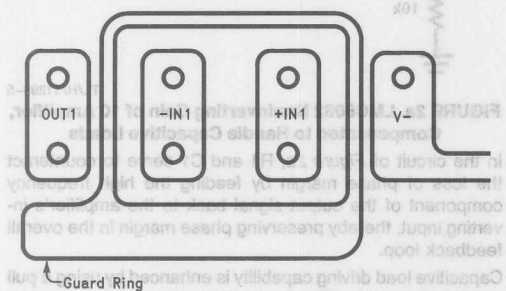


FIGURE 3. Example of Guard Ring in P.C. Board Layout

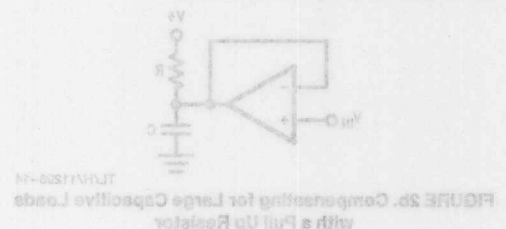
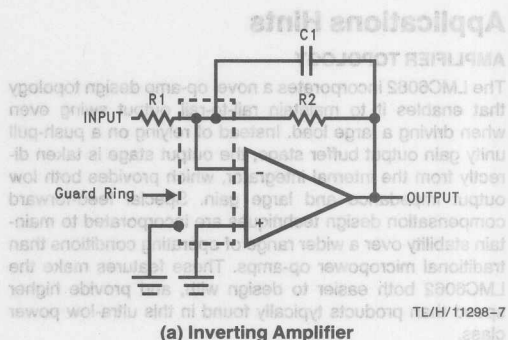
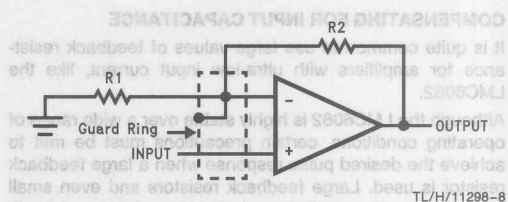


FIGURE 3b. Compensating for Large Capacitive Loads with a Pull Up Resistor

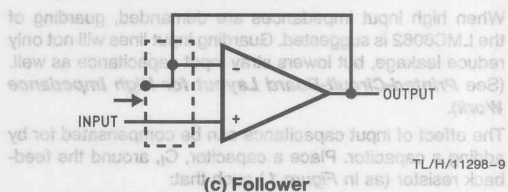
PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6062, typically less than 10 pA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakage are



(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 5*.

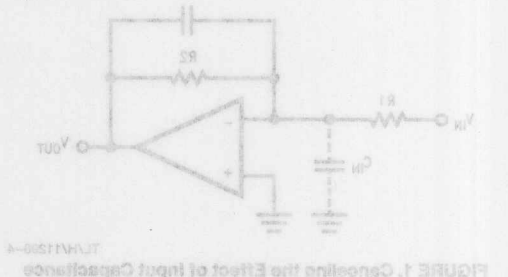
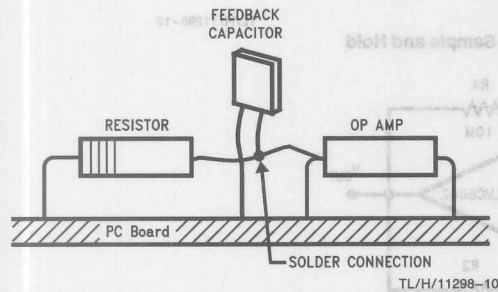


FIGURE 5. Cancelling the Effect of Input Capacitance

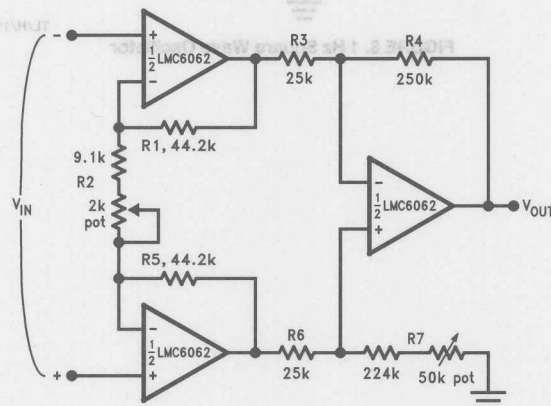
CAPACITIVE LOAD TOLERANCE
All full-to-full output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6062 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than 2.5 $\mu V/^{\circ}C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

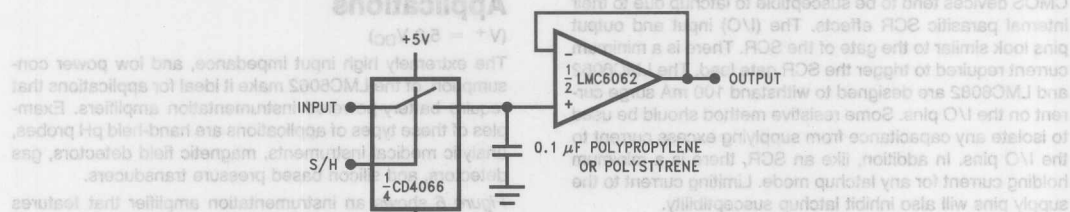


FIGURE 7. Low-Leakage Sample and Hold

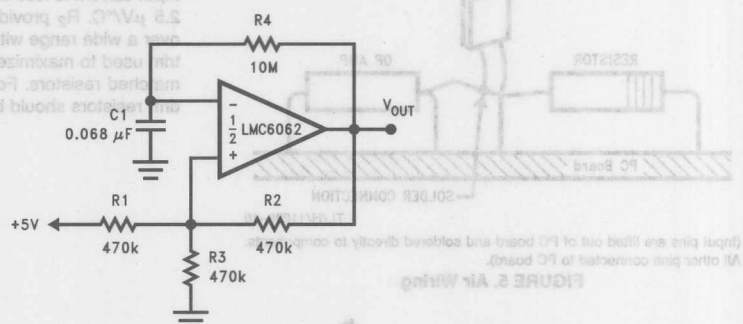


FIGURE 8. 1 Hz Square Wave Oscillator

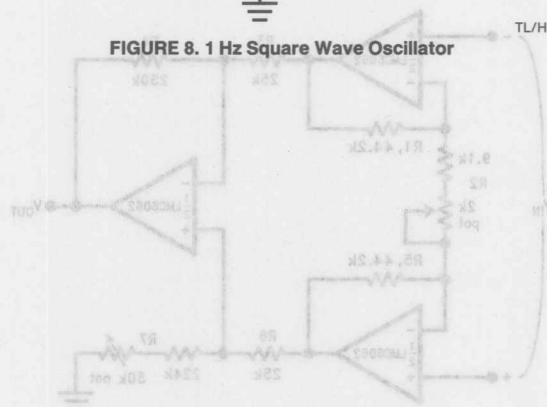
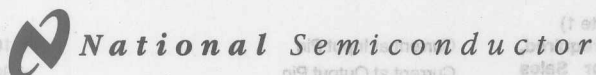


FIGURE 9. Instrumentation Amplifier



LMC6064 Precision CMOS Quad Micropower Operational Amplifier

General Description

The LMC6064 is a precision quad low offset voltage, micropower operational amplifier, capable of precision single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low power consumption make the LMC6064 ideally suited for battery powered applications.

Other applications using the LMC6064 include precision full-wave rectifiers, integrators, references, sample-and-hold circuits, and true instrumentation amplifiers.

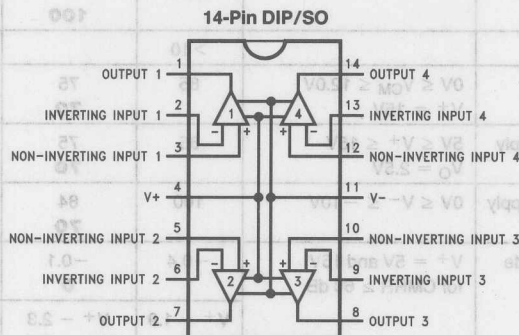
This device is built with National's advanced double-Poly Silicon-Gate CMOS process.

For designs that require higher speed, see the LMC6084 precision quad operational amplifier.

For single or dual operational amplifier with similar features, see the LMC6061 or LMC6062 respectively.

PATENT PENDING

Connection Diagram



Top View

TL/H/11466-1

Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|----------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 14-Pin Molded DIP | LMC6064AMN | LMC6064AIN LMC6064IN | N14A | Rail |
| 14-Pin Small Outline | | LMC6064AIM LMC6064IM | M14A | Rail Tape and Reel |
| 14-Pin Ceramic DIP | LMC6064AMJ | | J14A | Rail |

Features (Typical Unless Otherwise Noted)

- Low offset voltage 100 μ V
- Ultra low supply current 16 μ A/Amplifier
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing within 10 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 140 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Hand-held analytic instruments
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

Office/Distributors for availability and specifications.

| | |
|---|---|
| Differential Input Voltage | ± Supply Voltage |
| Voltage at Input/Output Pin | (V ⁺) + 0.3V, (V ⁻) - 0.3V |
| Supply Voltage (V ⁺ - V ⁻) | 16V |
| Output Short Circuit to V ⁺ | (Note 1) |
| Output Short Circuit to V ⁻ | (Note 2) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Junction Temperature | 150°C |
| ESD Tolerance (Note 4) | 2 kV |

| | |
|-----------------------------|----------|
| Current at Output Pin | ±30 mA |
| Current at Power Supply Pin | 40 mA |
| Power Dissipation | (Note 3) |

Operating Ratings (Note 1)

| | |
|---|---------------------------------|
| Temperature Range | -55°C ≤ T _J ≤ +125°C |
| LMC6064AM | -40°C ≤ T _J ≤ +85°C |
| LMC6064AI, LMC6064I | 4.5V ≤ V ⁺ ≤ 15.5V |
| Supply Voltage | 4.5V ≤ V ⁺ ≤ 15.5V |
| Thermal Resistance (θ _{JA}) (Note 12) | 81°C/W |
| 14-Pin Molded DIP | 126°C/W |
| 14-Pin SO | (Note 10) |
| Power Dissipation | (Note 10) |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6064AM Limit (Note 6) | LMC6064AI Limit (Note 6) | LMC6064I Limit (Note 6) | Units | |
|-------------------|--|--|----------------------------------|---|---|---|--------------------------|-------------|
| V _{OS} | Input Offset Voltage | | 100 | 350 1200 | 350 900 | 800 1300 | μV Max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C | |
| I _B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max | |
| I _{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max | |
| R _{IN} | Input Resistance | | > 10 | | | | Tera Ω | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 85 | 75 70 | 75 72 | 66 63 | dB Min | |
| + PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 85 | 75 70 | 75 72 | 66 63 | dB Min | |
| − PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V | 100 | 84 70 | 84 81 | 74 71 | dB Min | |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V for CMRR ≥ 60 dB | −0.4 V ⁺ − 1.9 | −0.1 0 V ⁺ − 2.3 V ⁺ − 2.6 | −0.1 0 V ⁺ − 2.3 V ⁺ − 2.5 | −0.1 0 V ⁺ − 2.3 V ⁺ − 2.5 | V Max V Min | |
| A _V | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 4000 | 400 200 | 400 300 | 300 200 | V/mV Min |
| | | | Sinking | 3000 | 180 70 | 180 100 | 90 60 | V/mV Min |
| | | R _L = 25 kΩ (Note 7) | Sourcing | 3000 | 400 150 | 400 150 | 200 80 | V/mV Min |
| | | | Sinking | 2000 | 100 35 | 100 50 | 70 35 | V/mV Min |

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6064AM Limit (Note 6) | LMC6064AI Limit (Note 6) | LMC6064I Limit (Note 6) | Units |
|--------|-------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|-----------------|
| V_O | Output Swing | $V^+ = 5V$ $R_L = 100\text{ k}\Omega$ to $2.5V$ | 4.995 | 4.990 4.970 | 4.990 4.980 | 4.950 4.925 | V_{-2} Min |
| | | | 0.005 | 0.010 0.030 | 0.010 0.020 | 0.050 0.075 | V_{+2} Max |
| | | | 4.990 | 4.975 4.955 | 4.975 4.965 | 4.950 4.850 | V_{-1} Min |
| | | $V^+ = 5V$ $R_L = 25\text{ k}\Omega$ to $2.5V$ | 0.010 | 0.020 0.045 | 0.020 0.035 | 0.050 0.150 | V_{+1} Max |
| | | | 14.990 | 14.975 14.955 | 14.975 14.965 | 14.950 14.925 | V_{-1} Min |
| | | | 0.010 | 0.025 0.050 | 0.025 0.035 | 0.050 0.075 | V_{+1} Max |
| | | $V^+ = 15V$ $R_L = 100\text{ k}\Omega$ to $7.5V$ | 14.965 | 14.900 14.800 | 14.900 14.850 | 14.850 14.800 | V_{-1} Min |
| | | | 0.025 | 0.050 0.200 | 0.050 0.150 | 0.100 0.200 | V_{+1} Max |
| | | | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | | 21 | 16 7 | 16 8 | 16 8 | mA Min |
| I_O | Output Current $V^+ = 15V$ | Sourcing, $V_O = 0V$ | 25 | 15 9 | 15 10 | 15 10 | mA Min |
| | | Sinking, $V_O = 13V$ (Note 11) | 35 | 24 7 | 24 8 | 24 8 | mA Min |
| I_S | Supply Current | All Four Amplifiers $V^+ = +5V$, $V_O = 1.5V$ | 64 | 76 120 | 76 92 | 92 112 | μA Max |
| | | All Four Amplifiers $V^+ = +15V$, $V_O = 7.5V$ | 80 | 94 140 | 94 110 | 114 132 | μA Max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6064AM Limit (Note 6) | LMC6064AI Limit (Note 6) | LMC6064I Limit (Note 6) | Units |
|------------|------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|------------------------|
| SR | Slew Rate | (Note 8) | 35 | 20 8 | 20 10 | 15 7 | V/ms Min |
| GBW | Gain-Bandwidth Product | | 100 | | | | kHz |
| θ_m | Phase Margin | | 50 | | | | Deg |
| | Amp-to-Amp Isolation | (Note 9) | 155 | | | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 83 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 1\text{ kHz}$, $A_V = -5$ $R_L = 100\text{ k}\Omega$, $V_O = 2\text{ V}_{PP}$ $\pm 5\text{V}$ Supply | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{Max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{Max})} - T_A)/\theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 100 Hz to produce $V_O = 12\text{ V}_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 11: Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

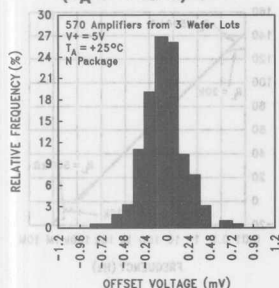
Note 12: All numbers apply for packages soldered directly into a PC board.

Note 13: For guaranteed Military Temperature Range parameters see RETSMC6064X.

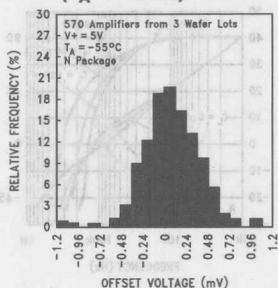
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

LMC6064

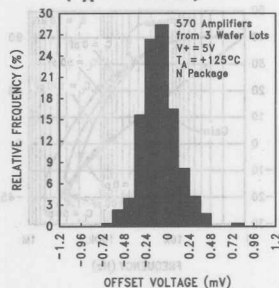
**Distribution of LMC6064
Input Offset Voltage
($T_A = +25^\circ C$)**



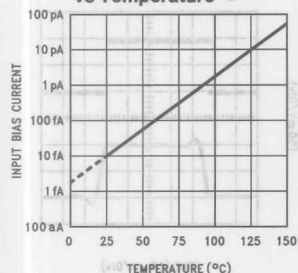
**Distribution of LMC6064
Input Offset Voltage
($T_A = -55^\circ C$)**



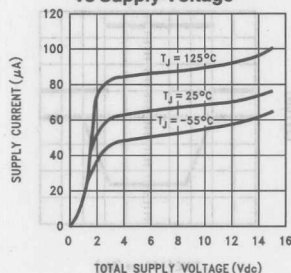
**Distribution of LMC6064
Input Offset Voltage
($T_A = +125^\circ C$)**



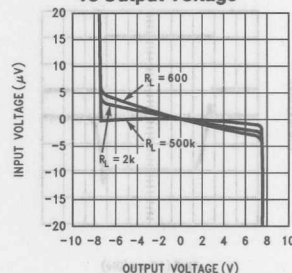
**Input Bias Current
vs Temperature**



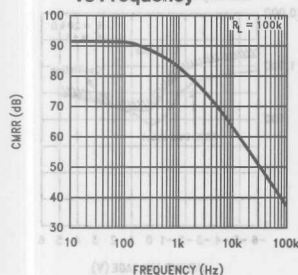
**Supply Current
vs Supply Voltage**



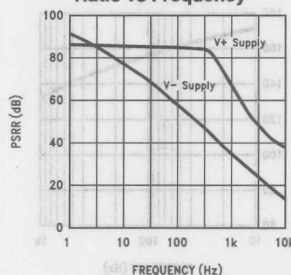
**Input Voltage
vs Output Voltage**



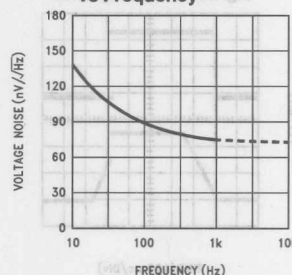
**Common Mode
Rejection Ratio
vs Frequency**



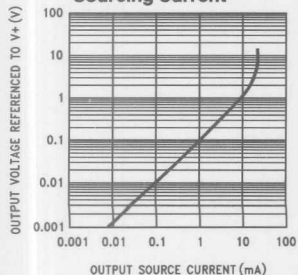
**Power Supply Rejection
Ratio vs Frequency**



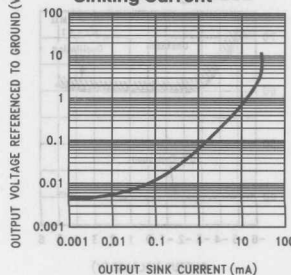
**Input Voltage Noise
vs Frequency**



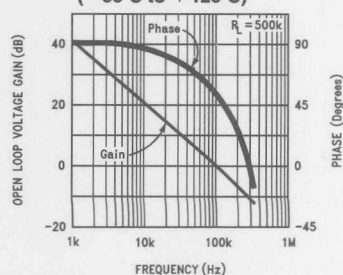
**Output Characteristics
Sourcing Current**

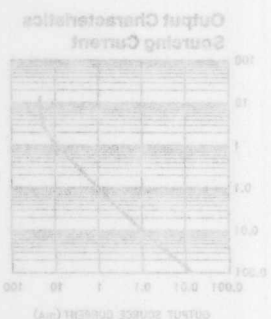
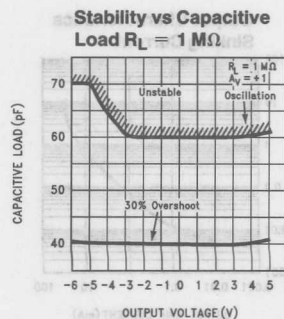
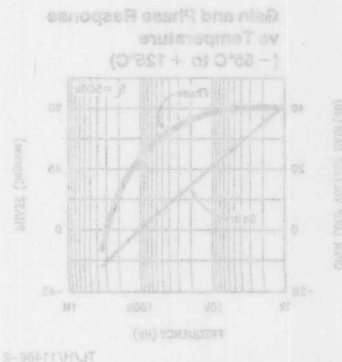
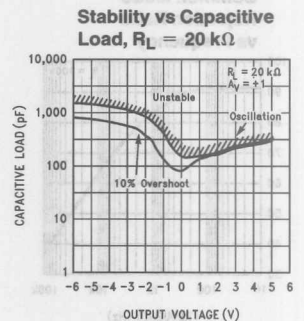
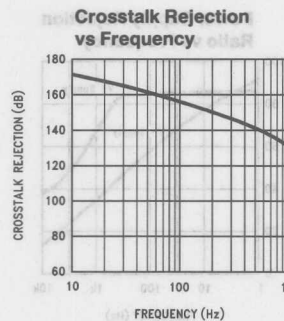
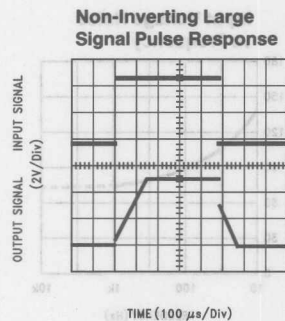
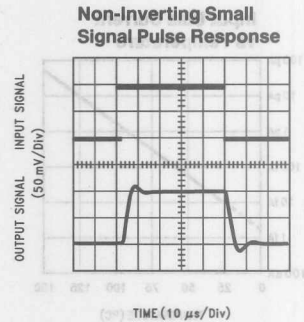
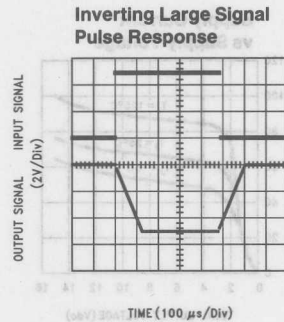
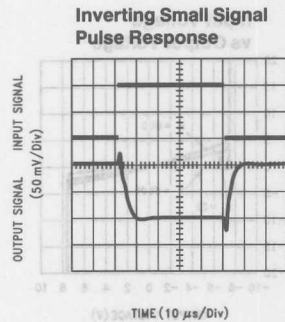
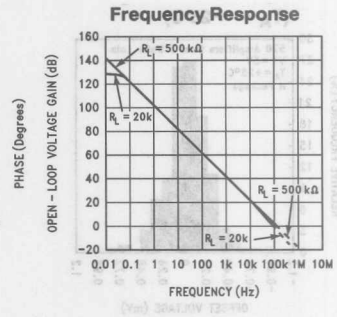
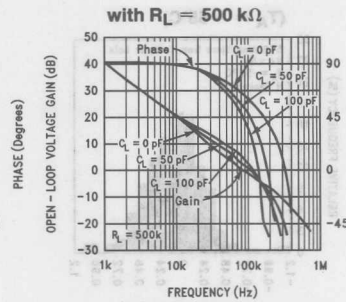
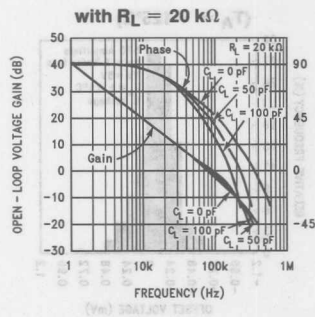


**Output Characteristics
Sinking Current**



**Gain and Phase Response
vs Temperature
($-55^\circ C$ to $+125^\circ C$)**





Applications Hints

AMPLIFIER TOPOLOGY

The LMC6064 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6064 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6064.

Although the LMC6064 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6064 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor. Place a capacitor, C_f , around the feedback resistor (as in Figure 1) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and the LMC662 for a more detailed discussion on compensating for input capacitance.

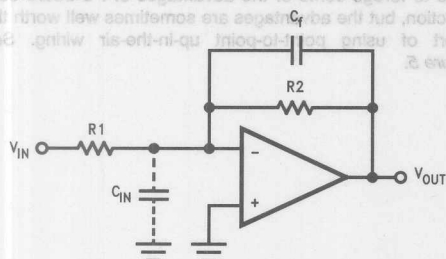


FIGURE 1. Canceling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominate pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2a.

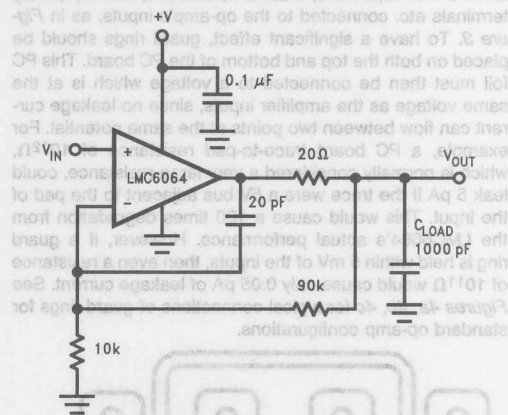


FIGURE 2a. LMC6064 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 2a, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting 10 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

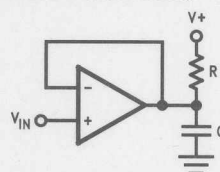


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6064, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are

Applications Hints (Continued)

quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6064's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6064's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

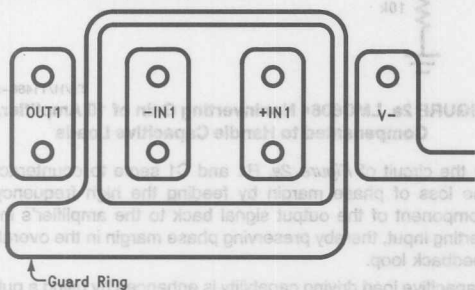


FIGURE 3. Example of Guard Ring in P.C. Board Layout

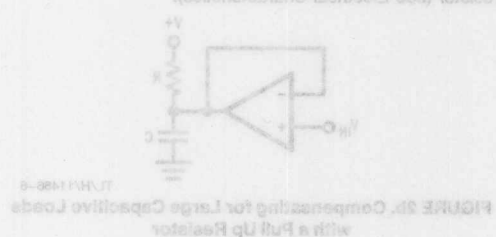


FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

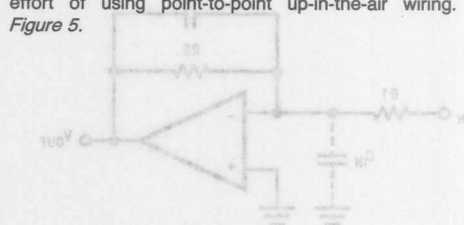
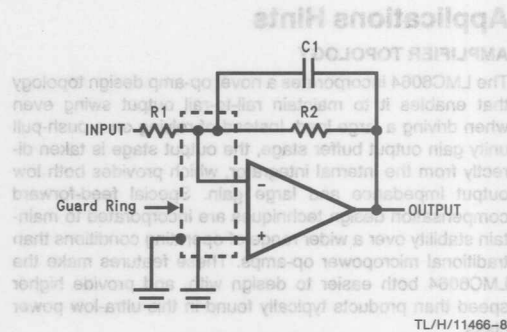
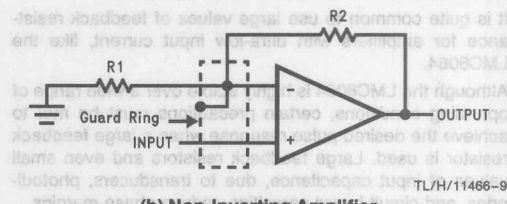


FIGURE 5. Cancelling the Effect of Input Capacitance

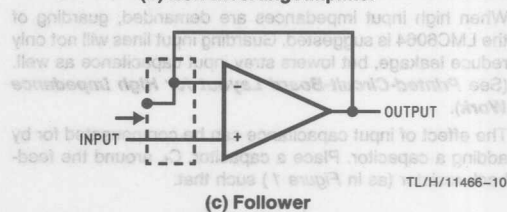
Capacitive load tolerance. All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in the integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).



(a) Inverting Amplifier

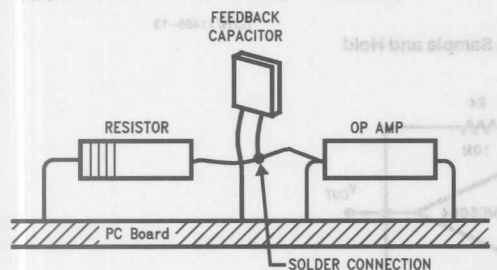


(b) Non-Inverting Amplifier



(c) Follower

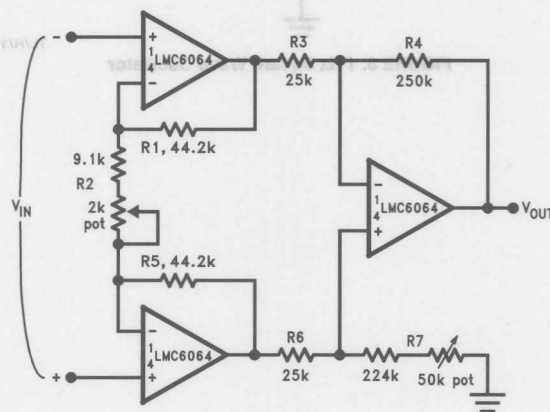
internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6064 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring



TL/H/11466-12

If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6064 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 100$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than $2.5 \mu V/^{\circ}C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{DC}$) (Continued)

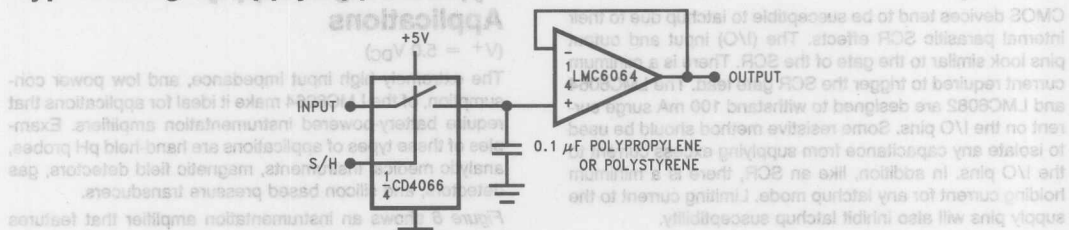


FIGURE 7. Low-Leakage Sample and Hold

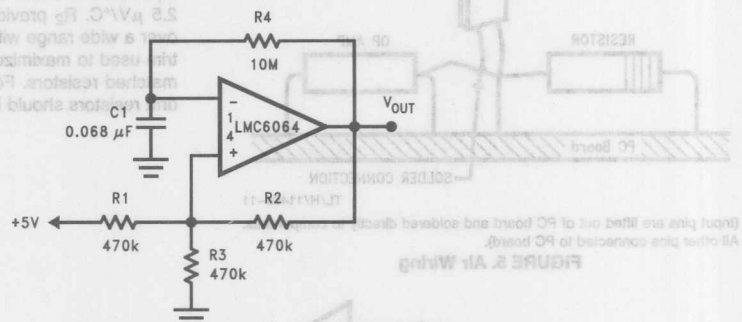


FIGURE 8. 1 Hz Square Wave Oscillator

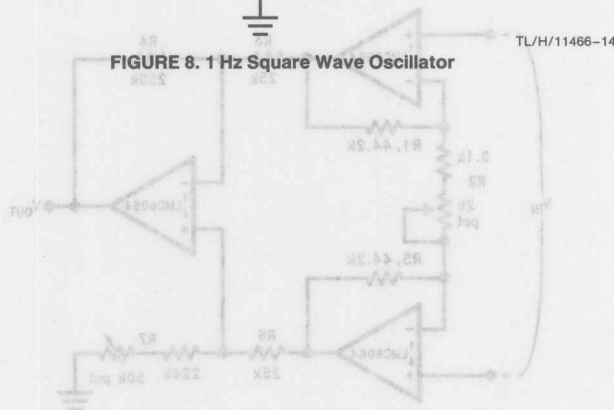


FIGURE 9. Instrumentation Amplifier

LMC6081 Precision CMOS Single Operational Amplifier

General Description

The LMC6081 is a precision low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6081 ideally suited for precision circuit applications.

Other applications using the LMC6081 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6061 precision micropower operational amplifier.

For a dual or quad operational amplifier with similar features, see the LMC6082 or LMC6084 respectively.

Features (Typical unless otherwise stated)

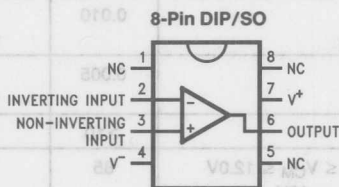
- Low offset voltage 150 μ V
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V_{-}
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

PATENT PENDING

Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 8-Pin Molded DIP | LMC6081AMN | LMC6081AIN LMC6081IIN | N08E | Rail |
| 8-Pin Small Outline | | LMC6081AIM LMC6081IIM | M08A | Rail Tape and Reel |

Office/Distributors for availability and specifications.

| | |
|---|---|
| Differential Input Voltage | ± Supply Voltage |
| Voltage at Input/Output Pin | (V ⁺) + 0.3V, (V ⁻) - 0.3V |
| Supply Voltage (V ⁺ - V ⁻) | 16V |
| Output Short Circuit to V ⁺ | (Note 10) |
| Output Short Circuit to V ⁻ | (Note 2) |
| Lead Temperature (Soldering, 10 Sec.) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Junction Temperature | 150°C |

| | |
|-----------------------------|----------|
| Current at Input Pin | ± 10 mA |
| Current at Output Pin | ± 30 mA |
| Current at Power Supply Pin | 40 mA |
| Power Dissipation | (Note 3) |

Operating Ratings (Note 1)

| | |
|--|---------------------------------|
| Temperature Range | -55°C ≤ T _J ≤ +125°C |
| LMC6081AM | -55°C ≤ T _J ≤ +125°C |
| LMC6081AI, LMC6081I | -40°C ≤ T _J ≤ +85°C |
| Supply Voltage | 4.5V ≤ V ⁺ ≤ 15.5V |
| Thermal Resistance (θ _{JA}), (Note 11) | |
| N Package, 8-Pin Molded DIP | 115°C/W |
| M Package, 8-Pin Surface Mount | 193°C/W |
| Power Dissipation (Note 9) | |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1M unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6081AM Limit (Note 6) | LMC6081AI Limit (Note 6) | LMC6081I Limit (Note 6) | Units | |
|-------------------|--|--|----------------------|--|--|--|------------|-------------|
| V _{OS} | Input Offset Voltage | | 150 | 350 1000 | 350 800 | 800 1300 | μV Max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C | |
| I _B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max | |
| I _{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max | |
| R _{IN} | Input Resistance | | > 10 | | | | Tera Ω | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 85 | 75 72 | 75 72 | 66 63 | dB Min | |
| + PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 85 | 75 72 | 75 72 | 66 63 | dB Min | |
| − PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V | 94 | 84 81 | 84 81 | 74 71 | dB Min | |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V for CMRR ≥ 60 dB | −0.4 | −0.1 0 | −0.1 0 | −0.1 0 | V Max | |
| | | | V ⁺ − 1.9 | V ⁺ − 2.3 V ⁺ − 2.6 | V ⁺ − 2.3 V ⁺ − 2.5 | V ⁺ − 2.3 V ⁺ − 2.5 | V Min | |
| A _V | Large Signal Voltage Gain | R _L = 2 kΩ (Note 7) | Sourcing | 1400 | 400 300 | 400 300 | 300 200 | V/mV Min |
| | | | Sinking | 350 | 180 70 | 180 100 | 90 60 | V/mV Min |
| | | R _L = 600Ω (Note 7) | Sourcing | 1200 | 400 150 | 400 150 | 200 80 | V/mV Min |
| | | | Sinking | 150 | 100 35 | 100 50 | 70 35 | V/mV Min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6081AM Limit (Note 6) | LMC6081AI Limit (Note 6) | LMC6081I Limit (Note 6) | Units |
|-------------------|--------------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|----------------------|
| V_O V Min | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.80 4.70 | 4.80 4.73 | 4.75 4.67 | V Min |
| | | | 0.10 | 0.13 0.19 | 0.13 0.17 | 0.20 0.24 | V Max |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V | 4.61 | 4.50 4.24 | 4.50 4.31 | 4.40 4.21 | V Min |
| | | | 0.30 | 0.40 0.63 | 0.40 0.50 | 0.50 0.63 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 14.50 14.30 | 14.50 14.34 | 14.37 14.25 | V Min |
| | | | 0.26 | 0.35 0.48 | 0.35 0.45 | 0.44 0.56 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V | 13.90 | 13.35 12.80 | 13.35 12.86 | 12.92 12.44 | V Min |
| | | | 0.79 | 1.16 1.42 | 1.16 1.32 | 1.33 1.58 | V Max |
| | | Output Current $V^+ = 5\text{V}$ | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | | | 16 11 | 16 13 | 13 10 | mA Min |
| I_O | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 30 | 28 18 | 28 22 | 23 18 | mA Min |
| | | Sinking, $V_O = 13\text{V}$ (Note 10) | 34 | 28 19 | 28 22 | 23 18 | mA Min |
| | | | | | | | |
| I_S | Supply Current | $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | 450 | 750 900 | 750 900 | 750 900 | μA Max |
| | | $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | 550 | 850 950 | 850 950 | 850 950 | μA Max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6081AM Limit (Note 6) | LMC6081AI Limit (Note 6) | LMC6081 Limit (Note 6) | Units |
|----------|------------------------------|--|-----------------|--------------------------------|--------------------------------|------------------------------|-------------------------|
| SR | Slew Rate | (Note 8) | 1.5 | 0.8 0.5 | 0.8 0.6 | 0.8 0.6 | V/ μs Min |
| GBW | Gain-Bandwidth Product | | 1.3 | | | | MHz |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{\text{PP}}$ $\pm 5\text{V Supply}$ | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{Max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{Max})} - T_A) / \theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{\text{CM}} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

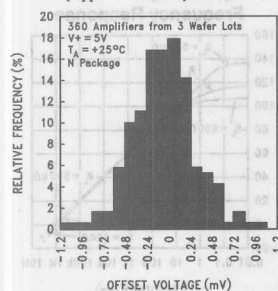
Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$.

Note 10: Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

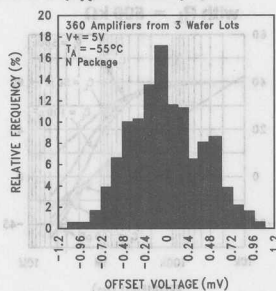
Note 11: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

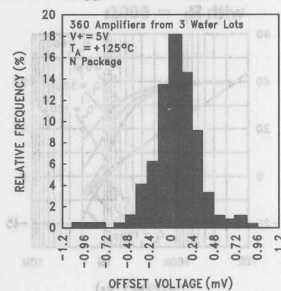
**Distribution of LMC6081
Input Offset Voltage
($T_A = +25^\circ C$)**



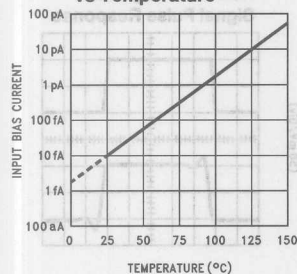
**Distribution of LMC6081
Input Offset Voltage
($T_A = -55^\circ C$)**



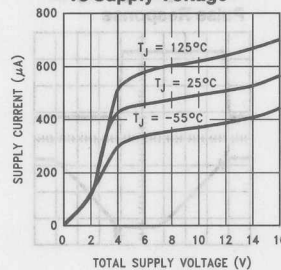
**Distribution of LMC6081
Input Offset Voltage
($T_A = +125^\circ C$)**



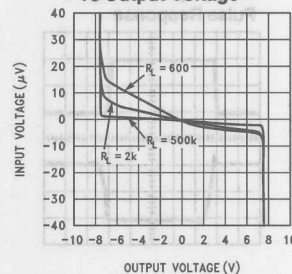
**Input Bias Current
vs Temperature**



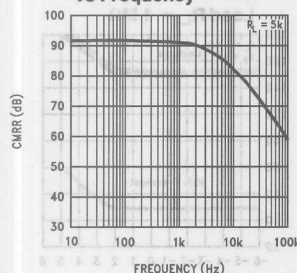
**Supply Current
vs Supply Voltage**



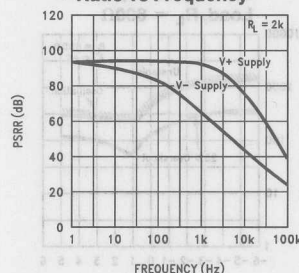
**Input Voltage
vs Output Voltage**



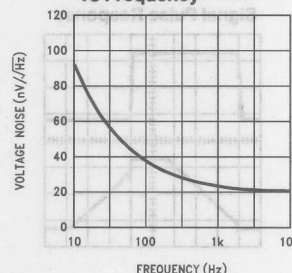
**Common Mode
Rejection Ratio
vs Frequency**



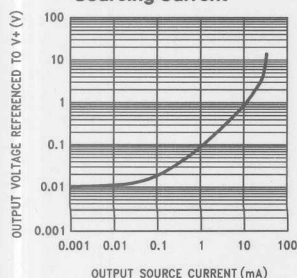
**Power Supply Rejection
Ratio vs Frequency**



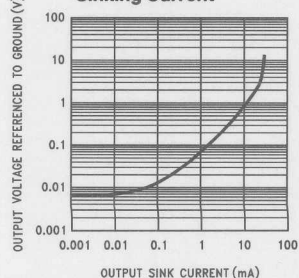
**Input Voltage Noise
vs Frequency**



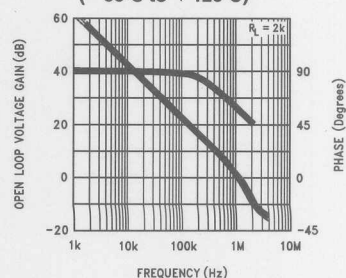
**Output Characteristics
Sourcing Current**



**Output Characteristics
Sinking Current**



**Gain and Phase Response
vs Temperature
($-55^\circ C$ to $+125^\circ C$)**

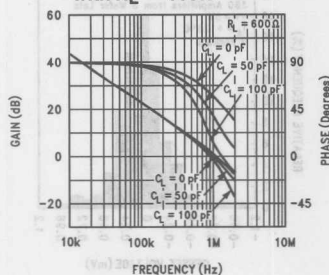


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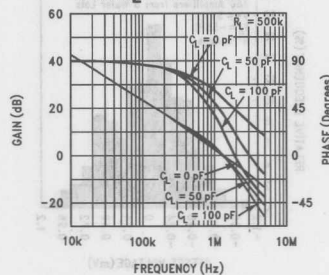
Typical Performance Characteristics (Continued)

$V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

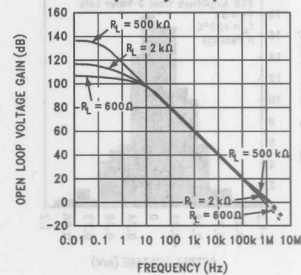
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



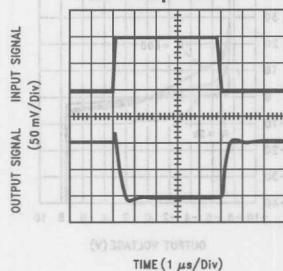
Gain and Phase Response vs Capacitive Load with $R_L = 500k\Omega$



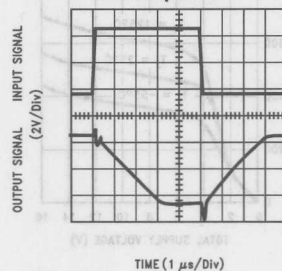
Open Loop Frequency Response



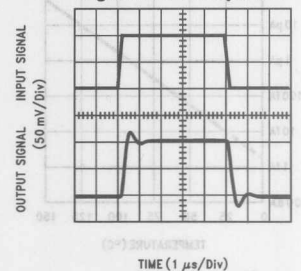
Inverting Small Signal Pulse Response



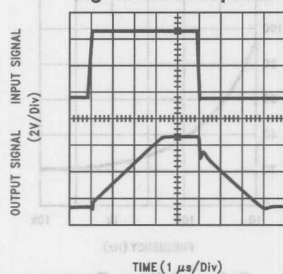
Inverting Large Signal Pulse Response



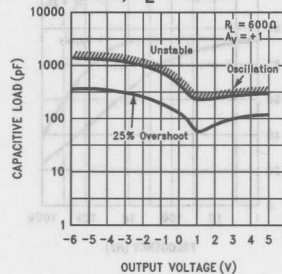
Non-Inverting Small Signal Pulse Response



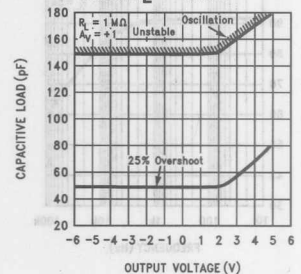
Non-Inverting Large Signal Pulse Response



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1M\Omega$



TL/H/11423-3

Applications Hints

AMPLIFIER TOPOLOGY

The LMC6081 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6081 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6081.

Although the LMC6081 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6081 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad \text{or} \quad R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

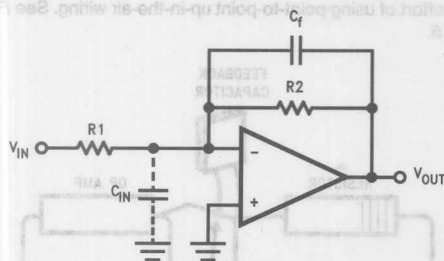


FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

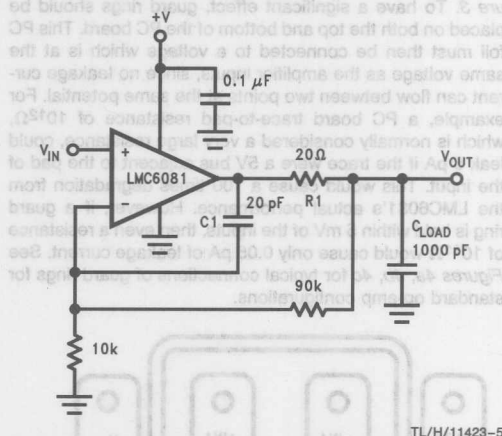


FIGURE 2a. LMC6081 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see electrical characteristics).

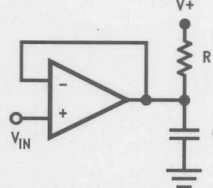


FIGURE 2b: Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6081, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6081's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6081's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

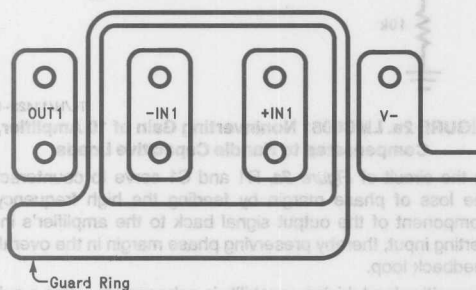


FIGURE 3. Example of Guard Ring in P.C. Board Layout

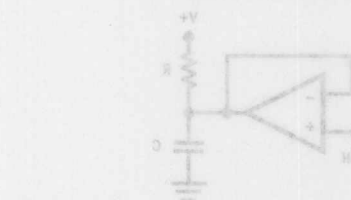


FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

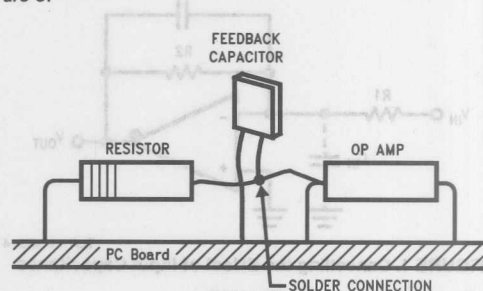


FIGURE 5. Air Wiring

Latchup

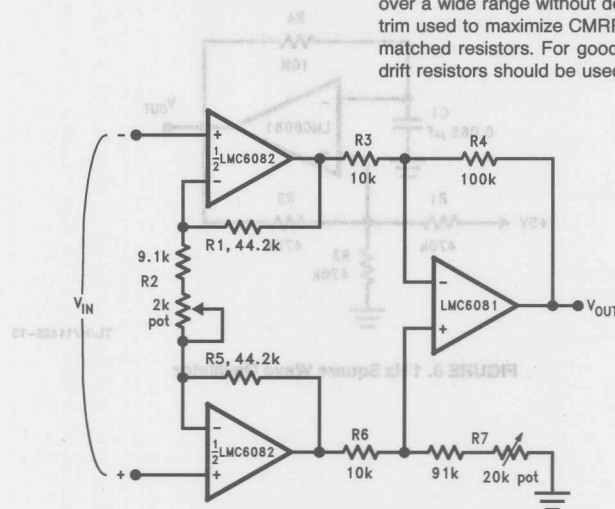
CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6061 and LMC6081 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6081 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($> 10^{14} \Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than $2.5 \mu V/^{\circ}C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.



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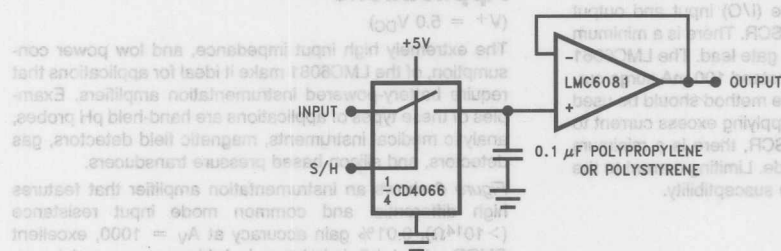
If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

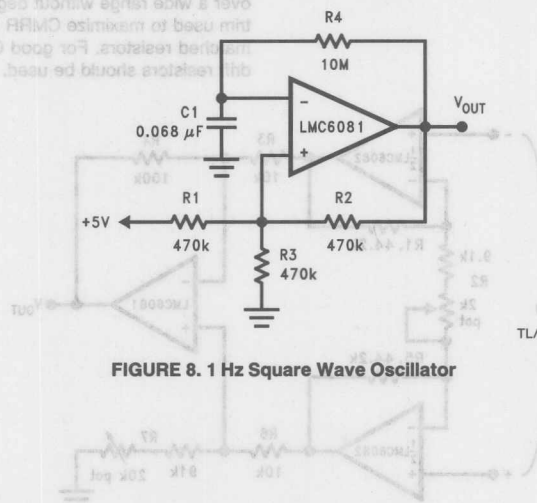
FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications ($V^+ = 5.0 \text{ V}_{\text{DC}}$) (Continued)



TL/H/11423-12

FIGURE 7. Low-Leakage Sample and Hold



TL/H/11423-13

FIGURE 8. 1 Hz Square Wave Oscillator

LMC6082 Precision CMOS Dual Operational Amplifier

General Description

The LMC6082 is a precision dual low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6082 ideally suited for precision circuit applications.

Other applications using the LMC6082 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6062 precision dual micropower operational amplifier.

Features (Typical unless otherwise stated)

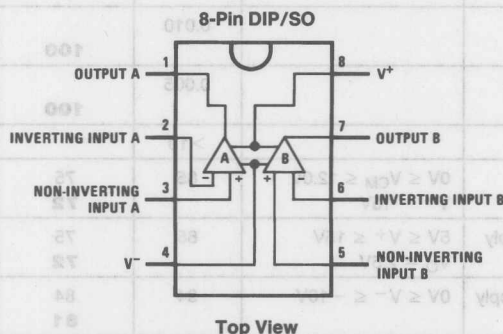
- Low offset voltage 150 μ V
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V_{-}
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

PATENT PENDING

Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------------|-------------------|-------------------------|-------------|-----------------------|
| | Military | Industrial | | |
| | -55°C to +125°C | -40°C to +85°C | | |
| 8-Pin Molded DIP | LMC6082AMN | LMC6082AIN LMC6082IN | N08E | Rail |
| 8-Pin Small Outline | | LMC6082AIM LMC6082IM | M08A | Rail Tape and Reel |

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage \pm Supply Voltage
Voltage at Input/Output Pin $(V^+) + 0.3V$,
 $(V^-) - 0.3V$

Supply Voltage $(V^+ - V^-)$ 16V

Output Short Circuit to V^+ (Note 11)

Output Short Circuit to V^- (Note 2)

Lead Temperature (Soldering, 10 Sec.) 260°C

Storage Temp. Range -65°C to $+150^\circ\text{C}$

Junction Temperature 150°C

ESD Tolerance (Note 4) 2 kV

Current at Input Pin ± 10 mA

Current at Output Pin ± 30 mA

Current at Power Supply Pin 40 mA

Power Dissipation (Note 3)

Operating Ratings (Note 1)

Temperature Range

LMC6082AM $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

LMC6082AI, LMC6082I $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$

Supply Voltage $4.5V \leq V^+ \leq 15.5V$

Thermal Resistance (θ_{JA}) (Note 12)

8-Pin Molded DIP 115°C/W

8-Pin SO 193°C/W

Power Dissipation (Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6082AM Limit (Note 6) | LMC6082AI Limit (Note 6) | LMC6082I Limit (Note 6) | Units |
|------------|--|---|-----------------|--|--|--|------------------------|
| V_{OS} | Input Offset Voltage | | 150 | 350 1000 | 350 800 | 800 1300 | μV Max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | $\mu V/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max |
| I_{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max |
| R_{IN} | Input Resistance | | >10 | | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 12.0V$ $V^+ = 15V$ | 85 | 75 72 | 75 72 | 66 63 | dB Min |
| +PSRR | Positive Power Supply Rejection Ratio | $5V \leq V^+ \leq 15V$ $V_O = 2.5V$ | 85 | 75 72 | 75 72 | 66 63 | dB Min |
| -PSRR | Negative Power Supply Rejection Ratio | $0V \leq V^- \leq -10V$ | 94 | 84 81 | 84 81 | 74 71 | dB Min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5V$ and $15V$ for CMRR ≥ 60 dB | -0.4 | -0.1 0 | -0.1 0 | -0.1 0 | V Max |
| | | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.6$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.5$ | V Min |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ (Note 7) | Sourcing | 1400 400 | 400 300 | 300 200 | V/mV Min |
| | | | Sinking | 350 70 | 180 100 | 90 60 | V/mV Min |
| | | $R_L = 600\Omega$ (Note 7) | Sourcing | 1200 150 | 400 150 | 200 80 | V/mV Min |
| | | | Sinking | 150 35 | 100 50 | 70 35 | V/mV Min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6082AM Limit (Note 6) | LMC6082AI Limit (Note 6) | LMC6082I Limit (Note 6) | Units |
|--------|---|---|-----------------|--------------------------------|--------------------------------|-------------------------------|-----------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.80 4.70 | 4.80 4.73 | 4.75 4.67 | V Min |
| | | | 0.10 | 0.13 0.19 | 0.13 0.17 | 0.20 0.24 | V Max |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V | 4.61 | 4.50 4.24 | 4.50 4.31 | 4.40 4.21 | V Min |
| | | | 0.30 | 0.40 0.63 | 0.40 0.50 | 0.50 0.63 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 14.50 14.30 | 14.50 14.34 | 14.37 14.25 | V Min |
| | | | 0.26 | 0.35 0.48 | 0.35 0.45 | 0.44 0.56 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V | 13.90 | 13.35 12.80 | 13.35 12.86 | 12.92 12.44 | V Min |
| | | | 0.79 | 1.16 1.42 | 1.16 1.32 | 1.33 1.58 | V Max |
| | I_O Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | Sinking, $V_O = 5\text{V}$ | 21 | 16 11 | 16 13 | 13 10 | mA Min |
| I_O | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 30 | 28 18 | 28 22 | 23 18 | mA Min |
| | | Sinking, $V_O = 13\text{V}$ (Note 11) | 34 | 28 19 | 28 22 | 23 18 | mA Min |
| I_S | Supply Current | Both Amplifiers $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | 0.9 | 1.5 1.8 | 1.5 1.8 | 1.5 1.8 | mA Max |
| | | Both Amplifiers $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | 1.1 | 1.7 2 | 1.7 2 | 1.7 2 | mA Max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6082AM Limit (Note 6) | LMC6082AI Limit (Note 6) | LMC6082I Limit (Note 6) | Units |
|----------|------------------------------|---|-----------------|--------------------------------|--------------------------------|-------------------------------|-------------------------|
| SR | Slew Rate | (Note 8) | 1.5 | 0.8 0.5 | 0.8 0.6 | 0.8 0.6 | V/ μs Min |
| GBW | Gain-Bandwidth Product | | 1.3 | | | | MHz |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| | Amp-to-Amp Isolation | (Note 9) | 140 | | | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ | 22 | | | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{PP}$ $\pm 5\text{V}$ Supply | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(\text{Max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{Max})} - T_A) / \theta_{JA}$.

Note 4: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{PP}$.

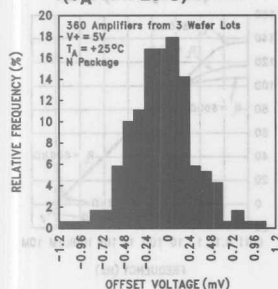
Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

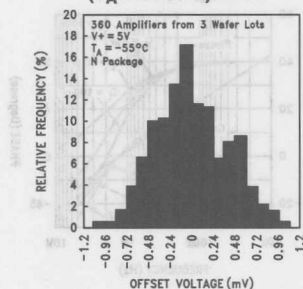
Note 12: All numbers apply for packages soldered directly into a PC board.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

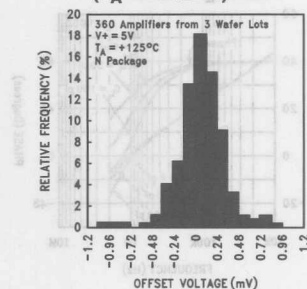
**Distribution of LMC6082
Input Offset Voltage
($T_A = +25^\circ C$)**



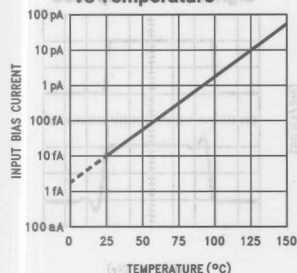
**Distribution of LMC6082
Input Offset Voltage
($T_A = -55^\circ C$)**



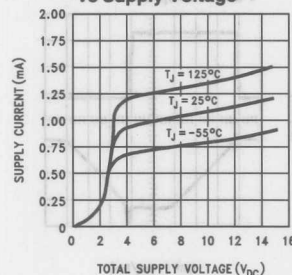
**Distribution of LMC6082
Input Offset Voltage
($T_A = +125^\circ C$)**



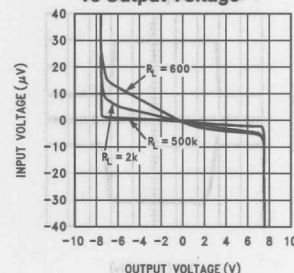
**Input Bias Current
vs Temperature**



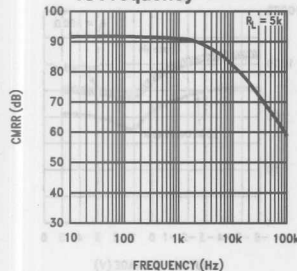
**Supply Current
vs Supply Voltage**



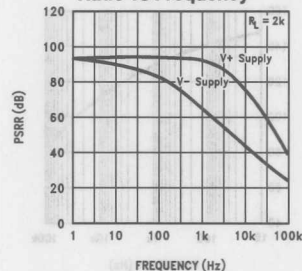
**Input Voltage
vs Output Voltage**



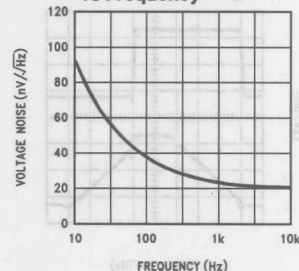
**Common Mode
Rejection Ratio
vs Frequency**



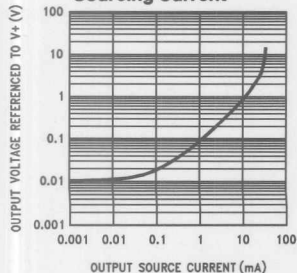
**Power Supply Rejection
Ratio vs Frequency**



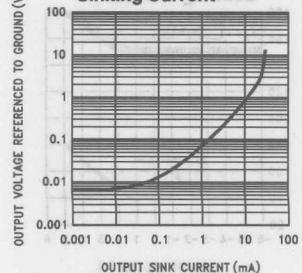
**Input Voltage Noise
vs Frequency**



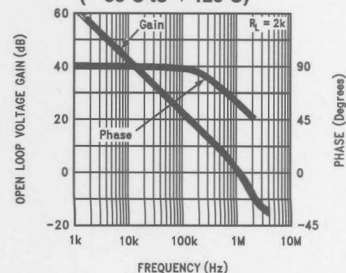
**Output Characteristics
Sourcing Current**



**Output Characteristics
Sinking Current**

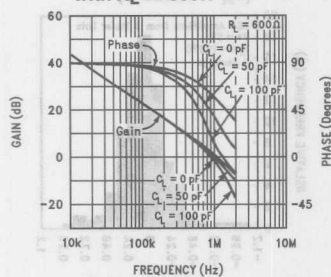


**Gain and Phase Response
vs Temperature
($-55^\circ C$ to $+125^\circ C$)**

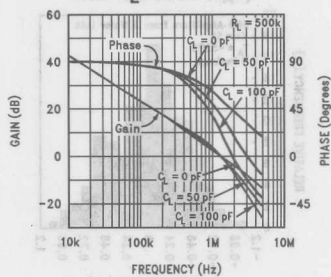


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

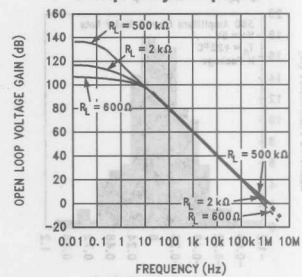
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



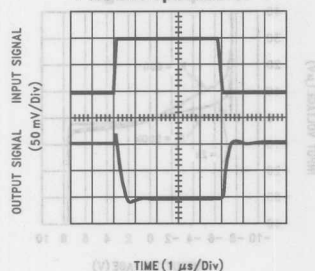
Gain and Phase Response vs Capacitive Load with $R_L = 500k\Omega$



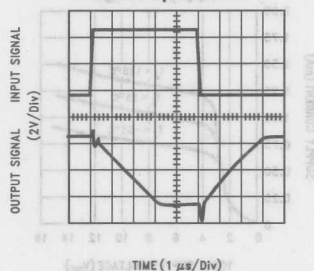
Open Loop Frequency Response



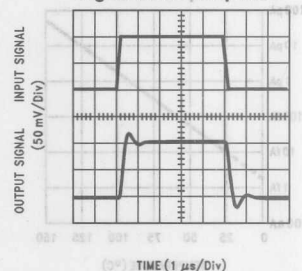
Inverting Small Signal Pulse Response



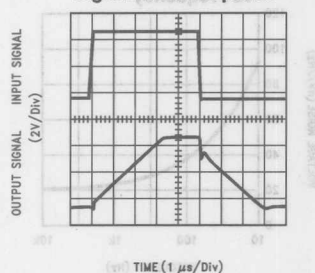
Inverting Large Signal Pulse Response



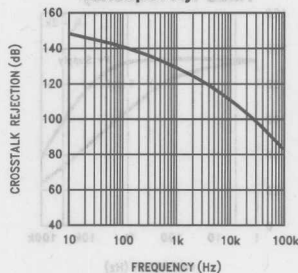
Non-Inverting Small Signal Pulse Response



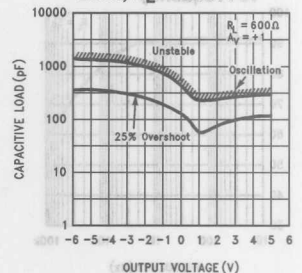
Non-Inverting Large Signal Pulse Response



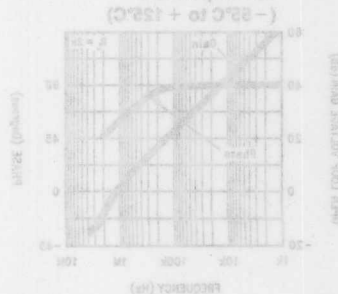
Crosstalk Rejection vs Frequency



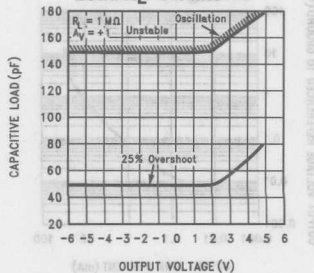
Stability vs Capacitive Load, $R_L = 600\Omega$



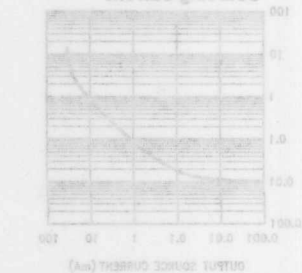
Gain and Phase Response vs Temperature



Stability vs Capacitive Load $R_L = 1M\Omega$



Output Sourcing Current



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6082 incorporates a novel op-amp design topology that enables it to maintain rail to rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6082 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6082.

Although the LMC6082 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6082 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

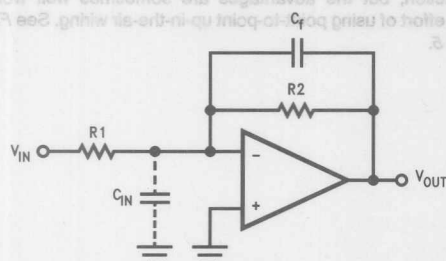


FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

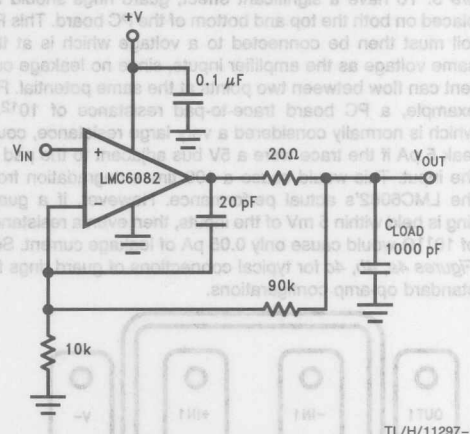


FIGURE 2a. LMC6082 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

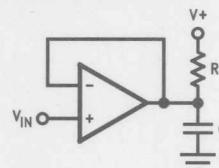


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6082, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

be appreciable. To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6082's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6082's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

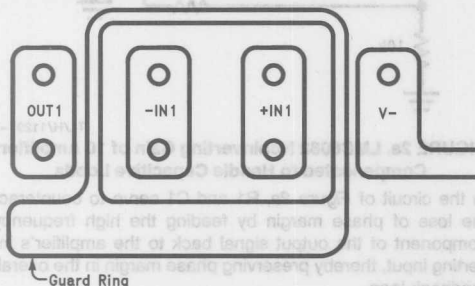


FIGURE 3. Example of Guard Ring in P.C. Board Layout

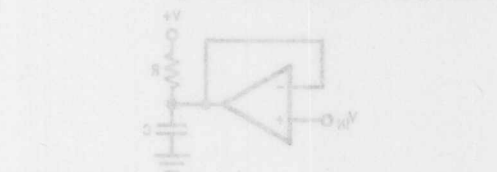
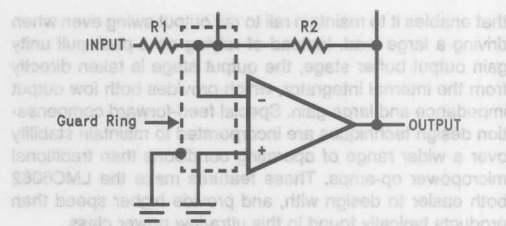
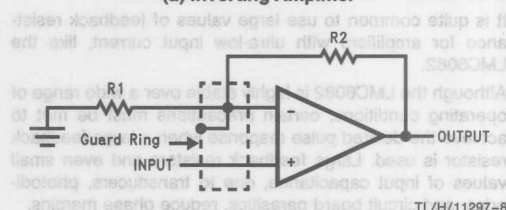


FIGURE 5a. Compensating for Large Capacitive Loads with a Pull-Up Resistor

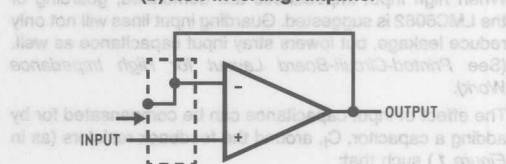
PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6082, typically less than 10 pA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakage are quite simple. First, the user must not ignore the surface



(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower

FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

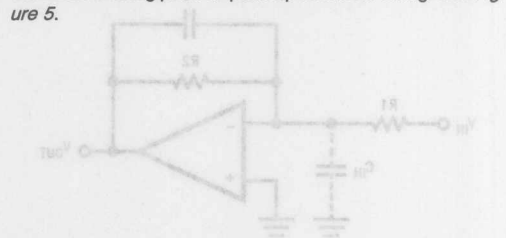
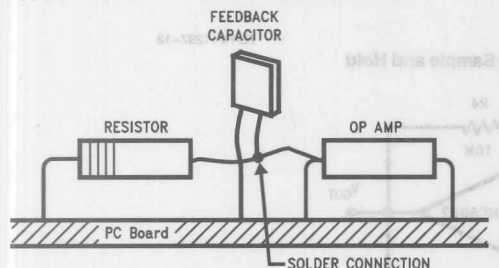


FIGURE 5. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE All full-output operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in the integrator stage. The frequency action of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

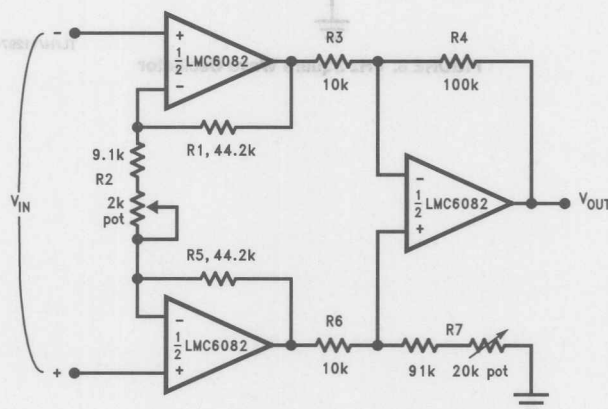
Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6062 and LMC6082 are designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_V \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6082 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_V = 1000$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than $2.5 \mu V/^{\circ}C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

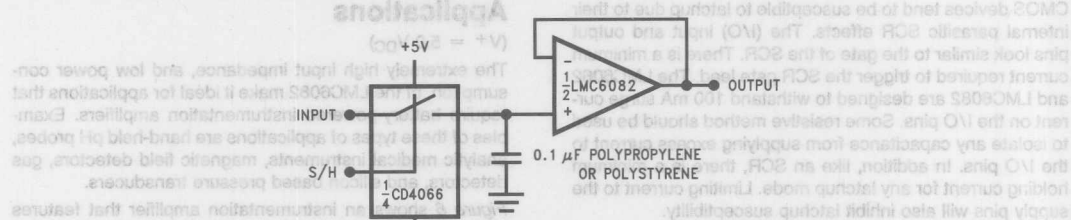


FIGURE 7. Low-Leakage Sample and Hold

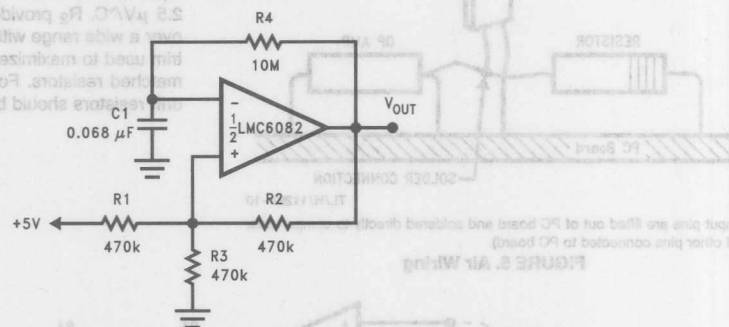


FIGURE 8. 1 Hz Square Wave Oscillator

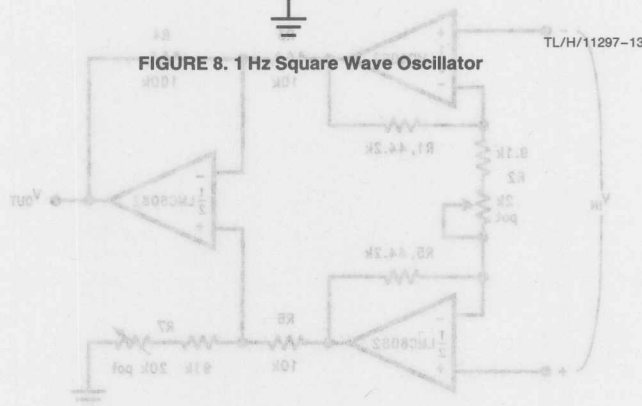


FIGURE 9. Instrumentation Amplifier

LMC6084 Precision CMOS Quad Operational Amplifier

General Description

The LMC6084 is a precision quad low offset voltage operational amplifier, capable of single supply operation. Performance characteristics include ultra low input bias current, high voltage gain, rail-to-rail output swing, and an input common mode voltage range that includes ground. These features, plus its low offset voltage, make the LMC6084 ideally suited for precision circuit applications.

Other applications using the LMC6084 include precision full-wave rectifiers, integrators, references, and sample-and-hold circuits.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

For designs with more critical power demands, see the LMC6064 precision quad micropower operational amplifier.

For a single or dual operational amplifier with similar features, see the LMC6081 or LMC6082 respectively.

Features (Typical unless otherwise stated)

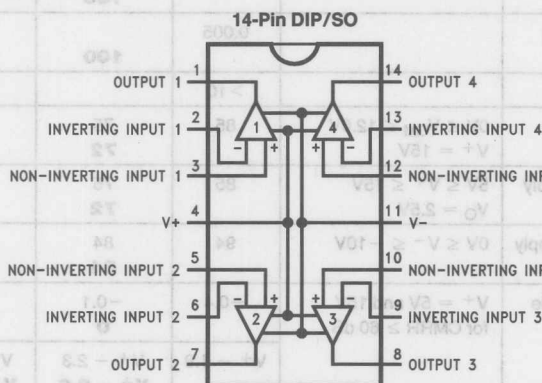
- Low offset voltage $150 \mu\text{V}$
- Operates from 4.5V to 15V single supply
- Ultra low input bias current 10 fA
- Output swing to within 20 mV of supply rail, 100k load
- Input common-mode range includes V^-
- High voltage gain 130 dB
- Improved latchup immunity

Applications

- Instrumentation amplifier
- Photodiode and infrared detector preamplifier
- Transducer amplifiers
- Medical instrumentation
- D/A converter
- Charge amplifier for piezoelectric transducers

PATENT PENDING

Connection Diagram



Top View

TL/H/11467-1

Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|----------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 14-Pin Molded DIP | LMC6084AMN | LMC6084AIN LMC6084IN | N14A | Rail |
| 14-Pin Small Outline | | LMC6084AIM LMC6084IM | M14A | Rail Tape and Reel |

For MIL-STD-883C qualified products, please contact your local National Semiconductor Sales Office or Distributor for availability and specification information.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage \pm Supply Voltage
 Voltage at Input/Output Pin $(V^+) + 0.3V$,
 $(V^-) - 0.3V$

Supply Voltage $(V^+ - V^-)$ 16V

Output Short Circuit to V^+ (Note 11)

Output Short Circuit to V^- (Note 2)

Lead Temperature (Soldering, 10 Sec.) 260°C

Storage Temp. Range -65°C to $+150^\circ\text{C}$

Junction Temperature 150°C

ESD Tolerance (Note 4) 2 kV

Current at Input Pin ± 10 mA

Current at Output Pin ± 30 mA

Current at Power Supply Pin 40 mA

Power Dissipation (Note 3)

Operating Ratings (Note 1)

Temperature Range $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

LMC6084AM $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$

LMC6084AI, LMC6084I

Supply Voltage $4.5V \leq V^+ \leq 15.5V$

Thermal Resistance (θ_{JA}) (Note 12)

14-Pin Molded DIP 81°C/W

14-Pin SO 126°C/W

Power Dissipation (Note 10)

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6084AM Limit (Note 6) | LMC6084AI Limit (Note 6) | LMC6084I Limit (Note 6) | Units | |
|-------------------|--|--|----------------------|--|--|--|------------|-------------|
| V _{OS} | Input Offset Voltage | | 150 | 350 1000 | 350 800 | 800 1300 | μV Max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C | |
| I _B | Input Bias Current | | 0.010 | 100 | 4 | 4 | pA Max | |
| I _{OS} | Input Offset Current | | 0.005 | 100 | 2 | 2 | pA Max | |
| R _{IN} | Input Resistance | | > 10 | | | | Tera Ω | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V | 85 | 75 72 | 75 72 | 66 63 | dB Min | |
| + PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V V _O = 2.5V | 85 | 75 72 | 75 72 | 66 63 | dB Min | |
| − PSRR | Negative Power Supply Rejection Ratio | 0V ≤ V [−] ≤ −10V | 94 | 84 81 | 84 81 | 74 71 | dB Min | |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V for CMRR ≥ 60 dB | −0.4 | −0.1 0 | −0.1 0 | −0.1 0 | V Max | |
| | | | V ⁺ − 1.9 | V ⁺ − 2.3 V ⁺ − 2.6 | V ⁺ − 2.3 V ⁺ − 2.5 | V ⁺ − 2.3 V ⁺ − 2.5 | V Min | |
| A _V | Large Signal Voltage Gain | R _L = 2 kΩ (Note 7) | Sourcing | 1400 | 400 300 | 400 300 | 300 200 | V/mV Min |
| | | | Sinking | 350 | 180 70 | 180 100 | 90 60 | V/mV Min |
| | | R _L = 600Ω (Note 7) | Sourcing | 1200 | 400 150 | 400 150 | 200 80 | V/mV Min |
| | | | Sinking | 150 | 100 35 | 100 50 | 70 35 | V/mV Min |

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6084AM Limit (Note 6) | LMC6084AI Limit (Note 6) | LMC6084I Limit (Note 6) | Units |
|--------|--------------------------------------|--|-----------------|--------------------------------|--------------------------------|-------------------------------|-----------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to 2.5V | 4.87 | 4.80 4.70 | 4.80 4.73 | 4.75 4.67 | V Min |
| | | | 0.10 | 0.13 0.19 | 0.13 0.17 | 0.20 0.24 | V Max |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to 2.5V | 4.61 | 4.50 4.24 | 4.50 4.31 | 4.40 4.21 | V Min |
| | | | 0.30 | 0.40 0.63 | 0.40 0.50 | 0.50 0.63 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to 7.5V | 14.63 | 14.50 14.30 | 14.50 14.34 | 14.37 14.25 | V Min |
| | | | 0.26 | 0.35 0.48 | 0.35 0.45 | 0.44 0.56 | V Max |
| | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to 7.5V | 13.90 | 13.35 12.80 | 13.35 12.86 | 12.92 12.44 | V Min |
| | | | 0.79 | 1.16 1.42 | 1.16 1.32 | 1.33 1.58 | V Max |
| | | Sourcing, $V_O = 0\text{V}$ | 22 | 16 8 | 16 10 | 13 8 | mA Min |
| | | | 21 | 16 11 | 16 13 | 13 10 | mA Min |
| I_O | Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 30 | 28 18 | 28 22 | 23 18 | mA Min |
| | | Sinking, $V_O = 13\text{V}$ (Note 11) | 34 | 28 19 | 28 22 | 23 18 | mA Min |
| | | All Four Amplifiers $V^+ = +5\text{V}$, $V_O = 1.5\text{V}$ | 1.8 | 3.0 3.6 | 3.0 3.6 | 3.0 3.6 | mA Max |
| | | All Four Amplifiers $V^+ = +15\text{V}$, $V_O = 7.5\text{V}$ | 2.2 | 3.4 4.0 | 3.4 4.0 | 3.4 4.0 | mA Max |

$V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6084AM Limit (Note 6) | LMC6084AI Limit (Note 6) | LMC6084I Limit (Note 6) | Units |
|----------|------------------------------|--|-----------------|--------------------------------|--------------------------------|-------------------------------|-------------------|
| SR | Slew Rate | (Note 8) | 1.5 | 0.8 0.5 | 0.8 0.6 | 0.8 0.6 | V/ μ s Min |
| GBW | Gain-Bandwidth Product | | 1.3 | | | | MHz |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| | Amp-to-Amp Isolation | (Note 9) | 140 | | | | dB |
| e_n | Input-Referred Voltage Noise | F = 1 kHz | 22 | | | | nV/ \sqrt{Hz} |
| i_n | Input-Referred Current Noise | F = 1 kHz | 0.0002 | | | | pA/ \sqrt{Hz} |
| T.H.D. | Total Harmonic Distortion | F = 10 kHz, $A_V = -10$ $R_L = 2 k\Omega$, $V_O = 8 V_{PP}$ $\pm 5V$ Supply | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A) / \theta_{JA}$.

Note 4: Human body model, 1.5 k Ω in series with 100 pF.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 8: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred $V^+ = 15V$ and $R_L = 100 k\Omega$ connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12 V_{PP}$.

Note 10: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

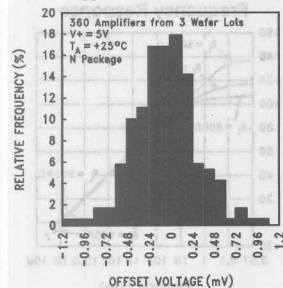
Note 11: Do not connect output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 12: All numbers apply for packages soldered directly into a PC board.

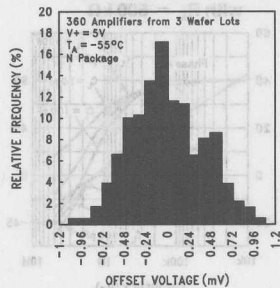
| | | | | | | | |
|-----|-----|-----|-----|-----|--|----------------|--|
| Am | 3.0 | 3.0 | 3.0 | 1.8 | All Four Amplifiers $V^+ = +5V$, $V_O = 1.5V$ | Supply Current | |
| Max | 3.0 | 3.0 | 3.0 | | | | |
| Am | 4.0 | 4.0 | 4.0 | 2.2 | All Four Amplifiers $V^+ = +15V$, $V_O = 7.5V$ | | |
| Max | 4.0 | 4.0 | 4.0 | | | | |

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified

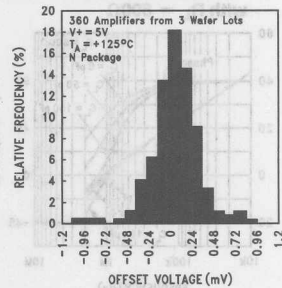
**Distribution of LMC6084
Input Offset Voltage
($T_A = +25^\circ C$)**



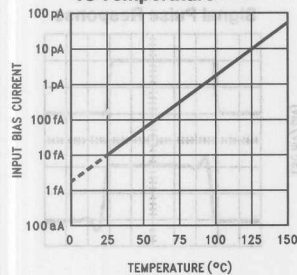
**Distribution of LMC6084
Input Offset Voltage
($T_A = -55^\circ C$)**



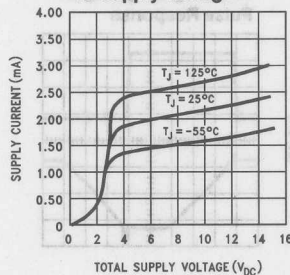
**Distribution of LMC6084
Input Offset Voltage
($T_A = +125^\circ C$)**



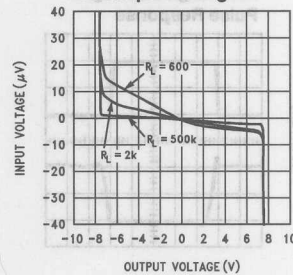
**Input Bias Current
vs Temperature**



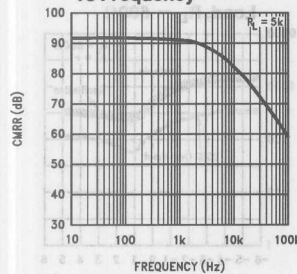
**Supply Current
vs Supply Voltage**



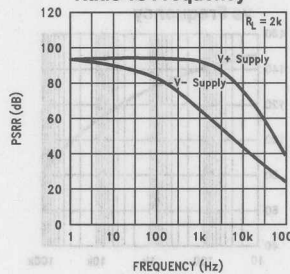
**Input Voltage
vs Output Voltage**



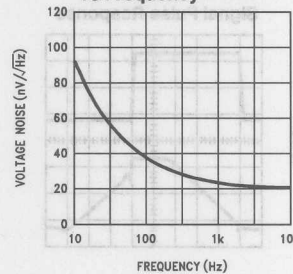
**Common Mode
Rejection Ratio
vs Frequency**



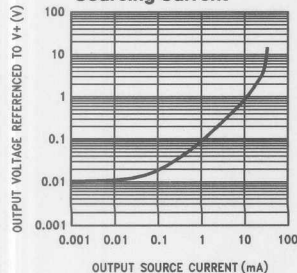
**Power Supply Rejection
Ratio vs Frequency**



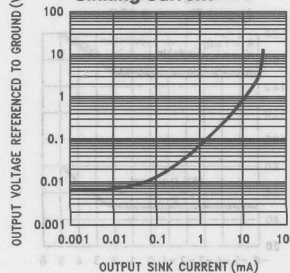
**Input Voltage Noise
vs Frequency**



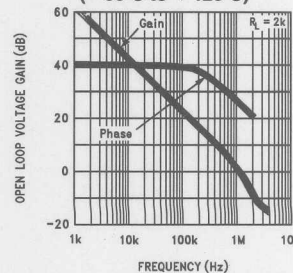
**Output Characteristics
Sourcing Current**



**Output Characteristics
Sinking Current**



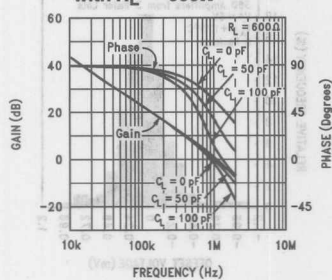
**Gain and Phase Response
vs Temperature
($-55^\circ C$ to $+125^\circ C$)**



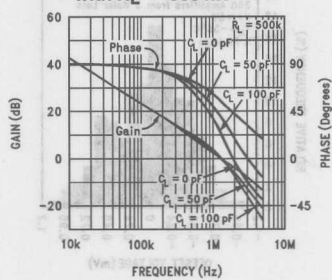
Typical Performance Characteristics

$V_S = \pm 7.5V$, $T_A = 25^\circ C$, Unless otherwise specified (Continued)

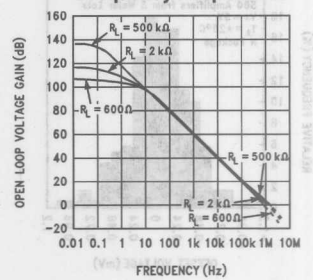
Gain and Phase Response vs Capacitive Load with $R_L = 600\Omega$



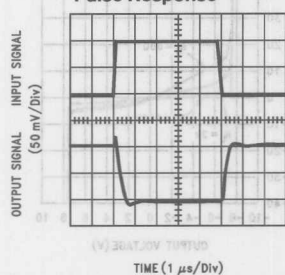
Gain and Phase Response vs Capacitive Load with $R_L = 500 k\Omega$



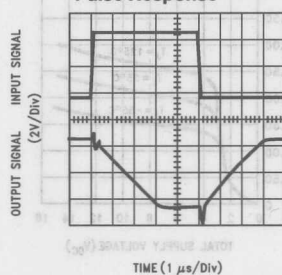
Open Loop Frequency Response



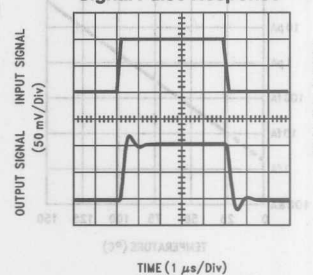
Inverting Small Signal Pulse Response



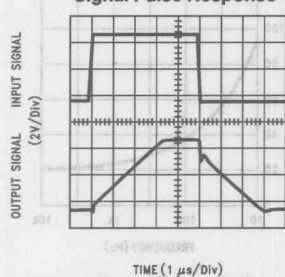
Inverting Large Signal Pulse Response



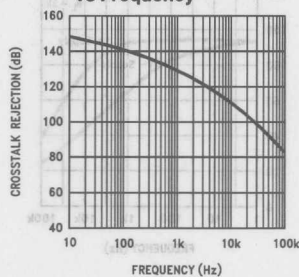
Non-Inverting Small Signal Pulse Response



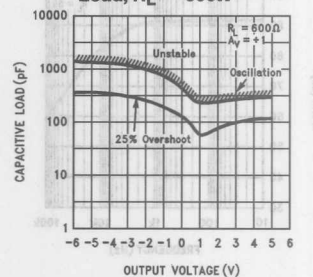
Non-Inverting Large Signal Pulse Response



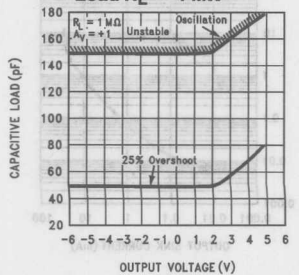
Crosstalk Rejection vs Frequency



Stability vs Capacitive Load, $R_L = 600\Omega$



Stability vs Capacitive Load $R_L = 1 M\Omega$



Applications Hints

AMPLIFIER TOPOLOGY

The LMC6084 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6084 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6084.

Although the LMC6084 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors and even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6084 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in *Figure 1*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f} \quad \text{or} \quad R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

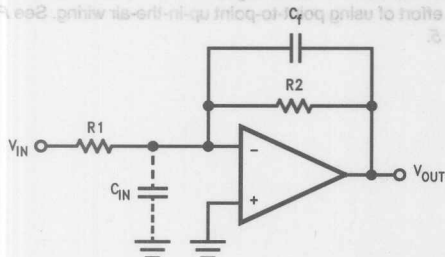


FIGURE 1. Cancelling the Effect of Input Capacitance

CAPACITIVE LOAD TOLERANCE

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see typical curves).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 2a*.

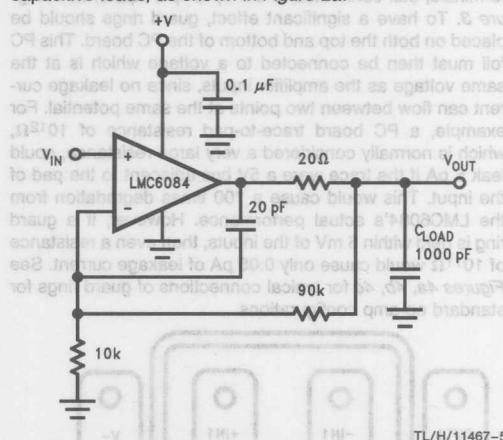


FIGURE 2a. LMC6084 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of *Figure 2a*, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 2b*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

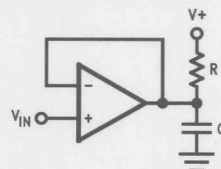


FIGURE 2b. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6084, typically less than 10 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface

be appreciable. To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6084's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 100 times degradation from the LMC6084's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

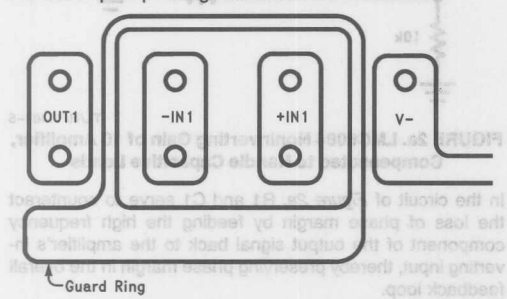
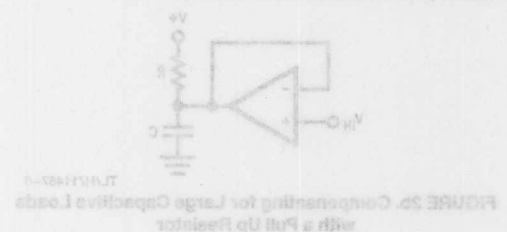
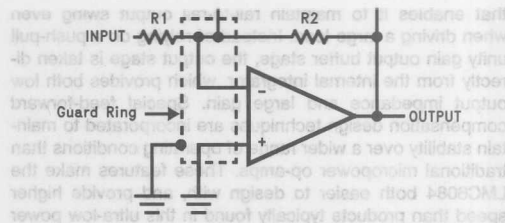


FIGURE 3. Example of Guard Ring in P.C. Board Layout

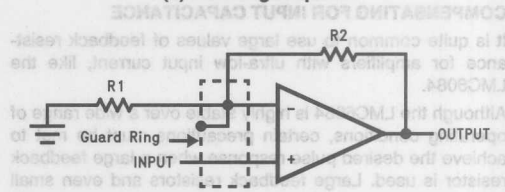
conducting 800 pA or more will significantly improve capacitive load response. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



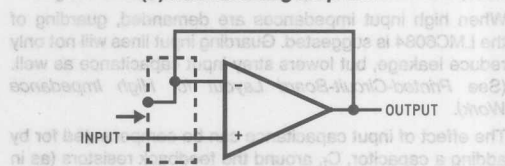
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6084, typically less than 10 pA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakage are quite simple. First, the user must not ignore the surface



(a) Inverting Amplifier



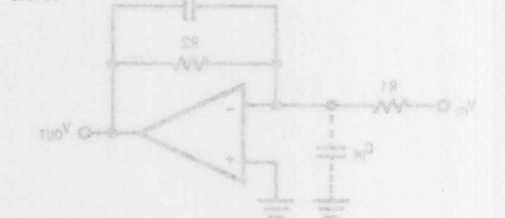
(b) Non-Inverting Amplifier



(c) Follower

FIGURE 4. Typical Connections of Guard Rings

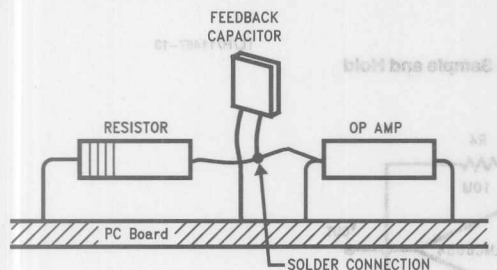
The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



capacitive load tolerance. At full-scale output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in the integrator stage. The frequency location of the dominant pole is affected by the relative load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate relative load in parallel with the capacitive load (see typical curves).

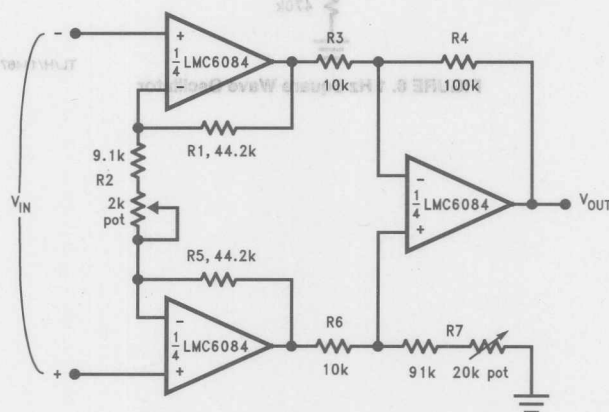
Latchup

CMOS devices tend to be susceptible to latchup due to their internal parasitic SCR effects. The (I/O) input and output pins look similar to the gate of the SCR. There is a minimum current required to trigger the SCR gate lead. The LMC6084 is designed to withstand 100 mA surge current on the I/O pins. Some resistive method should be used to isolate any capacitance from supplying excess current to the I/O pins. In addition, like an SCR, there is a minimum holding current for any latchup mode. Limiting current to the supply pins will also inhibit latchup susceptibility.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring



If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_v \approx 100$ for circuit shown ($R_2 = 9.822k$).

FIGURE 6. Instrumentation Amplifier

Typical Single-Supply Applications

($V^+ = 5.0 V_{DC}$)

The extremely high input impedance, and low power consumption, of the LMC6084 make it ideal for applications that require battery-powered instrumentation amplifiers. Examples of these types of applications are hand-held pH probes, analytic medical instruments, magnetic field detectors, gas detectors, and silicon based pressure transducers.

Figure 6 shows an instrumentation amplifier that features high differential and common mode input resistance ($>10^{14}\Omega$), 0.01% gain accuracy at $A_v = 1000$, excellent CMRR with 1 k Ω imbalance in bridge source resistance. Input current is less than 100 fA and offset drift is less than $2.5 \mu V/^\circ C$. R_2 provides a simple means of adjusting gain over a wide range without degrading CMRR. R_7 is an initial trim used to maximize CMRR without using super precision matched resistors. For good CMRR over temperature, low drift resistors should be used.

Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

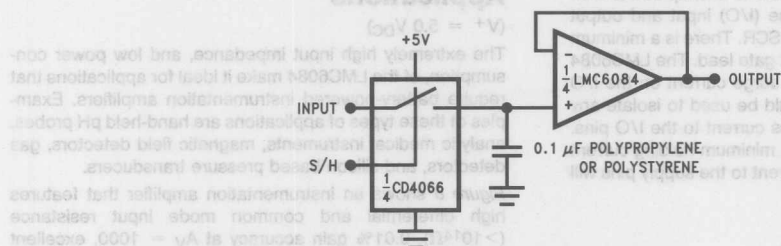


FIGURE 7. Low-Leakage Sample and Hold

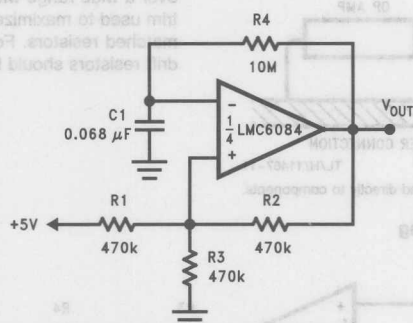


FIGURE 8. 1 Hz Square Wave Oscillator

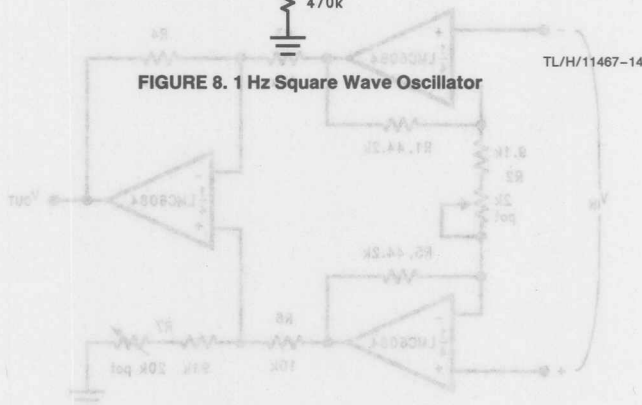


FIGURE 9. Instrumentation Amplifier

LMC6462 Dual/LMC6464 Quad Micropower, Rail-to-Rail Input and Output CMOS Operational Amplifier

General Description

The LMC6462/4 is a micropower version of the popular LMC6482/4, combining Rail-to-Rail Input and Output Range with very low power consumption.

The LMC6462/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier, guaranteed for loads down to 25 k Ω , assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high voltage gain makes it unique among rail-to-rail amplifiers. The LMC6462/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6462/4, with guaranteed specifications at 3V and 5V, is especially well-suited for low voltage applications. A quiescent power consumption of 60 μ W per amplifier (at $V_S = 3V$) can extend the useful life of battery operated systems. The amplifier's 150 fA input current, low offset voltage of 0.25 mV, and 85 dB CMRR maintain accuracy in battery-powered systems.

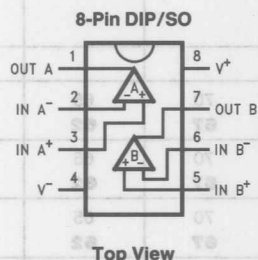
Features (Typical unless otherwise noted)

- Ultra Low Supply Current 20 μ A/Amplifier
- Guaranteed Characteristics at 3V and 5V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing (within 10 mV of rail, $V_S = 5V$ and $R_L = 25 k\Omega$)
- Low Input Current 150 fA
- Low Input Offset Voltage 0.25 mV

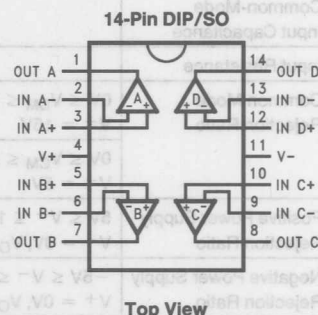
Applications

- Battery Operated Circuits
- Transducer Interface Circuits
- Portable Communication Devices
- Medical Applications
- Battery Monitoring

Connection Diagrams



TL/H/12051-1



TL/H/12051-2

Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|-------------------|-----------------------------|--|--------------|------------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 8-Pin Molded DIP | LMC6462AMN | LMC6462AIN, LMC6462BIN | N08E | Rails |
| 8-Pin SO-8 | | LMC6462AIM, LMC6462BIM LMC6462AIMX, LMC6462BIMX | M08A M08A | Rails Tape and Reel |
| 14-Pin Molded DIP | LMC6464AMN | LMC6464AIN, LMC6464BIN | N14A | Rails |
| 14-Pin SO-14 | | LMC6464AIM, LMC6464BIM LMC6464AIMX, LMC6464BIMX | M14A M14A | Rails Tape and Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|------------------------------------|------------------------------|
| ESD Tolerance (Note 2) | 2.0 kV |
| Differential Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin | $(V^+) + 0.3V, (V^-) - 0.3V$ |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Current at Input Pin (Note 12) | ± 5 mA |
| Current at Output Pin (Notes 3, 8) | ± 30 mA |
| Current at Power Supply Pin | 40 mA |
| Lead Temp. (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Boldface limits apply at the temperature extremes.

Operating Ratings (Note 1)

| | |
|--------------------------------------|--|
| Supply Voltage | $3.0V \leq V^+ \leq 15.5V$ |
| Junction Temperature Range | |
| LMC6462AM, LMC6464AM | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| LMC6462AI, LMC6464AI | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LMC6462BI, LMC6464BI | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 115°C/W |
| M Package, 8-Pin Surface Mount | 193°C/W |
| N Package, 14-Pin Molded DIP | 81°C/W |
| M Package, 14-Pin Surface Mount | 126°C/W |

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6462AI LMC6464AI Limit (Note 6) | LMC6462BI LMC6464BI Limit (Note 6) | LMC6462AM LMC6464AM Limit (Note 6) | Units |
|------------|--|--|-----------------|---|---|---|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.25 | 0.5 1.2 | 3.0 3.7 | 0.5 1.5 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.5 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Current | (Note 13) | 0.15 | 10 | 10 | 200 | pA max |
| I_{OS} | Input Offset Current | (Note 13) | 0.075 | 5 | 5 | 100 | pA max |
| C_{IN} | Common-Mode Input Capacitance | | 3 | | | | pF |
| R_{IN} | Input Resistance | | > 10 | | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 15.0V$, $V^+ = 15V$ | 85 | 70 67 | 65 62 | 70 65 | dB min |
| | | $0V \leq V_{CM} \leq 5.0V$, $V^+ = 5V$ | 85 | 70 67 | 65 62 | 70 65 | |
| + PSRR | Positive Power Supply Rejection Ratio | $5V \leq V^+ \leq 15V$, $V^- = 0V$, $V_O = 2.5V$ | 85 | 70 67 | 65 62 | 70 65 | dB min |
| - PSRR | Negative Power Supply Rejection Ratio | $-5V \leq V^- \leq -15V$, $V^+ = 0V$, $V_O = -2.5V$ | 85 | 70 67 | 65 62 | 70 65 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5V$ For CMRR ≥ 50 dB | -0.2 | -0.10 0.00 | -0.10 0.00 | -0.10 0.00 | V max |
| | | | 5.30 | 5.25 5.00 | 5.25 5.00 | 5.25 5.00 | V min |
| | | $V^+ = 15V$ For CMRR ≥ 50 dB | -0.2 | -0.15 0.00 | -0.15 0.00 | -0.15 0.00 | V max |
| | | | 15.30 | 15.25 15.00 | 15.25 15.00 | 15.25 15.00 | V min |

5V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}$.
Boldface limits apply at the temperature extremes. (Continued)

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6462AI LMC6464AI Limit (Note 6) | LMC6462BI LMC6464BI Limit (Note 6) | LMC6462AM LMC6464AM Limit (Note 6) | Units |
|----------|---------------------------------|---|-----------------|---|---|---|---------------|
| A_v | Large Signal Voltage Gain | $R_L = 100\text{ k}\Omega$ (Note 7) | Sourcing | 3000 | | | V/mV min |
| | | | Sinking | 400 | | | V/mV min |
| | | $R_L = 25\text{ k}\Omega$ (Note 7) | Sourcing | 2500 | | | V/mV min |
| | | | Sinking | 200 | | | V/mV min |
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | | 4.995 | 4.990 | 4.990 | V |
| | | | | 4.980 | 4.925 | 4.970 | min |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | | 0.005 | 0.010 | 0.010 | V |
| | | | | 0.020 | 0.075 | 0.030 | max |
| | | $V^+ = 5\text{V}$ $R_L = 25\text{ k}\Omega$ to $V^+/2$ | | 4.990 | 4.975 | 4.975 | V |
| | | | | 4.965 | 4.850 | 4.955 | min |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | | 0.010 | 0.020 | 0.020 | V |
| | | | | 0.035 | 0.150 | 0.045 | max |
| | | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | | 14.990 | 14.975 | 14.975 | V |
| | | | | 14.965 | 14.925 | 14.955 | min |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | | 19 | 19 | 19 | mA |
| | | | | 15 | 15 | 15 | min |
| | | Sinking, $V_O = 5\text{V}$ | | 27 | 22 | 22 | mA |
| | | | | 17 | 17 | 17 | min |
| | | Sourcing, $V_O = 0\text{V}$ | | 38 | 24 | 24 | mA |
| | | | | 17 | 17 | 17 | min |
| I_S | Supply Current | Dual, LMC6462 $V^+ = +5\text{V}$, $V_O = V^+/2$ | | 40 | 55 | 55 | μA |
| | | | | 70 | 70 | 75 | max |
| | | Quad, LMC6464 $V^+ = +5\text{V}$, $V_O = V^+/2$ | | 80 | 110 | 110 | μA |
| | | | | 140 | 140 | 150 | max |
| | | Dual, LMC6462 $V^+ = +15\text{V}$, $V_O = V^+/2$ | | 50 | 60 | 60 | μA |
| | | | | 70 | 70 | 75 | max |
| I_S | Supply Current | Quad, LMC6464 $V^+ = +15\text{V}$, $V_O = V^+/2$ | | 90 | 120 | 120 | μA |
| | | | | 140 | 140 | 150 | max |

Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6462AI LMC6464AI Limit (Note 6) | LMC6462BI LMC6464BI Limit (Note 6) | LMC6462AM LMC6464AM Limit (Note 6) | Units |
|----------|---------------------------------|--------------------------------------|-----------------|---|---|---|-----------------------|
| SR | Slew Rate | (Note 9) | 28 | 15 8 | 15 8 | 15 8 | V/ms min |
| GBW | Gain-Bandwidth Product | $V^+ = 15V$ | 50 | | | | kHz |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| G_m | Gain Margin | | 15 | | | | dB |
| | Amp-to-Amp Isolation | (Note 10) | 130 | | | | dB |
| e_n | Input-Referred Voltage Noise | $f = 1 \text{ kHz}$ $V_{CM} = 1V$ | 80 | | | | $nV/\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $f = 1 \text{ kHz}$ | 0.03 | | | | $pA/\sqrt{\text{Hz}}$ |

3V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6462AI LMC6464AI Limit (Note 6) | LMC6462BI LMC6464BI Limit (Note 6) | LMC6462AM LMC6464AM Limit (Note 6) | Units |
|------------|---------------------------------------|---------------------------------------|-----------------|---|---|---|------------------------|
| V_{OS} | Input Offset Voltage | | 0.9 | 2.0 2.7 | 3.0 3.7 | 2.0 3.0 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 2.0 | | | | $\mu V/^\circ\text{C}$ |
| I_B | Input Current | (Note 13) | 0.15 | 10 | 10 | 200 | pA |
| I_{OS} | Input Offset Current | (Note 13) | 0.075 | 5 | 5 | 100 | pA |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 3V$ | 74 | 60 | 60 | 60 | dB min |
| PSRR | Power Supply Rejection Ratio | $3V \leq V^+ \leq 15V$, $V^- = 0V$ | 80 | 60 | 60 | 60 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | For CMRR $\geq 50 \text{ dB}$ | -0.10 | 0.0 | 0.0 | 0.0 | V max |
| | | | 3.0 | 3.0 | 3.0 | 3.0 | V min |
| V_O | Output Swing | $R_L = 25 \text{ k}\Omega$ to $V^+/2$ | 2.95 | 2.9 | 2.9 | 2.9 | V min |
| | | | 0.15 | 0.1 | 0.1 | 0.1 | V max |
| I_S | Supply Current | Dual, LMC6462 $V_O = V^+/2$ | 40 | 55 70 | 55 70 | 55 70 | μA |
| | | Quad, LMC6464 $V_O = V^+/2$ | 80 | 110 140 | 110 140 | 110 140 | μA max |

3V AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$. **Boldface limits** apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6462AI LMC6464AI Limit (Note 6) | LMC6462BI LMC6464BI Limit (Note 6) | LMC6462AM LMC6464AM Limit (Note 6) | Units |
|--------|------------------------|------------|-----------------|---|---|---|-------|
| SR | Slew Rate | (Note 11) | 23 | | | | V/ms |
| GBW | Gain-Bandwidth Product | | 50 | | | | kHz |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF. All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $3.5V \leq V_O \leq 7.5V$.

Note 8: Do not short circuit output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

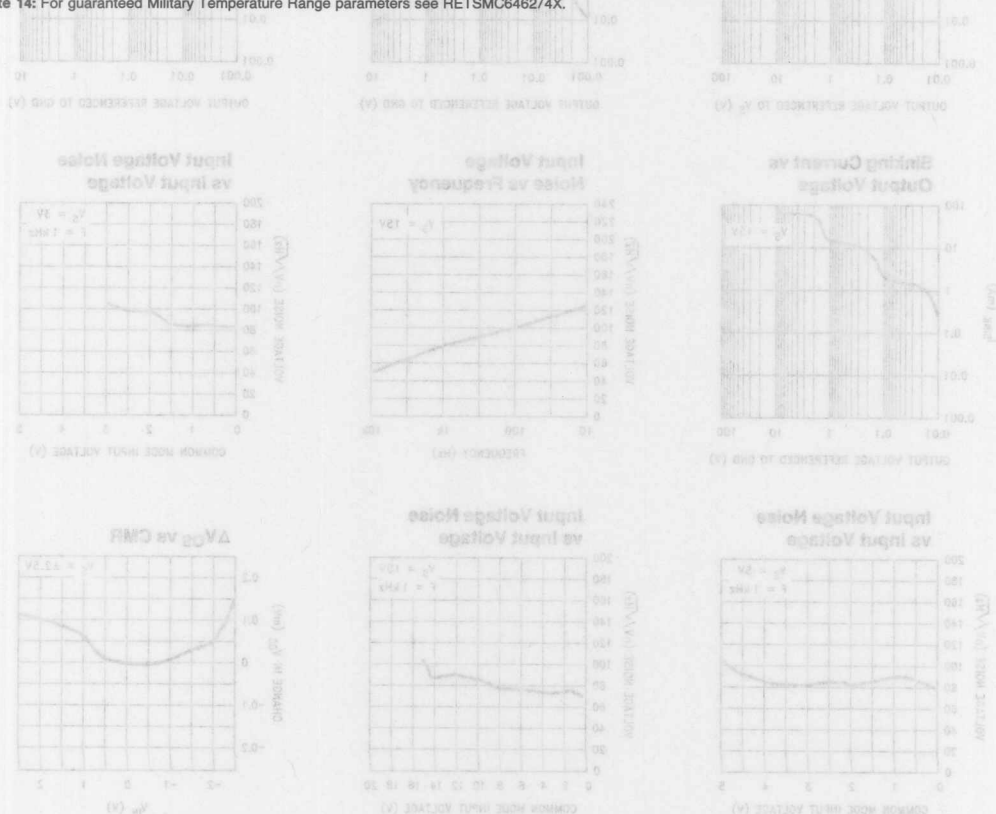
Note 10: Input referred, $V^+ = 15V$ and $R_L = 100$ k Ω connected to 7.5V. Each amp excited in turn with 1 kHz to produce $V_O = 12$ Vpp.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

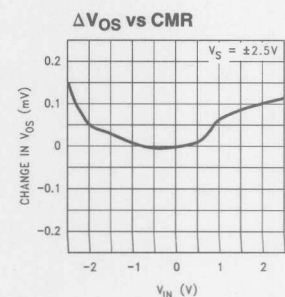
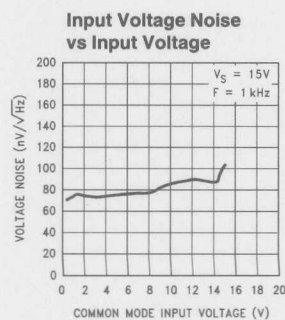
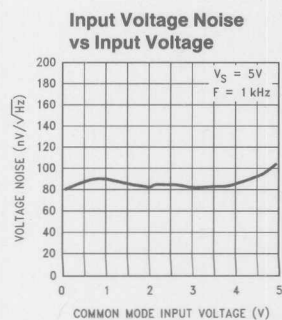
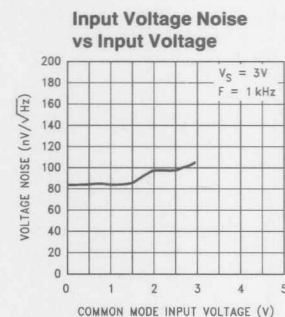
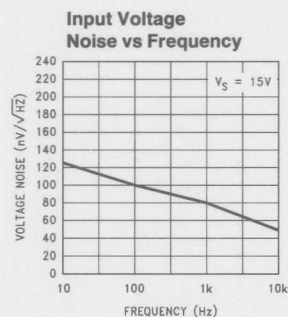
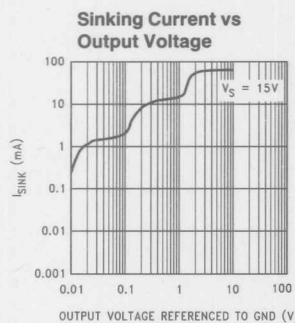
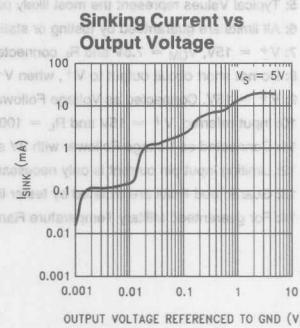
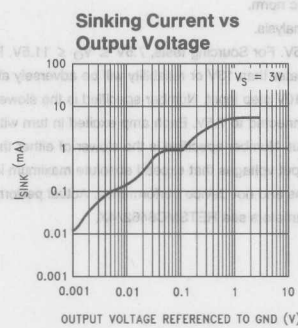
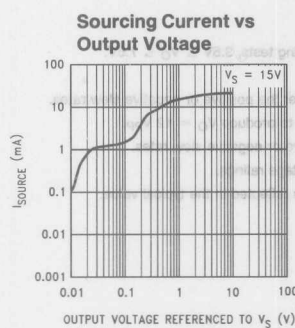
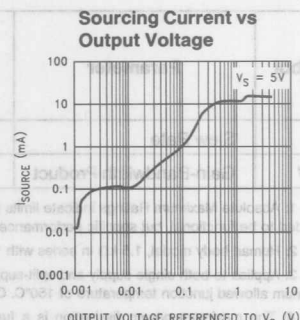
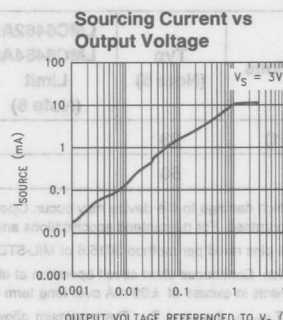
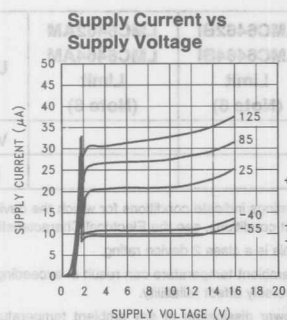
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6462/4X.



Typical Performance Characteristics

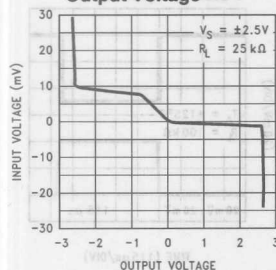
$V_S = +5V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified.



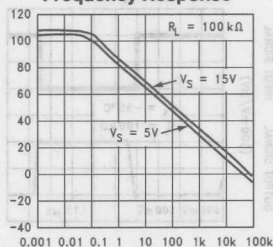
Typical Performance Characteristics (Continued)

$V_S = +5V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

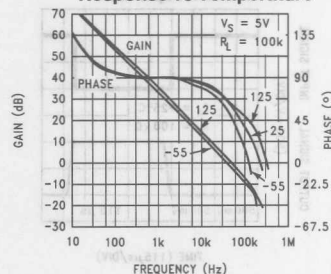
Input Voltage vs Output Voltage



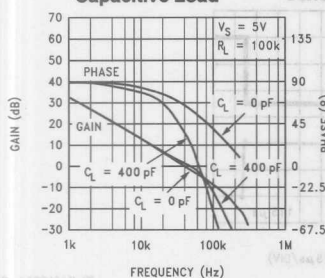
Open Loop Frequency Response



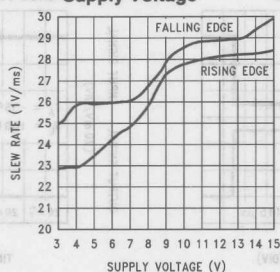
Open Loop Frequency Response vs Temperature



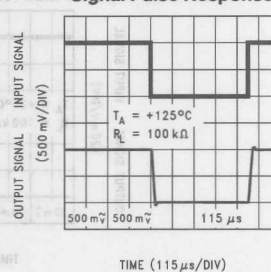
Gain and Phase vs Capacitive Load



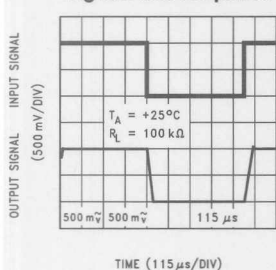
Slew Rate vs Supply Voltage



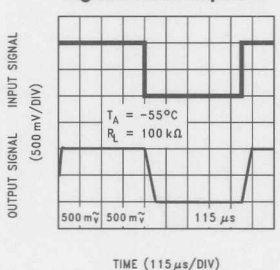
Non-Inverting Large Signal Pulse Response



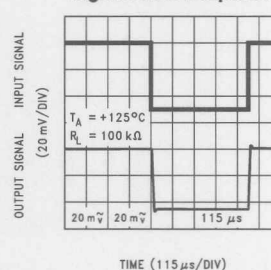
Non-Inverting Large Signal Pulse Response



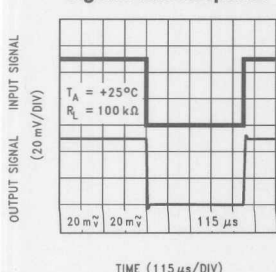
Non-Inverting Large Signal Pulse Response



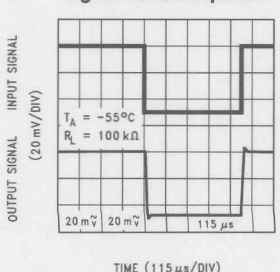
Non-Inverting Small Signal Pulse Response



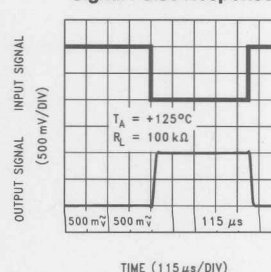
Non-Inverting Small Signal Pulse Response



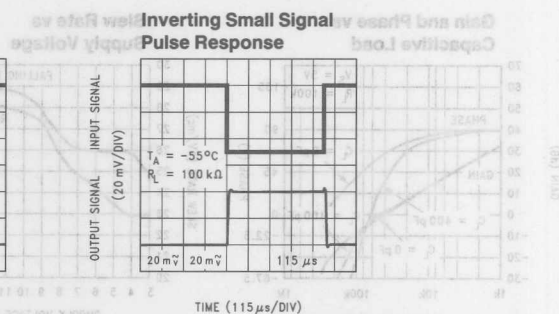
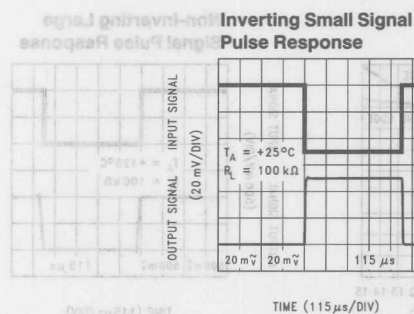
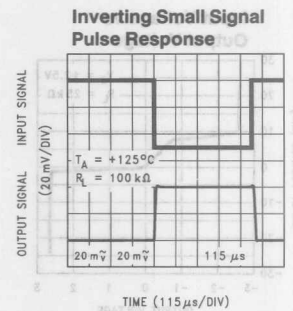
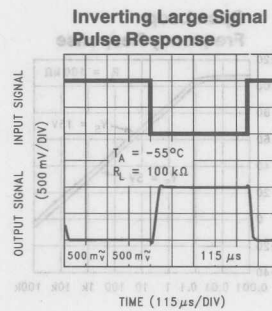
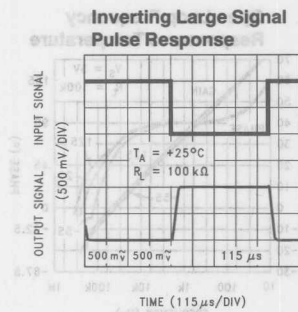
Non-Inverting Small Signal Pulse Response



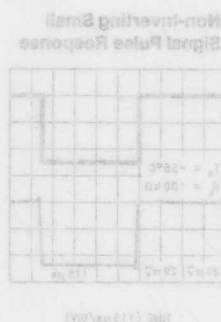
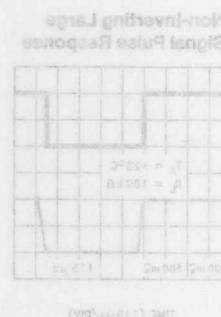
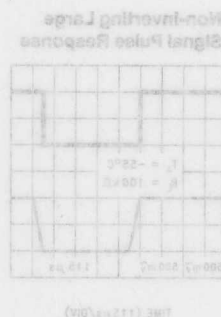
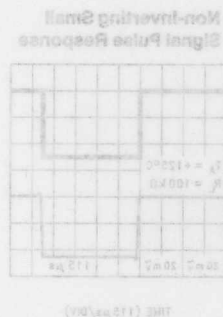
Inverting Large Signal Pulse Response



Typical Performance Characteristics (Continued)

 $V_S = +5V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

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Application Information

1.0 Input Common-Mode Voltage Range

The LMC6462/4 has a rail-to-rail input common-mode voltage range. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

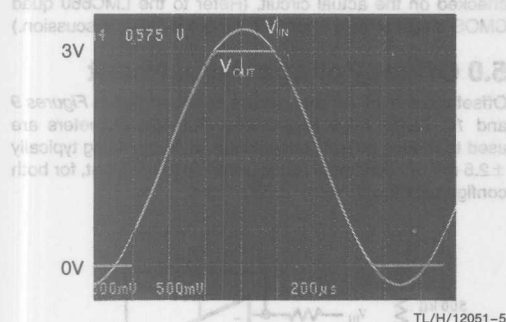


FIGURE 1. An Input Voltage Signal Exceeds the LMC6462/4 Power Supply Voltage with No Output Phase Inversion

The absolute maximum input voltage at $V^+ = 3V$ is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 2, can cause excessive current to flow in or out of the input pins, possibly affecting reliability. The input current can be externally limited to ± 5 mA, with an input resistor, as shown in Figure 3.

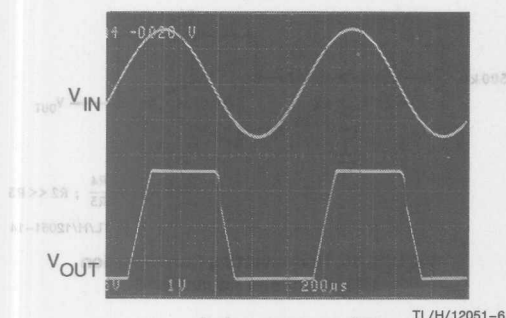


FIGURE 2. A $\pm 7.5V$ Input Signal Greatly Exceeds the 3V Supply in Figure 3 Causing No Phase Inversion Due to R_1

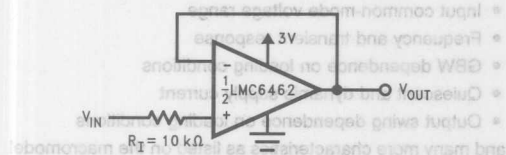


FIGURE 3. Input Current Protection for Voltages Exceeding the Supply Voltage

2.0 Rail-to-Rail Output

The approximated output resistance of the LMC6462/4 is 180Ω sourcing, and 130Ω sinking at $V_S = 3V$, and 110Ω sourcing and 83Ω sinking at $V_S = 5V$. The maximum output swing can be estimated as a function of load using the calculated output resistance.

3.0 Capacitive Load Tolerance

The LMC6462/4 can typically drive a 200 pF load with $V_S = 5V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration to capacitive load. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 4. If there is a resistive component of the load in parallel to the capacitive component, the isolation resistor and the resistive load create a voltage divider at the output. This introduces a DC error at the output.

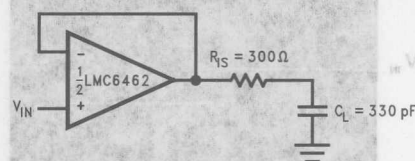


FIGURE 4. Resistive Isolation of a 300 pF Capacitive Load

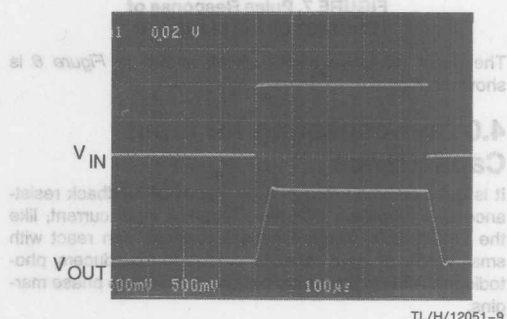


FIGURE 5. Pulse Response of the LMC6462/4 Circuit Shown in Figure 4

Figure 5 displays the pulse response of the LMC6462/4 circuit in Figure 4.

Another circuit, shown in Figure 6, is also used to indirectly drive capacitive loads. This circuit is an improvement to the circuit shown in Figure 4 because it provides DC accuracy as well as AC stability. R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R_1 and C_1 should be experimentally determined by the system designer for the desired pulse response. Increased capacitive drive is possible by increasing the value of the capacitor in the feedback loop.

Application Information (Continued)

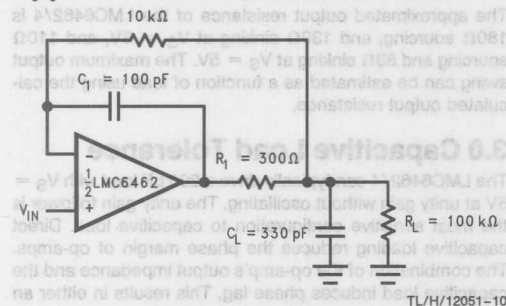


FIGURE 6. LMC6462 Non-Inverting Amplifier, Compensated to Handle a 300 pF Capacitive and 100 kΩ Resistive Load

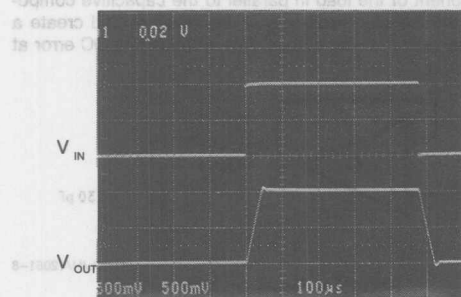


FIGURE 7. Pulse Response of LMC6462 Circuit in Figure 6

The pulse response of the circuit shown in Figure 6 is shown in Figure 7.

4.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6462/4. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

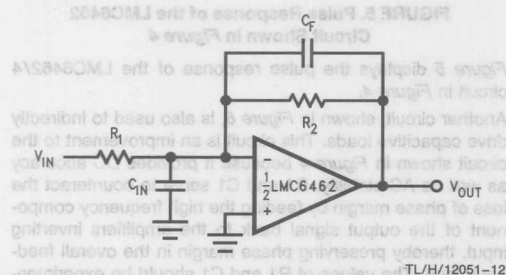


FIGURE 8. Canceling the Effect of Input Capacitance
The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 8), C_F , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F}$$

$$\text{or} \\ R_1 C_{IN} \leq R_2 C_F$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

5.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in Figures 9 and 10. Large value resistances and potentiometers are used to reduce power consumption while providing typically ± 2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5$ V.

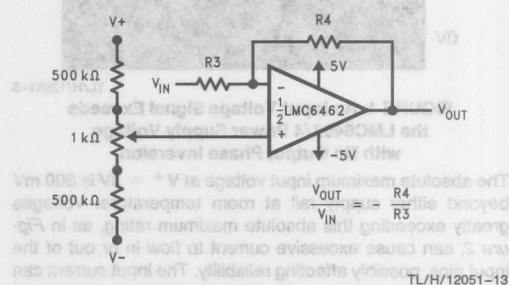


FIGURE 9. Inverting Configuration Offset Voltage Adjustment

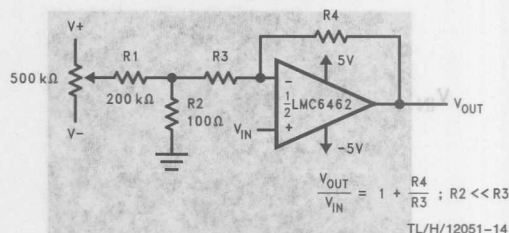


FIGURE 10. Non-Inverting Configuration Offset Voltage Adjustment

6.0 Spice Macromodel

A Spice macromodel is available for the LMC6462/4. This model includes a simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact the National Semiconductor Customer Response Center to obtain an operational amplifier Spice model library disk.

Application Information (Continued)

7.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6462/4, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6462's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 11. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 30 times degradation from the LMC6462/4's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 12a, 12b and 12c for typical connections of guard rings for standard op-amp configurations.

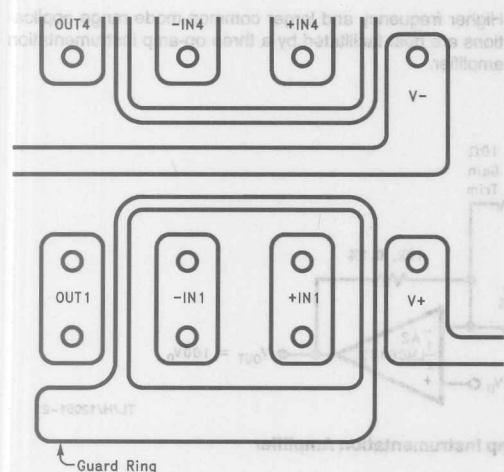


FIGURE 11. Example of Guard Ring in P.C. Board Layout

TL/H/12051-15

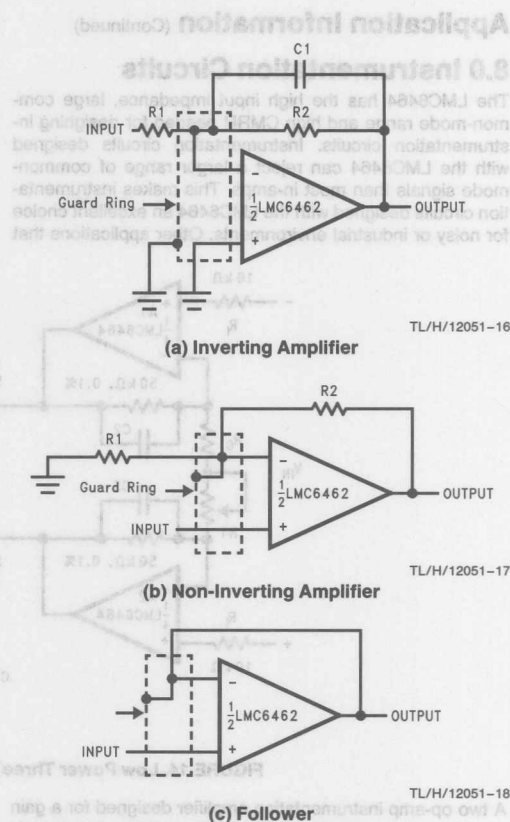
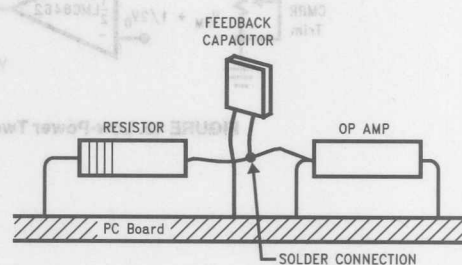


FIGURE 12. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 13.

FIGURE 13. Air Wiring
(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

TL/H/12051-19

Application Information (Continued)

8.0 Instrumentation Circuits

The LMC6464 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6464 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6464 an excellent choice for noisy or industrial environments. Other applications that

benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the three op-amp instrumentation circuit in Figure 14. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

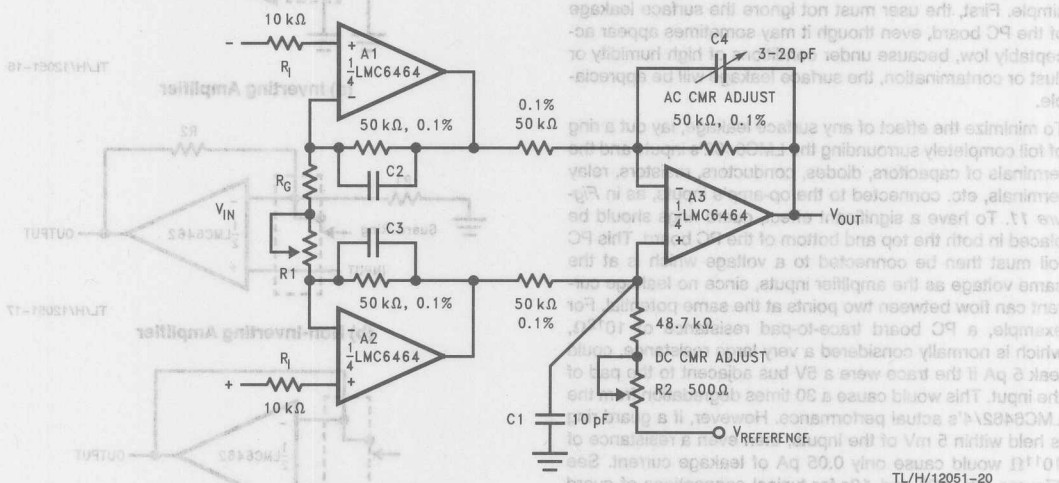


FIGURE 14. Low Power Three Op-Amp Instrumentation Amplifier

A two op-amp instrumentation amplifier designed for a gain of 100 is shown in Figure 15. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

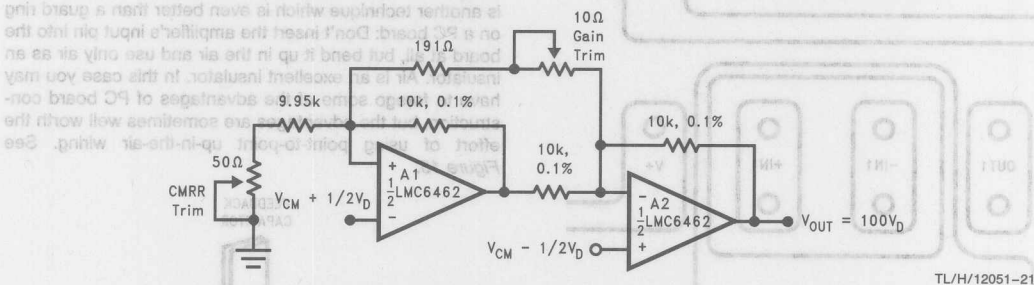


FIGURE 15. Low-Power Two-Op-Amp Instrumentation Amplifier

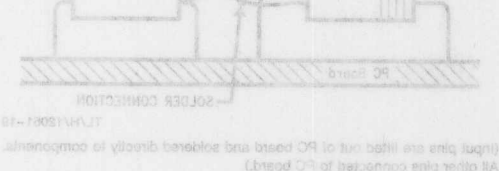


FIGURE 16. Air Wring

Application Information (Continued)

Typical Single-Supply Applications

TRANSDUCER INTERFACE CIRCUITS

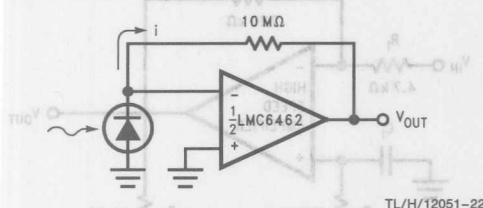


FIGURE 16. Photo Detector Circuit

Photocells can be used in portable light measuring instruments. The LMC6462, which can be operated off a battery, is an excellent choice for this circuit because of its very low input current and offset voltage.

LMC6462 AS A COMPARATOR

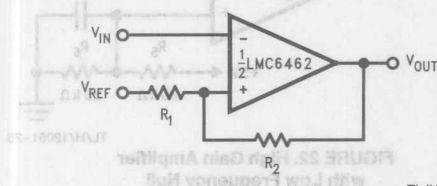
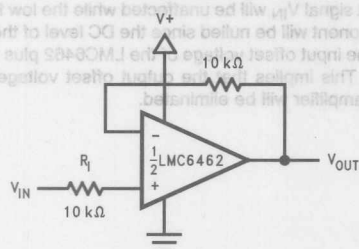
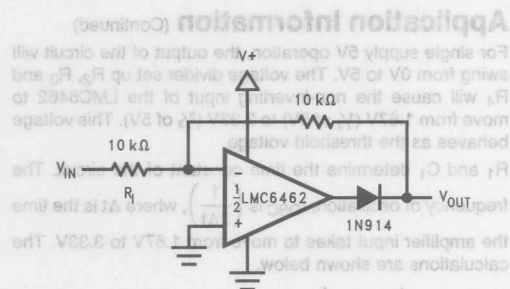


FIGURE 17. Comparator with Hysteresis

Figure 17 shows the application of the LMC6462 as a comparator. The hysteresis is determined by the ratio of the two resistors. The LMC6462 can thus be used as a micropower comparator, in applications where the quiescent current is an important parameter.

HALF-WAVE AND FULL-WAVE RECTIFIERS

FIGURE 18. Half-Wave Rectifier with Input Current Protection (R_I)FIGURE 19. Full-Wave Rectifier with Input Current Protection (R_I)

In Figures 18 and 19, R_I limits current into the amplifier since excess current can be caused by the input voltage exceeding the supply voltage.

PRECISION CURRENT SOURCE

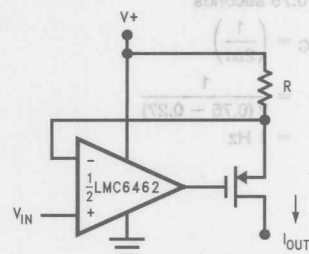


FIGURE 20. Precision Current Source

The output current I_{OUT} is given by:

$$I_{OUT} = \left(\frac{V^+ - V_{IN}}{R} \right)$$

OSCILLATORS

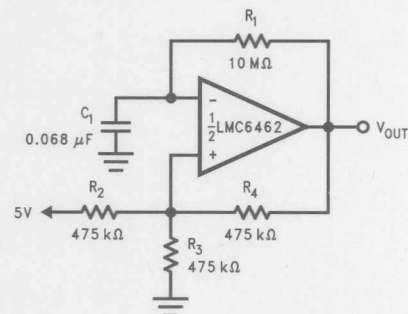


FIGURE 21. 1 Hz Square-Wave Oscillator

For single supply 5V operation, the output of the circuit will swing from 0V to 5V. The voltage divider set up R_2 , R_3 and R_4 will cause the non-inverting input of the LMC6462 to move from 1.67V ($\frac{1}{3}$ of 5V) to 3.33V ($\frac{2}{3}$ of 5V). This voltage behaves as the threshold voltage.

R_1 and C_1 determine the time constant of the circuit. The frequency of oscillation, f_{OSC} is $\left(\frac{1}{2\Delta t}\right)$, where Δt is the time the amplifier input takes to move from 1.67V to 3.33V. The calculations are shown below.

$$1.67 = 5 \left(1 - e^{-\frac{t_1}{\tau}}\right)$$

$$\text{where } \tau = RC = 0.68 \text{ seconds}$$

$$\rightarrow t_1 = 0.27 \text{ seconds}$$

and

$$3.33 = 5 \left(1 - e^{-\frac{t_2}{\tau}}\right)$$

$$\rightarrow t_2 = 0.75 \text{ seconds}$$

$$\text{Then, } f_{OSC} = \left(\frac{1}{2\Delta t}\right)$$

$$= \frac{1}{2(0.75 - 0.27)}$$

$$= 1 \text{ Hz}$$

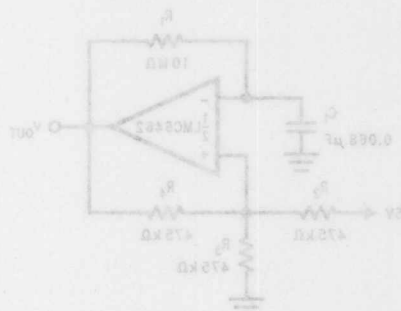


FIGURE 21. 1 Hz Square-Wave Oscillator

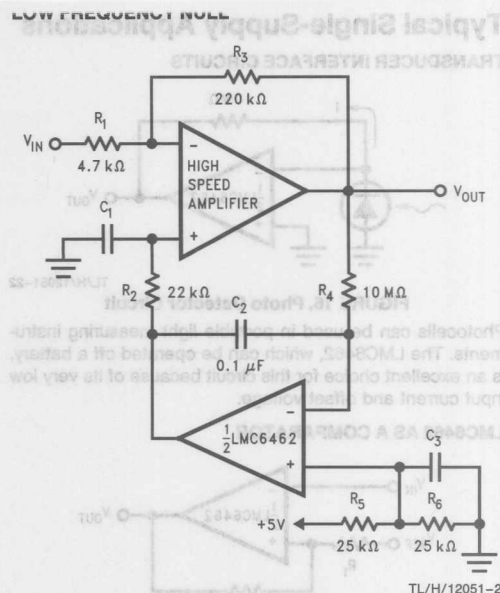
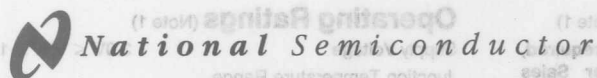


FIGURE 22. High Gain Amplifier with Low Frequency Null

Output offset voltage is the error introduced in the output voltage due to the inherent input offset voltage V_{OS} , of an amplifier.

Output Offset Voltage = (Input Offset Voltage) (Gain)

In the above configuration, the resistors R_5 and R_6 determine the nominal voltage around which the input signal, V_{IN} should be symmetrical. The high frequency component of the input signal V_{IN} will be unaffected while the low frequency component will be nulled since the DC level of the output will be the input offset voltage of the LMC6462 plus the bias voltage. This implies that the output offset voltage due to the top amplifier will be eliminated.



LMC6482 CMOS Dual Rail-To-Rail Input and Output Operational Amplifier

General Description

The LMC6482 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6482 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC272 and TLC277.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6482's rail-to-rail output swing. The LMC6482's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6482 especially well-suited for battery-operated systems.

See the LMC6484 data sheet for a Quad CMOS operational amplifier with these same features.

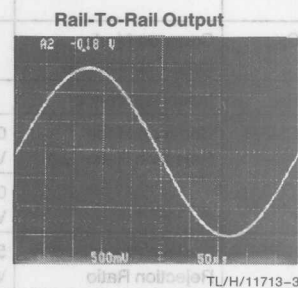
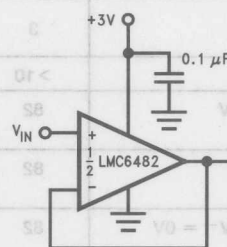
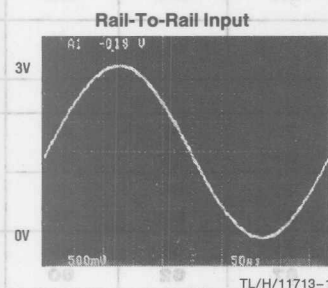
Features (Typical unless otherwise noted)

- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR 82 dB
- Ultra Low Input Current 20 fA
- High Voltage Gain ($R_L = 500 \text{ k}\Omega$) 130 dB
- Specified for 2 kΩ and 600Ω loads

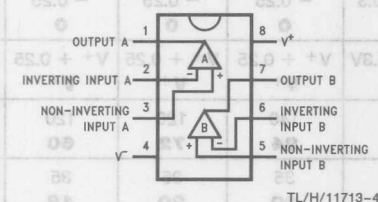
Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC272, TLC277

3V Single Supply Buffer Circuit



Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 8-Pin Molded DIP | LMC6482MN | LMC6482AIN LMC6482IN | N08E | Rail |
| 8-pin Small Outline | | LMC6482AIM LMC6482IM | M08A | Rail Tape and Reel |
| 8-pin Ceramic DIP | LMC6482AMJ/883 | | J08A | Rail |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|------------------------------|
| ESD Tolerance (Note 2) | 1.5 kV |
| Differential Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin | $(V^+) + 0.3V, (V^-) - 0.3V$ |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Current at Input Pin (Note 12) | ± 5 mA |
| Current at Output Pin (Notes 3, 8) | ± 30 mA |
| Current at Power Supply Pin | 40 mA |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Boldface limits apply at the temperature extremes.

Operating Ratings (Note 1)

| | |
|--------------------------------------|--|
| Supply Voltage | $3.0V \leq V^+ \leq 15.5V$ |
| Junction Temperature Range | |
| LMC6482AM | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| LMC6482AI, LMC6482I | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 90°C/W |
| M Package, 8-Pin Surface Mount | 155°C/W |

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6482AI Limit (Note 6) | LMC6482I Limit (Note 6) | LMC6482M Limit (Note 6) | Units | |
|-------------------|--|--|-----------------------|---|---|---|------------------|-------------|
| V _{OS} | Input Offset Voltage | | 0.11 | 0.750 1.35 | 3.0 3.7 | 3.0 3.8 | mV max | |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C | |
| I _B | Input Current | (Note 13) | 0.02 | 4.0 | 4.0 | 10.0 | pA max | |
| I _{OS} | Input Offset Current | (Note 13) | 0.01 | 2.0 | 2.0 | 5.0 | pA max | |
| C _{IN} | Common-Mode Input Capacitance | | 3 | | | | pF | |
| R _{IN} | Input Resistance | | > 10 | | | | TeraΩ | |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 15.0V V ⁺ = 15V | 82 | 70 67 | 65 62 | 65 60 | dB min | |
| | | 0V ≤ V _{CM} ≤ 5.0V V ⁺ = 5V | 82 | 70 67 | 65 62 | 65 60 | | |
| + PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V, V ⁻ = 0V V _O = 2.5V | 82 | 70 67 | 65 62 | 65 60 | dB min | |
| - PSRR | Negative Power Supply Rejection Ratio | -5V ≤ V ⁻ ≤ -15V, V ⁺ = 0V V _O = -2.5V | 82 | 70 67 | 65 62 | 65 60 | dB min | |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V For CMRR ≥ 50 dB | V ⁻ - 0.3 | - 0.25 0 | - 0.25 0 | - 0.25 0 | V max | |
| | | | V ⁺ + 0.3V | V ⁺ + 0.25 V⁺ | V ⁺ + 0.25 V⁺ | V ⁺ + 0.25 V⁺ | V min | |
| A _v | Large Signal Voltage Gain | R _L = 2 kΩ (Notes 7, 13) | Sourcing | 666 | 140 84 | 120 72 | 120 60 | V/mV min |
| | | | Sinking | 75 | 35 20 | 35 20 | 35 18 | V/mV min |
| | | R _L = 600Ω (Notes 7, 13) | Sourcing | 300 | 80 48 | 50 30 | 50 25 | V/mV min |
| | | | Sinking | 35 | 20 13 | 15 10 | 15 8 | V/mV min |

Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6482AI Limit (Note 6) | LMC6482I Limit (Note 6) | LMC6482M Limit (Note 6) | Units |
|----------|---|--|-----------------|--------------------------------|-------------------------------|-------------------------------|-----------|
| V_O | Output Swing | $V^+ = 5V$ $R_L = 2\text{ k}\Omega$ to $V^+ / 2$ | 4.9 | 4.8 4.7 | 4.8 4.7 | 4.8 4.7 | V min |
| | | | 0.1 | 0.18 0.24 | 0.18 0.24 | 0.18 0.24 | V max |
| | | $V^+ = 5V$ $R_L = 600\Omega$ to $V^+ / 2$ | 4.7 | 4.5 4.24 | 4.5 4.24 | 4.5 4.24 | V min |
| | | | 0.3 | 0.5 0.65 | 0.5 0.65 | 0.5 0.65 | V max |
| | | $V^+ = 15V$ $R_L = 2\text{ k}\Omega$ to $V^+ / 2$ | 14.7 | 14.4 14.2 | 14.4 14.2 | 14.4 14.2 | V min |
| | | | 0.16 | 0.32 0.45 | 0.32 0.45 | 0.32 0.45 | V max |
| | | $V^+ = 15V$ $R_L = 600\Omega$ to $V^+ / 2$ | 14.1 | 13.4 13.0 | 13.4 13.0 | 13.4 13.0 | V min |
| | | | 0.5 | 1.0 1.3 | 1.0 1.3 | 1.0 1.3 | V max |
| I_{SC} | Output Short Circuit Current $V^+ = 5V$ | Sourcing, $V_O = 0V$ | 20 | 16 12 | 16 12 | 16 10 | mA min |
| | | Sinking, $V_O = 5V$ | 15 | 11 9.5 | 11 9.5 | 11 8.0 | mA min |
| I_{SC} | Output Short Circuit Current $V^+ = 15V$ | Sourcing, $V_O = 0V$ | 30 | 28 22 | 28 22 | 28 20 | mA min |
| | | Sinking, $V_O = 12V$ (Note 8) | 30 | 30 24 | 30 24 | 30 22 | mA min |
| I_S | Supply Current | Both Amplifiers $V^+ = +5V$, $V_O = V^+ / 2$ | 1.0 | 1.4 1.8 | 1.4 1.8 | 1.4 1.9 | mA max |
| | | Both Amplifiers $V^+ = 15V$, $V_O = V^+ / 2$ | 1.3 | 1.6 1.9 | 1.6 1.9 | 1.6 2.0 | mA max |

1-850

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}$.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6482AI Limit (Note 6) | LMC6482I Limit (Note 6) | LMC6482M Limit (Note 6) | Units |
|------------|---------------------------------------|--|-----------------|--------------------------------|-------------------------------|-------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.9 | 2.0 2.7 | 3.0 3.7 | 3.0 3.8 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 2.0 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.02 | | | | pA |
| I_{OS} | Input Offset Current | | 0.01 | | | | pA |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 3\text{V}$ | 74 | 64 | 60 | 60 | dB min |
| PSRR | Power Supply Rejection Ratio | $3\text{V} \leq V^+ \leq 15\text{V}$, $V^- = 0\text{V}$ | 80 | 68 | 60 | 60 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | $V^- - 0.25$ | 0 | 0 | 0 | V max |
| | | | $V^+ + 0.25$ | V^+ | V^+ | V^+ | V min |
| V_O | Output Swing | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 2.8 | | | | V |
| | | | 0.2 | | | | V |
| | | $R_L = 600\Omega$ to $V^+/2$ | 2.7 | 2.5 | 2.5 | 2.5 | V min |
| | | | 0.37 | 0.6 | 0.6 | 0.6 | V max |
| I_S | Supply Current | Both Amplifiers | 0.825 | 1.2 1.5 | 1.2 1.5 | 1.2 1.6 | mA max |

AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$, and $R_L > 1\text{M}$.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6482AI Limit (Note 6) | LMC6482I Limit (Note 6) | LMC6482M Limit (Note 6) | Units |
|--------|---------------------------|---|-----------------|--------------------------------|-------------------------------|-------------------------------|------------------|
| SR | Slew Rate | (Note 11) | 0.9 | | | | V/ μs |
| GBW | Gain-Bandwidth Product | | 1.0 | | | | MHz |
| T.H.D. | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 2\text{ V}_{PP}$ | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF . All pins rated per method 3015.6 of MIL-STD-883. This is a Class 1 device rating.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $3.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: Do not short circuit output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{PP}$.

Note 11: Connected as voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

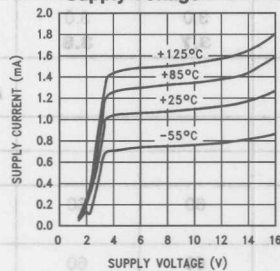
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature parameters see RETS6482X.

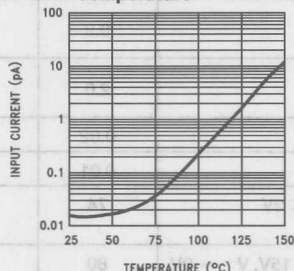
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

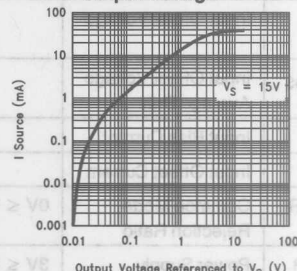
Supply Current vs Supply Voltage



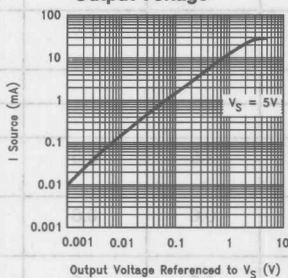
Input Current vs Temperature



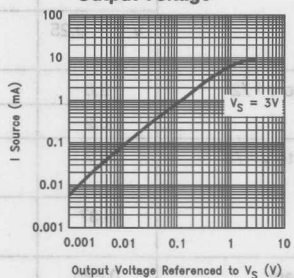
Sourcing Current vs Output Voltage



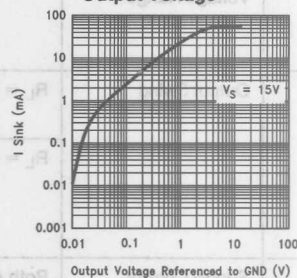
Sourcing Current vs Output Voltage



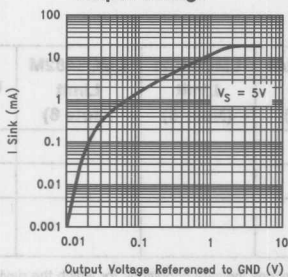
Sourcing Current vs Output Voltage



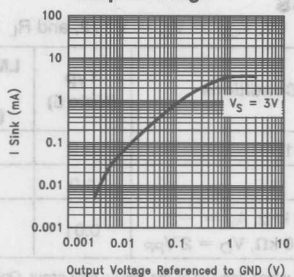
Sinking Current vs Output Voltage



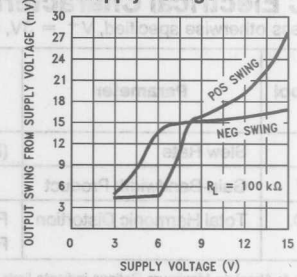
Sinking Current vs Output Voltage



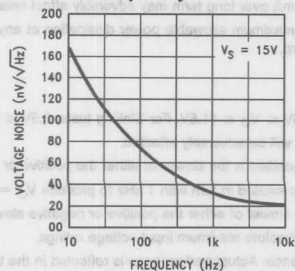
Sinking Current vs Output Voltage



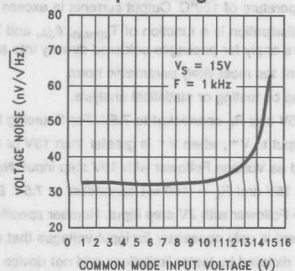
Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency

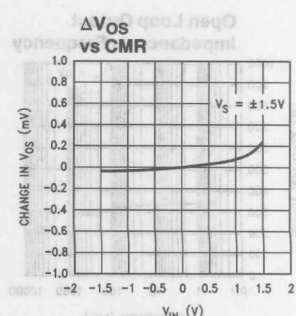
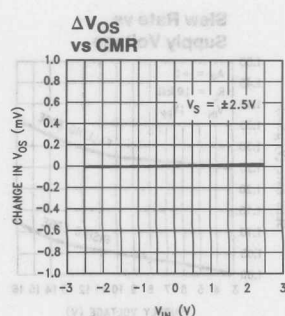
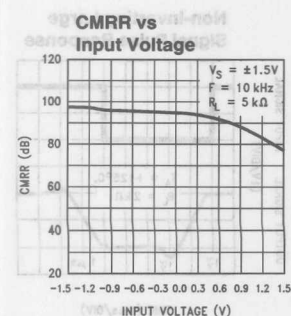
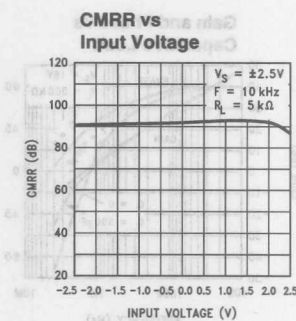
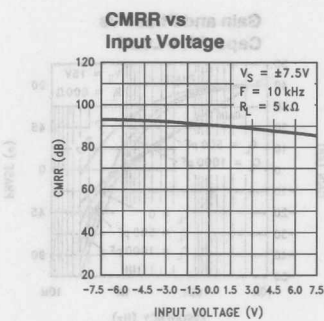
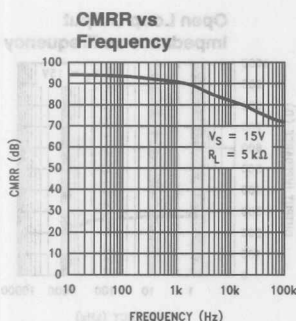
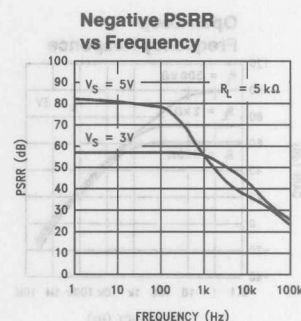
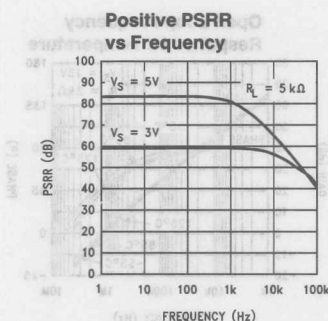
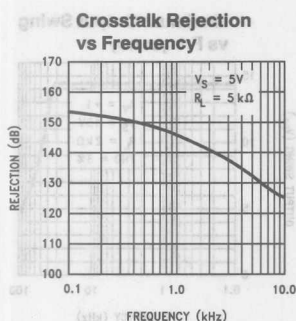
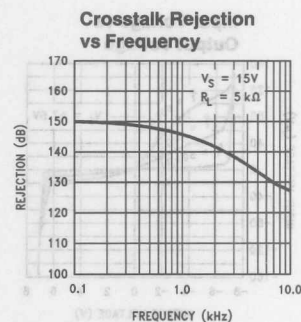
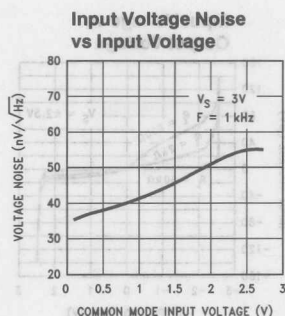
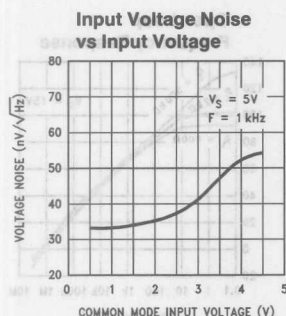


Input Voltage Noise vs Input Voltage

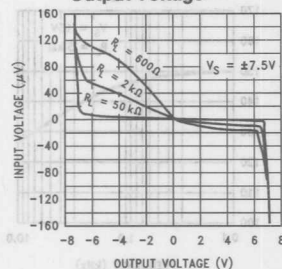
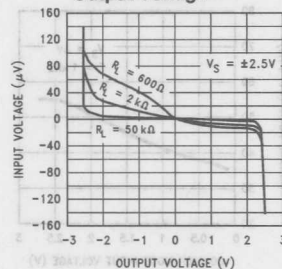
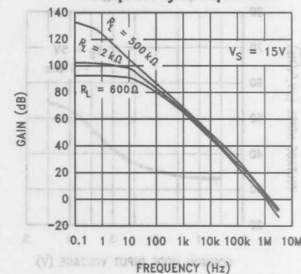
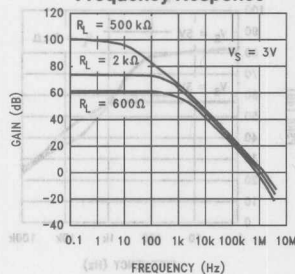
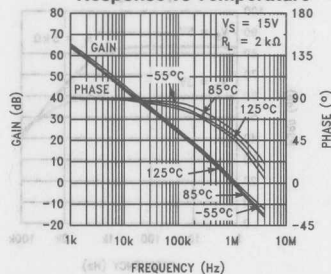
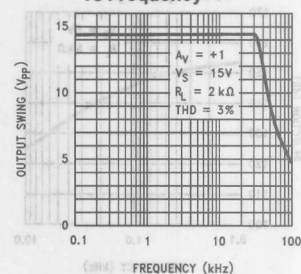
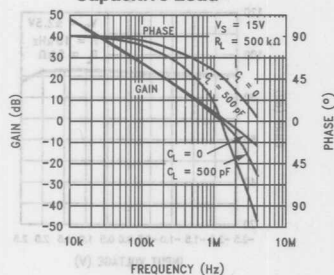
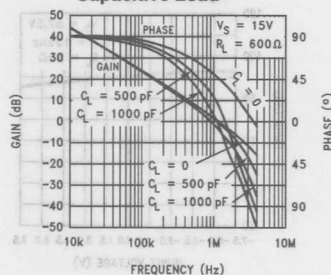
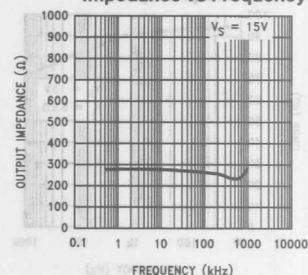
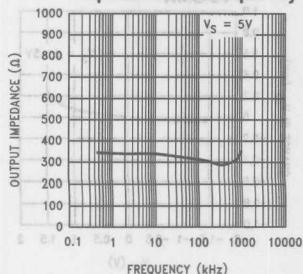
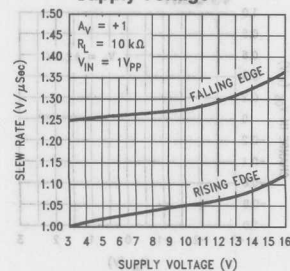
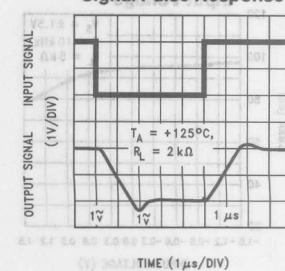


Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)



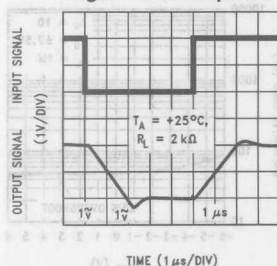
TL/H/11713-6

**Input Voltage vs
Output Voltage**

**Input Voltage vs
Output Voltage**

**Open Loop
Frequency Response**

**Open Loop
Frequency Response**

**Open Loop Frequency
Response vs Temperature**

**Maximum Output Swing
vs Frequency**

**Gain and Phase vs
Capacitive Load**

**Gain and Phase vs
Capacitive Load**

**Open Loop Output
Impedance vs Frequency**

**Open Loop Output
Impedance vs Frequency**

**Slew Rate vs
Supply Voltage**

**Non-Inverting Large
Signal Pulse Response**


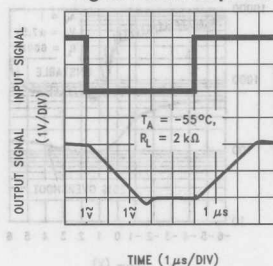
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

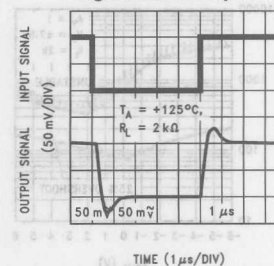
**Non-Inverting Large
Signal Pulse Response**



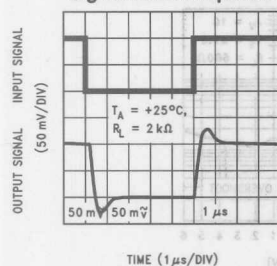
**Non-Inverting Large
Signal Pulse Response**



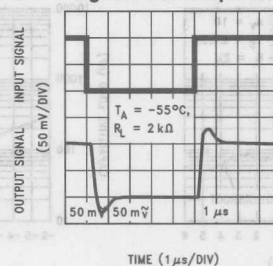
**Non-Inverting Small
Signal Pulse Response**



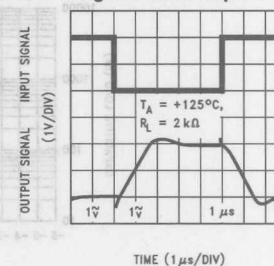
**Non-Inverting Small
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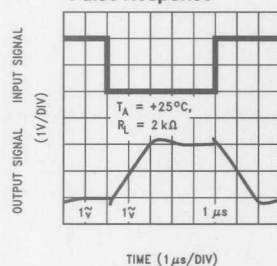
**Non-Inverting Small
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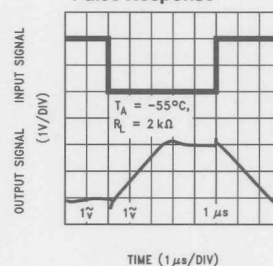
**Inverting Large
Signal Pulse Response**



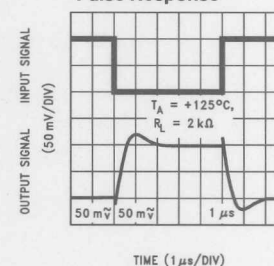
**Inverting Large Signal
Pulse Response**



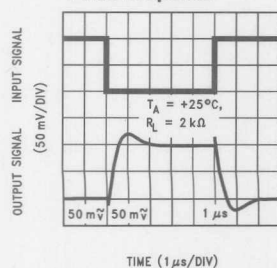
**Inverting Large Signal
Pulse Response**



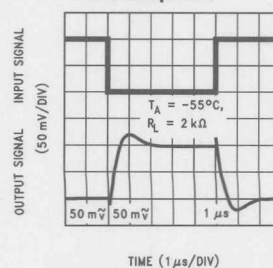
**Inverting Small Signal
Pulse Response**



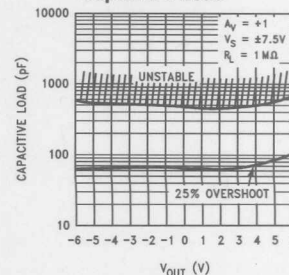
**Inverting Small Signal
Pulse Response**



**Inverting Small Signal
Pulse Response**

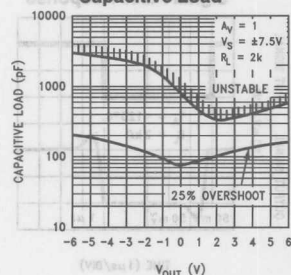
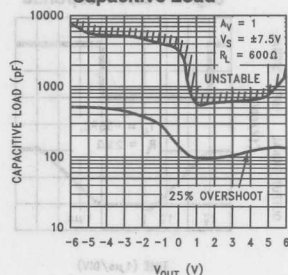
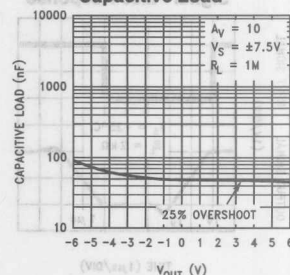
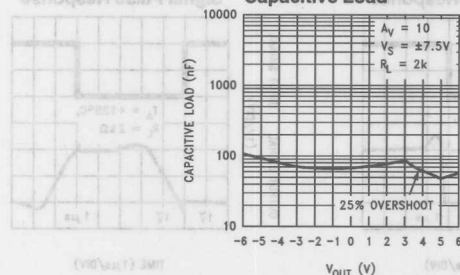
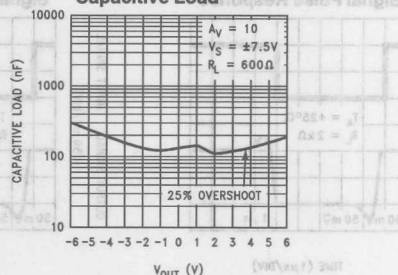


**Stability vs
Capacitive Load**

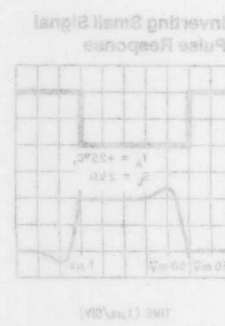
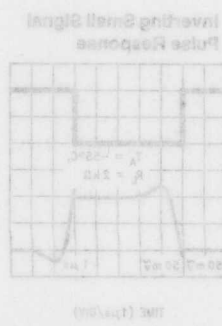
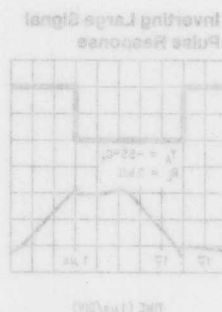
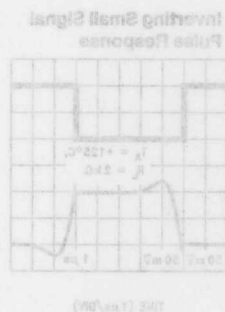


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Typical Performance Characteristics

 $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)Stability vs
Capacitive LoadStability vs
Capacitive LoadStability vs
Capacitive LoadStability vs
Capacitive LoadStability vs
Capacitive Load

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1.0 Amplifier Topology

The LMC6482 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6482's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6482 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

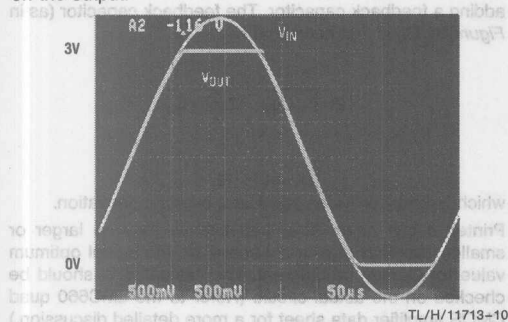


FIGURE 1. An Input Voltage Signal Exceeds the LMC6482 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 2, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

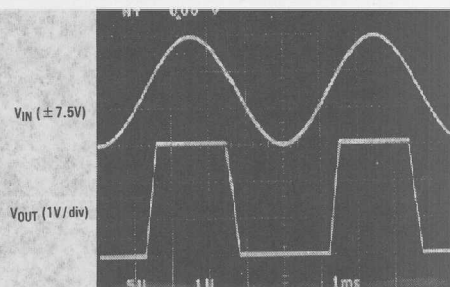


FIGURE 2. A $\pm 7.5V$ Input Signal Greatly Exceeds the 3V Supply in Figure 3 Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor (R_I) as shown in Figure 3.

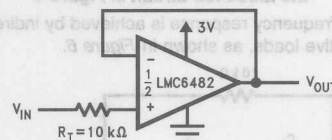


FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6482 is 180 Ω sourcing and 130 Ω sinking at $V_S = 3V$ and 110 Ω sourcing and 80 Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6482 can typically directly drive a 100 pF load with $V_S = 15V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 4. This simple technique is useful for isolating the capacitive inputs of multiplexers and A/D converters.

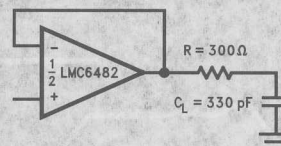


FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

Application Information (Continued)

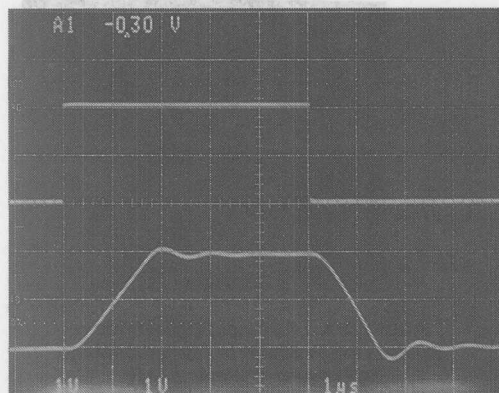


FIGURE 5. Pulse Response of the LMC6482 Circuit in Figure 4

Improved frequency response is achieved by indirectly driving capacitive loads, as shown in Figure 6.

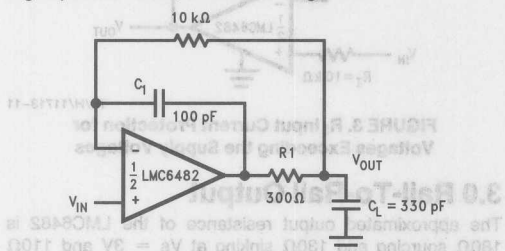


FIGURE 6. LMC6482 Noninverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifiers inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 7.

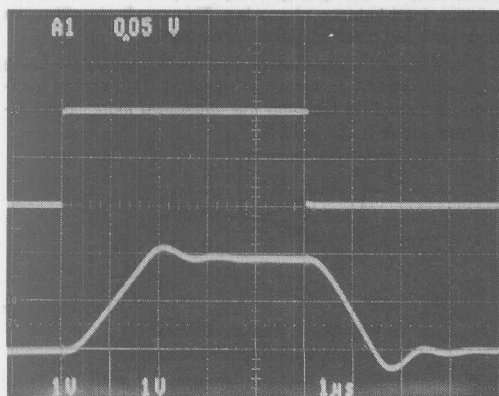


FIGURE 7. Pulse Response of LMC6482 Circuit in Figure 6

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6482. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuits board parasitics to reduce phase margins.

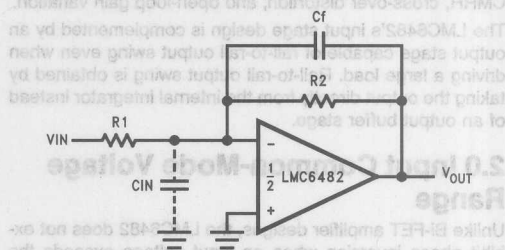


FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 8), C_f , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a bread-board, so the actual optimum value for C_f may be different. The values of C_f should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low input current of the LMC6482, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6482's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 9. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6482's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 10a, 10b, 10c for typical connections of guard rings for standard op-amp configurations.

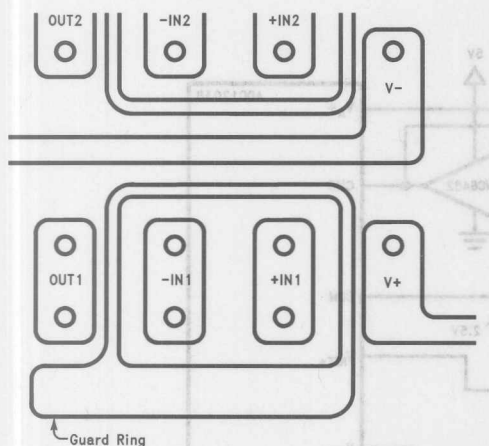
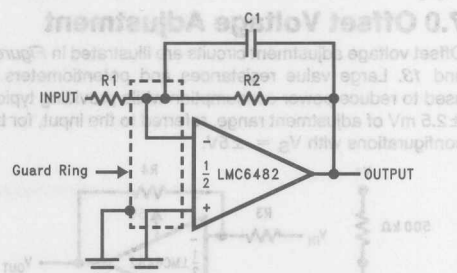


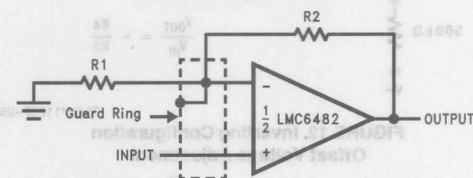
FIGURE 9. Example of Guard Ring in P.C. Board Layout

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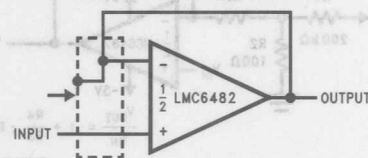
(a) Inverting Amplifier

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TL/H/11713-22

(b) Non-Inverting Amplifier

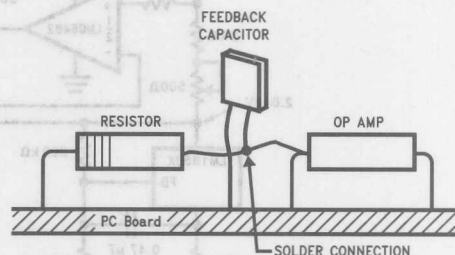


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(c) Follower

FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 11.



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(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

The diagram shows an inverting amplifier circuit using an LMC6482 op-amp. The input signal V_{IN} is connected to the inverting input (-) through a resistor $R3$. The non-inverting input (+) is connected to ground through a resistor $R4$. The output V_{OUT} is connected to the inverting input (-) through a feedback resistor $R4$. The op-amp is powered by a 5V supply and a -5V supply. The input signal V_{IN} is connected to the inverting input (-) through a resistor $R3$. The non-inverting input (+) is connected to ground through a resistor $R4$. The output V_{OUT} is connected to the inverting input (-) through a feedback resistor $R4$. The op-amp is powered by a 5V supply and a -5V supply.

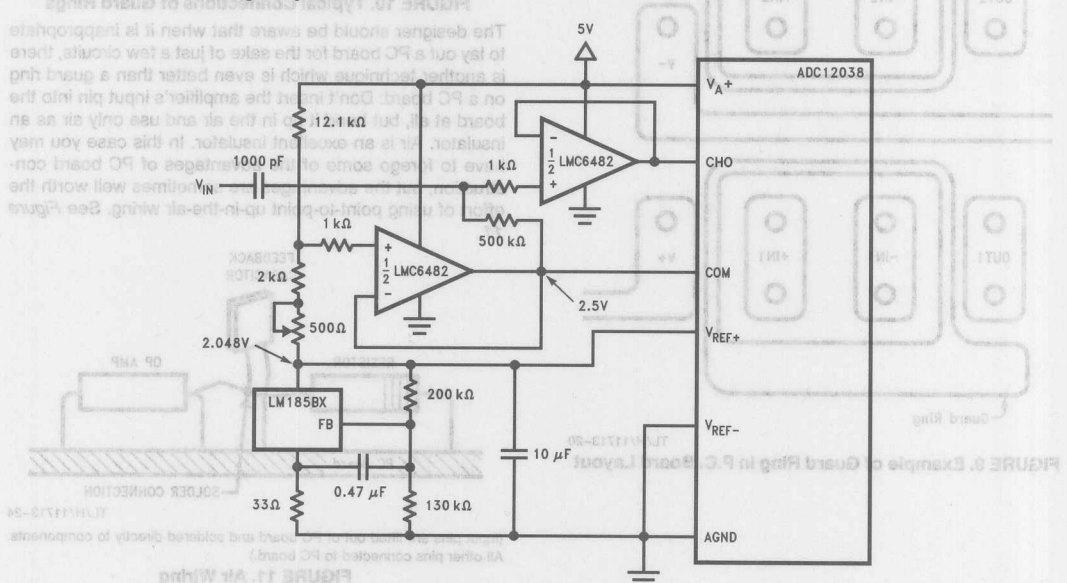
$$\frac{V_{OUT}}{V_{IN}} = - \frac{R4}{R3}$$

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_4}{R_3} ; R_2 < R_3$$

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Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6482 (Figure 14). Capable of using the full supply range, the LMC6482 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC4282 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ± 0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.



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Application Information (Continued)

10.0 Instrumentation Circuits

The LMC6482 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6482 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6482 an excellent choice of noisy or industrial environments. Other applications that

benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

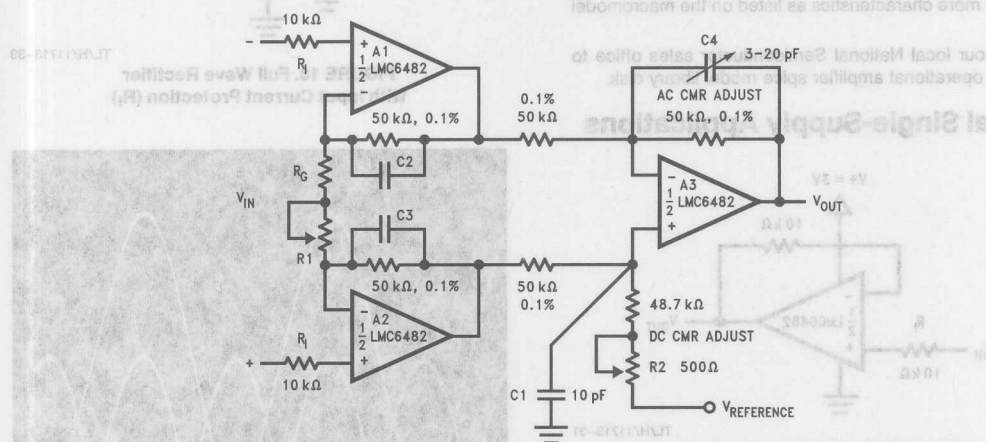


FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

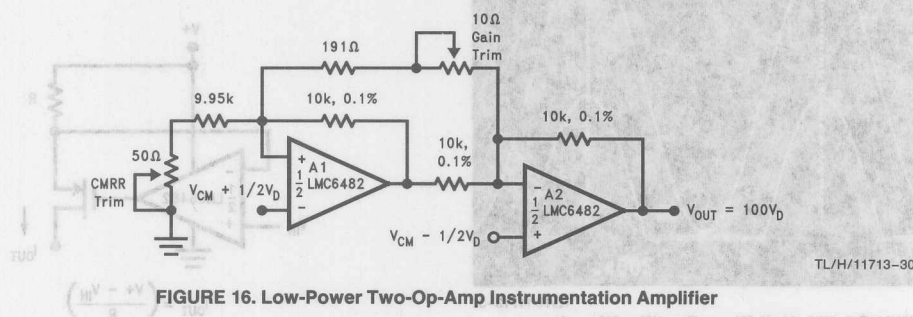


FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

11.0 Spice Macromodel

A spice macromodel is available for the LMC6482. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

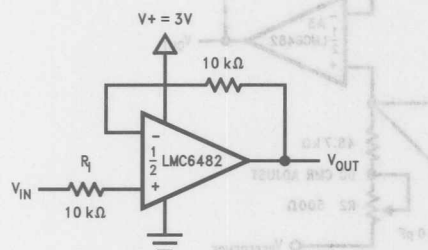


FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)

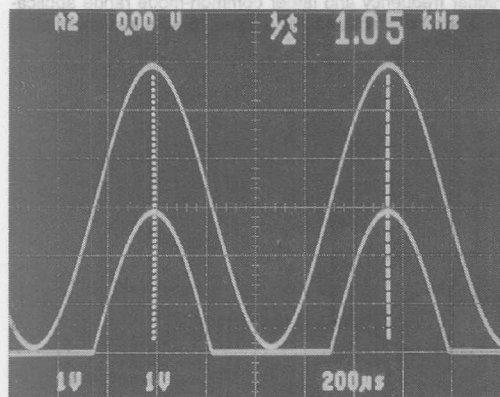


FIGURE 17A. Half-Wave Rectifier Waveform

The circuit in Figure 17 uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 18.

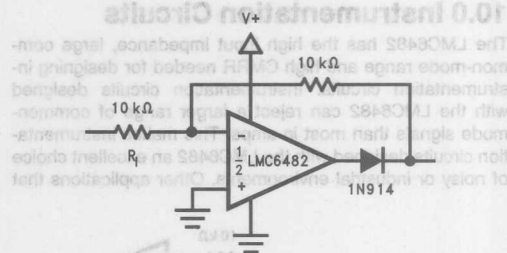


FIGURE 18. Full Wave Rectifier with Input Current Protection (R_I)

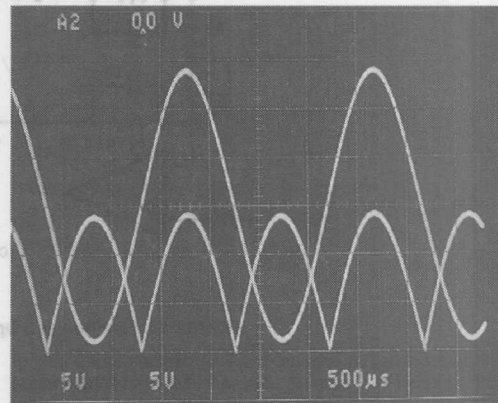
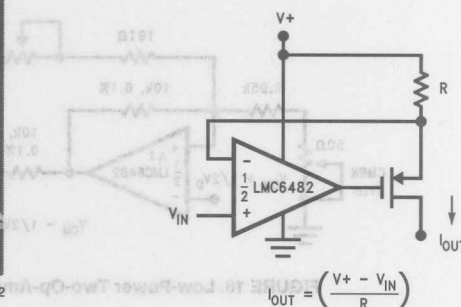


FIGURE 18A. Full Wave Rectifier Waveform



$$I_{OUT} = \left(\frac{V+ - V_{IN}}{R} \right)$$

FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications

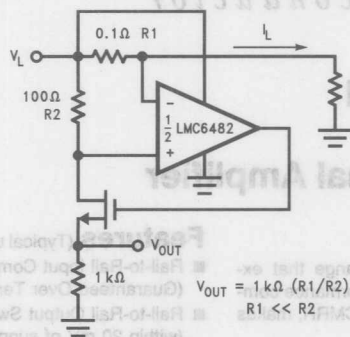


FIGURE 20. Positive Supply Current Sense

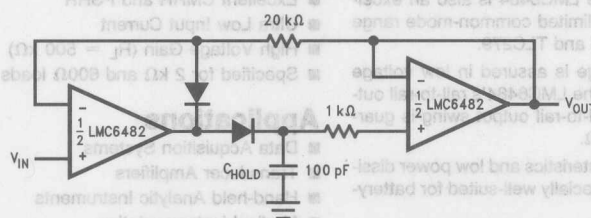


FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In Figure 21 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6482 has a negligible effect on droop.

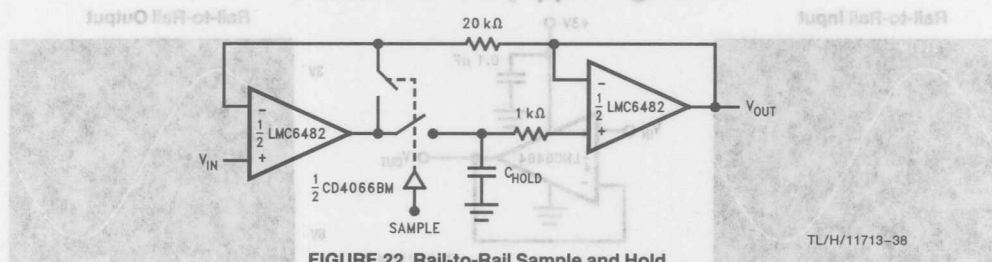


FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6482's high CMRR (82 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.

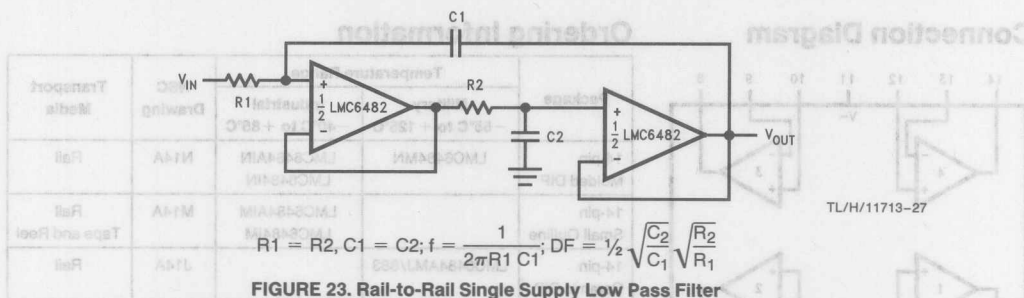


FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in Figure 23 can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6482 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

LMC6484 CMOS Quad Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6484 provides a common-mode range that extends to both supply rails. This rail-to-rail performance combined with excellent accuracy, due to a high CMRR, makes it unique among rail-to-rail input amplifiers.

It is ideal for systems, such as data acquisition, that require a large input signal range. The LMC6484 is also an excellent upgrade for circuits using limited common-mode range amplifiers such as the TLC274 and TLC279.

Maximum dynamic signal range is assured in low voltage and single supply systems by the LMC6484's rail-to-rail output swing. The LMC6484's rail-to-rail output swing is guaranteed for loads down to 600Ω.

Guaranteed low voltage characteristics and low power dissipation make the LMC6484 especially well-suited for battery-operated systems.

See the LMC6482 data sheet for a Dual CMOS operational amplifier with these same features.

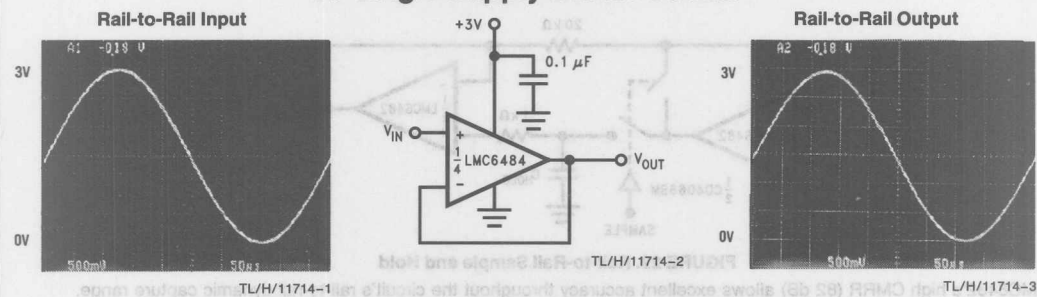
Features (Typical unless otherwise noted)

- Rail-to-Rail Input Common-Mode Voltage Range (Guaranteed Over Temperature)
- Rail-to-Rail Output Swing (within 20 mV of supply rail, 100 kΩ load)
- Guaranteed 3V, 5V and 15V Performance
- Excellent CMRR and PSRR 82 dB
- Ultra Low Input Current 20 fA
- High Voltage Gain ($R_L = 500 \text{ k}\Omega$) 130 dB
- Specified for 2 kΩ and 600Ω loads

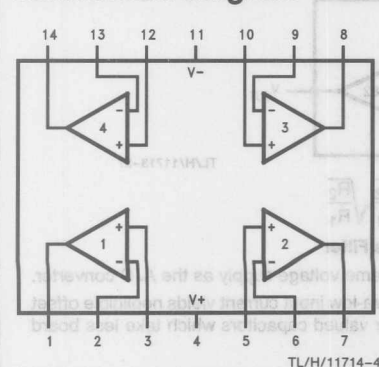
Applications

- Data Acquisition Systems
- Transducer Amplifiers
- Hand-held Analytic Instruments
- Medical Instrumentation
- Active Filter, Peak Detector, Sample and Hold, pH Meter, Current Source
- Improved Replacement for TLC274, TLC279

3V Single Supply Buffer Circuit



Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|----------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 14-pin Molded DIP | LMC6484MN | LMC6484AIN LMC6484IN | N14A | Rail |
| 14-pin Small Outline | | LMC6484AIM LMC6484IM | M14A | Rail Tape and Reel |
| 14-pin Ceramic DIP | LMC6484AMJ/883 | | J14A | Rail |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|----------------------|
| ESD Tolerance (Note 2) | 2.0 kV |
| Differential Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin (V^+) + 0.3V, (V^-) - 0.3V | |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Current at Input Pin (Note 12) | ± 5 mA |
| Current at Output Pin (Notes 3, 8) | ± 30 mA |
| Current at Power Supply Pin | 40 mA |
| Lead Temp. (Soldering, 10 sec.) | 260°C |

| | |
|-------------------------------|-----------------|
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

Operating Ratings (Note 1)

| | |
|--------------------------------------|--|
| Supply Voltage | $3.0V \leq V^+ \leq 15.5V$ |
| Junction Temperature Range | |
| LMC6484AM | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |
| LMC6484AI, LMC6484I | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Thermal Resistance (θ_{JA}) | |
| N Package, 14-Pin Molded DIP | 70°C/W |
| M Package, 14-Pin Surface Mount | 110°C/W |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1M$.

Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6484AI Limit (Note 6) | LMC6484I Limit (Note 6) | LMC6484M Limit (Note 6) | Units |
|-------------------|--|---|----------------------|---|---|---|-------------|
| V _{OS} | Input Offset Voltage | | 0.110 | 0.750 1.35 | 3.0 3.7 | 3.0 3.8 | mV max |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.0 | | | | μV/°C |
| I _B | Input Current | (Note 13) | 0.02 | 4.0 | 4.0 | 100 | pA max |
| I _{OS} | Input Offset Current | (Note 13) | 0.01 | 2.0 | 2.0 | 50 | pA max |
| C _{IN} | Common-Mode Input Capacitance | | 3 | | | | pF |
| R _{IN} | Input Resistance | | > 10 | | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 15.0V, V ⁺ = 15V | 82 | 70 67 | 65 62 | 65 60 | dB min |
| | | 0V ≤ V _{CM} ≤ 5.0V V ⁺ = 5V | 82 | 70 67 | 65 62 | 65 60 | |
| +PSRR | Positive Power Supply Rejection Ratio | 5V ≤ V ⁺ ≤ 15V, V ⁻ = 0V, V _O = 2.5V | 82 | 70 67 | 65 62 | 65 60 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | -5V ≤ V ⁻ ≤ -15V, V ⁺ = 0V, V _O = -2.5V | 82 | 70 67 | 65 62 | 65 60 | dB min |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 5V and 15V For CMRR ≥ 50 dB | V ⁻ - 0.3 | -0.25 0 | -0.25 0 | -0.25 0 | V max |
| | | | V ⁺ + 0.3 | V ⁺ + 0.25 V⁺ | V ⁺ + 0.25 V⁺ | V ⁺ + 0.25 V⁺ | V min |
| A _v | Large Signal Voltage Gain | R _L = 2kΩ (Notes 7, 13) | Sourcing | 666 84 | 140 72 | 120 60 | V/mV min |
| | | | Sinking | 75 20 | 35 20 | 35 18 | V/mV min |
| | | R _L = 600Ω (Notes 7, 13) | Sourcing | 300 48 | 50 30 | 50 25 | V/mV min |
| | | | Sinking | 35 13 | 15 10 | 15 8 | V/mV min |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}$. **Boldface** limits apply at the temperature extremes. (Continued)

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6484AI Limit (Note 6) | LMC6484I Limit (Note 6) | LMC6484M Limit (Note 6) | Units |
|----------|------------------------------|--|-----------------|--------------------------------|-------------------------------|-------------------------------|-----------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{k}\Omega$ to $V^+/2$ | 4.9 | 4.8 4.7 | 4.8 4.7 | 4.8 4.7 | V min |
| | | | 0.1 | 0.18 0.24 | 0.18 0.24 | 0.18 0.24 | V max |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to $V^+/2$ | 4.7 | 4.5 4.24 | 4.5 4.24 | 4.5 4.24 | V min |
| | | | 0.3 | 0.5 0.65 | 0.5 0.65 | 0.5 0.65 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{k}\Omega$ to $V^+/2$ | 14.7 | 14.4 14.2 | 14.4 14.2 | 14.4 14.2 | V min |
| | | | 0.16 | 0.32 0.45 | 0.32 0.45 | 0.32 0.45 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ to $V^+/2$ | 14.1 | 13.4 13.0 | 13.4 13.0 | 13.4 13.0 | V min |
| | | | 0.5 | 1.0 1.3 | 1.0 1.3 | 1.0 1.3 | V max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 20 | 16 12 | 16 12 | 16 10 | mA min |
| | | Sinking, $V_O = 5\text{V}$ | 15 | 11 9.5 | 11 9.5 | 11 8.0 | mA min |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 30 | 28 22 | 28 22 | 28 20 | mA min |
| | | Sinking, $V_O = 12\text{V}$ (Note 8) | 30 | 30 24 | 30 24 | 30 22 | mA min |
| I_S | Supply Current | All Four Amplifiers $V^+ = +5\text{V}$, $V_O = V^+/2$ | 2.0 | 2.8 3.6 | 2.8 3.6 | 2.8 3.8 | mA max |
| | | All Four Amplifiers $V^+ = +15\text{V}$, $V_O = V^+/2$ | 2.6 | 3.0 3.8 | 3.0 3.8 | 3.0 4.0 | mA max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6484A Limit (Note 6) | LMC6484I Limit (Note 6) | LMC6484M Limit (Note 6) | Units |
|----------|------------------------------|--|-----------------|-------------------------------|-------------------------------|-------------------------------|------------------------------|
| SR | Slew Rate | (Note 9) | 1.3 | 1.0 0.7 | 0.9 0.63 | 0.9 0.54 | V/ μs min |
| GBW | Gain-Bandwidth Product | $V^+ = 15\text{V}$ | 1.5 | | | | MHz |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| G_m | Gain Margin | | 15 | | | | dB |
| | Amp-to-Amp Isolation | (Note 10) | 150 | | | | dB |
| e_n | Input-Referred Voltage Noise | $f = 1\text{kHz}$ $V_{CM} = 1\text{V}$ | 37 | | | | $\text{nV}/\sqrt{\text{Hz}}$ |
| i_n | Input-Referred Current Noise | $f = 1\text{kHz}$ | 0.03 | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $f = 1\text{kHz}$, $A_V = -2$ $R_L = 10\text{k}\Omega$, $V_O = 4.1\text{V}_{PP}$ | 0.01 | | | | % |
| | | $f = 10\text{kHz}$, $A_V = -2$ $R_L = 10\text{k}\Omega$, $V_O = 8.5\text{V}_{PP}$ $V^+ = 10\text{V}$ | 0.01 | | | | % |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}$

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6484AI Limit (Note 6) | LMC6484I Limit (Note 6) | LMC6484M Limit (Note 6) | Units |
|------------|---------------------------------------|--|-----------------|--------------------------------|-------------------------------|-------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.9 | 2.0 2.7 | 3.0 3.7 | 3.0 3.8 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 2.0 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.02 | | | | pA |
| I_{OS} | Input Offset Current | | 0.01 | | | | pA |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 3\text{V}$ | 74 | 64 | 60 | 60 | dB min |
| PSRR | Power Supply Rejection Ratio | $3\text{V} \leq V^+ \leq 15\text{V}$, $V^- = 0\text{V}$ | 80 | 68 | 60 | 60 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | $V^- - 0.25$ | 0 | 0 | 0 | V max |
| | | | $V^+ + 0.25$ | V^+ | V^+ | V^+ | V min |
| V_O | Output Swing | $R_L = 2\text{ k}\Omega$ to $V^+/2$ | 2.8 | | | | V |
| | | | 0.2 | | | | V |
| | | $R_L = 600\Omega$ to $V^+/2$ | 2.7 | 2.5 | 2.5 | 2.5 | V min |
| | | | 0.37 | 0.6 | 0.6 | 0.6 | V max |
| I_S | Supply Current | All Four Amplifiers | 1.65 | 2.5 3.0 | 2.5 3.0 | 2.5 3.2 | mA max |

AC Electrical Characteristics

Unless otherwise specified, $V^+ = 3\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}$

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6484AI Limit (Note 6) | LMC6484I Limit (Note 6) | LMC6484M Limit (Note 6) | Units |
|--------|---------------------------|---|-----------------|--------------------------------|-------------------------------|-------------------------------|------------------|
| SR | Slew Rate | (Note 11) | 0.9 | | | | V/ μs |
| GBW | Gain-Bandwidth Product | | 1.0 | | | | MHz |
| T.H.D. | Total Harmonic Distortion | $f = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 2\text{ V}_{pp}$ | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF . All pins rated per method 3015.6 of MIL-STD-883. This is a class 2 device rating.

Note 3: Applies to both single supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $3.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: Do not short circuit output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of either the positive or negative slew rates.

Note 10: Input referred, $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{pp}$.

Note 11: Connected as Voltage Follower with 2V step input. Number specified is the slower of either the positive or negative slew rates.

Note 12: Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

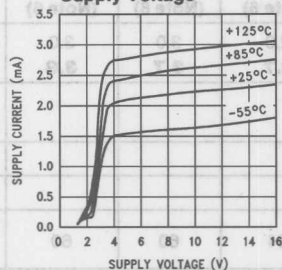
Note 13: Guaranteed limits are dictated by tester limitations and not device performance. Actual performance is reflected in the typical value.

Note 14: For guaranteed Military Temperature Range parameters see RETSMC6484X.

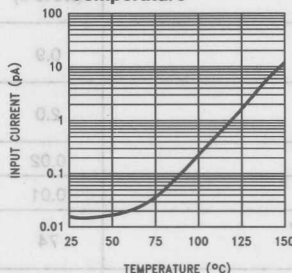
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified

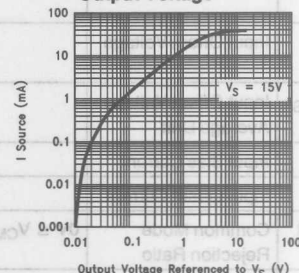
Supply Current vs Supply Voltage



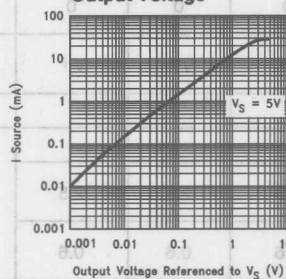
Input Current vs Temperature



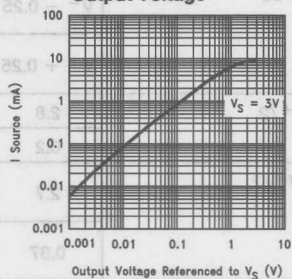
Sourcing Current vs Output Voltage



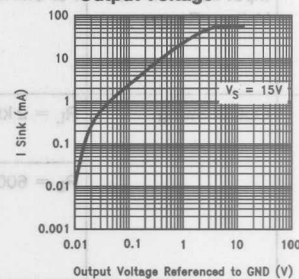
Sourcing Current vs Output Voltage



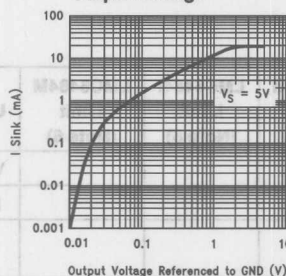
Sourcing Current vs Output Voltage



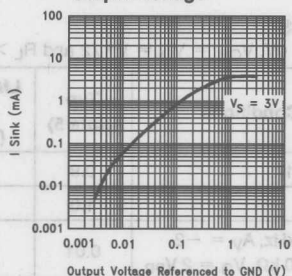
Sinking Current vs Output Voltage



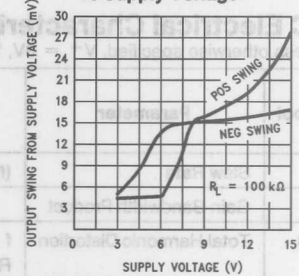
Sinking Current vs Output Voltage



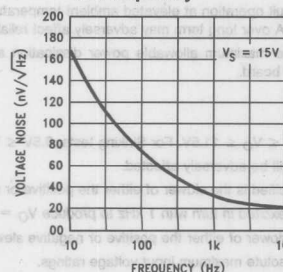
Sinking Current vs Output Voltage



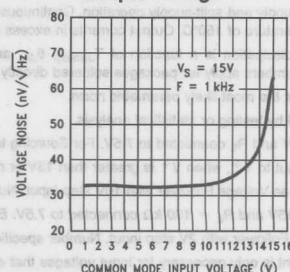
Output Voltage Swing vs Supply Voltage



Input Voltage Noise vs Frequency

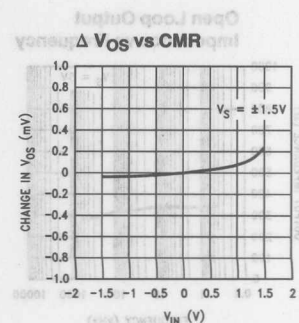
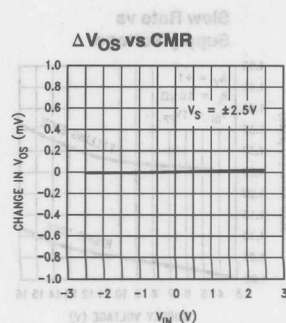
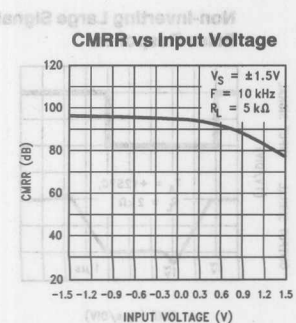
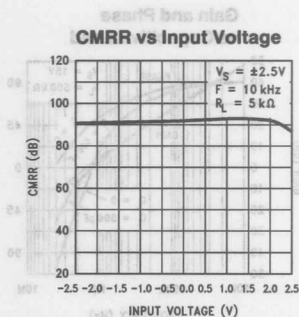
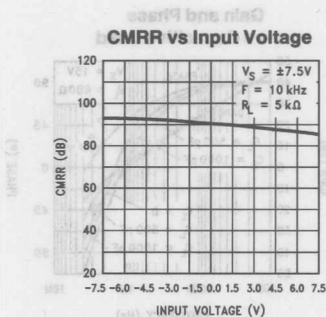
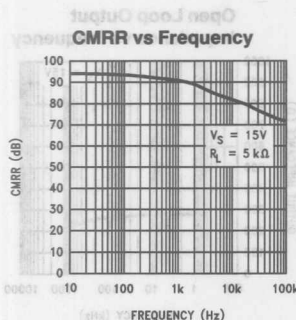
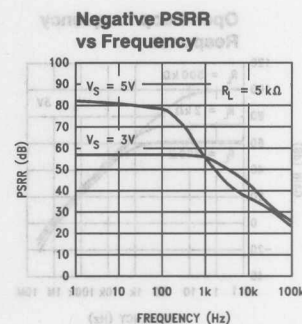
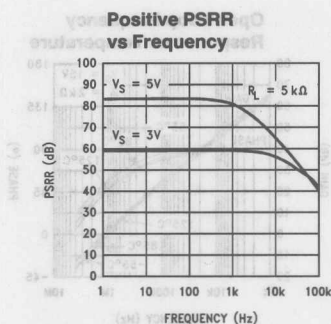
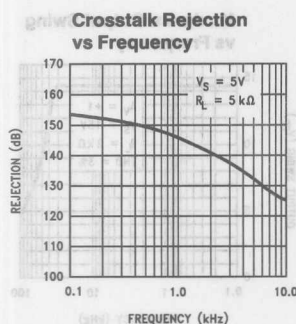
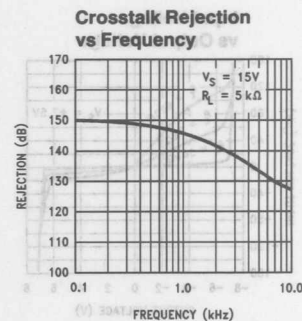
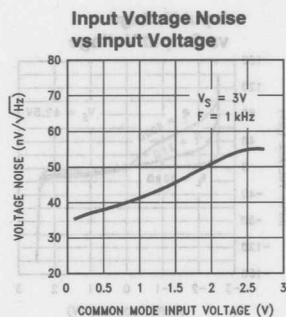
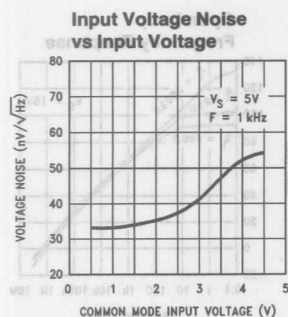


Input Voltage Noise vs Input Voltage

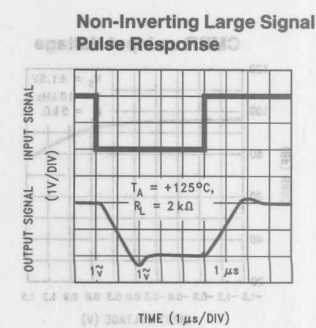
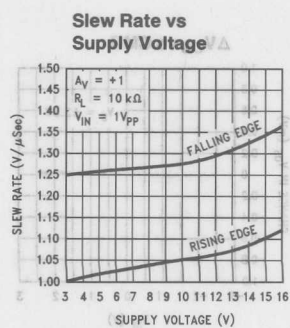
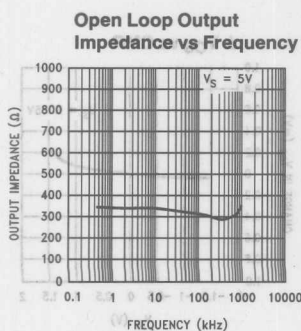
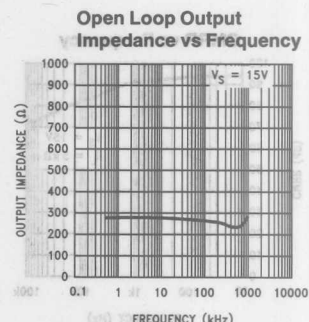
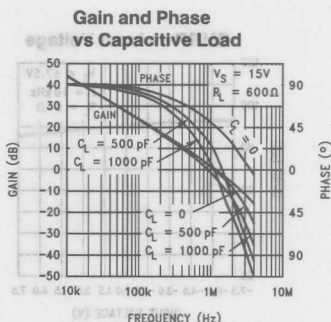
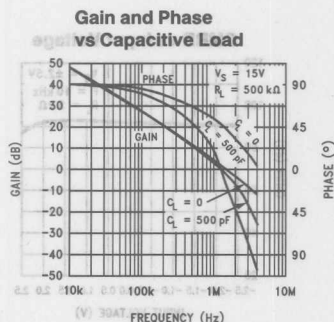
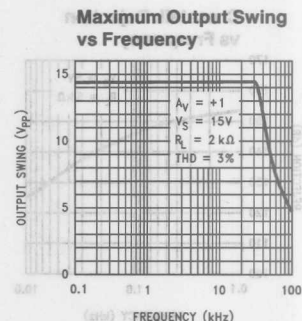
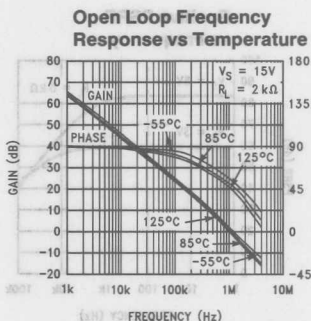
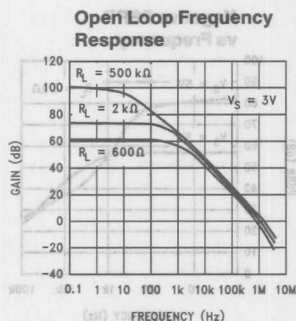
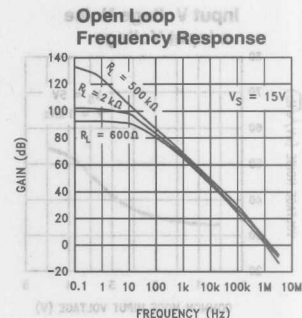
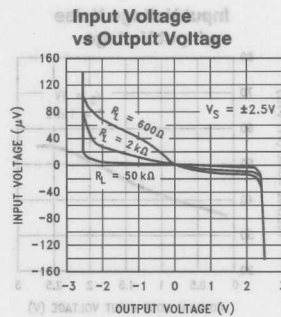
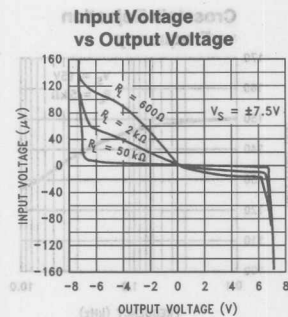


Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)



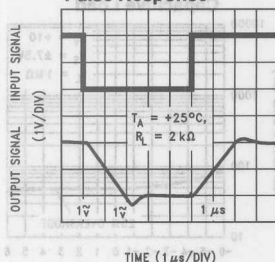
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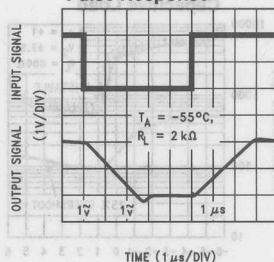
Typical Performance Characteristics

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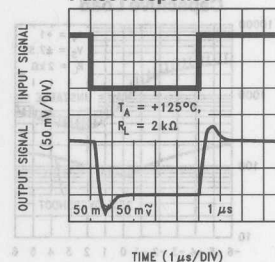
Non-Inverting Large Signal Pulse Response



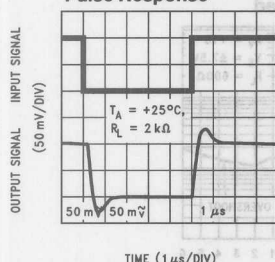
Non-Inverting Large Signal Pulse Response



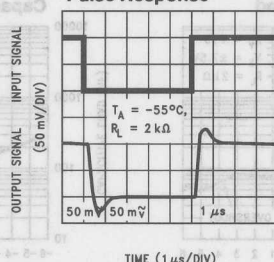
Non-Inverting Small Signal Pulse Response



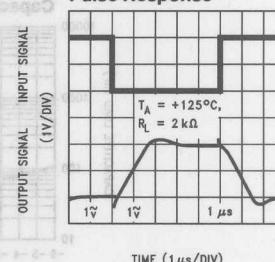
Non-Inverting Small Signal Pulse Response



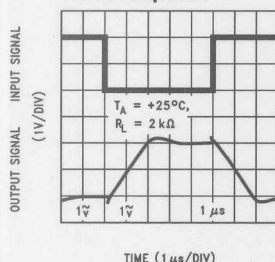
Non-Inverting Small Signal Pulse Response



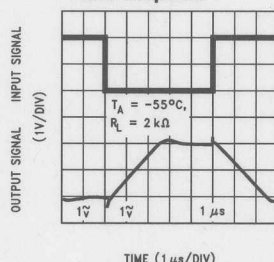
Inverting Large Signal Pulse Response



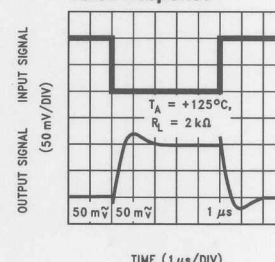
Inverting Large Signal Pulse Response



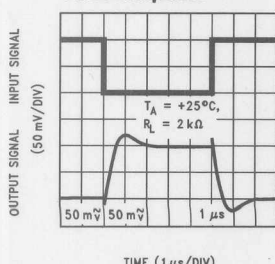
Inverting Large Signal Pulse Response



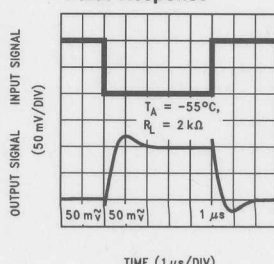
Inverting Small Signal Pulse Response



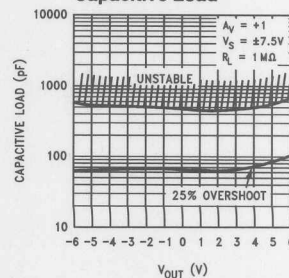
Inverting Small Signal Pulse Response



Inverting Small Signal Pulse Response

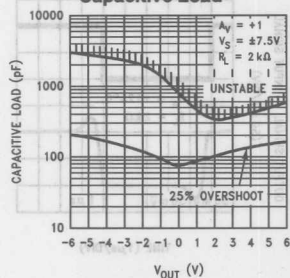
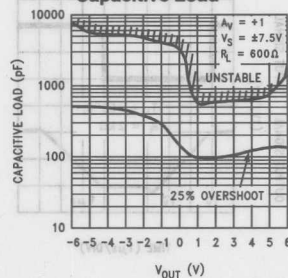
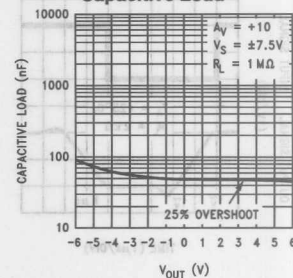
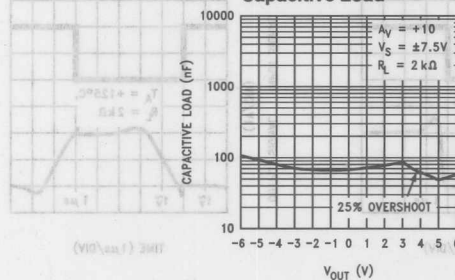
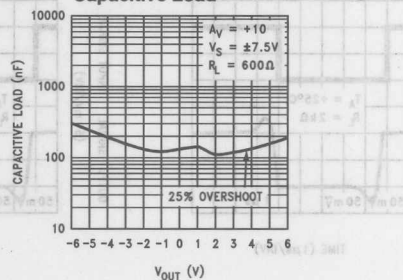


Stability vs Capacitive Load

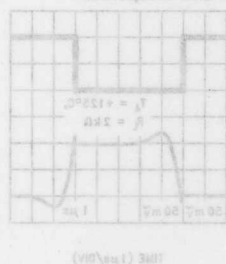
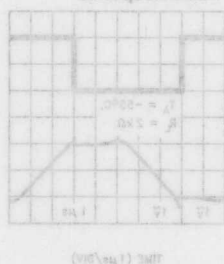
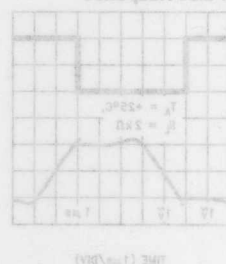
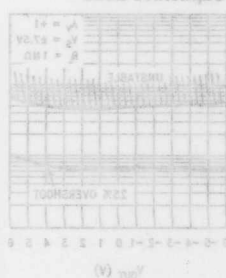
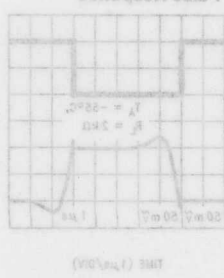
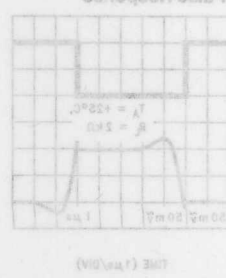


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Typical Performance Characteristics

 $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)Stability vs
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Capacitive Load

Application Information (Continued)

1.0 Amplifier Topology

The LMC6484 incorporates specially designed wide-compliance range current mirrors and the body effect to extend input common mode range to each supply rail. Complementary paralleled differential input stages, like the type used in other CMOS and bipolar rail-to-rail input amplifiers, were not used because of their inherent accuracy problems due to CMRR, cross-over distortion, and open-loop gain variation.

The LMC6484's input stage design is complemented by an output stage capable of rail-to-rail output swing even when driving a large load. Rail-to-rail output swing is obtained by taking the output directly from the internal integrator instead of an output buffer stage.

2.0 Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6484 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

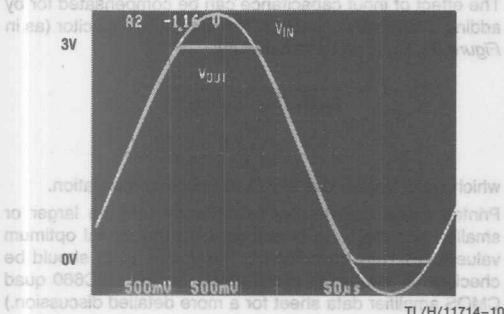


FIGURE 1. An Input Voltage Signal Exceeds the LMC6484 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in Figure 2, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

Application Information (Continued)

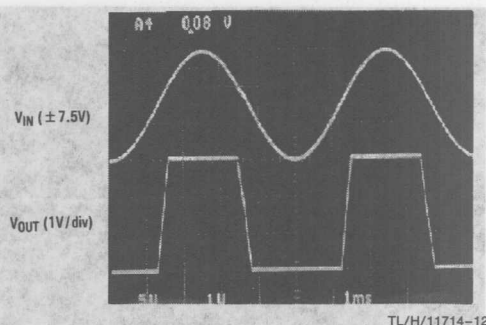


FIGURE 2. A $\pm 7.5V$ Input Signal Greatly Exceeds the 3V Supply in Figure 3 Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor as shown in Figure 3.

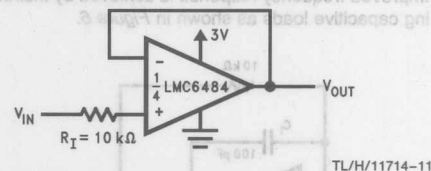


FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 Rail-To-Rail Output

The approximated output resistance of the LMC6484 is 180Ω sourcing and 130Ω sinking at $V_S = 3V$ and 110Ω sourcing and 83Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

4.0 Capacitive Load Tolerance

The LMC6484 can typically directly drive a 100 pF load with $V_S = 15V$ at unity gain without oscillating. The unity gain follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 4. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

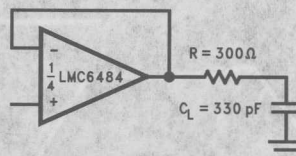
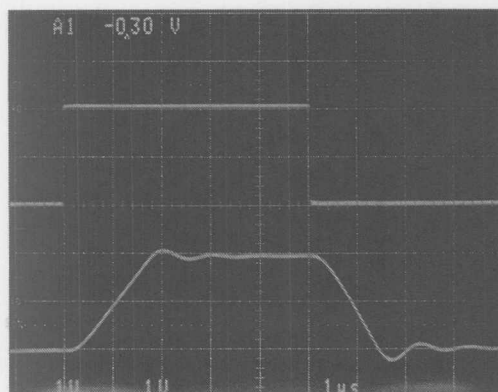


FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

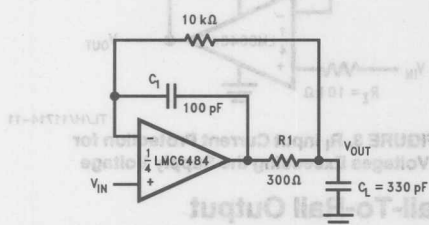
Application Information (Continued)



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FIGURE 5. Pulse Response of the LMC6484 Circuit in Figure 4

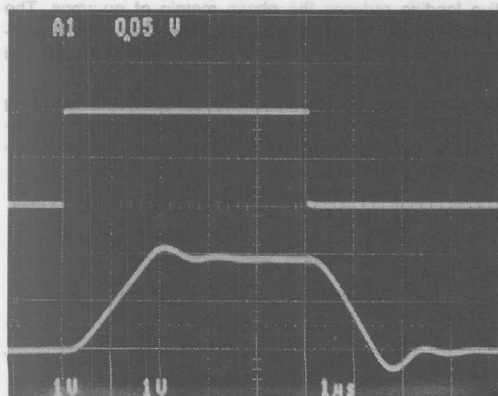
Improved frequency response is achieved by indirectly driving capacitive loads as shown in Figure 6.



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FIGURE 6. LMC6484 Non-Inverting Amplifier, Compensated to Handle a 330 pF Capacitive Load

R1 and C1 serve to counteract the loss of phase margin by feeding forward the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop. The values of R1 and C1 are experimentally determined for the desired pulse response. The resulting pulse response can be seen in Figure 7.

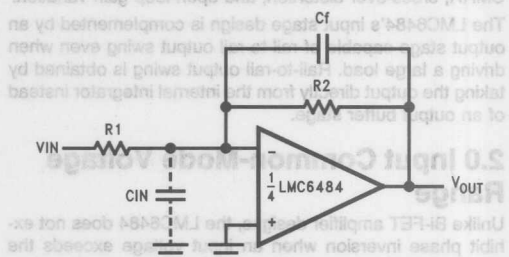


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FIGURE 7. Pulse Response of LMC6484 Circuit in Figure 6

5.0 Compensating for Input Capacitance

It is quite common to use large values of feedback resistance with amplifiers that have ultra-low input current, like the LMC6484. Large feedback resistors can react with small values of input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.



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FIGURE 8. Canceling the Effect of Input Capacitance

The effect of input capacitance can be compensated for by adding a feedback capacitor. The feedback capacitor (as in Figure 8), C_F , is first estimated by:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_F}$$

or

$$R_1 C_{IN} \leq R_2 C_F$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

Application Information (Continued)

6.0 Printed-Circuit-Board Layout 0.8 for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board, when one wishes to take advantage of the ultra-low input current of the LMC6484, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6484's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 9. To have a significant effect, guard rings should be placed in both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6484's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 10a, 10b and 10c for typical connections of guard rings for standard op-amp configurations.

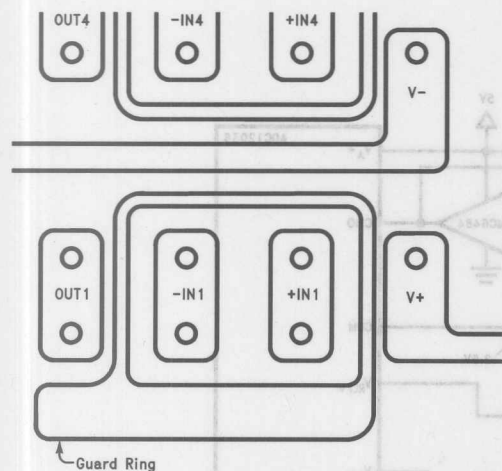


FIGURE 9. Example of Guard Ring in P.C. Board Layout

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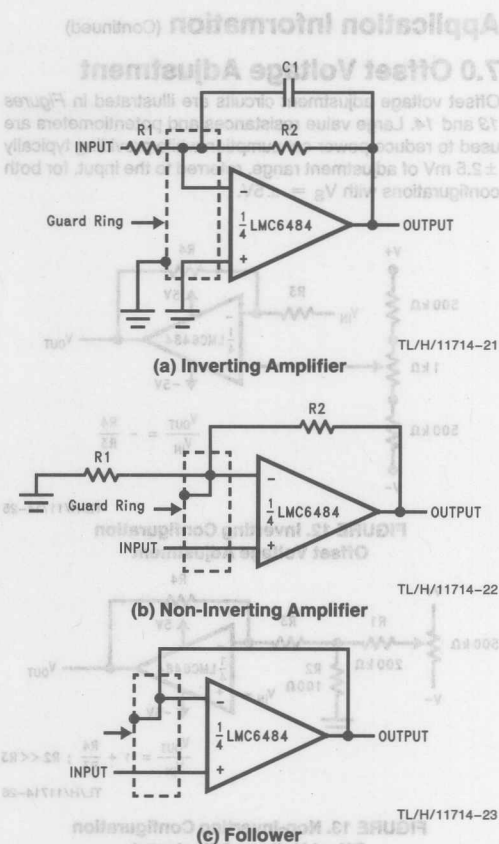
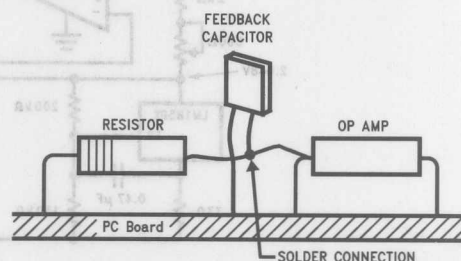


FIGURE 10. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 11.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 11. Air Wiring

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Application Information (Continued)

7.0 Offset Voltage Adjustment

Offset voltage adjustment circuits are illustrated in *Figures 13 and 14*. Large value resistances and potentiometers are used to reduce power consumption while providing typically ± 2.5 mV of adjustment range, referred to the input, for both configurations with $V_S = \pm 5$ V.

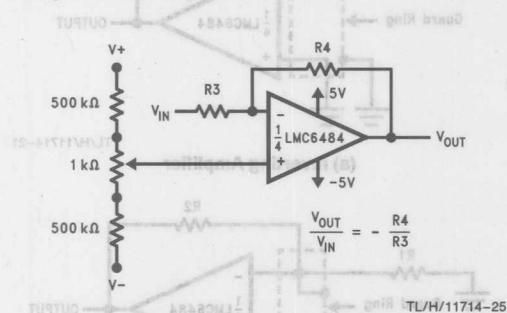


FIGURE 12. Inverting Configuration Offset Voltage Adjustment

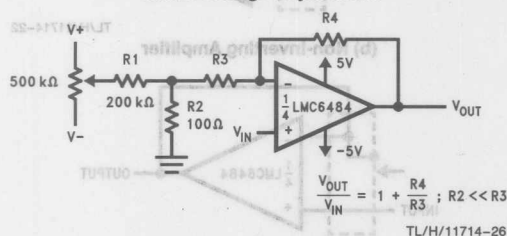


FIGURE 13. Non-Inverting Configuration Offset Voltage Adjustment

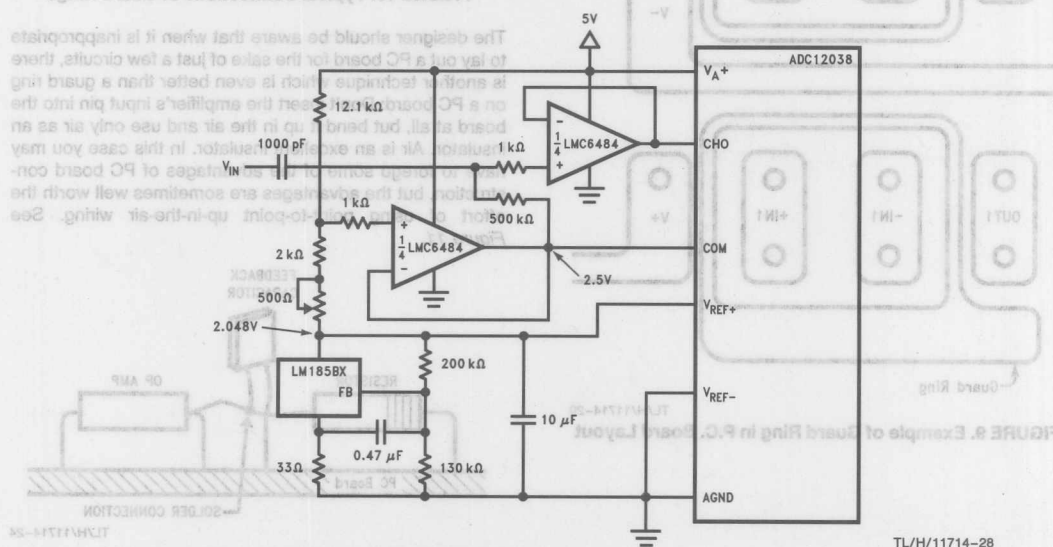


FIGURE 14. Operating from the same Supply Voltage, the LMC6484 buffers the ADC12038 maintaining excellent accuracy

8.0 Upgrading Applications

The LMC6484 quads and LMC6482 duals have industry standard pin outs to retrofit existing applications. System performance can be greatly increased by the LMC6484's features. The key benefit of designing in the LMC6484 is increased linear signal range. Most op-amps have limited input common mode ranges. Signals that exceed this range generate a non-linear output response that persists long after the input signal returns to the common mode range.

Linear signal range is vital in applications such as filters where signal peaking can exceed input common mode ranges resulting in output phase inversion or severe distortion.

9.0 Data Acquisition Systems

Low power, single supply data acquisition system solutions are provided by buffering the ADC12038 with the LMC6484 (*Figure 14*). Capable of using the full supply range, the LMC6484 does not require input signals to be scaled down to meet limited common mode voltage ranges. The LMC6484 CMRR of 82 dB maintains integral linearity of a 12-bit data acquisition system to ± 0.325 LSB. Other rail-to-rail input amplifiers with only 50 dB of CMRR will degrade the accuracy of the data acquisition system to only 8 bits.

Application Information (Continued)

10.0 Instrumentation Circuits

The LMC6484 has the high input impedance, large common-mode range and high CMRR needed for designing instrumentation circuits. Instrumentation circuits designed with the LMC6484 can reject a larger range of common-mode signals than most in-amps. This makes instrumentation circuits designed with the LMC6484 an excellent choice for noisy or industrial environments. Other applications that

benefit from these features include analytic medical instruments, magnetic field detectors, gas detectors, and silicon-based transducers.

A small valued potentiometer is used in series with R_g to set the differential gain of the 3 op-amp instrumentation circuit in *Figure 15*. This combination is used instead of one large valued potentiometer to increase gain trim accuracy and reduce error due to vibration.

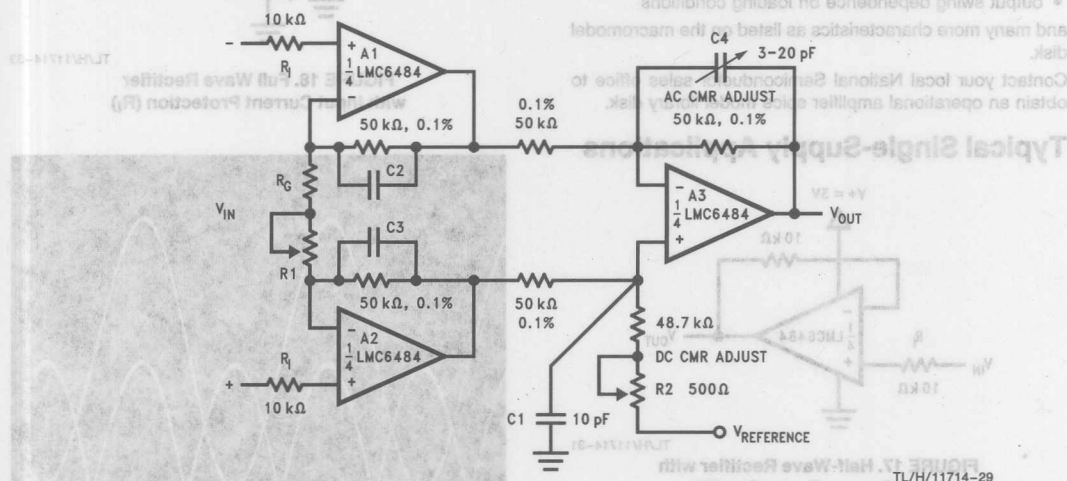


FIGURE 15. Low Power 3 Op-Amp Instrumentation Amplifier

A 2 op-amp instrumentation amplifier designed for a gain of 100 is shown in *Figure 16*. Low sensitivity trimming is made for offset voltage, CMRR and gain. Low cost and low power consumption are the main advantages of this two op-amp circuit.

Higher frequency and larger common-mode range applications are best facilitated by a three op-amp instrumentation amplifier.

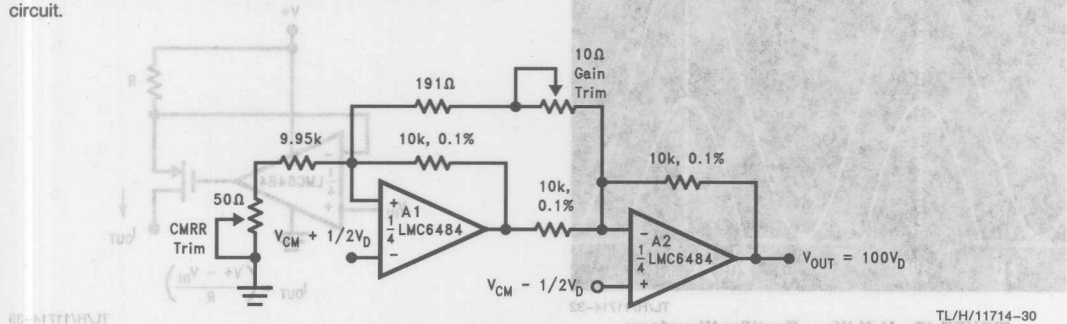


FIGURE 16. Low-Power Two-Op-Amp Instrumentation Amplifier

Application Information (Continued)

11.0 Spice Macromodel

A spice macromodel is available for the LMC6484. This model includes accurate simulation of:

- input common-mode voltage range
- frequency and transient response
- GBW dependence on loading conditions
- quiescent and dynamic supply current
- output swing dependence on loading conditions

and many more characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

Typical Single-Supply Applications

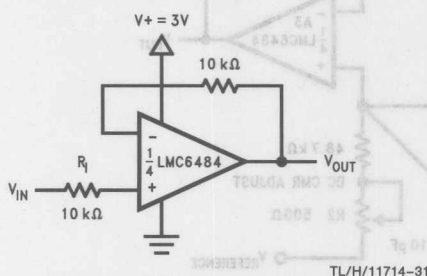


FIGURE 17. Half-Wave Rectifier with Input Current Protection (RI)

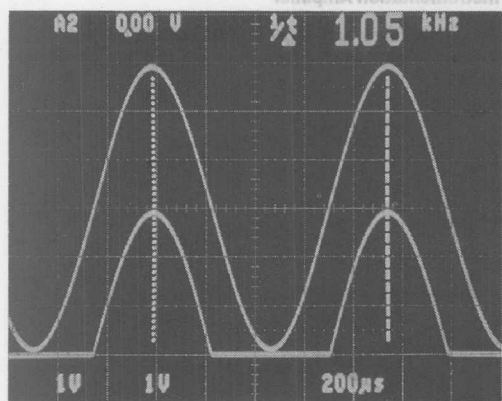


FIGURE 17a. Half-Wave Rectifier Waveform

The circuit in Figure 17 uses a single supply to half wave rectify a sinusoid centered about ground. R_I limits current into the amplifier caused by the input voltage exceeding the supply voltage. Full wave rectification is provided by the circuit in Figure 18.

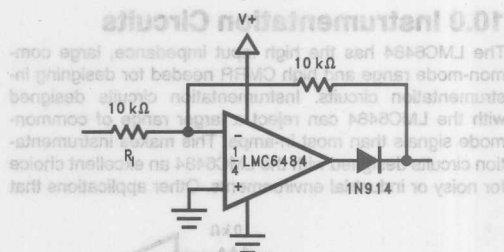


FIGURE 18. Full Wave Rectifier with Input Current Protection (R_I)

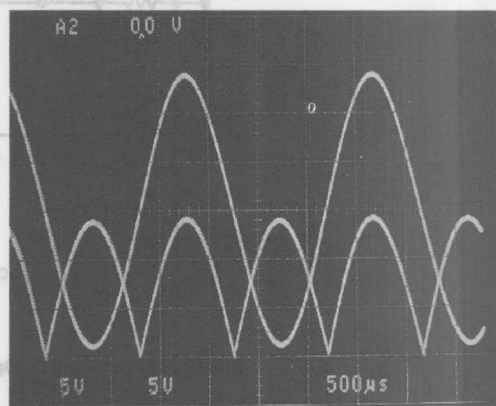


FIGURE 18a. Full Wave Rectifier Waveform

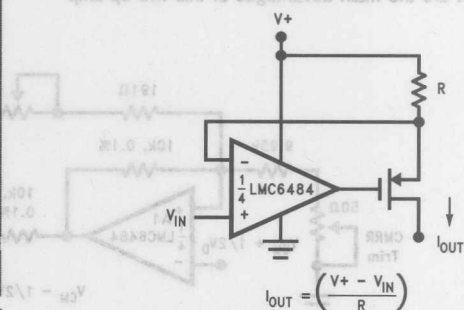


FIGURE 19. Large Compliance Range Current Source

Typical Single-Supply Applications (Continued)

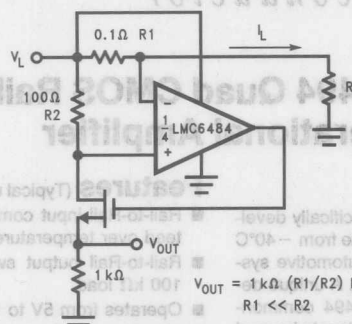


FIGURE 20. Positive Supply Current Sense

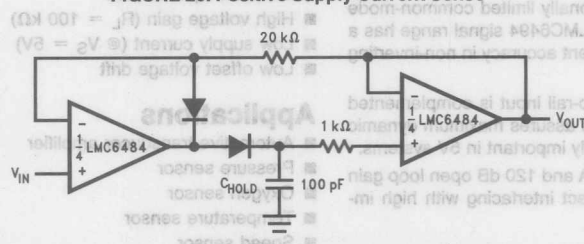


FIGURE 21. Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

In Figure 21 dielectric absorption and leakage is minimized by using a polystyrene or polyethylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. The ultra-low input current of the LMC6484 has a negligible effect on droop.

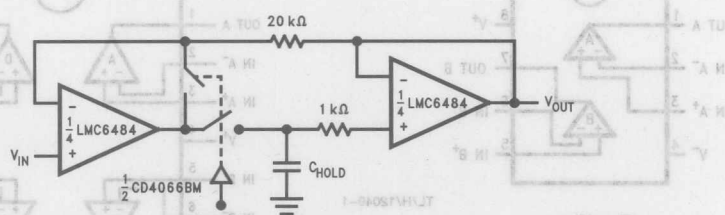


FIGURE 22. Rail-to-Rail Sample and Hold

The LMC6484's high CMRR (85 dB) allows excellent accuracy throughout the circuit's rail-to-rail dynamic capture range.

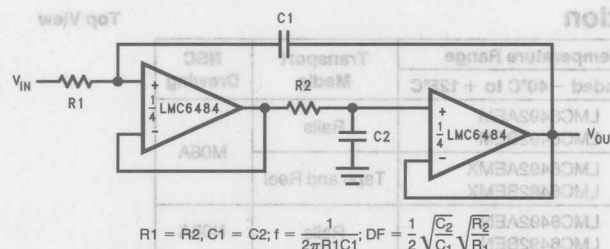
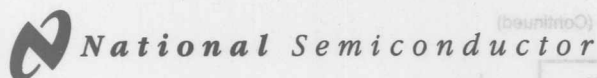


FIGURE 23. Rail-to-Rail Single Supply Low Pass Filter

The low pass filter circuit in Figure 23 can be used as an anti-aliasing filter with the same voltage supply as the A/D converter. Filter designs can also take advantage of the LMC6484 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.



LMC6492 Dual/LMC6494 Quad CMOS Rail-to-Rail Input and Output Operational Amplifier

General Description

The LMC6492/LMC6494 amplifiers were specifically developed for single supply applications that operate from -40°C to $+125^{\circ}\text{C}$. This feature is well-suited for automotive systems because of the wide temperature range. A unique design topology enables the LMC6492/LMC6494 common-mode voltage range to accommodate input signals beyond the rails. This eliminates non-linear output errors due to input signals exceeding a traditionally limited common-mode voltage range. The LMC6492/LMC6494 signal range has a high CMRR of 82 dB for excellent accuracy in non-inverting circuit configurations.

The LMC6492/LMC6494 rail-to-rail input is complemented by rail-to-rail output swing. This assures maximum dynamic signal range which is particularly important in 5V systems.

Ultra-low input current of 150 fA and 120 dB open loop gain provide high accuracy and direct interfacing with high impedance sources.

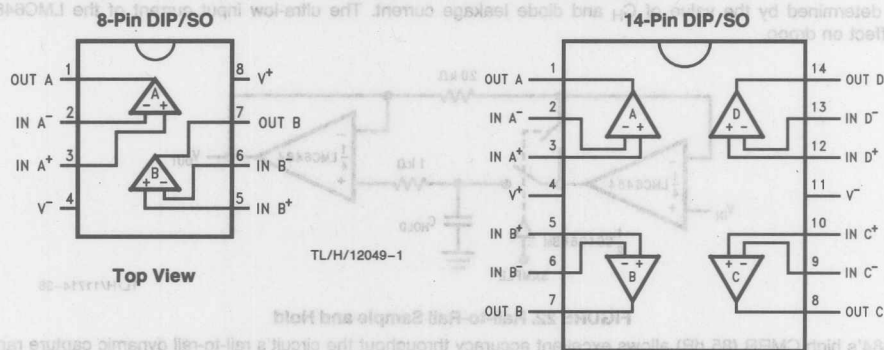
Features (Typical unless otherwise noted)

- Rail-to-Rail input common-mode voltage range, guaranteed over temperature
- Rail-to-Rail output swing within 20 mV of supply rail, 100 k Ω load
- Operates from 5V to 15V supply
- Excellent CMRR and PSRR 82 dB
- Ultra low input current 150 fA
- High voltage gain ($R_L = 100\text{ k}\Omega$) 120 dB
- Low supply current (@ $V_S = 5\text{V}$) 500 μA /Amplifier
- Low offset voltage drift 1.0 $\mu\text{V}/^{\circ}\text{C}$

Applications

- Automotive transducer amplifier
- Pressure sensor
- Oxygen sensor
- Temperature sensor
- Speed sensor

Connection Diagrams



Ordering Information

| Package | Temperature Range | Transport Media | NSC Drawing |
|----------------------|--|-----------------|-------------|
| | Extended -40°C to $+125^{\circ}\text{C}$ | | |
| 8-Pin Small Outline | LMC6492AEM LMC6492BEM | Rails | M08A |
| | LMC6492AEMX LMC6492BEMX | Tape and Reel | |
| 8-Pin Molded DIP | LMC6492AEN LMC6492BEN | Rails | N08A |
| 14-Pin Small Outline | LMC6494AEM LMC6494BEM | Rails | M14A |
| | LMC6494AEMX LMC6494BEMX | Tape and Reel | |
| 14-Pin Molded DIP | LMC6494AEN LMC6494BEN | Rails | N14A |

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------|------------------------------|
| ESD Tolerance (Note 2) | 2000V |
| Differential Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin | $(V^+) + 0.3V, (V^-) - 0.3V$ |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin (Note 3) | ± 30 mA |
| Current at Power Supply Pin | 40 mA |
| Lead Temp. (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

Junction Temperature Range

LMC6492AE, LMC6492BE $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ LMC6494AE, LMC6494BE $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ Thermal Resistance (θ_{JA})

N Package, 8-Pin Molded DIP 108°C/W

M Package, 8-Pin Surface Mount 171°C/W

N Package, 14-Pin Molded DIP 78°C/W

M Package, 14-Pin Surface Mount 118°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{ M}\Omega$.

Boldface limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6492AE LMC6494AE Limit (Note 6) | LMC6492BE LMC6494BE Limit (Note 6) | Units |
|------------|--|---|-----------------|---|---|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.11 | 3.0 3.8 | 6.0 6.8 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.0 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | (Note 11) | 0.15 | 200 | 200 | pA max |
| I_{OS} | Input Offset Current | (Note 11) | 0.075 | 100 | 100 | pA max |
| R_{IN} | Input Resistance | | > 10 | | | Tera Ω |
| C_{IN} | Common-Mode Input Capacitance | | 3 | | | pF |
| CMRR | Common-Mode Rejection Ratio | $0V \leq V_{CM} \leq 15V$ $V^+ = 15V$ | 82 | 65 60 | 63 58 | dB min |
| | | $0V \leq V_{CM} \leq 5V$ | 82 | 65 60 | 63 58 | |
| +PSRR | Positive Power Supply Rejection Ratio | $5V \leq V^+ \leq 15V$, $V_O = 2.5V$ | 82 | 65 60 | 63 58 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $0V \leq V^- \leq -10V$, $V_O = 2.5V$ | 82 | 65 60 | 63 58 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5V$ and $15V$ For CMRR ≥ 50 dB | $V^- - 0.3$ | -0.25 0 | -0.25 0 | V max |
| | | | $V^+ + 0.3$ | $V^+ + 0.25$ V^+ | $V^+ + 0.25$ V^+ | V min |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ Sourcing (Note 7) Sinking | 300 | | | V/mV min |
| | | | 40 | | | |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes (Continued)

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6492AE LMC6494AE Limit (Note 6) | LMC6492BE LMC6494BE Limit (Note 6) | Units |
|------------|------------------------------|--|-----------------|---|---|------------|
| V_O | Output Swing | $V^+ = 5\text{V}$ $R_L = 2\text{k}\Omega$ to $V^+/2$ | 4.9 | 4.8 4.7 | 4.8 4.7 | V_{\min} |
| | | | 0.1 | 0.18 0.24 | 0.18 0.24 | V_{\max} |
| | | $V^+ = 5\text{V}$ $R_L = 600\Omega$ to $V^+/2$ | 4.7 | 4.5 4.24 | 4.5 4.24 | V_{\min} |
| | | | 0.3 | 0.5 0.65 | 0.5 0.65 | V_{\max} |
| | | $V^+ = 15\text{V}$ $R_L = 2\text{k}\Omega$ to $V^+/2$ | 14.7 | 14.4 14.0 | 14.4 14.0 | V_{\min} |
| | | | 0.16 | 0.35 0.5 | 0.35 0.5 | V_{\max} |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 25 | 16 10 | 16 10 | mA |
| | | $V^+ = 5\text{V}$ | 22 | 11 8 | 11 8 | |
| | | Sinking, $V_O = 5\text{V}$ | | | | |
| | | | | | | |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 30 | 28 20 | 28 20 | mA |
| | | $V^+ = 15\text{V}$ | | | | |
| | | Sinking, $V_O = 5\text{V}$ (Note 8) | 30 | 30 22 | 30 22 | |
| | | | | | | |
| I_S | Supply Current | LMC6492 | 1.0 | 1.75 2.1 | 1.75 2.1 | mA |
| | | $V^+ = +5\text{V}$, $V_O = V^+/2$ | | | | |
| | | LMC6492 | 1.3 | 1.95 2.3 | 1.95 2.3 | |
| | | $V^+ = +15\text{V}$, $V_O = V^+/2$ | | | | |
| | | LMC6494 | 2.0 | 3.5 4.2 | 3.5 4.2 | |
| | | $V^+ = +5\text{V}$, $V_O = V^+/2$ | | | | |
| V_{\min} | Large Signal Voltage Gain | $R_L = 2\text{k}\Omega$ Sourcing (Note 7) | 40 | | | V/mV |
| | | $R_L = 2\text{k}\Omega$ Sinking | 300 | | | |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6492AE LMC6494AE Limit (Note 6) | LMC6492BE LMC6494BE Limit (Note 6) | Units |
|----------|---------------------------------|---|-----------------|---|---|------------------------|
| SR | Slew Rate | (Note 9) | 1.3 | 0.7 0.5 | 0.7 0.5 | $V/\mu\text{s min}$ |
| GBW | Gain-Bandwidth Product | $V^+ = 15\text{V}$ | 1.5 | | | MHz |
| ϕ_m | Phase Margin | | 50 | | | Deg |
| G_m | Gain Margin | | 15 | | | dB |
| | Amp-to-Amp Isolation | (Note 10) | 150 | | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ $V_{CM} = 1\text{V}$ | 37 | | | $\frac{nV}{\sqrt{Hz}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 0.06 | | | $\frac{pA}{\sqrt{Hz}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 1\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = -4.1\text{ V}_{pp}$ | 0.01 | | | % |
| | | $F = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 8.5\text{ V}_{pp}$ $V^+ = 10\text{V}$ | 0.01 | | | |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

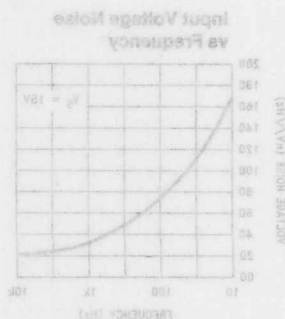
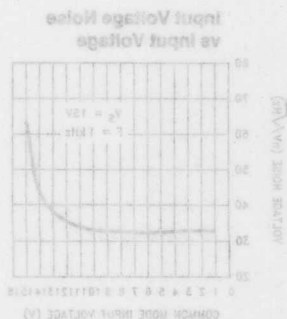
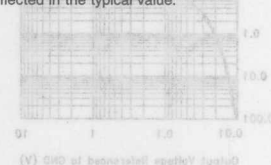
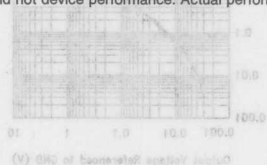
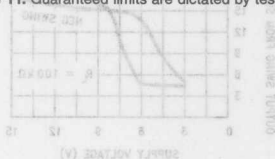
Note 7: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $3.5\text{V} \leq V_O \leq 7.5\text{V}$.

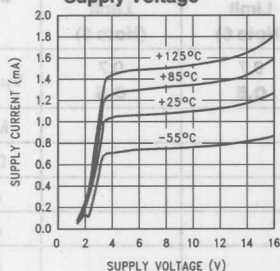
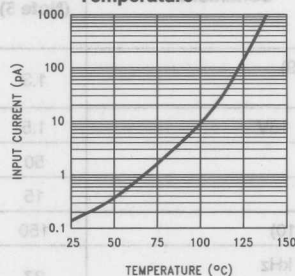
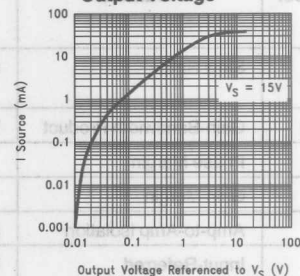
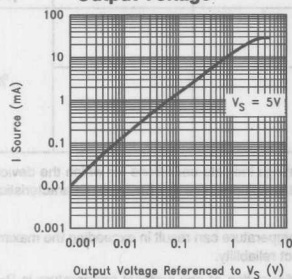
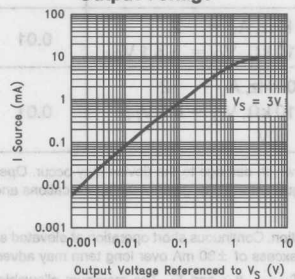
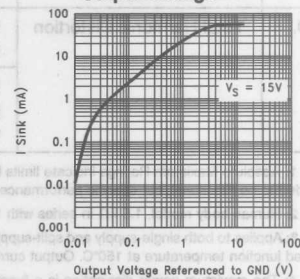
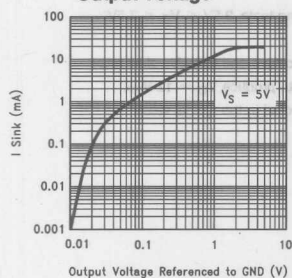
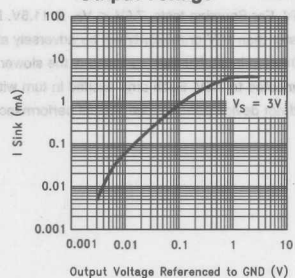
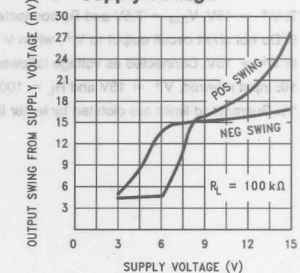
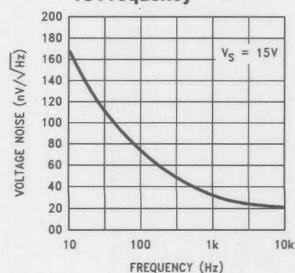
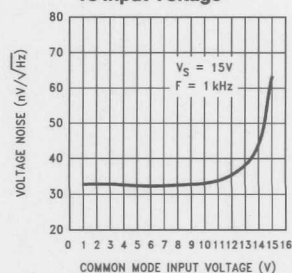
Note 8: Do not short circuit output to V^+ , when V^+ is greater than 13V or reliability will be adversely affected.

Note 9: $V^+ = 15\text{V}$, Connected as voltage follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

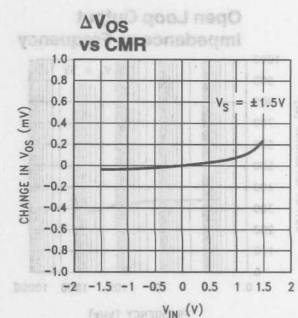
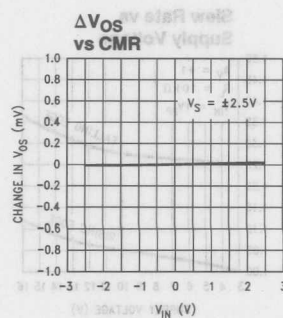
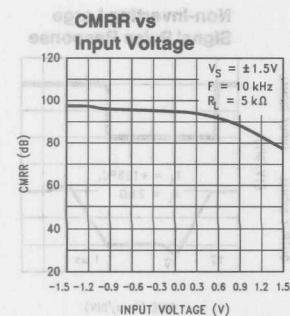
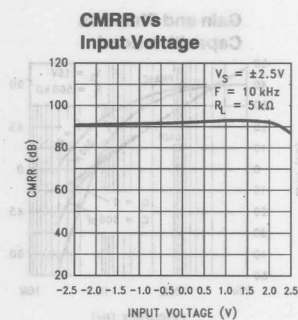
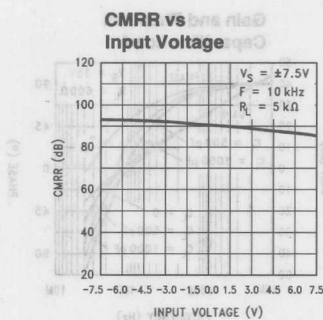
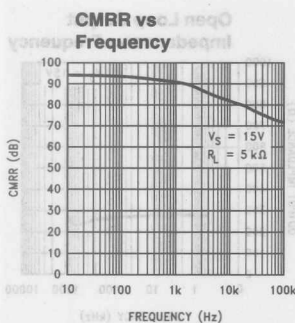
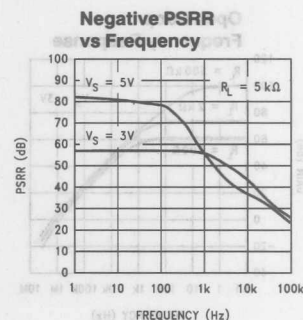
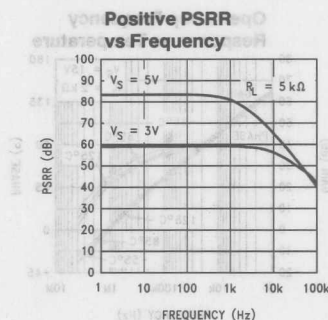
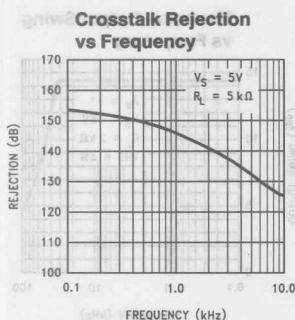
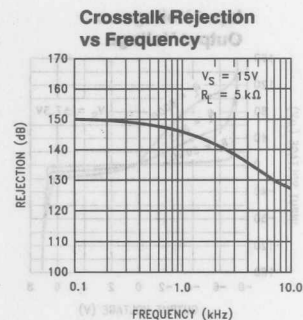
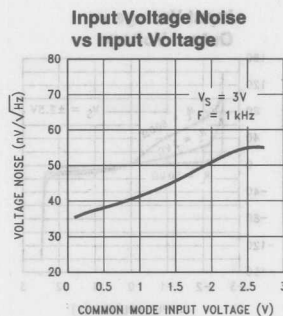
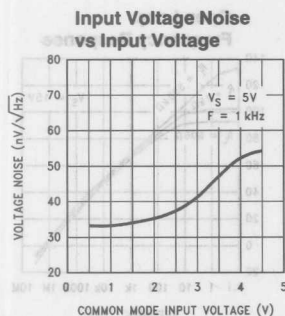
Note 10: Input referred, $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to 7.5V . Each amp excited in turn with 1 kHz to produce $V_O = 12\text{ V}_{pp}$.

Note 11: Guaranteed limits are dictated by tester limits and not device performance. Actual performance is reflected in the typical value.



Supply Current vs
Supply VoltageInput Current vs
TemperatureSourcing Current vs
Output VoltageSourcing Current vs
Output VoltageSourcing Current vs
Output VoltageSinking Current vs
Output VoltageSinking Current vs
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Output VoltageOutput Voltage Swing vs
Supply VoltageInput Voltage Noise
vs FrequencyInput Voltage Noise
vs Input Voltage

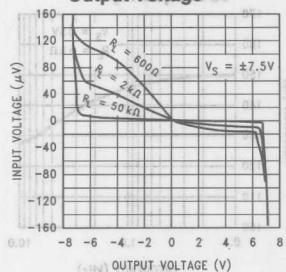
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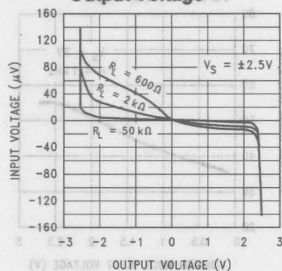
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

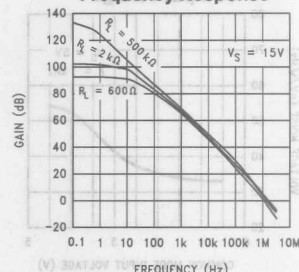
Input Voltage vs Output Voltage



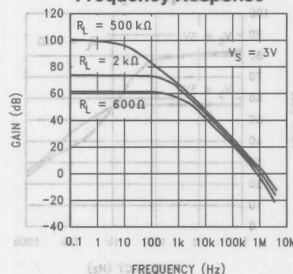
Input Voltage vs Output Voltage



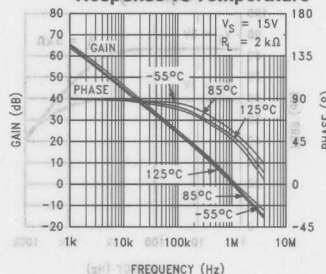
Open Loop Frequency Response



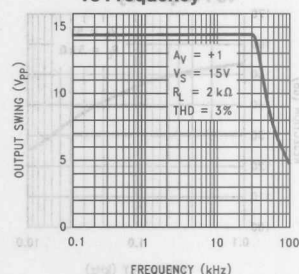
Open Loop Frequency Response



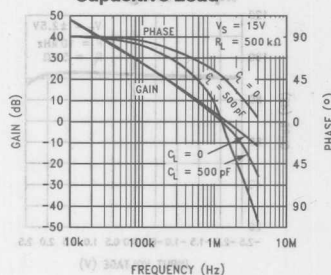
Open Loop Frequency Response vs Temperature



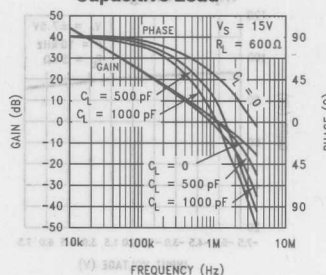
Maximum Output Swing vs Frequency



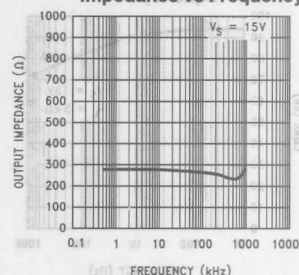
Gain and Phase vs Capacitive Load



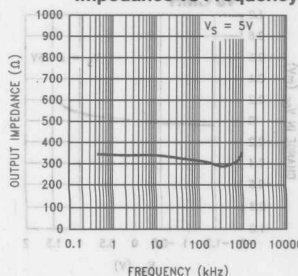
Gain and Phase vs Capacitive Load



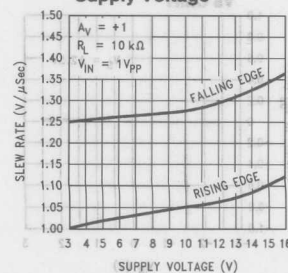
Open Loop Output Impedance vs Frequency



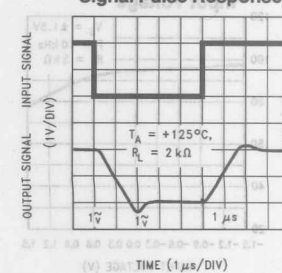
Open Loop Output Impedance vs Frequency



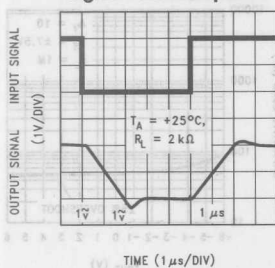
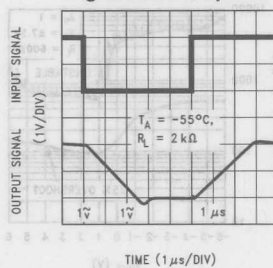
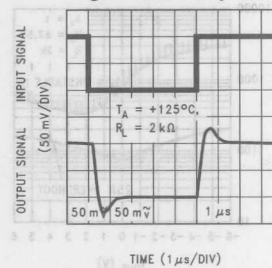
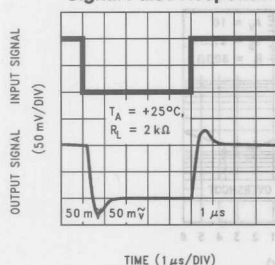
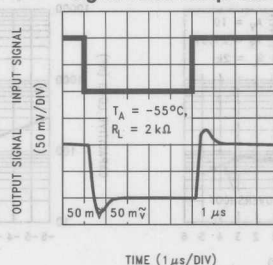
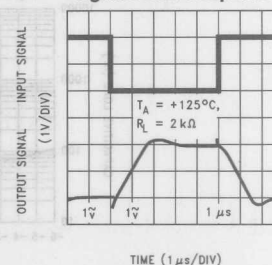
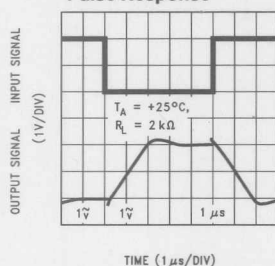
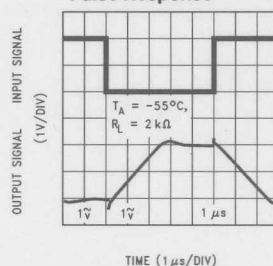
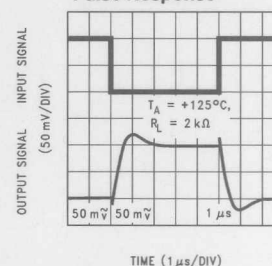
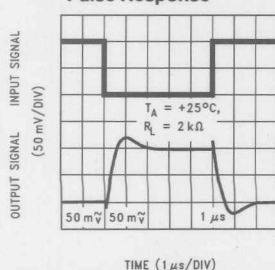
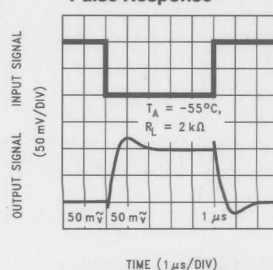
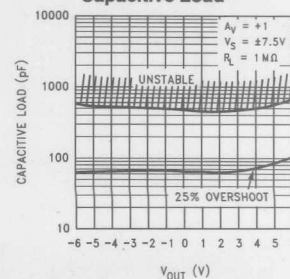
Slew Rate vs Supply Voltage



Non-Inverting Large Signal Pulse Response



Typical Performance Characteristics

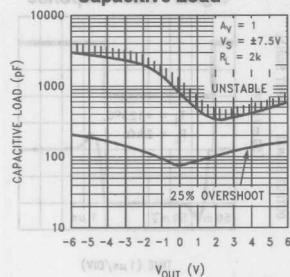
 $V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)Non-Inverting Large
Signal Pulse ResponseNon-Inverting Large
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Pulse ResponseInverting Small Signal
Pulse ResponseStability vs
Capacitive Load

TL/H/12049-6

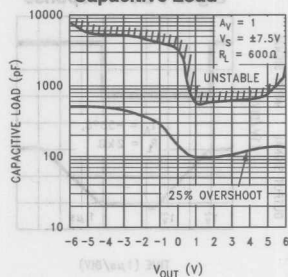
Typical Performance Characteristics

$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless otherwise specified (Continued)

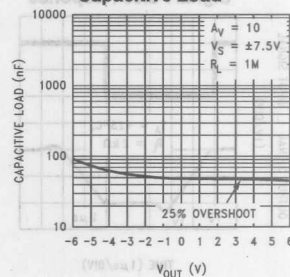
Stability vs Capacitive Load



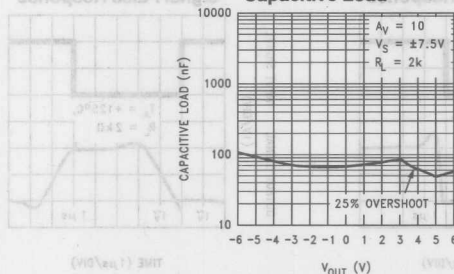
Stability vs Capacitive Load



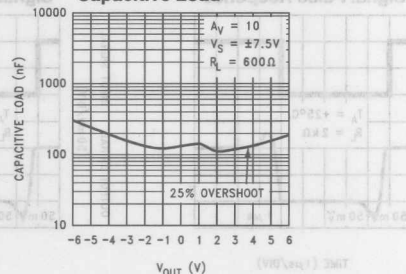
Stability vs Capacitive Load



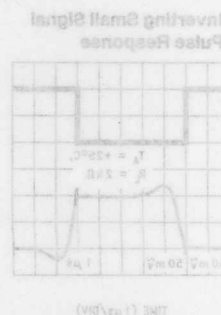
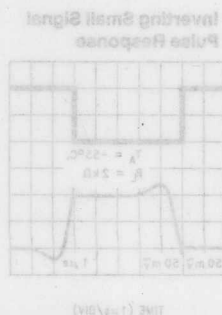
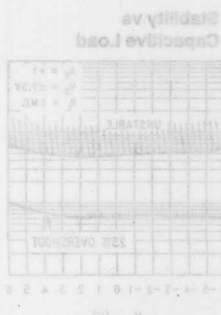
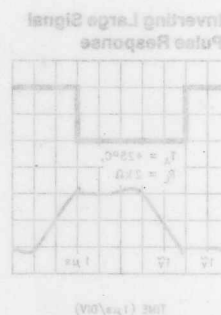
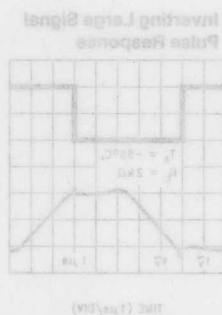
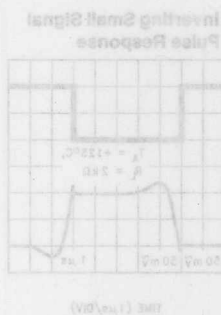
Stability vs Capacitive Load



Stability vs Capacitive Load



TL/H/12049-7



Input Common-Mode Voltage Range

Unlike Bi-FET amplifier designs, the LMC6492/4 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. *Figure 1* shows an input voltage exceeding both supplies with no resulting phase inversion on the output.

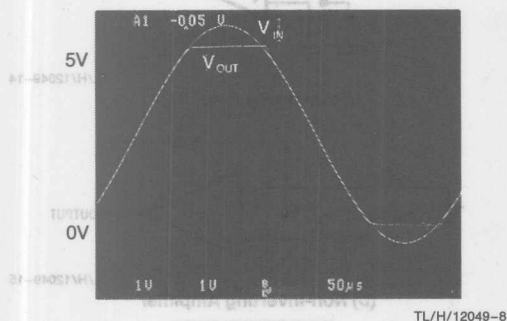


FIGURE 1. An Input Voltage Signal Exceeds the LMC6492/4 Power Supply Voltages with No Output Phase Inversion

The absolute maximum input voltage is 300 mV beyond either supply rail at room temperature. Voltages greatly exceeding this absolute maximum rating, as in *Figure 2*, can cause excessive current to flow in or out of the input pins possibly affecting reliability.

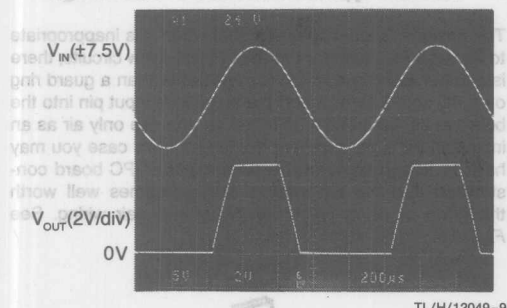


FIGURE 2. A $\pm 7.5V$ Input Signal Greatly Exceeds the 5V Supply in *Figure 3* Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor (R_I) as shown in *Figure 3*.

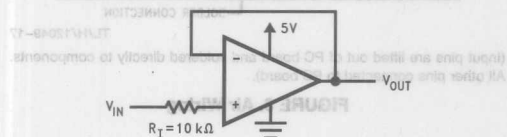


FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltages

Rail-to-Rail Output

The approximate output resistance of the LMC6492/4 is 110Ω sourcing and 80Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

Compensating for Input Capacitance

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6492/4.

Although the LMC6492/4 is highly stable over a wide range of operating conditions, certain precautions must be met to achieve the desired pulse response when a large feedback resistor is used. Large feedback resistors with even small values of input capacitance, due to transducers, photodiodes, and circuit board parasitics, reduce phase margins.

When high input impedances are demanded, guarding of the LMC6492/4 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

The effect of input capacitance can be compensated for by adding a capacitor, C_I , around the feedback resistors (as in *Figure 4*) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_I}$$

or

$$R_1 C_{IN} \leq R_2 C_I$$

Since it is often difficult to know the exact value of C_{IN} , C_I can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

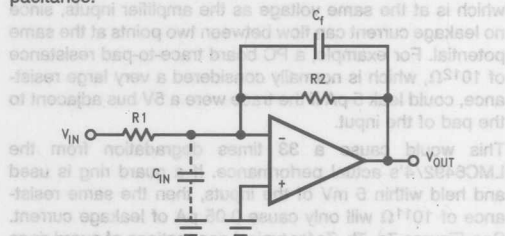


FIGURE 4. Cancelling the Effect of Input Capacitance

Capacitive Load Tolerance

All rail-to-rail output swing operational amplifiers have voltage gain in the output stage. A compensation capacitor is normally included in this integrator stage. The frequency location of the dominant pole is affected by the resistive load on the amplifier. Capacitive load driving capability can be optimized by using an appropriate resistive load in parallel with the capacitive load (see *Typical Curves*).

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in *Figure 5*.

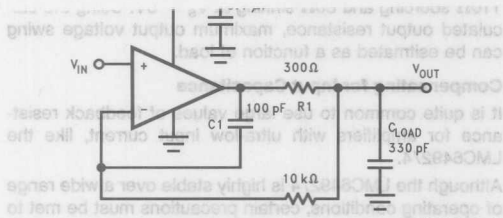


FIGURE 5. LMC6492/4 Noninverting Amplifier, Compensated to Handle Capacitive Loads

Printed-Circuit-Board Layout for High-Impedance Work

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6492/4, typically 150 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6492/4's inputs and the terminals of components connected to the op-amp's inputs, as in Figure 6. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{11} \Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input.

This would cause a 33 times degradation from the LMC6492/4's actual performance. If a guard ring is used and held within 5 mV of the inputs, then the same resistance of $10^{11} \Omega$ will only cause 0.05 pA of leakage current. See Figures 7a, 7b, 7c for typical connections of guard rings for standard op-amp configurations.

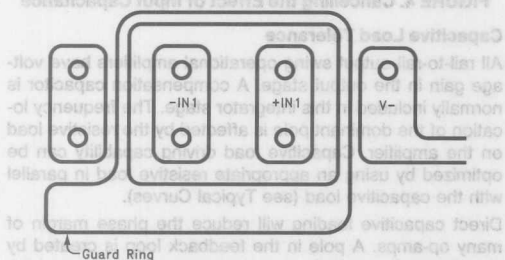
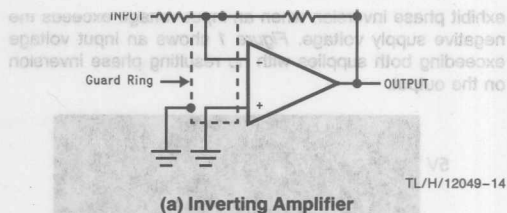
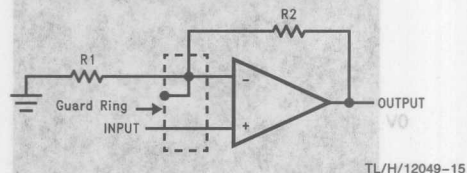


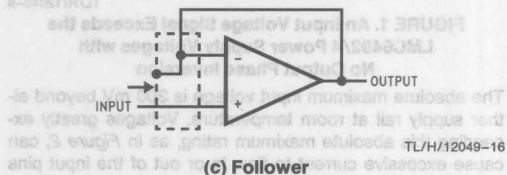
FIGURE 6. Examples of Guard Ring in PC Board Layout



(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower

FIGURE 7. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 8.

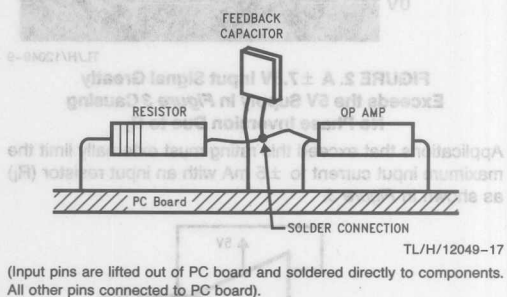
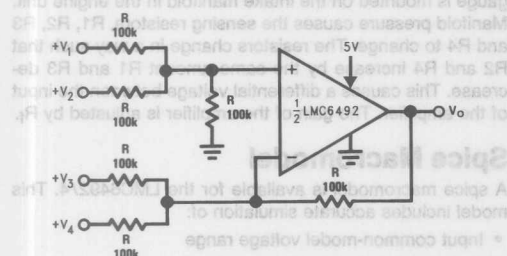


FIGURE 8. Air Wiring

Application Circuits

DC Summing Amplifier

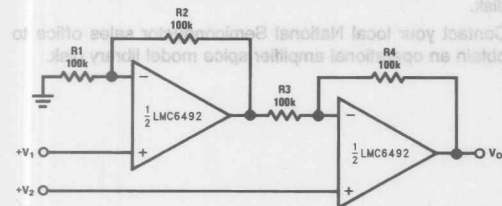
($V_{IN} \geq 0V_{DC}$ and $V_O \geq V_{DC}$)



Where: $V_O = V_1 + V_2 - V_3 - V_4$ TL/H/12049-18

($V_1 + V_2 \geq (V_3 + V_4)$ to keep $V_O > 0V_{DC}$)

High Input Z, DC Differential Amplifier



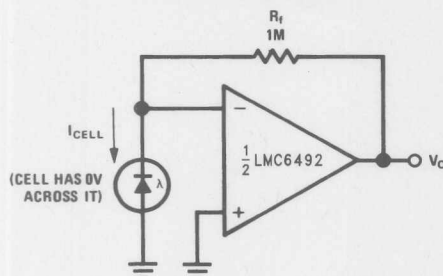
TL/H/12049-19

For $\frac{R_1}{R_2} = \frac{R_4}{R_3}$ (CMRR depends on this resistor ratio match)

$$V_O = 1 + \frac{R_4}{R_3} (V_2 - V_1)$$

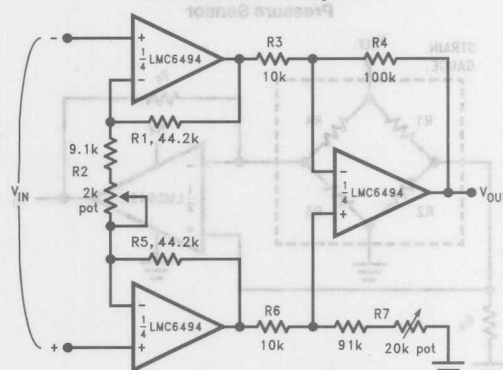
As shown: $V_O = 2(V_2 - V_1)$

Photo Voltaic-Cell Amplifier



TL/H/12049-20

Instrumentation Amplifier



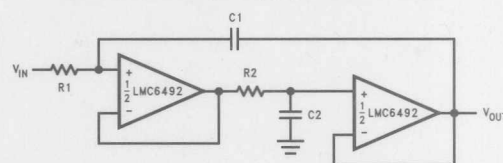
TL/H/12049-21

If $R_1 = R_5$, $R_3 = R_6$, and $R_4 = R_7$; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_2 + 2R_1}{R_2} \times \frac{R_4}{R_3}$$

$\therefore A_v \approx 100$ for circuit shown ($R_2 = 9.3k$).

Rail-to-Rail Single Supply Low Pass Filter

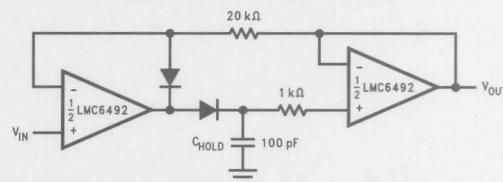


TL/H/12049-22

$$R_1 = R_2, C_1 = C_2; f = \frac{1}{2\pi R_1 C_1}; \text{Damping Factor} = \frac{1}{2} \sqrt{\frac{C_2}{C_1} \frac{R_2}{R_1}}$$

This low-pass filter circuit can be used as an anti-aliasing filter with the same supply as the A/D converter. Filter designs can also take advantage of the LMC6492/4 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller valued capacitors which take less board space and cost less.

Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range

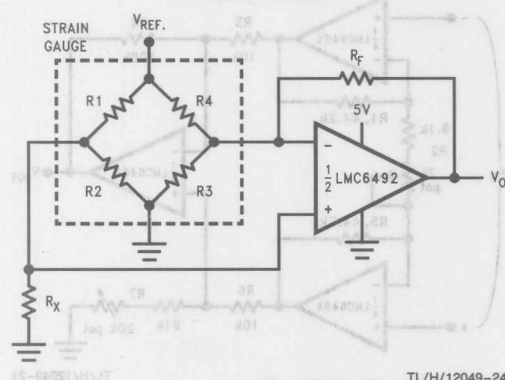


TL/H/12049-23

Dielectric absorption and leakage is minimized by using a polystyrene or polypropylene hold capacitor. The droop rate is primarily determined by the value of C_H and diode leakage current. Select low-leakage current diodes to minimize drooping.

Application Circuits (Continued)

Pressure Sensor

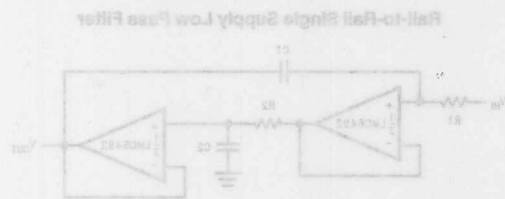


TL/H/12049-24

$$R_f = R_x$$

$$R_f \gg R_1, R_2, R_3, \text{ and } R_4$$

$$V_0 = \left(\frac{R_2}{R_1 + R_2} - \frac{R_3}{R_4 + R_3} \right) \frac{R_f (R_3 + R_4)}{R_3 R_4} V_{REF}$$

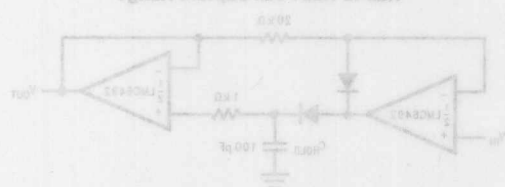


TL/H/12046-22

$$R_1 = R_2, C_1 = C_2, f = \frac{1}{2\pi R_1 C_1} \text{ Damping Factor} = \frac{R_2}{R_1} \frac{C_2}{C_1} \frac{V_1}{V_0}$$

The low-pass filter circuit can be used as an anti-aliasing filter with the same supply as the A/D converter. Filter design also take advantage of the LMC6492/4 ultra-low input current. The ultra-low input current yields negligible offset error even when large value resistors are used. This in turn allows the use of smaller value capacitors which take less board space and cost less.

Low Voltage Peak Detector with Rail-to-Rail Peak Capture Range



TL/H/12048-20

Dielectric absorption and leakage is minimized by using a polyethylene or polypropylene hold capacitor. The drop rate is primarily determined by the value of C_H and diode leakage current. Select low-leakage current diodes to minimize drooping.

Application Circuits

DC Summing Amplifier

In a manifold absolute pressure sensor application, a strain gauge is mounted on the intake manifold in the engine unit. Manifold pressure causes the sensing resistors, R_1 , R_2 , R_3 and R_4 to change. The resistors change in a way such that R_2 and R_4 increase by the same amount R_1 and R_3 decrease. This causes a differential voltage between the input of the amplifier. The gain of the amplifier is adjusted by R_f .

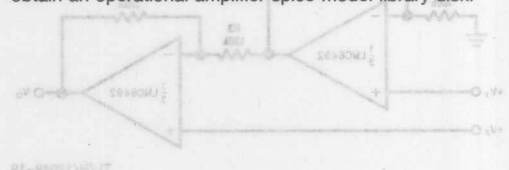
Spice Macromodel

A spice macromodel is available for the LMC6492/4. This model includes accurate simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions

and many other characteristics as listed on the macromodel disk.

Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.



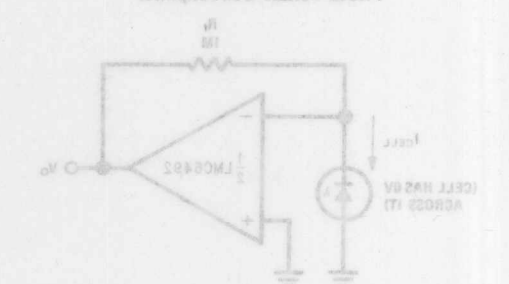
TL/H/12048-19

$$R_{or} \frac{R_1}{R_2} = \frac{R_1}{R_2} \text{ (CMRR depends on this resistor ratio match)}$$

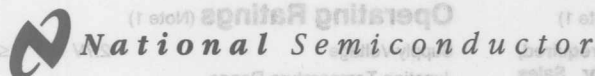
$$V_0 = 1 + \frac{R_1}{R_2} (V_2 - V_1)$$

$$\text{As shown: } V_0 = 2(V_2 - V_1)$$

Photo-Voltaic Cell Amplifier



TL/H/12048-20



LMC6574 Quad/LMC6572 Dual Low Voltage (2.7V and 3V) Operational Amplifier

General Description

Low voltage operation and low power dissipation make the LMC6574/2 ideal for battery-powered systems.

3V amplifier performance is backed by 2.7V guarantees to ensure operation throughout battery lifetime. These guarantees also enable analog circuits to operate from the same 3.3V supply used for digital logic.

Battery life is maximized because each amplifier dissipates only micro-watts of power.

The LMC6574/2 does not sacrifice functionality for low voltage operation. The LMC6574/2 generates 120 dB of open-loop gain just like a conventional amplifier, but the LMC6574/2 can do this from a 2.7V supply.

These amplifiers are designed with features that optimize low voltage operation. The output voltage swings rail-to-rail to maximize signal-to-noise ratio and dynamic signal range. The common-mode input voltage range extends from 800 mV below the positive supply to 100 mV below ground.

This device is built with National's advanced Double-Poly Silicon-Gate CMOS process.

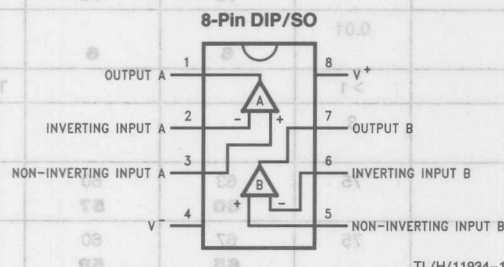
Features (Typical unless otherwise noted)

- Guaranteed 2.7V and 3V Performance
- Rail-to-Rail Output Swing (within 5 mV of supply rail, 100 k Ω load)
- Ultra-Low Supply Current 40 μ A/Amplifier
- Low Cost
- Ultra-Low Input Current 20 fA
- High Voltage Gain @ $V_S = 2.7V$, $R_L = 100$ k Ω 120 dB
- Specified for 100 k Ω and 5 k Ω loads

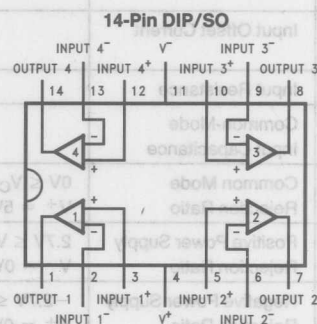
Applications

- Transducer Amplifier
- Portable or Remote Equipment
- Battery-Operated Instruments
- Data Acquisition Systems
- Medical Instrumentation
- Improved Replacement for TLV2322 and TLV2324

Connection Diagrams



Order Number LMC6572AIN, LMC6572BIN,
LMC6572AIM or LMC6572BIM
See NS Package Number N08E or M08A



Order Number LMC6574AIN, LMC6574BIN,
LMC6574AIM or LMC6574BIM
See NS Package Number N14A or M14A

Ordering Information

| Package | Temperature Range Industrial, -40°C to +85°C | NSC Drawing | Transport Media |
|----------------------|---|-------------|-----------------|
| 8-Pin Molded DIP | LMC6572AIN, LMC6572BIN | N08E | Rail |
| 8-Pin Small Outline | LMC6572AIM, LMC6572BIM | M08A | Rail |
| | LMC6572AIMX, LMC6572BIMX | | Tape and Reel |
| 14-Pin Molded DIP | LMC6574AIN, LMC6574BIN | N14A | Rail |
| 14-Pin Small Outline | LMC6574AIM, LMC6574BIM | M14A | Rail |
| | LMC6574AIMX, LMC6574BIMX | | Tape and Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|---|
| ESD Tolerance (Note 2) | 2000V |
| Differential Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin | (V ⁺) + 0.3V, (V ⁻) - 0.3V |
| Supply Voltage (V ⁺ - V ⁻) | 12V |
| Current at Input Pin | \pm 5 mA |
| Current at Output Pin (Note 3) | \pm 10 mA |
| Current at Power Supply Pin | 35 mA |
| Lead Temperature (Soldering, 10 Seconds) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

2.7V DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. V⁺ = 2.7V, V⁻ = 0V, V_{CM} = V_O = V⁺/2 and R_L > 1M Ω .

Boldface limits apply at the temperature extremes.

Operating Ratings (Note 1)

| | |
|--------------------------------------|--|
| Supply Voltage | 2.7V \leq V ⁺ \leq 11V |
| Junction Temperature Range | |
| LMC6572AI, LMC6572BI | -40°C \leq T _J \leq +85°C |
| LMC6574AI, LMC6574BI | -40°C \leq T _J \leq +85°C |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 115°C/W |
| M Package, 8-Pin Surface Mount | 193°C/W |
| N Package, 14-Pin Molded DIP | 81°C/W |
| M Package, 14-Pin Surface Mount | 126°C/W |

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6574AI LMC6572AI Limit (Note 6) | LMC6574BI LMC6572BI Limit (Note 6) | Units |
|-------------------|--|--|----------------------|--|--|-----------|
| V _{OS} | Input Offset Voltage | V ⁺ = 2.7V and 3V | 0.5 | 3 3.5 | 7 7.5 | mV Max |
| TCV _{OS} | Input Offset Voltage Average Drift | | 1.5 | | | μV/°C |
| I _B | Input Current | | 0.02 | 10 | 10 | pA Max |
| I _{OS} | Input Offset Current | | 0.01 | 6 | 6 | pA Max |
| R _{IN} | Input Resistance | | > 1 | | | Tera Ω |
| C _{IN} | Common-Mode Input Capacitance | | 3 | | | pF |
| CMRR | Common Mode Rejection Ratio | 0V ≤ V _{CM} ≤ 3.5V V ⁺ = 5V | 75 | 63 60 | 60 57 | dB Min |
| + PSRR | Positive Power Supply Rejection Ratio | 2.7V ≤ V ⁺ ≤ 5V, V ⁻ = 0V | 75 | 67 65 | 60 58 | dB Min |
| - PSRR | Negative Power Supply Rejection Ratio | -2.7V ≤ V ⁻ ≤ -5V, V ⁺ = 0V | 83 | 75 73 | 67 65 | dB Min |
| V _{CM} | Input Common-Mode Voltage Range | V ⁺ = 2.7V and 3V for CMRR ≥ 50 dB | -0.1 | -0.05 0 | -0.05 0 | V Max |
| | | | V ⁺ - 0.8 | V ⁺ - 1.0 V ⁺ - 1.3 | V ⁺ - 1.0 V ⁺ - 1.3 | V Min |
| A _v | Large Signal Voltage Gain | R _L = 100 kΩ (Note 7) | Sourcing | 1000 | | V/mV |
| | | | Sinking | 500 | | V/mV |

2.7V DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$ and $R_L > 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6574AI LMC6572AI Limit (Note 6) | LMC6574BI LMC6572BI Limit (Note 6) | Units |
|----------|---------------------------------|--|-----------------|---|---|----------------------|
| V_O | Output Swing | $V^+ = 2.7\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 2.695 | 2.68 2.66 | 2.65 2.62 | V Min |
| | | | 0.005 | 0.03 0.05 | 0.06 0.09 | V Max |
| | | $V^+ = 2.7\text{V}$ $R_L = 5\text{ k}\Omega$ to $V^+/2$ | 2.66 | 2.55 2.45 | 2.45 2.35 | V Min |
| | | | 0.04 | 0.15 0.25 | 0.25 0.35 | V Max |
| | | $V^+ = 3\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+/2$ | 2.995 | 2.98 2.96 | 2.95 2.93 | V Min |
| | | | 0.005 | 0.03 0.05 | 0.06 0.09 | V Max |
| | | $V^+ = 3\text{V}$ $R_L = 5\text{ k}\Omega$ to $V^+/2$ | 2.96 | 2.85 2.75 | 2.75 2.65 | V Min |
| | | | 0.04 | 0.15 0.25 | 0.25 0.35 | V Max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ | 6.0 | 4.0 3.0 | 3.0 2.0 | mA Min |
| | | Sinking, $V_O = 2.7\text{V}$ | 4.0 | 3.0 2.0 | 2.5 1.5 | mA Min |
| I_S | Supply Current | Quad Package $V^+ = +2.7\text{V}$, $V_O = V^+/2$ | 160 | 240 280 | 240 280 | μA Max |
| | | Quad Package $V^+ = +3\text{V}$, $V_O = V^+/2$ | 160 | 240 280 | 240 280 | μA Max |
| | | Dual Package $V^+ = +2.7\text{V}$, $V_O = V^+/2$ | 80 | 120 140 | 120 140 | μA Max |
| | | Dual Package $V^+ = +3\text{V}$, $V_O = V^+/2$ | 80 | 120 140 | 120 140 | μA Max |

Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6574AI LMC6572AI Limit (Note 6) | LMC6574BI LMC6572BI Limit (Note 6) | Units |
|----------|---------------------------------|---|-----------------|---|---|-----------------|
| SR | Slew Rate | $V^+ = 2.7V$ and $3V$ (Note 8) | 90 | 30 10 | 30 10 | V/ms Min |
| GBW | Gain-Bandwidth Product | $V^+ = 3V$ | 0.22 | | | MHz |
| ϕ_m | Phase Margin | | 60 | | | Deg |
| G_m | Gain Margin | | 12 | | | dB |
| | Amp-to-Amp Isolation | (Note 9) | 120 | | | dB |
| e_{nM} | Input-Referred Voltage Noise | $F = 1$ kHz $V_{CM} = 1V$ | 45 | | | nV/ \sqrt{Hz} |
| i_{nM} | Input-Referred Current Noise | $F = 1$ kHz | 0.002 | | | pA/ \sqrt{Hz} |
| T.H.D. | Total Harmonic Distortion | $F = 10$ kHz, $A_V = -2$ $R_L = 10$ k Ω , $V_O = 1.0$ V _{pp} | 0.05 | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

Note 4: The maximum power dissipation is a function of $T_{J(Max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(Max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

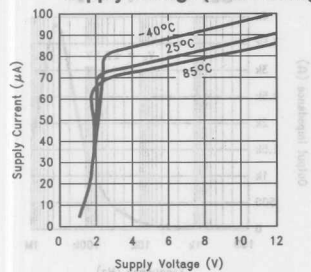
Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 3V$, $V_{CM} = 1.5V$ and R_L connected to 1.5V. For Sourcing tests, $1.5V \leq V_O \leq 2.5V$. For Sinking tests, $0.5V \leq V_O \leq 1.5V$.

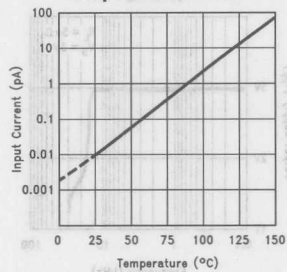
Note 8: Connected as Voltage Follower with 1.0V step input. Number specified is the slower of the positive and negative slew rates.

Note 9: Input referred, $V^+ = 3V$ and $R_L = 100$ k Ω connected to 1.5V. Each amp excited in turn with 1 KHz to produce $V_O = 2$ V_{pp}.

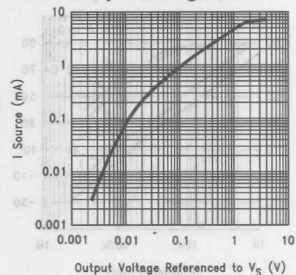
Supply Voltage (Dual Package)



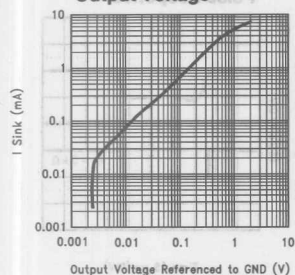
Temperature



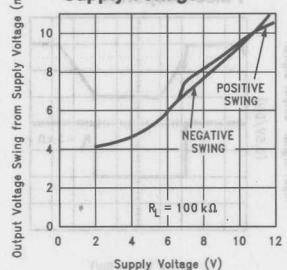
Output Voltage



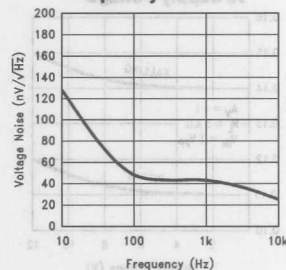
Sinking Current vs Output Voltage



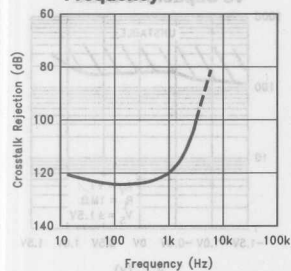
Output Voltage Swing vs Supply Voltage



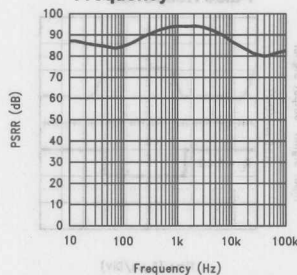
Input Voltage Noise vs Frequency



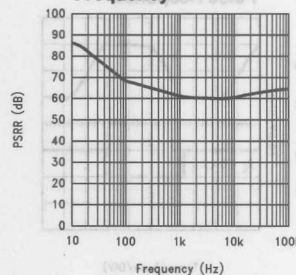
Crosstalk Rejection vs Frequency



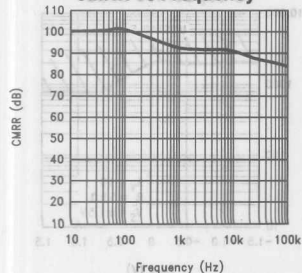
Positive PSRR vs Frequency



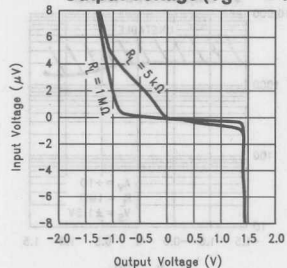
Negative PSRR vs Frequency



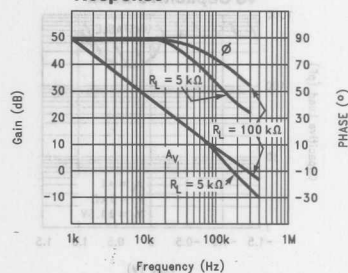
CMRR vs Frequency



Input Voltage vs Output Voltage ($V_S = \pm 1.5$)

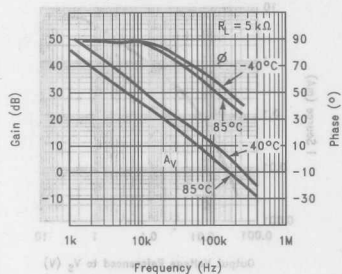


Open Loop Frequency Response

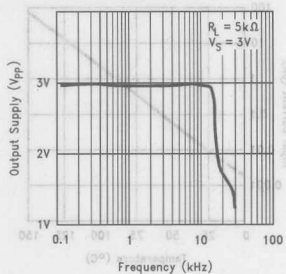


Typical Performance Characteristics (Continued) $V_S = +3V$, $T_A = 25^\circ C$, Unless otherwise specified

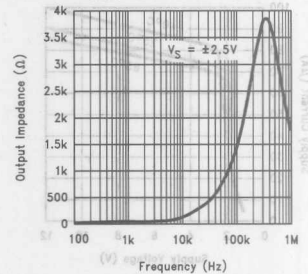
Open Loop Frequency Response vs Temperature



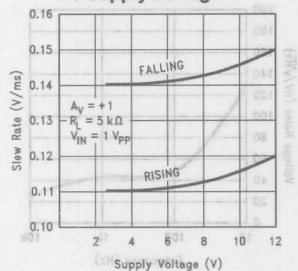
Maximum Output Swing vs Frequency



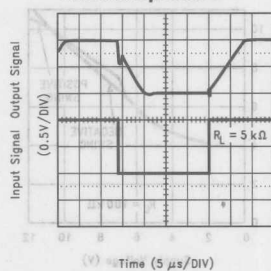
Supply Current vs Frequency



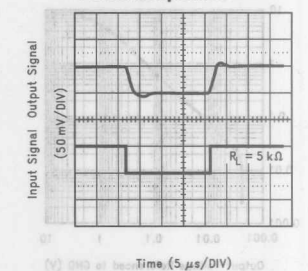
Slew Rate vs Supply Voltage



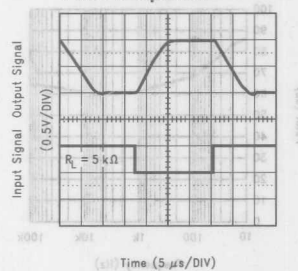
Non-Inverting Large Signal Pulse Response



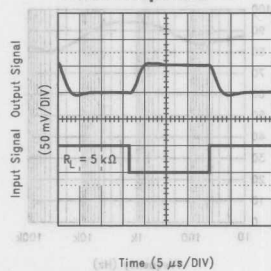
Non-Inverting Small Signal Pulse Response



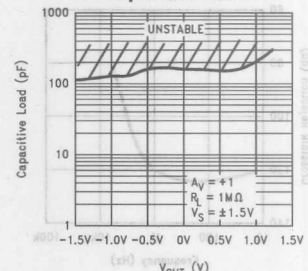
Inverting Large Signal Pulse Response



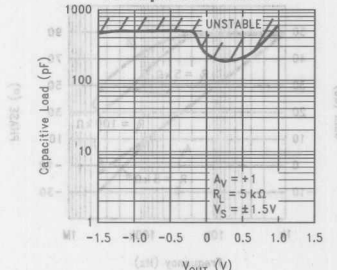
Inverting Small Signal Pulse Response



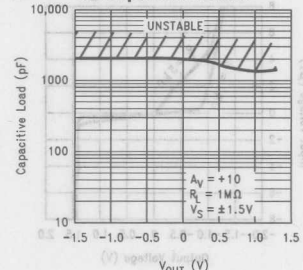
Stability vs Capacitive Load



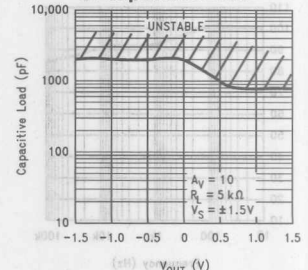
Stability vs Capacitive Load



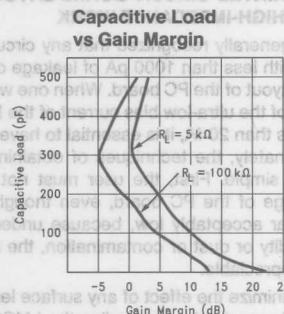
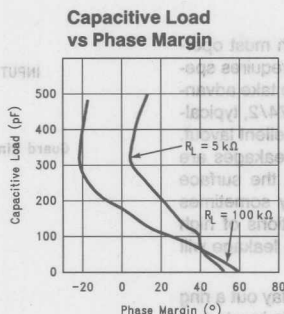
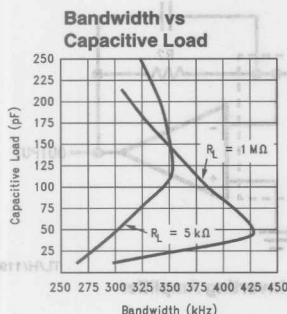
Stability vs Capacitive Load



Stability vs Capacitive Load



Typical Performance Characteristics (Continued) $V_S = +3V$, $T_A = 25^\circ C$, Unless otherwise specified



Applications Hints

1.0 LOW VOLTAGE AMPLIFIER TOPOLOGY

The LMC6574/2 incorporates a novel op-amp design topology that enables it to maintain rail-to-rail output swing even when driving a large load. Instead of relying on a push-pull unity gain output buffer stage, the output stage is taken directly from the internal integrator, which provides both low output impedance and large gain. Special feed-forward compensation design techniques are incorporated to maintain stability over a wider range of operating conditions than traditional micropower op-amps. These features make the LMC6574/2 both easier to design with, and provide higher speed than products typically found in this ultra-low power class.

2.0 COMPENSATING FOR INPUT CAPACITANCE

It is quite common to use large values of feedback resistance for amplifiers with ultra-low input current, like the LMC6574/2.

Although the LMC6574/2 is highly stable over a wide range of operating conditions, a large feedback resistor will react even with small values of capacitance at the input of the op-amp to reduce phase margin. The capacitance at the input of the op-amp comes from transducers, photodiodes and circuit board parasitics.

The effect of input capacitance can be compensated for by adding a capacitor, C_f , around the feedback resistors (as in Figure 1) such that:

$$\frac{1}{2\pi R_1 C_{IN}} \geq \frac{1}{2\pi R_2 C_f}$$

or

$$R_1 C_{IN} \leq R_2 C_f$$

Since it is often difficult to know the exact value of C_{IN} , C_f can be experimentally adjusted so that the desired pulse response is achieved. Refer to the LMC660 and LMC662 for a more detailed discussion on compensating for input capacitance.

When high input impedances are demanded, guarding of the LMC6574/2 is suggested. Guarding input lines will not only reduce leakage, but lowers stray input capacitance as well. (See *Printed-Circuit-Board Layout for High Impedance Work*).

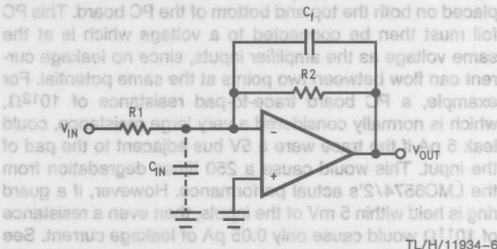


FIGURE 1. Cancelling the Effect of Input Capacitance

3.0 CAPACITIVE LOAD TOLERANCE

Direct capacitive loading will reduce the phase margin of many op-amps. A pole in the feedback loop is created by the combination of the op-amp's output impedance and the capacitive load. This pole induces phase lag at the unity-gain crossover frequency of the amplifier resulting in either an oscillatory or underdamped pulse response. With a few external components, op amps can easily indirectly drive capacitive loads, as shown in Figure 2.

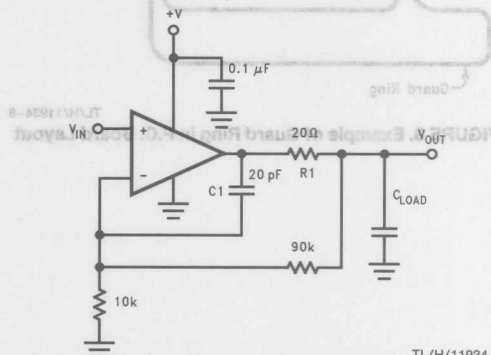


FIGURE 2. LMC6574/2 Noninverting Gain of 10 Amplifier, Compensated to Handle Capacitive Loads

In the circuit of Figure 2, R_1 and C_1 serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

Applications Hints (Continued)

4.0 PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC6574/2, typically less than 20 fA, it is essential to have an excellent layout. Fortunately, the techniques of obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC6574/2's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs, as in Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of the input. This would cause a 250 times degradation from the LMC6574/2's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations.

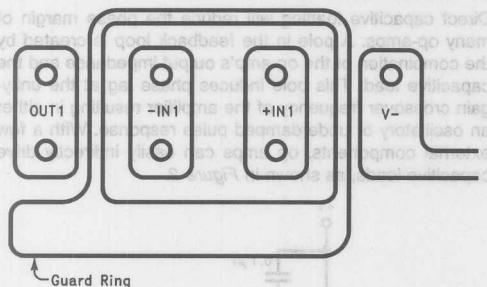
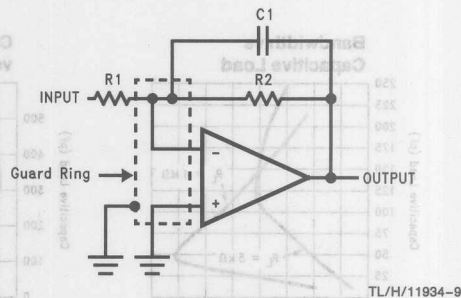
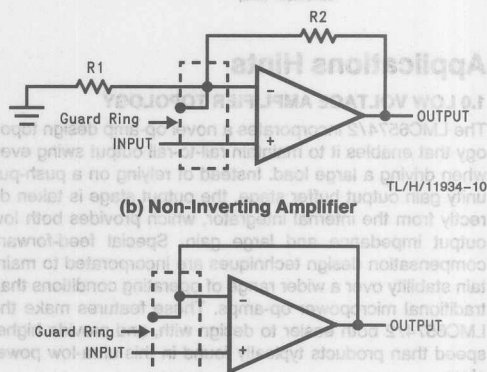


FIGURE 3. Example of Guard Ring in P.C. Board Layout

TL/H/11934-8



(a) Inverting Amplifier



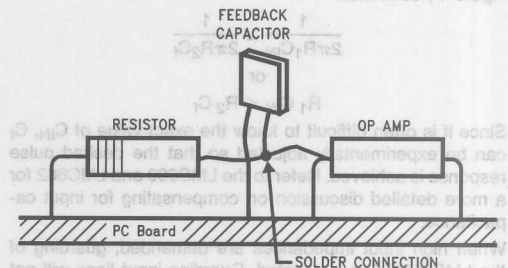
(b) Non-Inverting Amplifier

(c) Follower

TL/H/11934-11

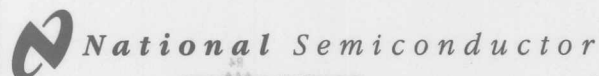
FIGURE 4. Typical Connections of Guard Rings

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board).

FIGURE 5. Air Wiring



LMC6582 Dual/LMC6584 Quad Low Voltage, Rail-To-Rail Input and Output CMOS Operational Amplifier

General Description

The LMC6582/4 is a high performance operational amplifier which can operate over a wide range of supply voltages, from 1.8V to 10V. It has guaranteed specs at 1.8V, 2.2V, 3V, 5V, and 10V.

The LMC6582/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high open-loop voltage gain makes it unique among rail-to-rail CMOS amplifiers. The LMC6582/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6582/4 has been designed specifically to improve system performance in low voltage applications. Guaranteed operation down to 1.8V means that this family of amplifiers can operate at the end of discharge (EOD) voltages of several popular batteries. The amplifier's 80 fA input current, 0.5 mV offset voltage, and 82 dB CMRR maintain accuracy in battery-powered systems.

For a single, dual or quad CMOS amplifier with similar specs and a powerdown mode, refer to the LMC6681/2/4 data sheet.

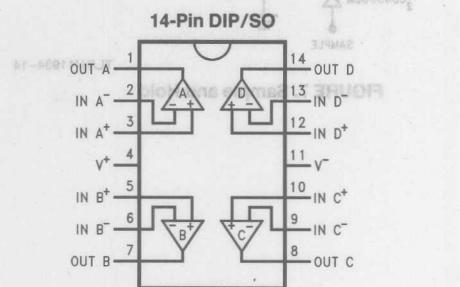
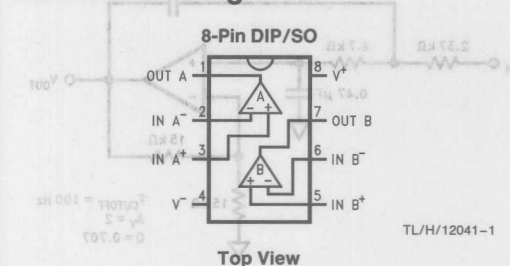
Features (Typical unless otherwise noted)

- Guaranteed Specs at 1.8V, 2.2V, 3V, 5V, 10V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing
(within 10 mV of supply rail, @ $V_S = 3V$ and $R_L = 10 k\Omega$)
- CMRR and PSRR 82 dB
- Ultra Low Input Current 80 fA
- High Voltage Gain ($V_S = 3V$, $R_L = 10 k\Omega$) 120 dB
- Unity Gain Bandwidth 1.2 MHz

Applications

- Battery Operated Systems
- Sensor Amplifiers
- Portable Communication Devices
- Medical Instrumentation
- Level Detectors, Sample-and-Hold Circuits
- Battery Monitoring

Connection Diagrams



Ordering Information

| Package | Temperature Range Industrial, -40°C to +85°C | NSC Drawing | Transport Media |
|----------------------|--|----------------|------------------------|
| 8-pin Molded DIP | LMC6582AIN, LMC6582BIN | N08E | Rails |
| 8-pin Small Outline | LMC6582AIM, LMC6582BIM LMC6582AIMX, LMC6582BIMX | M08A M08A | Rails Tape and Reel |
| 14-pin Molded DIP | LMC6584AIN, LMC6584BIN | N14A | Rails |
| 14-pin Small Outline | LMC6584AIM, LMC6584BIM LMC6584AIMX, LMC6584BIMX | M14A M14A | Rails Tape and Reel |

LMC6681 Single/LMC6682 Dual/LMC6684 Quad Low Voltage, Rail-To-Rail Input and Output CMOS Amplifier with Powerdown

General Description

The LMC6681/2/4 is a high performance operational amplifier which can operate over a wide range of supply voltages, from 1.8V to 10V. It has guaranteed specs at 1.8V, 2.2V, 3V, 5V, and 10V.

The LMC6681/2/4 provides an input common-mode voltage range that exceeds both rails. The rail-to-rail output swing of the amplifier assures maximum dynamic signal range. This rail-to-rail performance of the amplifier, combined with its high open-loop voltage gain makes it unique among CMOS rail-to-rail amplifiers. The LMC6681/2/4 is an excellent upgrade for circuits using limited common-mode range amplifiers.

The LMC6681/2/4 has a powerdown mode which can be triggered externally. In this powerdown mode, the supply current decreases from 1.4 mA (for two amplifiers) to 1.5 μ A (for two amplifiers). The LMC6684 has two powerdown options. Each of the powerdown pins disables two amplifiers.

The LMC6681/2/4 has been designed specifically to improve system performance in low voltage applications. The amplifier's 80 fA input current, 0.5 mV offset voltage, and 82 dB CMRR maintain accuracy in battery-powered systems.

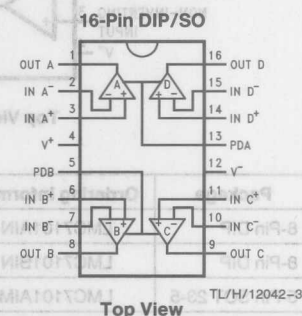
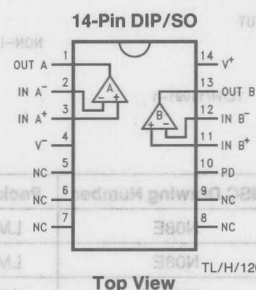
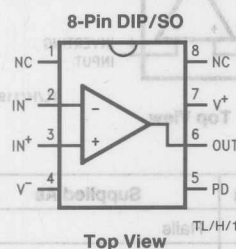
Features (Typical unless otherwise noted)

- Guaranteed Specs at 1.8V, 2.2V, 3V, 5V, 10V
- Rail-to-Rail Input Common-Mode Voltage Range
- Rail-to-Rail Output Swing (within 10 mV of supply rail, @ $V_S = 3V$ and $R_L = 10 k\Omega$)
- Powerdown Mode $I_{S OFF} \leq 1.5 \mu A/\text{Amplifier}$ (Guaranteed at $V_S = 1.8V, 2.2V, 3V$, and 5V)
- Ultra Low Input Current 80 fA
- High Voltage Gain ($V_S = 3V, R_L = 10 k\Omega$) 120 dB
- Unity Gain Bandwidth 1.2 MHz

Applications

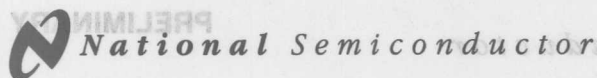
- Battery Operated Circuits
- Sensor Amplifiers
- Portable Communication Devices
- Medical Instrumentation
- Battery Monitoring Circuits
- Level Detectors, Sample-and-Hold Circuits

Connection Diagrams



Ordering Information

| Package | Temperature Range | NSC | |
|----------------------|--------------------------|---------|-----------------|
| | | Drawing | Transport Media |
| 8-Pin Molded DIP | LMC6681AIN, LMC6681BIN | N08E | Rails |
| 8-Pin Small Outline | LMC6681AIM, LMC6681BIM | M08A | Rails |
| | LMC6681AIMX, LMC6681BIMX | M08A | Tape and Reel |
| 14-Pin Molded DIP | LMC6682AIN, LMC6682BIN | N14A | Rails |
| 14-Pin Small Outline | LMC6682AIM, LMC6682BIM | M14A | Rails |
| | LMC6682AIMX, LMC6682BIMX | M14A | Tape and Reel |
| 16-Pin Molded DIP | LMC6684AIN, LMC6684BIN | N16A | Rails |
| 16-Pin Small Outline | LMC6684AIM, LMC6684BIM | M16A | Rails |
| | LMC6684AIMX, LMC6684BIMX | M16A | Tape and Reel |



LMC7101 Tiny Low Power Operational Amplifier with Rail-To-Rail Input and Output

General Description

The LMC7101 is a high performance CMOS operational amplifier available in the space saving SOT 23-5 Tiny package. This makes the LMC7101 ideal for space and weight critical designs. The performance is similar to a single amplifier of the LMC6482/4 type, with rail-to-rail input and output, high open loop gain, low distortion, and low supply currents. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

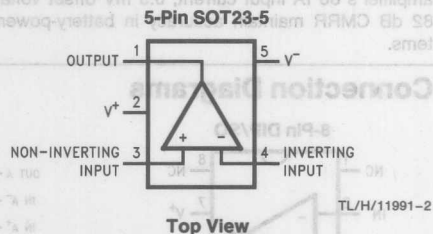
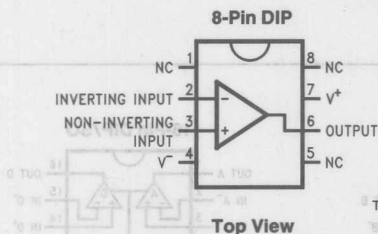
Features

- Tiny SOT23-5 package saves space—typical circuit layouts take half the space of SO-8 designs
- Guaranteed specs at 2.7V, 3V, 5V, 15V supplies
- Typical supply current 0.5 mA at 5V
- Typical total harmonic distortion of 0.01% at 5V
- 1.0 MHz gain-bandwidth
- Similar to popular LMC6482/4
- Input common-mode range includes V_{-} and V_{+}
- Tiny package outside dimensions—120 x 118 x 56 mils, 3.05 x 3.00 x 1.43 mm

Applications

- Mobile communications
- Notebooks and PDAs
- Battery powered products
- Sensor interface

Connection Diagrams



| Package | Ordering Information | NSC Drawing Number | Package Marking | Supplied As |
|----------------|----------------------|--------------------|-----------------|----------------------------|
| 8-Pin DIP | LMC7101AIN | N08E | LMC7101AIN | Rails |
| 8-Pin DIP | LMC7101BIN | N08E | LMC7101BIN | Rails |
| 5-Pin SOT 23-5 | LMC7101AIM5 | MA05A | A00A | 250 Units on Tape and Reel |
| 5-Pin SOT 23-5 | LMC7101BIM5 | MA05A | A00B | 250 Units on Tape and Reel |
| 5-Pin SOT 23-5 | LMC7101AIM5X | MA05A | A00A | 3k Units Tape and Reel |
| 5-Pin SOT 23-5 | LMC7101BIM5X | MA05A | A00B | 3k Units Tape and Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------|------------------------------|
| ESD Tolerance (Note 2) | 2000V |
| Difference Input Voltage | \pm Supply Voltage |
| Voltage at Input/Output Pin | $(V^+) + 0.3V, (V^-) - 0.3V$ |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin (Note 3) | ± 35 mA |
| Current at Power Supply Pin | 35 mA |
| Lead Temp. (Soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

Recommended Operating Conditions (Note 1)

| | |
|--------------------------------------|---|
| Supply Voltage | $2.7V \leq V^+ \leq 15.5V$ |
| Junction Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LMC7101AI, LMC7101BI | |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-Pin Molded DIP | 115°C/W |
| M05A Package, 5-Pin Surface Mt. | 325°C/W |

2.7V Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+/2$ and $R_L > 1$ M Ω . **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|------------|---------------------------------------|--|-----------------|--------------------------------|--------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | $V^+ = 2.7V$ | 0.11 | 6 | 9 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 1.0 | 64 | 64 | pA max |
| I_{OS} | Input Offset Current | | 0.5 | 32 | 32 | pA max |
| R_{IN} | Input Resistance | | > 1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | $0V \leq V_{CM} \leq 2.7V$ $V^+ = 2.7V$ | 70 | 55 | 50 | dB min |
| V_{CM1} | Input Common-Mode Voltage Range | $V^+ = V$ For CMRR ≥ 50 dB | 0.0 | 0.0 | 0.0 | V min |
| | | | 3.0 | 2.7 | 2.7 | V max |
| PSRR | Power Supply Rejection Ratio | $V^+ = 1.35V$ to $1.65V$ $V^- = -1.35V$ to $-1.65V$ $V_{CM} = 0$ | 60 | 50 | 45 | dB min |
| C_{IN} | Common-Mode Input Capacitance | | 3 | | | pF |
| V_O | Output Swing | $R_L = 2$ k Ω | 2.45 | 2.15 | 2.15 | V min |
| | | | 0.25 | 0.5 | 0.5 | V max |
| | | $R_L = 10$ k Ω | 2.68 | 2.64 | 2.64 | V min |
| | | | 0.025 | 0.06 | 0.06 | V max |
| I_S | Supply Current | | 0.5 | 0.81 0.95 | 0.81 0.95 | mA max |
| SR | Slew Rate | (Note 8) | 0.7 | | | V/ μs |
| GBW | Gain-Bandwidth Product | | 0.6 | | | MHz |

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|------------|---------------------------------------|--|-----------------|--------------------------------|--------------------------------|-------------------|
| V_{OS} | Input Offset Voltage | | 0.11 | 4 6 | 7 9 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1 | | | $\mu V/^{\circ}C$ |
| I_B | Input Current | | 1.0 | 64 | 64 | pA max |
| I_{OS} | Input Offset Current | | 0.5 | 32 | 32 | pA max |
| R_{IN} | Input Resistance | | > 1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | $0V \leq V_{CM} \leq 3V$ $V^+ = 3V$ | 74 | 64 | 60 | db min |
| V_{CM} | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | 0.0 | 0.0 | 0.0 | V min |
| | | | 3.3 | 3.0 | 3.0 | V max |
| PSRR | Power Supply Rejection Ratio | $V^+ = 1.5V$ to $7.5V$ $V^- = -1.5V$ to $-7.5V$ $V_O = V_{CM} = 0$ | 80 | 68 | 60 | dB min |
| C_{IN} | Common-Mode Input Capacitance | | 3 | | | pF |
| V_O | Output Swing | $R_L = 2\text{ k}\Omega$ | 2.8 | 2.6 | 2.6 | V min |
| | | | 0.2 | 0.4 | 0.4 | V max |
| | | $R_L = 600\Omega$ | 2.7 | 2.5 | 2.5 | V min |
| | | | 0.37 | 0.6 | 0.6 | V max |
| I_S | Supply Current | | 0.5 | 0.81 0.95 | 0.81 0.95 | mA max |
| PSRR | Power Supply Rejection Ratio | $V^+ = 1.35V$ to $7.5V$ $V^- = -1.35V$ to $-7.5V$ $V_O = 0$ | | | | dB min |
| C_{IN} | Common-Mode Input Capacitance | | 3 | | | pF |
| V_O | Output Swing | $R_L = 2\text{ k}\Omega$ | 2.8 | 2.6 | 2.6 | V min |
| | | | 0.2 | 0.4 | 0.4 | V max |
| | | $R_L = 600\Omega$ | 2.7 | 2.5 | 2.5 | V min |
| | | | 0.37 | 0.6 | 0.6 | V max |
| I_S | Supply Current | | 0.5 | 0.81 0.95 | 0.81 0.95 | mA max |
| SR | Slew Rate | (Note 5) | 0.7 | | | V/ μs |
| GBW | Gain-Bandwidth Product | | 0.8 | | | MHz |

| Symbol | Parameter | Conditions | Limit (Note 5) | Limit (Note 6) | Limit (Note 6) | Units |
|------------|--|--|----------------|----------------|----------------|-------------------|
| V_{OS} | Input Offset Voltage | $V^+ = 5V$ | 0.11 | 3 5 | 7 9 | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.0 | | | $\mu V/^{\circ}C$ |
| I_B | Input Current | | 1 | 64 | 64 | pA max |
| I_{OS} | Input Offset Current | | 0.5 | 32 | 32 | pA max |
| R_{IN} | Input Resistance | | >1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | $0V \leq V_{CM} \leq 5V$ | 82 | 65 60 | 60 55 | db min |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+ = 5V$ to $15V$ $V^- = 0V, V_O = 1.5V$ | 82 | 70 65 | 65 62 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $V^- = -5V$ to $-15V$ $V^+ = 0V, V_O = -1.5V$ | 82 | 70 65 | 65 62 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | For CMRR ≥ 50 dB | -0.3 | -0.20 0.00 | -0.20 0.00 | V min |
| | | | 5.3 | 5.20 5.00 | 5.20 5.00 | V max |
| C_{IN} | Common-Mode Input Capacitance | | 3 | | | pF |
| V_O | Output Swing | $R_L = 2 k\Omega$ | 4.9 | 4.7 4.6 | 4.7 4.6 | V min |
| | | | 0.1 | 0.18 0.24 | 0.18 0.24 | V max |
| | | $R_L = 600\Omega$ | 4.7 | 4.5 4.24 | 4.5 4.24 | V min |
| | | | 0.3 | 0.5 0.65 | 0.5 0.65 | V max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0V$ | 24 | 16 11 | 16 11 | mA min |
| | | Sinking, $V_O = 5V$ | 19 | 11 7.5 | 11 7.5 | mA min |
| I_S | Supply Current | | 0.5 | 0.85 1.0 | 0.85 1.0 | mA max |

5V AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|--------|---------------------------|---|-----------------|--------------------------------|--------------------------------|------------------------|
| T.H.D. | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 4.0\text{ V}_{pp}$ | 0.01 | | | % |
| SR | Slew Rate | | 1.0 | | | $\text{V}/\mu\text{s}$ |
| GBW | Gain-Bandwidth Product | | 1.0 | | | MHz |

15V DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{ M}\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|------------|---------------------------------------|--|-----------------|--------------------------------|--------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 0.11 | | | mV max |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.0 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Current | | 1.0 | 64 | 64 | pA max |
| I_{OS} | Input Offset Current | | 0.5 | 32 | 32 | pA max |
| R_{IN} | Input Resistance | | > 1 | | | Tera Ω |
| CMRR | Common-Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 15\text{V}$ | 82 | 70 65 | 65 60 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $V^+ = 5\text{V to } 15\text{V}$ $V^- = 0\text{V}$, $V_O = 1.5\text{V}$ | 82 | 70 65 | 65 62 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $V^- = -5\text{V to } -15\text{V}$ $V^+ = 0\text{V}$, $V_O = -1.5\text{V}$ | 82 | 70 65 | 65 62 | dB min |
| V_{CM} | Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ For CMRR $\geq 50\text{ dB}$ | -0.3 | -0.20 0.00 | -0.20 0.00 | V min |
| | | | 15.3 | 15.20 15.00 | 15.20 15.00 | V max |
| A_V | Large Signal Voltage Gain | $R_L = 2\text{ k}\Omega$ Sourcing (Note 7) | 340 | 80 40 | 80 40 | V/mV |
| | | Sinking | 24 | 15 10 | 15 10 | |
| | | $R_L = 600\Omega$ Sourcing (Note 7) | 300 | 34 | 34 | V/mV |
| | | Sinking | 15 | 6 | 6 | |
| C_{IN} | Input Capacitance | | 3 | | | pF |
| V_O | Output Swing | $V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ | 14.7 | 14.4 14.2 | 14.4 14.2 | V min |
| | | | 0.16 | 0.32 0.45 | 0.32 0.45 | V max |
| | | $V^+ = 15\text{V}$ $R_L = 600\Omega$ | 14.1 | 13.4 13.0 | 13.4 13.0 | V min |
| | | | 0.5 | 1.0 1.3 | 1.0 1.3 | V max |
| I_{SC} | Output Short Circuit Current | Sourcing, $V_O = 0\text{V}$ (Note 9) | 50 | 30 20 | 30 20 | mA min |
| | | Sinking, $V_O = 12\text{V}$ (Note 9) | 50 | 30 20 | 30 20 | mA min |
| I_S | Supply Current | | 0.8 | 1.50 1.71 | 1.50 1.71 | mA max |

15V AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 15\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = V^+/2$ and $R_L = 1\text{M}\Omega$. **Boldface** limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7101AI Limit (Note 6) | LMC7101BI Limit (Note 6) | Units |
|----------|---------------------------------|---|-----------------|--------------------------------|--------------------------------|--------------------------------------|
| SR | Slew Rate | $V^+ = 15\text{V}$ (Note 8) | 1.1 | 0.5 0.4 | 0.5 0.4 | $\text{V}/\mu\text{s}$ min |
| GBW | Gain-Bandwidth Product | $V^+ = 15\text{V}$ | 1.1 | | | MHz |
| ϕ_m | Phase Margin | | 45 | | | Deg |
| G_m | Gain Margin | | 10 | | | dB |
| e_n | Input-Referred Voltage Noise | $F = 1\text{ kHz}$ $V_{CM} = 1\text{V}$ | 37 | | | $\frac{\text{nV}}{\sqrt{\text{Hz}}}$ |
| i_n | Input-Referred Current Noise | $F = 1\text{ kHz}$ | 1.5 | | | $\frac{\text{fA}}{\sqrt{\text{Hz}}}$ |
| T.H.D. | Total Harmonic Distortion | $F = 10\text{ kHz}$, $A_V = -2$ $R_L = 10\text{ k}\Omega$, $V_O = 8.5\text{ V}_{PP}$ | 0.01 | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, $1.5\text{ k}\Omega$ in series with 100 pF .

Note 3: Applies to both single-supply and split-supply operation. Continuous short operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature at 150°C .

Note 4: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $PD = (T_{J(\text{max})} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

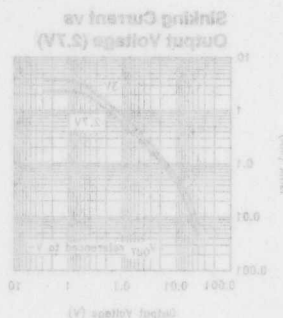
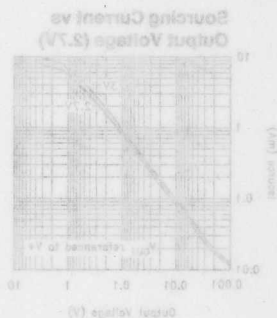
Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: $V^+ = 15\text{V}$, $V_{CM} = 1.5\text{V}$ and R_L connect to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 12.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 8: $V^+ = 15\text{V}$. Connected as a Voltage Follower with a 10V step input. Number specified is the slower of the positive and negative slew rates. $R_L = 100\text{ k}\Omega$ connected to 7.5V . Amp excited with 1 kHz to produce $V_O = 10\text{ V}_{PP}$.

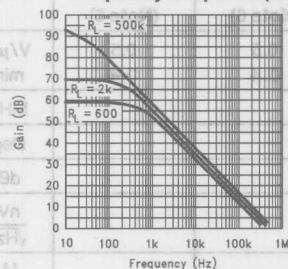
Note 9: Do not short circuit output to V^+ when V^+ is greater than 12V or reliability will be adversely affected.



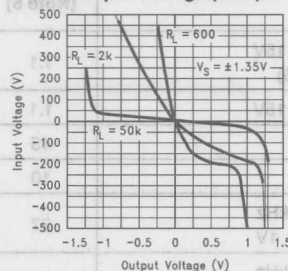
Typical Performance Characteristics $V_S = +2.7V$, Single Supply, $T_A = 25^\circ C$ unless specified

2.7V PERFORMANCE

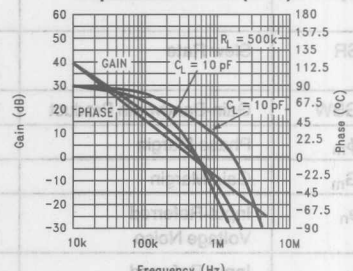
Open Loop Frequency Response (2.7V)



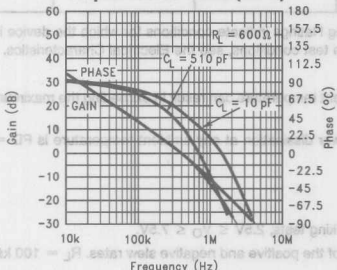
Input Voltage vs Output Voltage (2.7V)



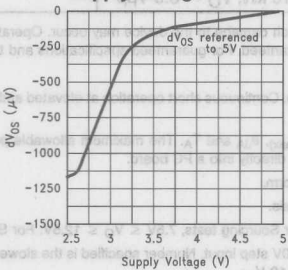
Gain and Phase vs Capacitance Load (2.7V)



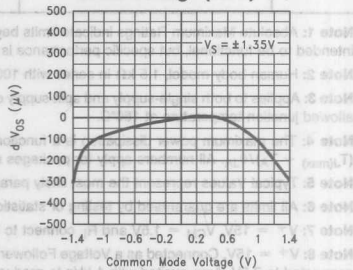
Gain and Phase vs Capacitance Load (2.7V)



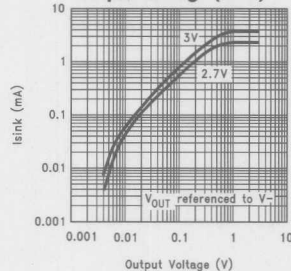
dVos vs Supply Voltage



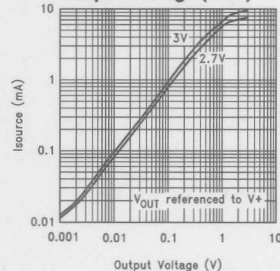
dVos vs Common Mode Voltage (2.7V)



Sinking Current vs Output Voltage (2.7V)



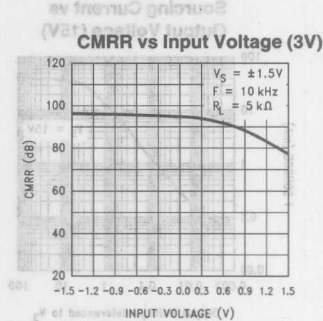
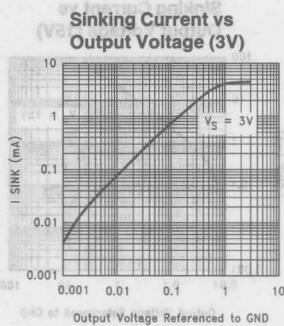
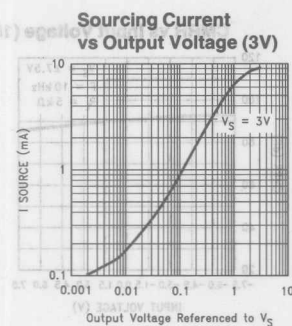
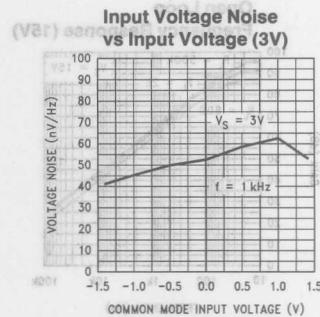
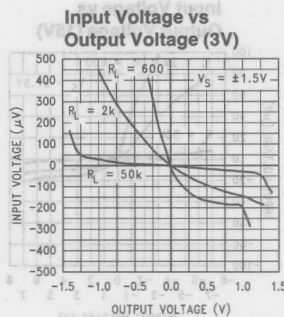
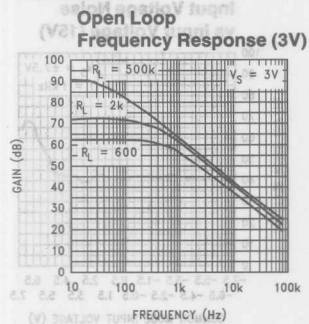
Sourcing Current vs Output Voltage (2.7V)



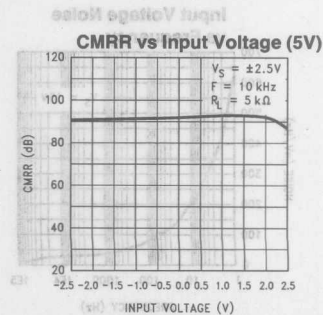
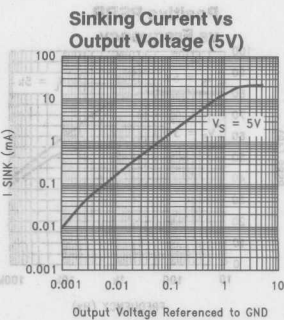
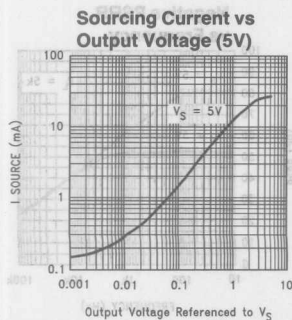
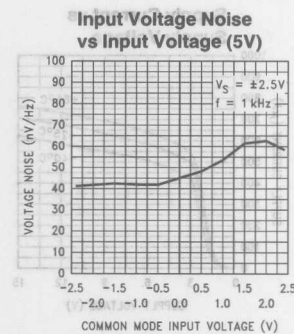
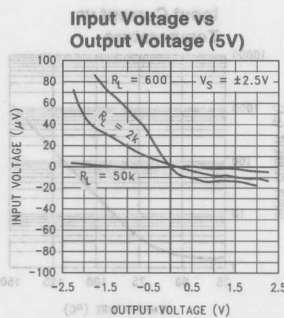
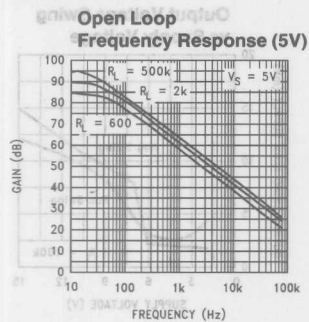
Typical Performance Characteristics

Single Supply, $T_A = 25^\circ\text{C}$ unless specified (Continued)

3V PERFORMANCE

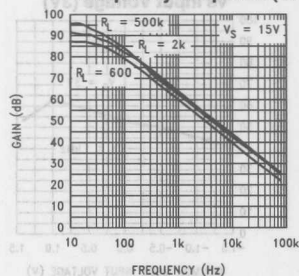


5V PERFORMANCE

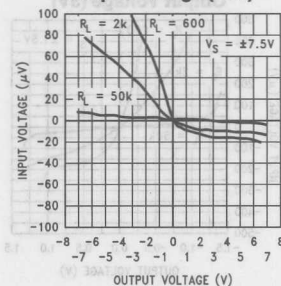


TL/H/11991-3

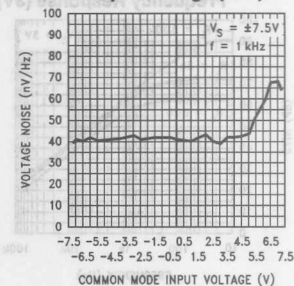
**Open Loop
Frequency Response (15V)**



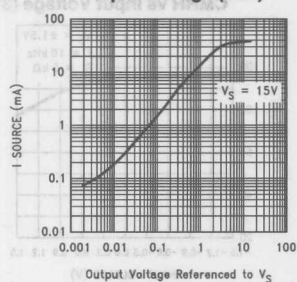
**Input Voltage vs
Output Voltage (15V)**



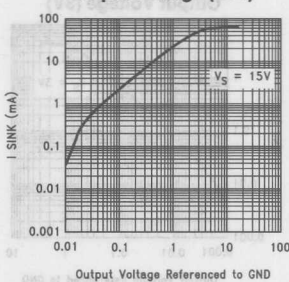
**Input Voltage Noise
vs Input Voltage (15V)**



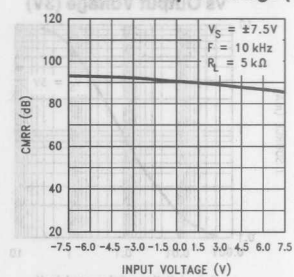
**Sourcing Current vs
Output Voltage (15V)**



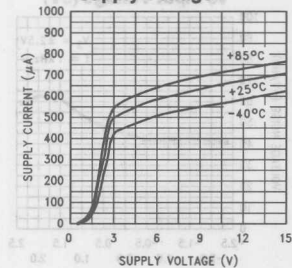
**Sinking Current vs
Output Voltage (15V)**



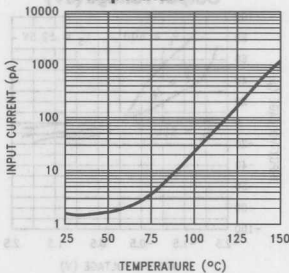
CMRR vs Input Voltage (15V)



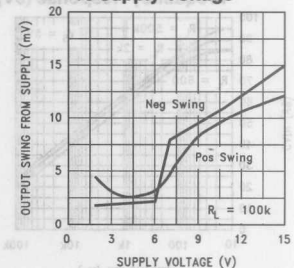
**Supply Current vs
Supply Voltage**



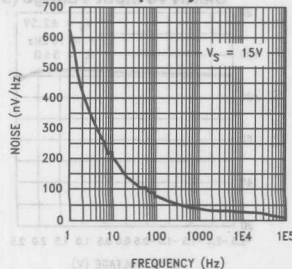
**Input Current vs
Temperature**



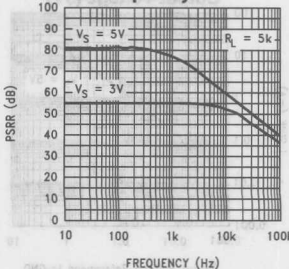
**Output Voltage Swing
vs Supply Voltage**



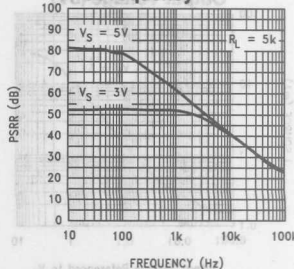
**Input Voltage Noise
vs Frequency**



**Positive PSRR
vs Frequency**

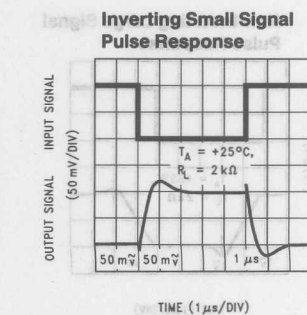
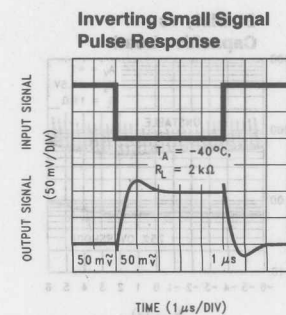
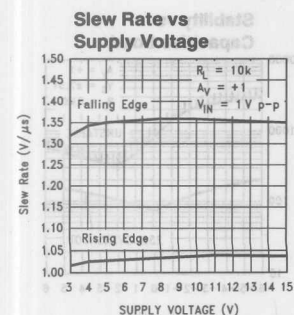
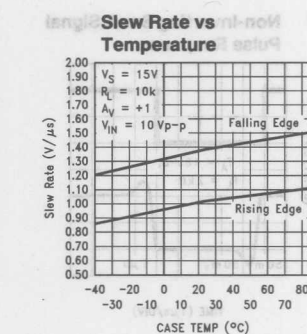
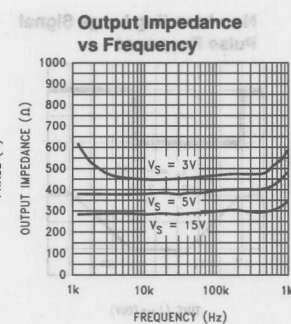
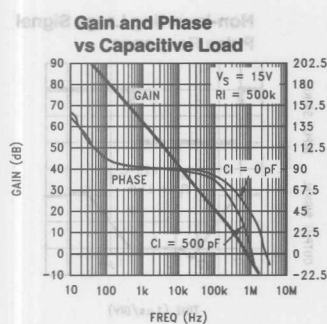
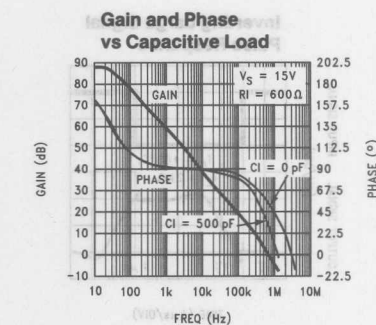
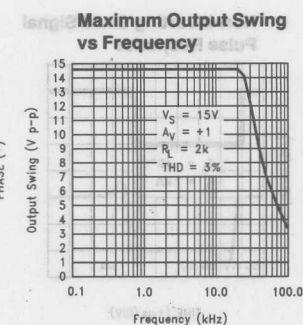
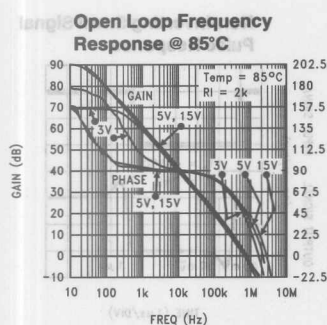
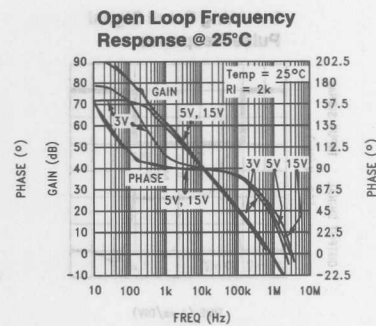
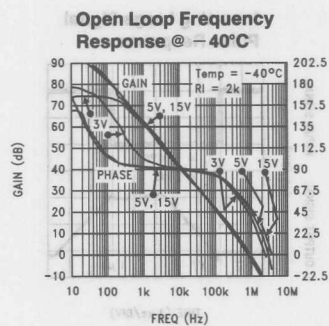
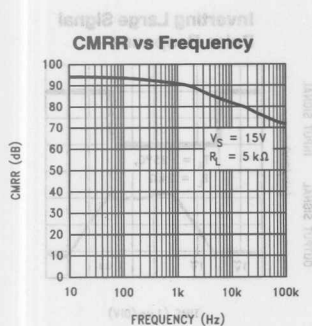


**Negative PSRR
vs Frequency**



Typical Performance Characteristics

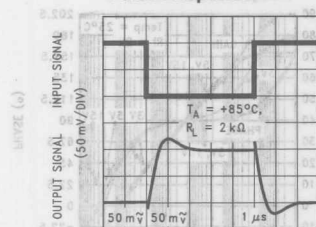
$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified (Continued)



Typical Performance Characteristics

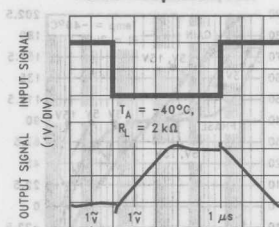
$V_S = +15V$, Single Supply, $T_A = 25^\circ C$ unless specified (Continued)

Inverting Small Signal Pulse Response



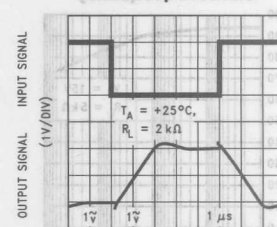
TIME (1 μs/DIV)

Inverting Large Signal Pulse Response



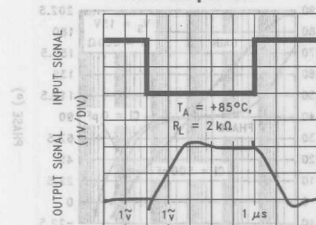
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Inverting Large Signal Pulse Response



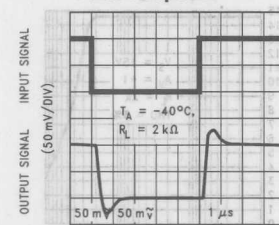
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Inverting Large Signal Pulse Response



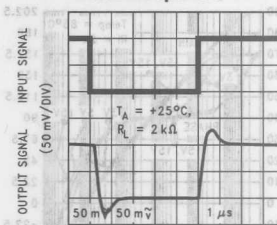
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Non-Inverting Small Signal Pulse Response



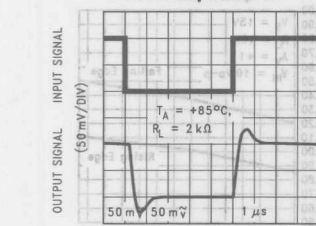
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Non-Inverting Small Signal Pulse Response



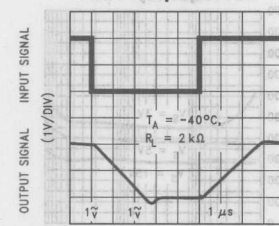
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Non-Inverting Small Signal Pulse Response



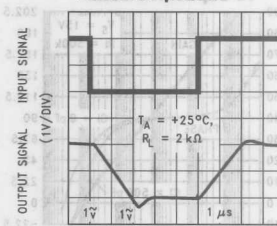
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Non-Inverting Large Signal Pulse Response



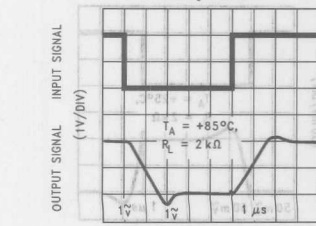
TIME (1 μs/DIV)

Non-Inverting Large Signal Pulse Response



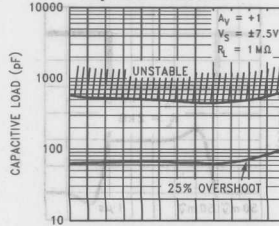
TIME (1 μs/DIV)

Non-Inverting Large Signal Pulse Response



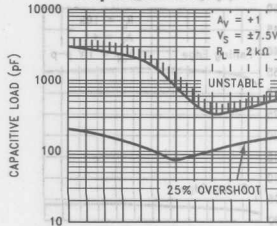
TIME (1 μs/DIV)

Stability vs Capacitive Load



OUT (V)

Stability vs Capacitive Load



OUT (V)

Application Information

1.0 Benefits of the LMC7101

Tiny Amp

Size. The small footprint of the SOT 23-5 packaged Tiny amp, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny amp makes it possible to use it in PCMCIA type III cards.

Signal Integrity. Signals can pick up noise between the signal source and the amplifier. By using a physically smaller amplifier package, the Tiny amp can be placed closer to the signal source, reducing noise pickup and increasing signal integrity. The Tiny amp can also be placed next to the signal destination, such as a buffer for the reference of an analog to digital converter.

Simplified Board Layout. The Tiny amp can simplify board layout in several ways. First, by placing an amp where amps are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny amps instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7101 amplifiers packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Tapes of ten for prototyping. The SOT23-5 packaged devices are available in convenient and economical ten unit tapes for prototypes, evaluation, and small production runs.

Low THD. The high open loop gain of the LMC7101 amp allows it to achieve very low audio distortion—typically 0.01% at 10 kHz with a 10 k Ω load at 5V supplies. This makes the Tiny an excellent for audio, modems, and low frequency signal processing.

Low Supply Current. The typical 0.5 mA supply current of the LMC7101 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7101 is characterized at 15V, 5V and 3V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7101 a good choice for devices where the voltage may vary over the life of the batteries.

2.0 Input Common Mode Voltage Range

The LMC7101 does not exhibit phase inversion when an input voltage exceeds the negative supply voltage. Figure 1 shows an input voltage exceeding both supplies with no resulting phase inversion of the output.

The absolute maximum input voltage is 300 mV beyond either rail at room temperature. Voltages greatly exceeding this maximum rating, as in Figure 2, can cause excessive current to flow in or out of the input pins, adversely affecting reliability.

Typical Performance Characteristics

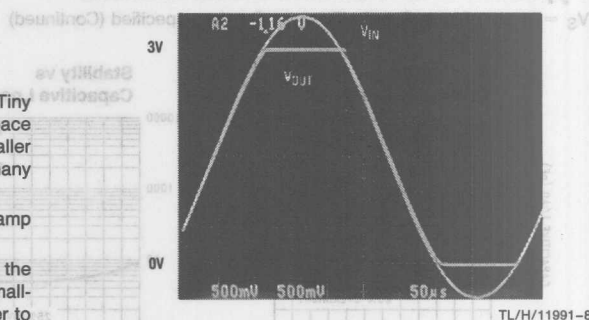


FIGURE 1. An Input Voltage Signal Exceeds the LMC7101 Power Supply Voltages with No Output Phase Inversion

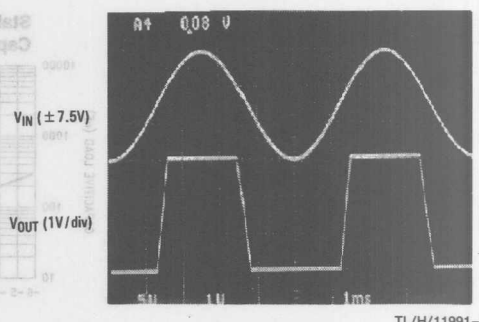


FIGURE 2. A $\pm 7.5V$ Input Signal Greatly Exceeds the 3V Supply in Figure 3 Causing No Phase Inversion Due to R_I

Applications that exceed this rating must externally limit the maximum input current to ± 5 mA with an input resistor as shown in Figure 3.

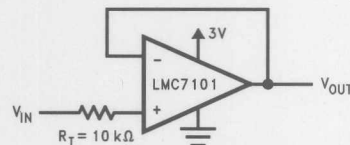


FIGURE 3. R_I Input Current Protection for Voltages Exceeding the Supply Voltage

3.0 Rail-To-Rail Output

The approximate output resistance of the LMC7101 is 180 Ω sourcing and 130 Ω sinking at $V_S = 3V$ and 110 Ω sourcing and 80 Ω sinking at $V_S = 5V$. Using the calculated output resistance, maximum output voltage swing can be estimated as a function of load.

follower is the most sensitive configuration. Direct capacitive loading reduces the phase margin of op-amps. The combination of the op-amp's output impedance and the capacitive load induces phase lag. This results in either an underdamped pulse response or oscillation.

Capacitive load compensation can be accomplished using resistive isolation as shown in Figure 4. This simple technique is useful for isolating the capacitive input of multiplexers and A/D converters.

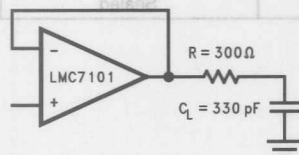


FIGURE 4. Resistive Isolation of a 330 pF Capacitive Load

5.0 Compensating for Input Capacitance when Using Large Value Feedback Resistors

When using very large value feedback resistors, (usually > 500 kΩ) the large feedback resistance can react with the input capacitance due to transducers, photodiodes, and circuit board parasitics to reduce phase margins.

$$\frac{2\pi R_1 C_{IN}}{1} \approx \frac{2\pi R_2 C_F}{1}$$

or

$$R_1 C_{IN} \leq R_2 C_F$$

which typically provides significant overcompensation.

Printed circuit board stray capacitance may be larger or smaller than that of a breadboard, so the actual optimum value for C_F may be different. The values of C_F should be checked on the actual circuit. (Refer to the LMC660 quad CMOS amplifier data sheet for a more detailed discussion.)

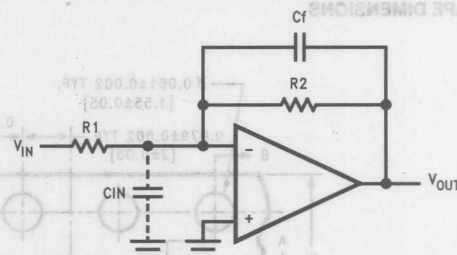
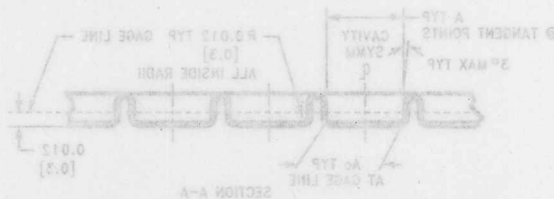
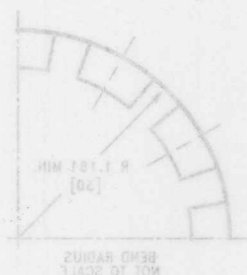


FIGURE 5. Cancelling the Effect of Input Capacitance



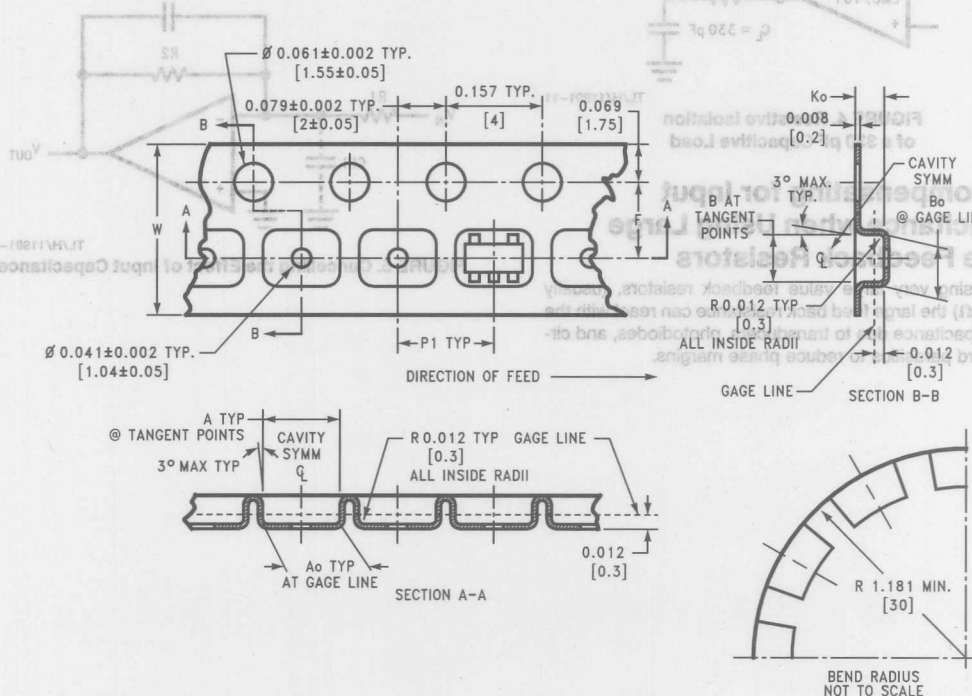
| 8 mm | DIM A | DIM B | DIM C | DIM D | DIM E | DIM F | DIM G | DIM H | DIM I | DIM J | DIM K | DIM L | DIM M | DIM N | DIM O | DIM P | DIM Q | DIM R | DIM S | DIM T | DIM U | DIM V | DIM W | DIM X | DIM Y | DIM Z | DIM AA | DIM AB | DIM AC | DIM AD | DIM AE | DIM AF | DIM AG | DIM AH | DIM AI | DIM AJ | DIM AK | DIM AL | DIM AM | DIM AN | DIM AO | DIM AP | DIM AQ | DIM AR | DIM AS | DIM AT | DIM AU | DIM AV | DIM AW | DIM AX | DIM AY | DIM AZ | DIM BA | DIM BB | DIM BC | DIM BD | DIM BE | DIM BF | DIM BG | DIM BH | DIM BI | DIM BJ | DIM BK | DIM BL | DIM BM | DIM BN | DIM BO | DIM BP | DIM BQ | DIM BR | DIM BS | DIM BT | DIM BU | DIM BV | DIM BW | DIM BX | DIM BY | DIM BZ | DIM CA | DIM CB | DIM CC | DIM CD | DIM CE | DIM CF | DIM CG | DIM CH | DIM CI | DIM CJ | DIM CK | DIM CL | DIM CM | DIM CN | DIM CO | DIM CP | DIM CQ | DIM CR | DIM CS | DIM CT | DIM CU | DIM CV | DIM CW | DIM CX | DIM CY | DIM CZ | DIM DA | DIM DB | DIM DC | DIM DD | DIM DE | DIM DF | DIM DG | DIM DH | DIM DI | DIM DJ | DIM DK | DIM DL | DIM DM | DIM DN | DIM DO | DIM DP | DIM DQ | DIM DR | DIM DS | DIM DT | DIM DU | DIM DV | DIM DW | DIM DX | DIM DY | DIM DZ | DIM EA | DIM EB | DIM EC | DIM ED | DIM EE | DIM EF | DIM EG | DIM EH | DIM EI | DIM EJ | DIM EK | DIM EL | DIM EM | DIM EN | DIM EO | DIM EP | DIM EQ | DIM ER | DIM ES | DIM ET | DIM EU | DIM EV | DIM EW | DIM EX | DIM EY | DIM EZ | DIM FA | DIM FB | DIM FC | DIM FD | DIM FE | DIM FF | DIM FG | DIM FH | DIM FI | DIM FJ | DIM FK | DIM FL | DIM FM | DIM FN | DIM FO | DIM FP | DIM FQ | DIM FR | DIM FS | DIM FT | DIM FU | DIM FV | DIM FW | DIM FX | DIM FY | DIM FZ | DIM GA | DIM GB | DIM GC | DIM GD | DIM GE | DIM GF | DIM GG | DIM GH | DIM GI | DIM GJ | DIM GK | DIM GL | DIM GM | DIM GN | DIM GO | DIM GP | DIM GQ | DIM GR | DIM GS | DIM GT | DIM GU | DIM GV | DIM GW | DIM GX | DIM GY | DIM GZ | DIM HA | DIM HB | DIM HC | DIM HD | DIM HE | DIM HF | DIM HG | DIM HH | DIM HI | DIM HJ | DIM HK | DIM HL | DIM HM | DIM HN | DIM HO | DIM HP | DIM HQ | DIM HR | DIM HS | DIM HT | DIM HU | DIM HV | DIM HW | DIM HX | DIM HY | DIM HZ | DIM IA | DIM IB | DIM IC | DIM ID | DIM IE | DIM IF | DIM IG | DIM IH | DIM II | DIM IJ | DIM IK | DIM IL | DIM IM | DIM IN | DIM IO | DIM IP | DIM IQ | DIM IR | DIM IS | DIM IT | DIM IU | DIM IV | DIM IW | DIM IX | DIM IY | DIM IZ | DIM JA | DIM JB | DIM JC | DIM JD | DIM JE | DIM JF | DIM JG | DIM JH | DIM JI | DIM JJ | DIM JK | DIM JL | DIM JM | DIM JN | DIM JO | DIM JP | DIM JQ | DIM JR | DIM JS | DIM JT | DIM JU | DIM JV | DIM JW | DIM JX | DIM JY | DIM JZ | DIM KA | DIM KB | DIM KC | DIM KD | DIM KE | DIM KF | DIM KG | DIM KH | DIM KI | DIM KJ | DIM KK | DIM KL | DIM KM | DIM KN | DIM KO | DIM KP | DIM KQ | DIM KR | DIM KS | DIM KT | DIM KU | DIM KV | DIM KW | DIM KX | DIM KY | DIM KZ | DIM LA | DIM LB | DIM LC | DIM LD | DIM LE | DIM LF | DIM LG | DIM LH | DIM LI | DIM LJ | DIM LK | DIM LL | DIM LM | DIM LN | DIM LO | DIM LP | DIM LQ | DIM LR | DIM LS | DIM LT | DIM LU | DIM LV | DIM LW | DIM LX | DIM LY | DIM LZ | DIM MA | DIM MB | DIM MC | DIM MD | DIM ME | DIM MF | DIM MG | DIM MH | DIM MI | DIM MJ | DIM MK | DIM ML | DIM MM | DIM MN | DIM MO | DIM MP | DIM MQ | DIM MR | DIM MS | DIM MT | DIM MU | DIM MV | DIM MW | DIM MX | DIM MY | DIM MZ | DIM NA | DIM NB | DIM NC | DIM ND | DIM NE | DIM NF | DIM NG | DIM NH | DIM NI | DIM NJ | DIM NK | DIM NL | DIM NM | DIM NN | DIM NO | DIM NP | DIM NQ | DIM NR | DIM NS | DIM NT | DIM NU | DIM NV | DIM NW | DIM NX | DIM NY | DIM NZ | DIM OA | DIM OB | DIM OC | DIM OD | DIM OE | DIM OF | DIM OG | DIM OH | DIM OI | DIM OJ | DIM OK | DIM OL | DIM OM | DIM ON | DIM OO | DIM OP | DIM OQ | DIM OR | DIM OS | DIM OT | DIM OU | DIM OV | DIM OW | DIM OX | DIM OY | DIM OZ | DIM PA | DIM PB | DIM PC | DIM PD | DIM PE | DIM PF | DIM PG | DIM PH | DIM PI | DIM PJ | DIM PK | DIM PL | DIM PM | DIM PN | DIM PO | DIM PP | DIM PQ | DIM PR | DIM PS | DIM PT | DIM PU | DIM PV | DIM PW | DIM PX | DIM PY | DIM PZ | DIM QA | DIM QB | DIM QC | DIM QD | DIM QE | DIM QF | DIM QG | DIM QH | DIM QI | DIM QJ | DIM QK | DIM QL | DIM QM | DIM QN | DIM QO | DIM QP | DIM QQ | DIM QR | DIM QS | DIM QT | DIM QU | DIM QV | DIM QW | DIM QX | DIM QY | DIM QZ | DIM RA | DIM RB | DIM RC | DIM RD | DIM RE | DIM RF | DIM RG | DIM RH | DIM RI | DIM RJ | DIM RK | DIM RL | DIM RM | DIM RN | DIM RO | DIM RP | DIM RQ | DIM RR | DIM RS | DIM RT | DIM RU | DIM RV | DIM RW | DIM RX | DIM RY | DIM RZ | DIM SA | DIM SB | DIM SC | DIM SD | DIM SE | DIM SF | DIM SG | DIM SH | DIM SI | DIM SJ | DIM SK | DIM SL | DIM SM | DIM SN | DIM SO | DIM SP | DIM SQ | DIM SR | DIM SS | DIM ST | DIM SU | DIM SV | DIM SW | DIM SX | DIM SY | DIM SZ | DIM TA | DIM TB | DIM TC | DIM TD | DIM TE | DIM TF | DIM TG | DIM TH | DIM TI | DIM TJ | DIM TK | DIM TL | DIM TM | DIM TN | DIM TO | DIM TP | DIM TQ | DIM TR | DIM TS | DIM TT | DIM TU | DIM TV | DIM TW | DIM TX | DIM TY | DIM TZ | DIM UA | DIM UB | DIM UC | DIM UD | DIM UE | DIM UF | DIM UG | DIM UH | DIM UI | DIM UJ | DIM UK | DIM UL | DIM UM | DIM UN | DIM UO | DIM UP | DIM UQ | DIM UR | DIM US | DIM UT | DIM UY | DIM UZ | DIM VA | DIM VB | DIM VC | DIM VD | DIM VE | DIM VF | DIM VG | DIM VH | DIM VI | DIM VJ | DIM VK | DIM VL | DIM VM | DIM VN | DIM VO | DIM VP | DIM VQ | DIM VR | DIM VS | DIM VT | DIM VU | DIM VV | DIM VW | DIM VX | DIM VY | DIM VZ | DIM WA | DIM WB | DIM WC | DIM WD | DIM WE | DIM WF | DIM WG | DIM WH | DIM WI | DIM WJ | DIM WK | DIM WL | DIM WM | DIM WN | DIM WO | DIM WP | DIM WQ | DIM WR | DIM WS | DIM WT | DIM WU | DIM WV | DIM WW | DIM WX | DIM WY | DIM WZ | DIM XA | DIM XB | DIM XC | DIM XD | DIM XE | DIM XF | DIM XG | DIM XH | DIM XI | DIM XJ | DIM XK | DIM XL | DIM XM | DIM XN | DIM XO | DIM XP | DIM XQ | DIM XR | DIM XS | DIM XT | DIM XU | DIM XV | DIM XW | DIM XX | DIM XY | DIM XZ | DIM YA | DIM YB | DIM YC | DIM YD | DIM YE | DIM YF | DIM YG | DIM YH | DIM YI | DIM YJ | DIM YK | DIM YL | DIM YM | DIM YN | DIM YO | DIM YP | DIM YQ | DIM YR | DIM YS | DIM YT | DIM YU | DIM YV | DIM YW | DIM YX | DIM YY | DIM YZ | DIM ZA | DIM ZB | DIM ZC | DIM ZD | DIM ZE | DIM ZF | DIM ZG | DIM ZH | DIM ZI | DIM ZJ | DIM ZK | DIM ZL | DIM ZM | DIM ZN | DIM ZO | DIM ZP | DIM ZQ | DIM ZR | DIM ZS | DIM ZT | DIM ZU | DIM ZV | DIM ZW | DIM ZX | DIM ZY | DIM ZZ |
|------|-------|-------|-------|-------|-------|-------|---------------|---------------|-------|---------------|---------------|-------|---------------|-------|-------|-------|---------------|-------|-------|-------|---------------|-------|-------|-------|---------------|-------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|---------------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------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| | 0.130 | 0.134 | 0.130 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.028 ± 0.004 | 0.137 | 0.278 ± 0.015 | 0.130 ± 0.005 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.130 ± 0.005 | 0.138 | 0.130 | 0.138 | 0.1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

| Tape Section | # Cavities | Cavity Status | Cover Tape Status |
|-----------------------|------------|---------------|-------------------|
| Leader (Start End) | 0 (min) | Empty | Sealed |
| | 75 (min) | Empty | Sealed |
| Carrier | 3000 | Filled | Sealed |
| | 250 | Filled | Sealed |
| Trailer (Hub End) | 125 (min) | Empty | Sealed |
| | 0 (min) | Empty | Sealed |

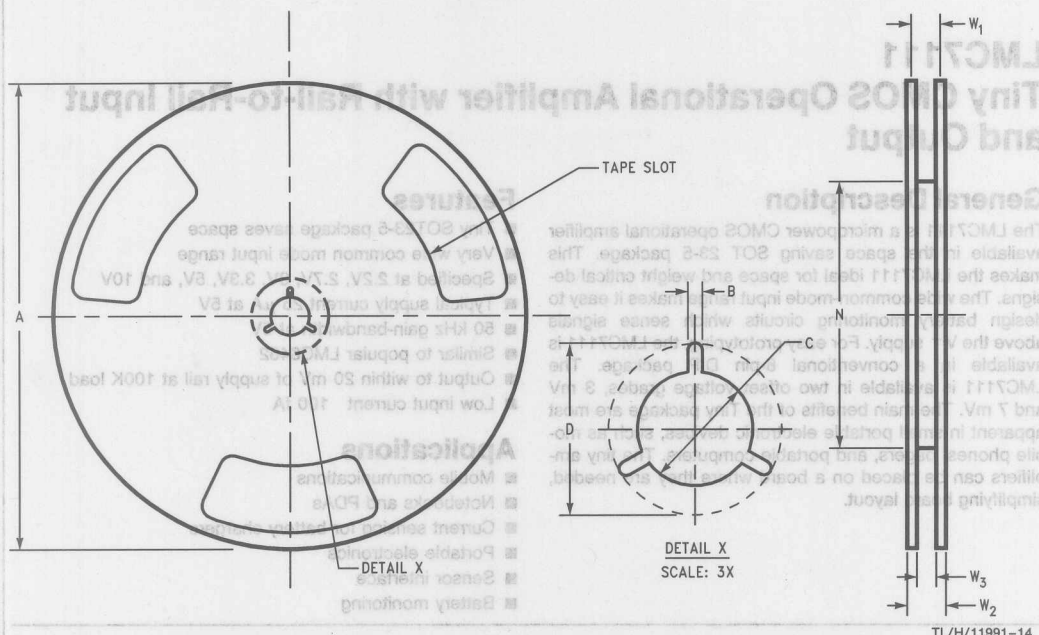
TAPE DIMENSIONS



| 8 mm | 0.130 (3.3) | 0.124 (3.15) | 0.130 (3.3) | 0.126 (3.2) | 0.138 ± 0.002 (3.5 ± 0.05) | 0.055 ± 0.004 (1.4 ± 0.11) | 0.157 (4) | 0.315 ± 0.012 (8 ± 0.3) |
|-----------|----------------|-----------------|----------------|----------------|-------------------------------|-------------------------------|--------------|----------------------------|
| Tape Size | DIM A | DIM Ao | DIM B | DIM Bo | DIM F | DIM Ko | DIM P1 | DIM W |

SOT-23-5 Tape and Reel Specification (Continued)

REEL DIMENSIONS



| 8 mm | 7.00 | 0.059 | 0.512 | 0.795 | 2.165 | $0.331 + 0.059/-0.000$ | 0.567 | $W1 \pm 0.078/-0.039$ |
|-----------|--------|-------|-------|-------|-------|------------------------|-------|-----------------------|
| | 330.00 | 1.50 | 13.00 | 20.20 | 55.00 | $8.40 + 1.50/-0.00$ | 14.40 | $W1 + 2.00/-1.00$ |
| Tape Size | A | B | C | D | N | W1 | W2 | W3 |

6.0 SPICE Macromodel

A SPICE macromodel is available for the LMC7101. This model includes simulation of:

- Input common-mode voltage range
- Frequency and transient response
- GBW dependence on loading conditions
- Quiescent and dynamic supply current
- Output swing dependence on loading conditions and many more characteristics as listed on the macro model disk. Contact your local National Semiconductor sales office to obtain an operational amplifier spice model library disk.

| Package | Ordering Information | NSC Drawing Number | Package Marking | Transport Media |
|---------------|----------------------|--------------------|-----------------|----------------------------|
| 8-Pin DIP | LMC7111AIN | NO8E | LMC7111AIN | Reels |
| 8-Pin DIP | LMC7111BIN | NO8E | LMC7111BIN | Reels |
| 8-Pin SOT23-5 | LMC7111AIMS | MA05A | A01A | 250 Units on Tape and Reel |
| 8-Pin SOT23-5 | LMC7111BIMS | MA05A | A01B | 250 Units on Tape and Reel |
| 8-Pin SOT23-5 | LMC7111AIMSX | MA05A | A01A | 3K Units on Tape and Reel |
| 8-Pin SOT23-5 | LMC7111BIMSX | MA05A | A01B | 3K Units on Tape and Reel |

LMC7111

Tiny CMOS Operational Amplifier with Rail-to-Rail Input and Output

General Description

The LMC7111 is a micropower CMOS operational amplifier available in the space saving SOT 23-5 package. This makes the LMC7111 ideal for space and weight critical designs. The wide common-mode input range makes it easy to design battery monitoring circuits which sense signals above the V^+ supply. For easy prototyping, the LMC7111 is available in a conventional 8-pin DIP package. The LMC7111 is available in two offset voltage grades, 3 mV and 7 mV. The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, and portable computers. The tiny amplifiers can be placed on a board where they are needed, simplifying board layout.

Features

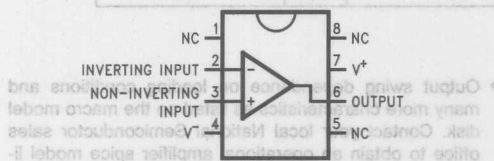
- Tiny SOT23-5 package saves space
- Very wide common mode input range
- Specified at 2.2V, 2.7V, 3V, 3.3V, 5V, and 10V
- Typical supply current 25 μ A at 5V
- 50 kHz gain-bandwidth at 5V
- Similar to popular LMC6462
- Output to within 20 mV of supply rail at 100K load
- Low input current 100 fA

Applications

- Mobile communications
- Notebooks and PDAs
- Current sensing for battery chargers
- Portable electronics
- Sensor interface
- Battery monitoring

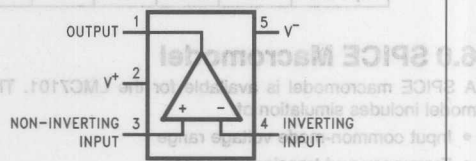
Connection Diagrams

| 8-Pin DIP | 5-Pin SOT23-5 |
|-----------------------|-----------------------|
| 1 NC | 1 OUTPUT |
| 2 INVERTING INPUT | 2 V^+ |
| 3 NON-INVERTING INPUT | 3 NON-INVERTING INPUT |
| 4 V^- | 4 INVERTING INPUT |
| 5 NC | 5 V^- |
| 6 OUTPUT | |
| 7 V^+ | |
| 8 NC | |



Top View

TL/H/12352-1

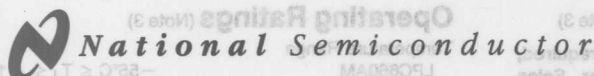


Top View

TL/H/12352-2

Ordering Information

| Package | Ordering Information | NSC Drawing Number | Package Marking | Transport Media |
|---------------|----------------------|--------------------|-----------------|----------------------------|
| 8-Pin DIP | LMC7111AIN | N08E | LMC7111AIN | Rails |
| 8-Pin DIP | LMC7111BIN | N08E | LMC7111BIN | Rails |
| 5-Pin SOT23-5 | LMC7111AIM5 | MA05A | A01A | 250 Units on Tape and Reel |
| 5-Pin SOT23-5 | LMC7111BIM5 | MA05A | A01B | 250 Units on Tape and Reel |
| 5-Pin SOT23-5 | LMC7111AIM5X | MA05A | A01A | 3K Units on Tape and Reel |
| 5-Pin SOT23-5 | LMC7111BIM5X | MA05A | A01B | 3K Units on Tape and Reel |



LPC660

Low Power CMOS Quad Operational Amplifier

General Description

The LPC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS} , drift, and broadband noise as well as voltage gain (into 100 k Ω and 5 k Ω) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 1 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC662 datasheet for a Dual CMOS operational amplifier and LPC661 datasheet for a single CMOS operational amplifier with these same features.

Applications

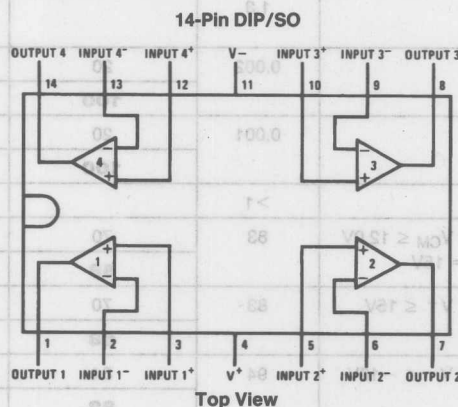
- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator

- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (1 mW)
- Specified for 100 k Ω and 5 k Ω loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μ V/ $^{\circ}$ C
- Ultra low input bias current 2 fA
- Input common-mode includes V_{-}
- Operation range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/ μ s
- Full military temp. range available

Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|--------------------------------|-------------------|------------------------|-------------|--------------------|
| | Military | Industrial | | |
| 14-Pin Side Brazed Ceramic DIP | LPC660AMD | | D14E | Rail |
| 14-Pin Small Outline | | LPC660AIM or LPC660IIM | M14A | Rail Tape and Reel |
| 14-Pin Molded DIP | | LPC660AIN or LPC660IIN | N14A | Rail |
| 14-Pin Ceramic DIP | LPC660AMJ/883 | | J14A | Rail |

Office/Distributors for availability and specifications.

| | |
|--|------------------------------------|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Output Short Circuit to V^+ | (Note 11) |
| Output Short Circuit to V^- | (Note 1) |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Storage Temp. Range | -65°C to +150°C |
| Junction Temperature (Note 2) | 150°C |
| ESD Rating (C = 100 pF, R = 1.5 k Ω) | 1000V |
| Power Dissipation | (Note 2) |
| Current at Input Pin | \pm 5 mA |
| Current at Output Pin | \pm 18 mA |
| Voltage at Input/Output Pin | (V^+) + 0.3V, (V^-) - 0.3V |
| Current at Power Supply Pin | 35 mA |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$, and $R_L > 1\text{M}$ unless otherwise specified.

| | |
|---|---|
| LPC660AI | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LPC660I | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| Supply Range | 4.75V to 15.5V |
| Power Dissipation | (Note 9) |
| Thermal Resistance (θ_{JA}), (Note 10) | |
| 14-Pin Ceramic DIP | 90°C/W |
| 14-Pin Molded DIP | 85°C/W |
| 14-Pin SO | 115°C/W |
| 14-Pin Side Braided Ceramic DIP | 90°C/W |

| Parameter | Conditions | Typ | LPC660AM LPC660AMJ/883 | LPC660AI | LPC660I | Units |
|--|---|-------------|-------------------------------|-------------------------------|-------------------------------|------------------------------|
| | | | Limit (Notes 4, 8) | Limit (Note 4) | Limit (Note 4) | |
| Input Offset Voltage | | 1 | 3 | 3 | 6 | mV |
| | | | 3.5 | 3.3 | 6.3 | max |
| Input Offset Voltage Average Drift | | 1.3 | | | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | | 0.002 | 20 | | | pA |
| | | | 100 | 4 | 4 | max |
| Input Offset Current | | 0.001 | 20 | | | pA |
| | | | 100 | 2 | 2 | max |
| Input Resistance | | > 1 | | | | Tera Ω |
| Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12.0\text{V}$ $V^+ = 15\text{V}$ | 83 | 70 | 70 | 63 | dB |
| | | | 68 | 68 | 61 | min |
| Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ | 83 | 70 | 70 | 63 | dB |
| | | | 68 | 68 | 61 | min |
| Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 84 | 84 | 74 | dB |
| | | | 82 | 83 | 73 | min |
| Input Common Mode Voltage Range | $V^+ = 5\text{V} \text{ \& \; } 15\text{V}$ For CMRR > 50 dB | -0.4 | -0.1 | -0.1 | -0.1 | V |
| | | | 0 | 0 | 0 | max |
| | | $V^+ - 1.9$ | $V^+ - 2.3$ | $V^+ - 2.3$ | $V^+ - 2.3$ | V |
| | | | $V^+ - 2.6$ | $V^+ - 2.5$ | $V^+ - 2.5$ | min |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

$V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L > 1M$ unless otherwise specified. (Continued)

| Parameter | Conditions | Typ | LPC660AM LPC660AMJ/883 | LPC660AI | LPC660I | Units |
|-------------------------------|--|--------|---------------------------|-------------------|-------------------|---------|
| | | | Limit (Notes 4, 8) | Limit (Note 4) | Limit (Note 4) | |
| Large Signal Voltage Gain | $R_L = 100\text{ k}\Omega$ (Note 5) Sourcing | 1000 | 400 | 400 | 300 | V/mV |
| | | | 250 | 300 | 200 | min |
| | Sinking | 500 | 180 | 180 | 90 | V/mV |
| | | | 70 | 120 | 70 | min |
| | $R_L = 5\text{ k}\Omega$ (Note 5) Sourcing | 1000 | 200 | 200 | 100 | V/mV |
| | | | 150 | 160 | 80 | min |
| Output Swing | $V^+ = 5V$ $R_L = 100\text{ k}\Omega$ to $V^+ / 2$ | 4.987 | 4.970 | 4.970 | 4.940 | V |
| | | | 4.950 | 4.950 | 4.910 | min |
| | $V^+ = 5V$ $R_L = 5\text{ k}\Omega$ to $V^+ / 2$ | 4.940 | 4.850 | 4.850 | 4.750 | V |
| | | | 4.750 | 4.750 | 4.650 | min |
| | $V^+ = 15V$ $R_L = 100\text{ k}\Omega$ to $V^+ / 2$ | 14.970 | 14.920 | 14.920 | 14.880 | V |
| | | | 14.880 | 14.880 | 14.820 | min |
| Output Current $V^+ = 5V$ | Sourcing, $V_O = 0V$ | 22 | 16 | 16 | 13 | mA |
| | | | 12 | 14 | 11 | min |
| | Sinking, $V_O = 5V$ | 21 | 16 | 16 | 13 | mA |
| | | | 12 | 14 | 11 | min |
| Output Current $V^+ = 15V$ | Sourcing, $V_O = 0V$ | 40 | 19 | 28 | 23 | mA |
| | | | 19 | 25 | 20 | min |
| | Sinking, $V_O = 13V$ (Note 11) | 39 | 19 | 28 | 23 | mA |
| | | | 19 | 24 | 19 | min |
| Supply Current | All Four Amplifiers $V_O = 1.5V$ | 160 | 200 | 200 | 240 | μA |
| | | | 250 | 230 | 270 | max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5$, and $R_L > 1\text{M}$ unless otherwise specified.

| Parameter | Conditions | Typ | LPC660AM LPC660AMJ/883 | LPC660AI | LPC660I | Units |
|------------------------------|--|-------------------|---------------------------|-------------|-------------|------------------------|
| Limit (Notes 4, 8) | Limit (Note 4) | Limit (Note 4) | | | | |
| Slew Rate | (Note 6) | 0.11 | 0.07 | 0.07 | 0.05 | V/ μs |
| | | | 0.04 | 0.05 | 0.03 | min |
| Gain-Bandwidth Product | | 0.35 | | | | MHz |
| Phase Margin | | 50 | | | | Deg |
| Gain Margin | | 17 | | | | dB |
| Amp-to-Amp Isolation | (Note 7) | 130 | | | | dB |
| Input Referred Voltage Noise | $F = 1\text{ kHz}$ | 42 | | | | nV/ $\sqrt{\text{Hz}}$ |
| Input Referred Current Noise | $F = 1\text{ kHz}$ | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion | $F = 1\text{ kHz}$, $A_V = -10$, $R_L = 100\text{ k}\Omega$, $V_O = 8\text{ V}_{PP}$ | 0.01 | | | | % |

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 6: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15\text{V}$ and $R_L = 100\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{PP}$.

Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC660AMJ/883 RETS specification complied fully with the boldface limits in this column. The LPC660AMJ/883 may also be procured to a Standard Military Drawing specification.

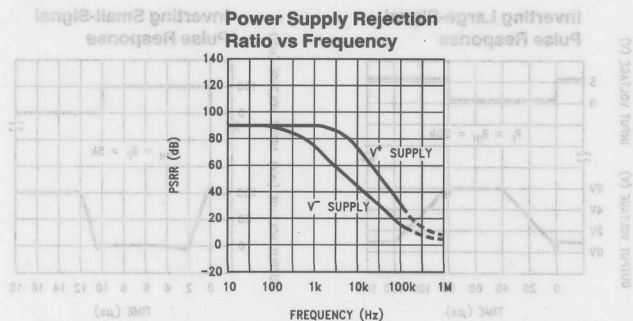
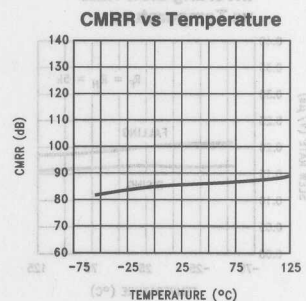
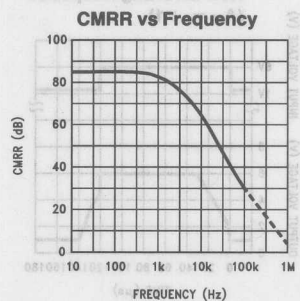
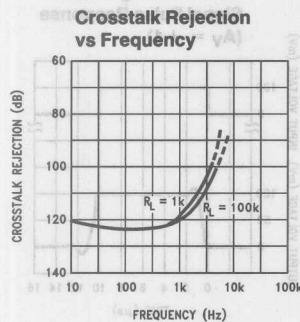
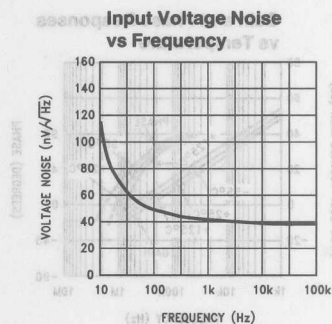
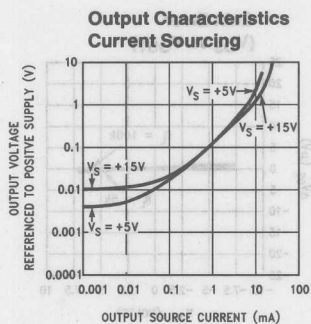
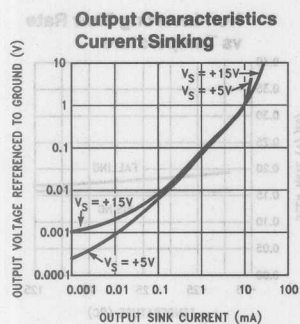
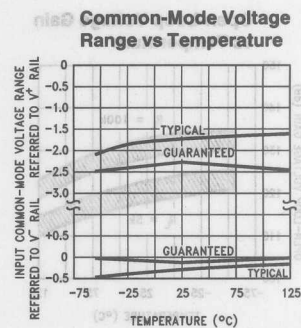
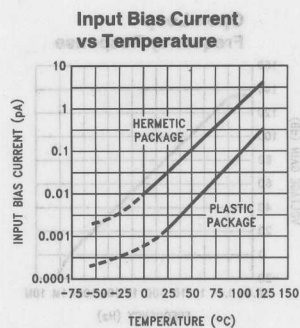
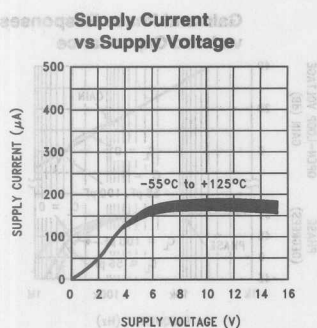
Note 9: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

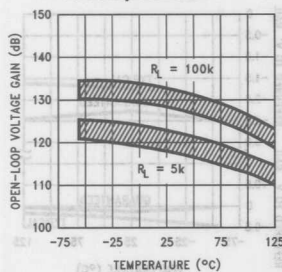
| | | | | | | |
|----------------|------|------|------|-----|---|--------------------|
| V | 0.85 | 0.85 | 0.85 | 1.4 | $V^+ = 15\text{V}$ $R_L = 5\text{ k}\Omega$ to $V^+/2$ | |
| min | 0.85 | 0.85 | 0.85 | 1.4 | | |
| V | 0.35 | 0.35 | 0.35 | 0.1 | | |
| max | 0.4 | 0.4 | 0.4 | 0.1 | | |
| Am | 18 | 18 | 18 | 22 | Sourcing $V_O = 0\text{V}$ | Output Current |
| min | 18 | 18 | 18 | 22 | | $V^+ = 5\text{V}$ |
| Am | 18 | 18 | 18 | 21 | Sinking $V_O = 8\text{V}$ | |
| min | 18 | 18 | 18 | 21 | | |
| Am | 23 | 23 | 19 | 40 | Sourcing $V_O = 0\text{V}$ | Output Current |
| min | 23 | 23 | 19 | 40 | | $V^+ = 15\text{V}$ |
| Am | 23 | 23 | 19 | 39 | Sinking $V_O = 13\text{V}$ | |
| min | 19 | 24 | 21 | 39 | (Note 11) | |
| A _q | 240 | 200 | 200 | 180 | All Four Amplifiers | Supply Current |
| max | 270 | 230 | 230 | 180 | $V_O = 1.5\text{V}$ | |

Typical Performance Characteristics $V_S = \pm 7.5V, T_A = 25^\circ C$ unless otherwise specified

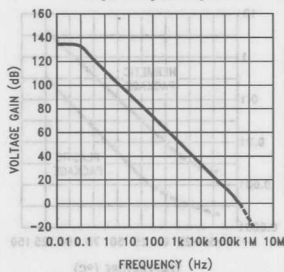


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

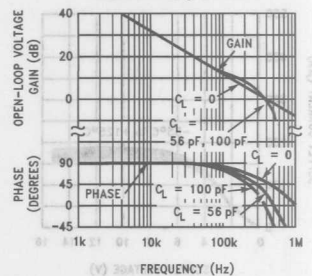
Open-Loop Voltage Gain vs Temperature



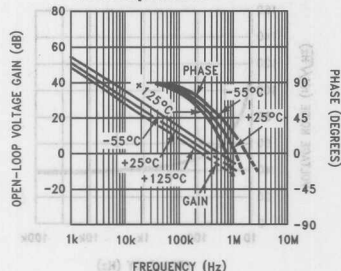
Open-Loop Frequency Response



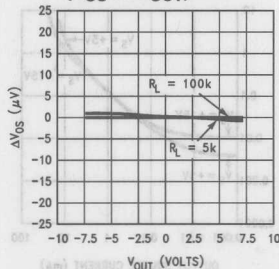
Gain and Phase Responses vs Load Capacitance



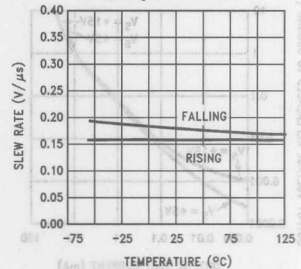
Gain and Phase Responses vs Temperature



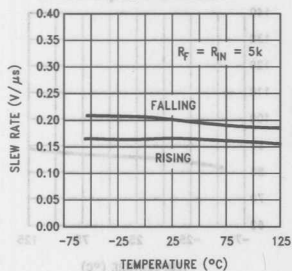
Gain Error (V_{OS} vs V_{OUT})



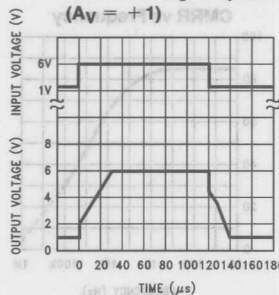
Non-Inverting Slew Rate vs Temperature



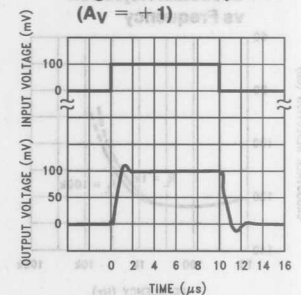
Inverting Slew Rate vs Temperature



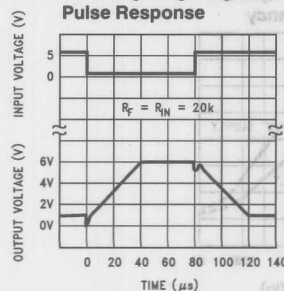
Large-Signal Pulse Non-Inverting Response ($A_v = +1$)



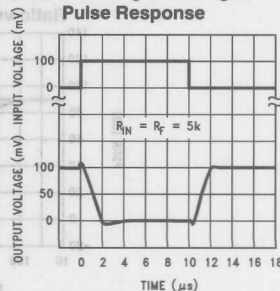
Non-Inverting Small Signal Pulse Response ($A_v = +1$)



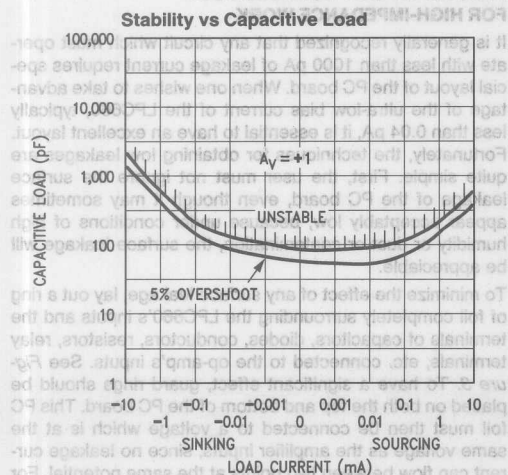
Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response



Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ (Continued)



Note: Avoid resistive loads of less than 500Ω , as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC660 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

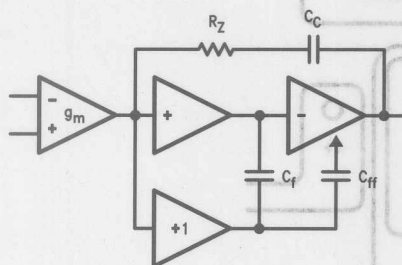
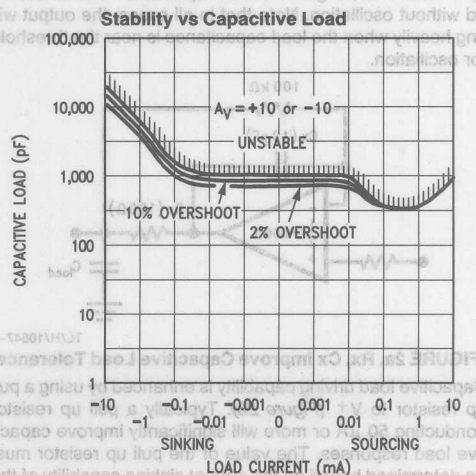


FIGURE 1. LPC660 Circuit Topology (Each Amplifier)



The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least $5k\Omega$. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of $5k\Omega$ or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500Ω without instability.

COMPENSATING INPUT CAPACITANCE

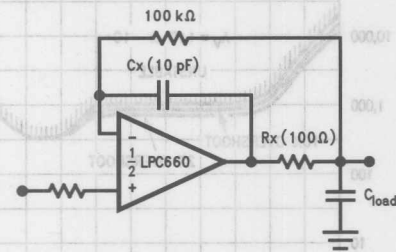
Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor ($5pF$ to $10pF$) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

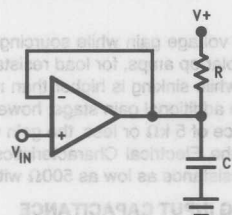
for oscillation.



TL/H/10547-7

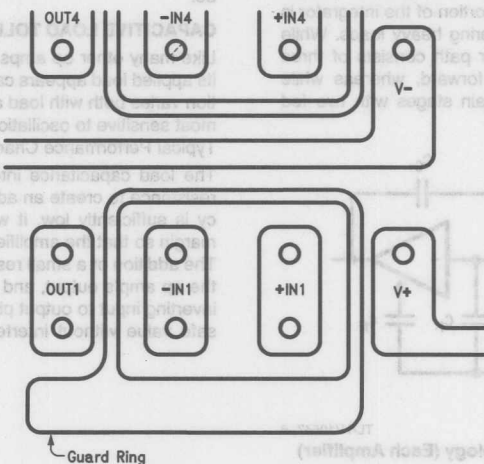
FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



TL/H/10547-26

FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor



TL/H/10547-19

FIGURE 3. Example of Guard Ring in P.C. Board Layout using the LPC660

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC660, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 4d.

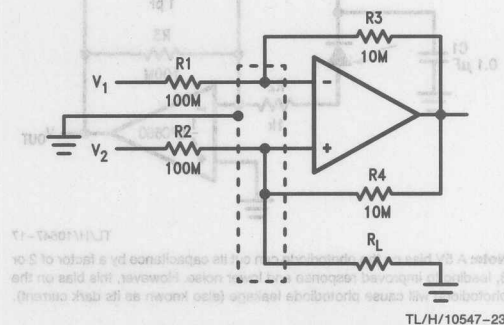
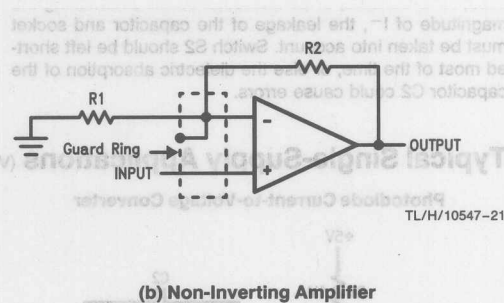
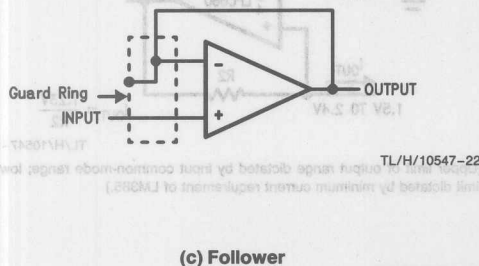
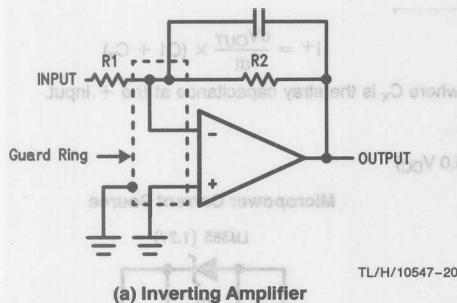


FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

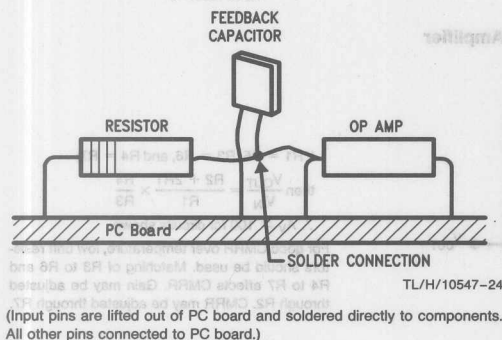


FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 6 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C_2$$

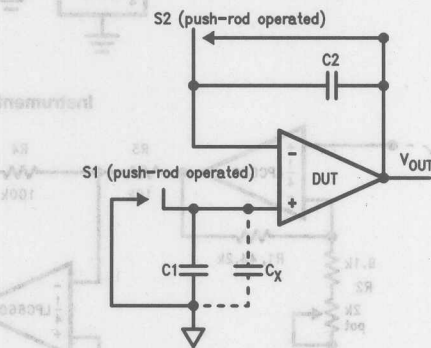


FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^- , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

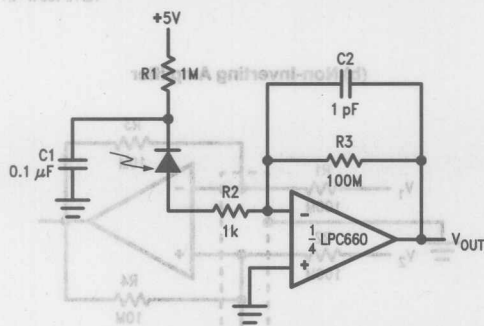
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

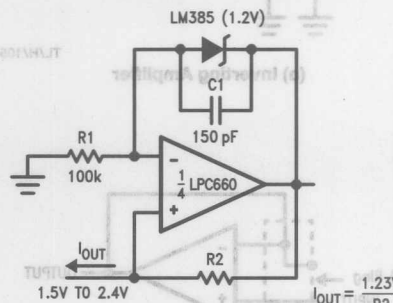
Photodiode Current-to-Voltage Converter



TL/H/10547-17

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

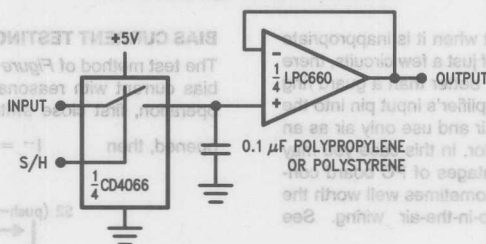
Micropower Current Source



TL/H/10547-18

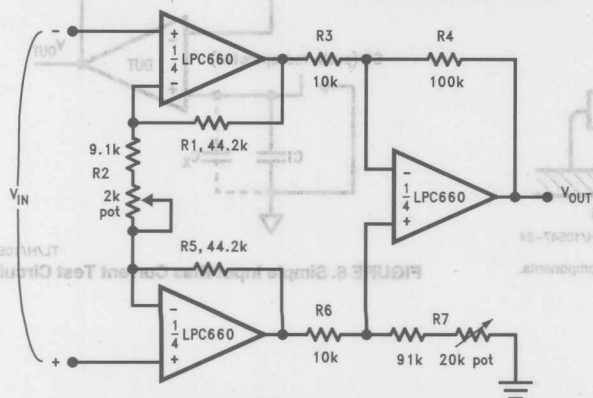
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



TL/H/10547-8

Instrumentation Amplifier



TL/H/10547-9

If $R1 = R5$, $R3 = R6$, and $R4 = R7$;

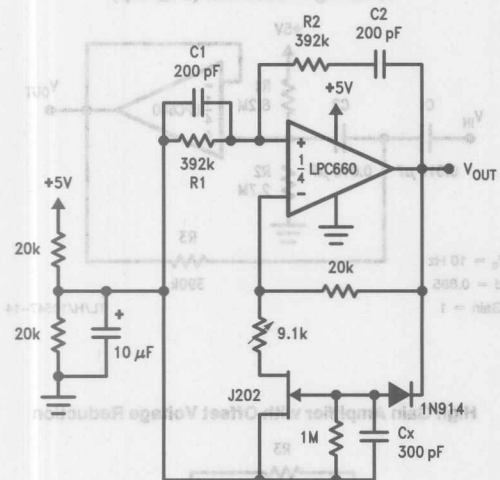
$$\text{then } \frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R1} \times \frac{R4}{R3}$$

$\therefore A_v \approx 100$ for circuits shown.

For good CMRR over temperature, low drift resistors should be used. Matching of $R3$ to $R6$ and $R4$ to $R7$ affects CMRR. Gain may be adjusted through $R2$. CMRR may be adjusted through $R7$.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DO}$) (Continued)

Sine-Wave Oscillator



TL/H/10547-10

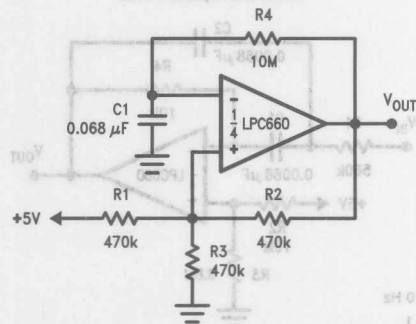
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{osc} = 1/2\pi RC$$

where $R = R1 = R2$ and $C = C1 = C2$.

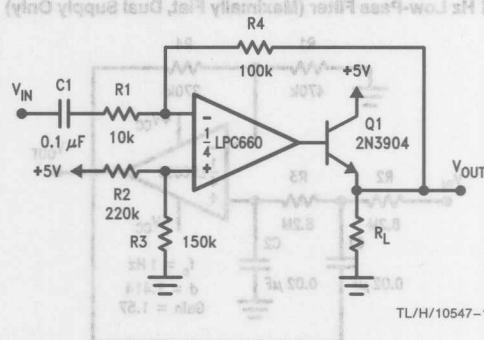
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



TL/H/10547-11

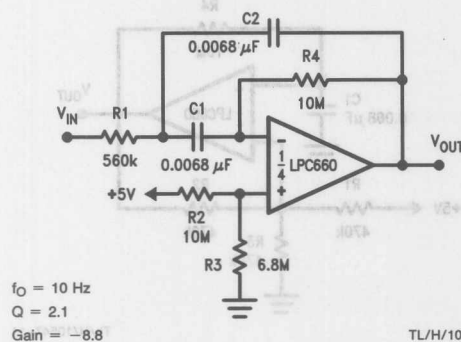
Power Amplifier



TL/H/10547-12

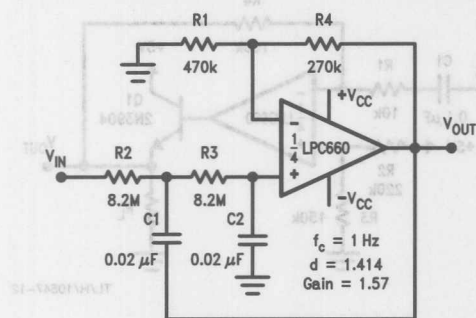
Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

10 Hz Bandpass Filter



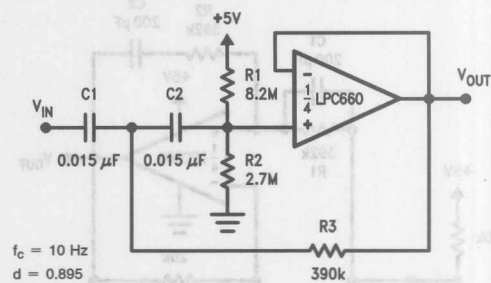
TL/H/10547-13

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



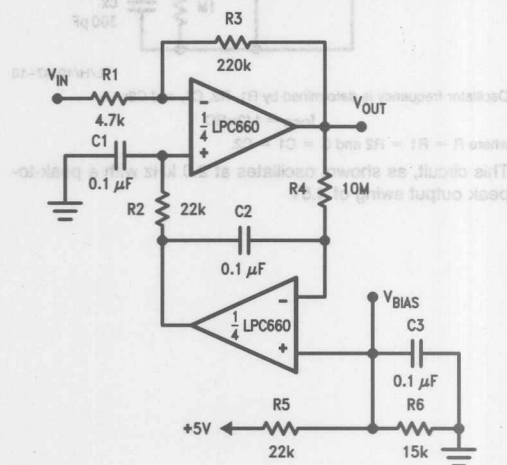
TL/H/10547-15

10 Hz High-Pass Filter (2 dB Dip)



TL/H/10547-14

High Gain Amplifier with Offset Voltage Reduction



TL/H/10547-16

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS} .

LPC661

Low Power CMOS Operational Amplifier

General Description

The LPC661 CMOS operational amplifier is ideal for operation from a single supply. It features a wide range of operating supply voltage from +5V to +15V, rail-to-rail output swing and an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS} , drift, and broadband noise as well as voltage gain (into 100 k Ω and 5 k Ω) are all equal to or better than widely accepted bipolar equivalents, while the supply current requirement is typically 55 μ A.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier or the LPC662 data sheet for a Dual CMOS operational amplifier with these same features.

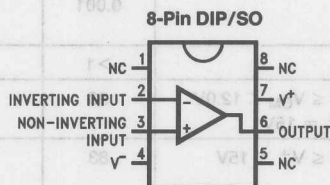
Features

(Typical unless otherwise noted)

- Rail-to-rail output swing
- Low supply current
- Specified for 100 k Ω and 5 k Ω loads

55 μ A

Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|---------------------|-----------------------------|------------------------------|-------------|-----------------------|
| | Military -55°C to +125°C | Industrial -40°C to +85°C | | |
| 8-Pin Small Outline | | LPC661AIM LPC661IM | M08A | Tape and Reel Rail |
| 8-Pin Molded DIP | LPC661AMN | LPC661AIN LPC661IN | N08E | Rail |

- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μ V/°C
- Ultra low input bias current 2 fA
- Input common-mode range includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/ μ s

Applications

- High-impedance buffer
- Precision current-to-voltage converter
- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) 16V
Differential Input Voltage \pm Supply Voltage
Output Short Circuit to V^+ (Note 9)
Output Short Circuit to V^- (Note 2)
Storage Temperature Range -65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 10 sec.) 260°C
Junction Temperature (Note 3) 150°C
Power Dissipation (Note 3)
ESD Rating ($C=100\text{ pF}$, $R=1.5\text{ k}\Omega$) 1000V

Current at Output Pin $\pm 18\text{ mA}$
Voltage Input/Output Pin (V^+) $+0.3\text{V}$, (V^-) -0.3V
Current at Power Supply Pin 35 mA

Operating Ratings (Note 1)

Supply Voltage $4.75\text{V} \leq V^+ \leq 15.5\text{V}$
Junction Temperature Range
LPC661AM $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$
LPC661AI $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
LPC661I $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ (Note 7)
Power Dissipation
Thermal Resistance (θ_{JA}) (Note 8)
8-Pin DIP 101°C/W
8-Pin SO 165°C/W

DC Electrical Characteristics

The following specifications apply for $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$, and $R_L = 1\text{M}$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ\text{C}$.

| Symbol | Parameter | Conditions | Typ | LPC661AM Limit (Note 4) | LPC661AI Limit (Note 4) | LPC661I Limit (Note 4) | Units (Limit) |
|------------|--|--|-------------|--|--|--|------------------------------|
| V_{OS} | Input Offset Voltage | | 1 | 3 3.5 | 3 3.3 | 6 6.3 | mV |
| TCV_{OS} | Input Offset Voltage Average Drift | | 1.3 | | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 0.002 | 20 100 | | | pA max |
| I_{OS} | Input Offset Current | | 0.001 | 20 100 | 2 | 2 | pA max |
| R_{IN} | Input Resistance | | >1 | | | | Tera Ω |
| CMRR | Common Mode Rejection Ratio | $0\text{V} \leq V_{CM} \leq 12.0\text{V}$ $V^+ = 15\text{V}$ | 83 | 70 68 | 70 68 | 63 61 | dB min |
| +PSRR | Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ | 83 | 70 68 | 70 68 | 63 61 | dB min |
| -PSRR | Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 84 82 | 84 83 | 74 73 | dB min |
| V_{CM} | Input Common Mode Voltage Range | $V^+ = 5\text{V}$ and 15V for CMRR $\geq 50\text{ dB}$ | -0.4 | -0.1 0 | -0.1 0 | -0.1 0 | V max |
| | | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.6$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.5$ | V min |
| A_V | Large Signal Voltage Gain | Sourcing $R_L = 100\text{ k}\Omega$ (Note 5) | 1000 | 400 250 | 400 300 | 300 200 | V/mV min |
| | | Sinking $R_L = 100\text{ k}\Omega$ (Note 5) | 500 | 180 70 | 180 120 | 90 70 | V/mV min |
| | | Sourcing $R_L = 5\text{ k}\Omega$ (Note 5) | 1000 | 200 150 | 200 160 | 100 80 | V/mV min |
| | | Sinking $R_L = 5\text{ k}\Omega$ (Note 5) | 250 | 100 35 | 100 60 | 50 40 | V/mV min |

DC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted. **Boldface** limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$. (Continued)

| Symbol | Parameter | Conditions | Typ | LPC661AM Limit (Note 4) | LPC661AI Limit (Note 4) | LPC661I Limit (Note 4) | Units (Limit) |
|--------|-------------------------------|---|--------|-------------------------------|-------------------------------|------------------------------|------------------|
| V_O | Output Swing | $V^+ = 5V$ $R_L = 100\text{ k}\Omega$ to $2.5V$ | 4.987 | 4.970 4.950 | 4.970 4.950 | 4.940 4.910 | V min |
| | | | 0.004 | 0.030 0.050 | 0.030 0.050 | 0.060 0.090 | V max |
| | | | 4.940 | 4.850 4.750 | 4.850 4.750 | 4.750 4.650 | V min |
| | | $V^+ = 5V$ $R_L = 5\text{ k}\Omega$ to $2.5V$ | 0.040 | 0.150 0.250 | 0.150 0.250 | 0.250 0.350 | V max |
| | | | 14.970 | 14.920 14.880 | 14.920 14.880 | 14.880 14.820 | V min |
| | | | 0.007 | 0.030 0.050 | 0.030 0.050 | 0.060 0.090 | V max |
| | | $V^+ = 15V$ $R_L = 100\text{ k}\Omega$ to $7.5V$ | 14.840 | 14.680 14.600 | 14.680 14.600 | 14.580 14.480 | V min |
| | | | 0.110 | 0.220 0.300 | 0.220 0.300 | 0.320 0.400 | V max |
| | | | | | | | |
| | | | | | | | |
| I_O | Output Current $V^+ = 5V$ | Sourcing, $V_O = 0V$ | 22 | 16 12 | 16 14 | 13 11 | mA min |
| | | Sinking, $V_O = 5V$ | 21 | 16 12 | 16 14 | 13 11 | mA min |
| I_O | Output Current $V^+ = 15V$ | Sourcing, $V_O = 0V$ | 40 | 19 19 | 28 25 | 23 20 | mA min |
| | | Sinking, $V_O = 13V$ (Note 9) | 39 | 19 19 | 28 24 | 23 19 | mA min |
| I_S | Supply Current | $V^+ = 5V$, $V_O = 1.5V$ | 55 | 60 70 | 60 70 | 70 85 | μA max |
| | | $V^+ = 15V$, $V_O = 1.5V$ | 58 | 75 85 | 75 85 | 90 105 | μA max |

AC Electrical Characteristics

The following specifications apply for $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$, and $R_L = 1M$ unless otherwise noted.

Boldface limits apply at the temperature extremes; all other limits $T_J = 25^\circ C$.

| Symbol | Parameter | Conditions | Typ | LPC661AM Limit (Note 4) | LPC661AI Limit (Note 4) | LPC661I Limit (Note 4) | Units (Limit) |
|----------|------------------------------|--|--------|-------------------------------|-------------------------------|------------------------------|-------------------|
| SR | Slew Rate | (Note 6) | 0.11 | 0.07 | 0.07 | 0.05 | V/ μs min |
| GBW | Gain-Bandwidth Product | | 350 | | | | kHz |
| ϕ_m | Phase Margin | | 50 | | | | Deg |
| G_M | Gain Margin | | 17 | | | | dB |
| e_n | Input Referred Voltage Noise | $F = 1 \text{ kHz}$ | 42 | | | | nV/ \sqrt{Hz} |
| i_n | Input Referred Current Noise | $F = 1 \text{ kHz}$ | 0.0002 | | | | pA/ \sqrt{Hz} |
| T.H.D. | Total Harmonic Distortion | $F = 1 \text{ kHz}$, $A_V = -10$ $R_L = 100 \text{ k}\Omega$, $V_O = 8 \text{ V}_{pp}$ $V^+ = 15V$ | 0.01 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 2: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of $150^\circ C$. Output currents in excess of $\pm 30 \text{ mA}$ over long term may adversely affect reliability.

Note 3: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A) / \theta_{JA}$.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to $7.5V$. For sourcing tests, $7.5V \leq V_O \leq 11.5V$. For sinking tests, $2.5V \leq V_O \leq 7.5V$.

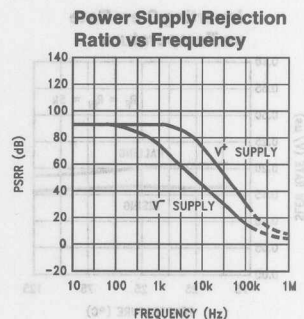
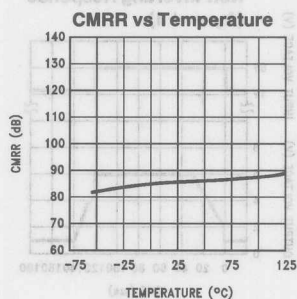
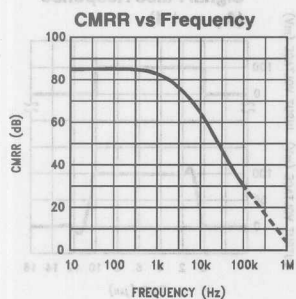
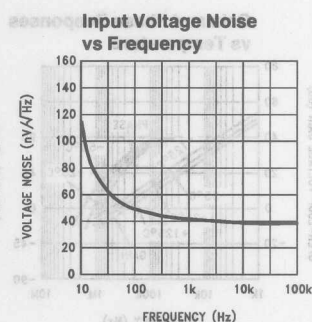
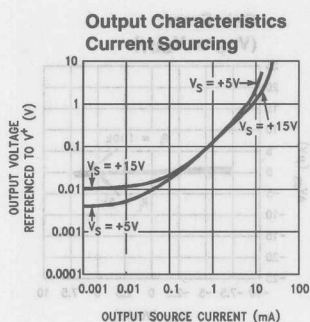
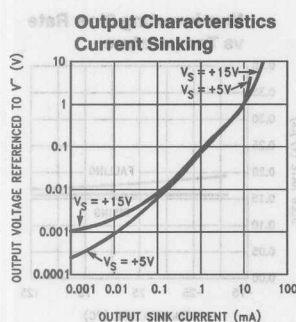
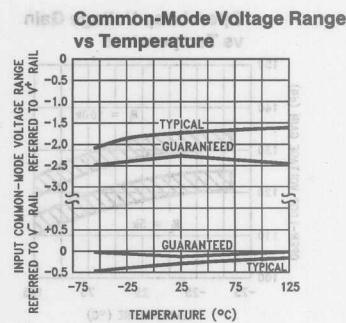
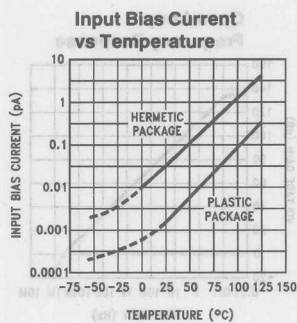
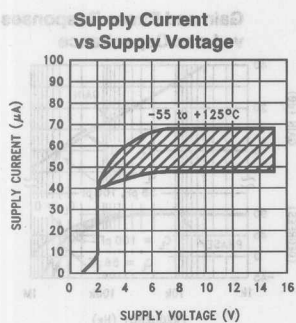
Note 6: $V^+ = 15V$. Connected as Voltage Follower with $10V$ step input. Number specified is the slower of the positive and negative slew rates.

Note 7: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A) / \theta_{JA}$.

Note 8: All numbers apply for packages soldered directly into a PC board.

Note 9: Do not connect output to V^+ when V^+ is greater than $13V$ or reliability may be adversely affected.

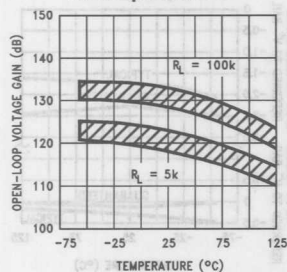
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified



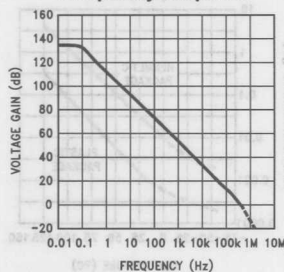
TL/H/11227-2

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

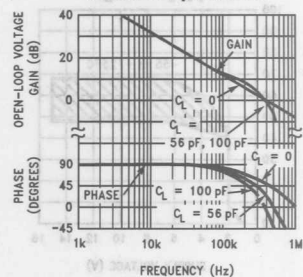
Open-Loop Voltage Gain vs Temperature



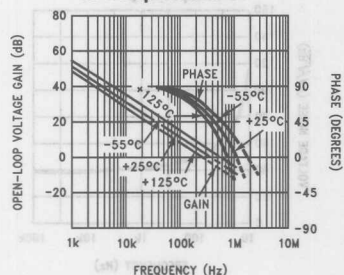
Open-Loop Frequency Response



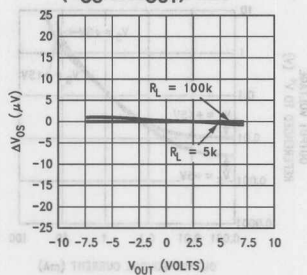
Gain and Phase Responses vs Load Capacitance



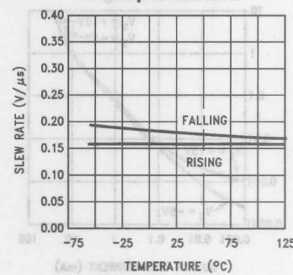
Gain and Phase Responses vs Temperature



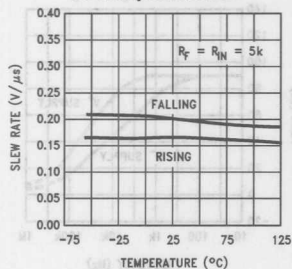
Gain Error (V_{OS} vs V_{OUT})



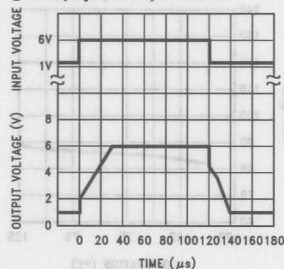
Non-Inverting Slew Rate vs Temperature



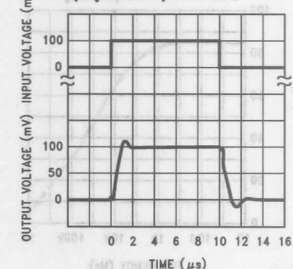
Inverting Slew Rate vs Temperature



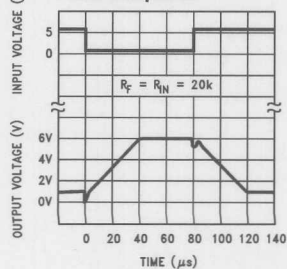
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



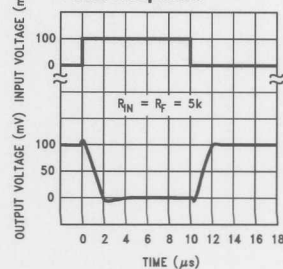
Non-Inverting Small Signal Pulse Response ($A_V = +1$)

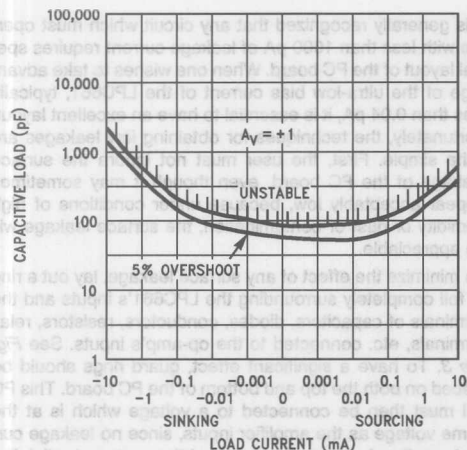


Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response





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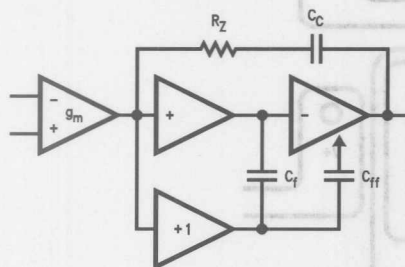
Note: Avoid resistive loads of less than 500 Ω , as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

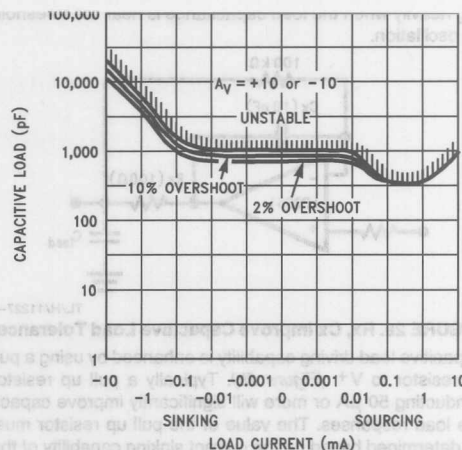
The topology chosen for the LPC661 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.



TL/H/11227-6

FIGURE 1. LPC661 Circuit Topology



TL/H/11227-5

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, for load resistance of at least 5 k Ω . The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 k Ω or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500 Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

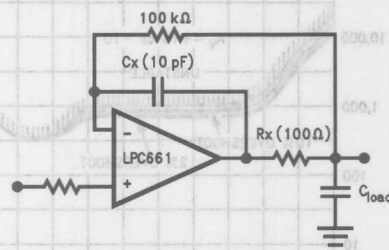
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC661 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

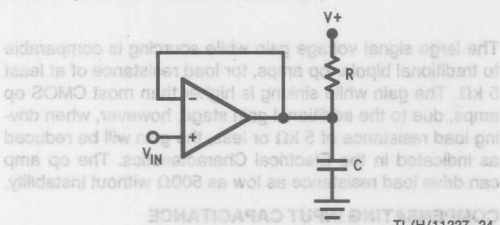
operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/11227-7

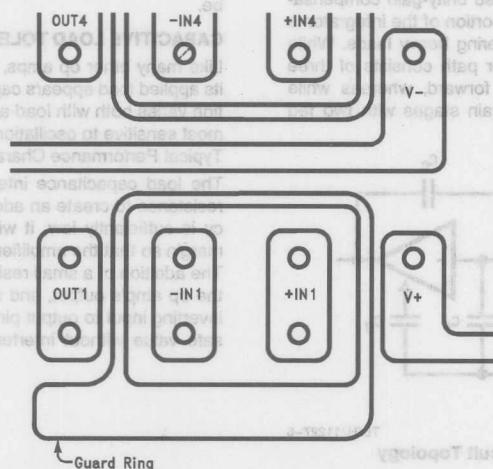
FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting 50 μ A or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



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FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor



TL/H/11227-8

FIGURE 3. Example of Guard Ring in P.C. Board Layout, Using the LPC660

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC661, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC661's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 4d.

Application Hints (Continued)

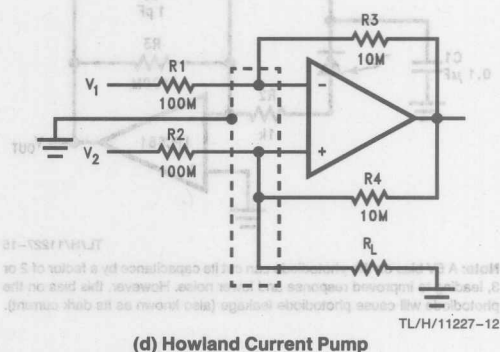
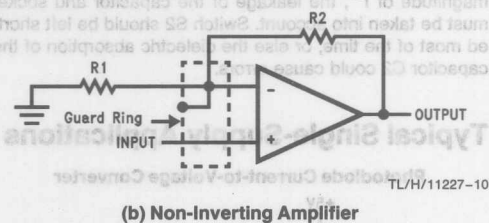
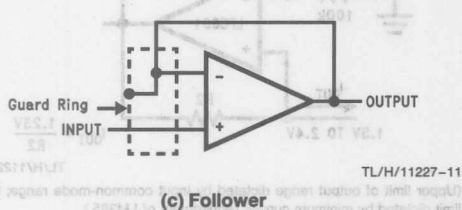
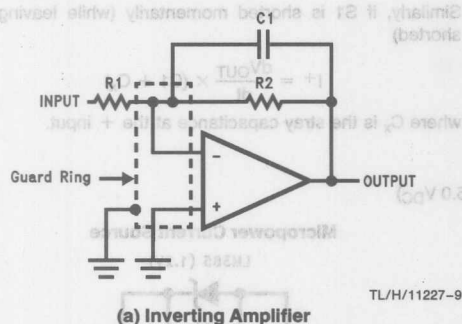
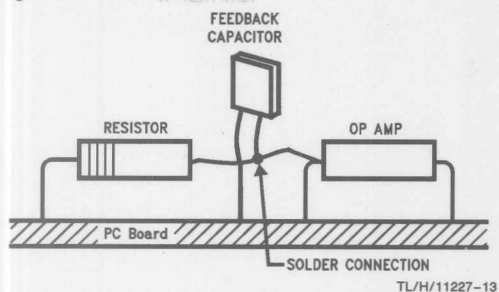


FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 5. Air Wiring

BIAS CURRENT TESTING

The test method of Figure 6 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

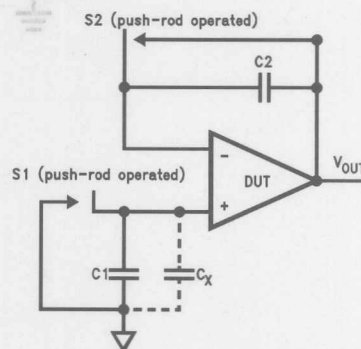


FIGURE 6. Simple Input Bias Current Test Circuit

Application Hints (Continued)

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I^- , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

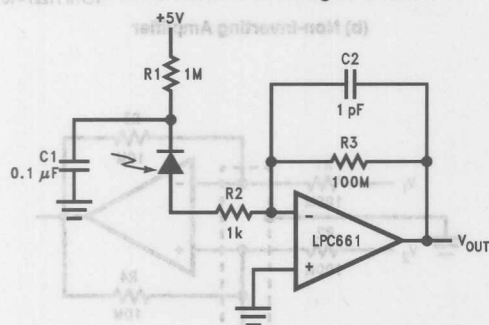
Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I^+ = \frac{dV_{OUT}}{dt} \times (C_1 + C_x)$$

where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$)

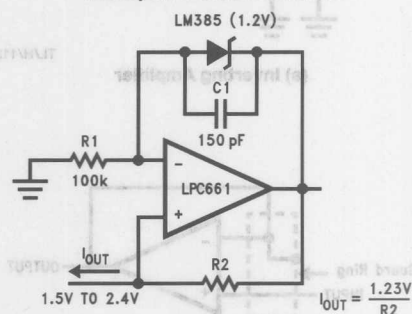
Photodiode Current-to-Voltage Converter



TL/H/11227-15

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

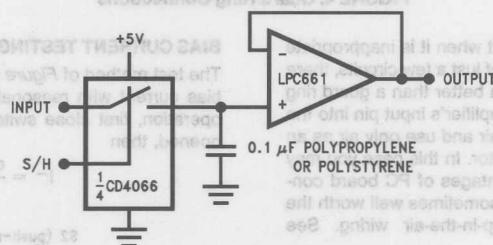
Micropower Current Source



TL/H/11227-16

(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

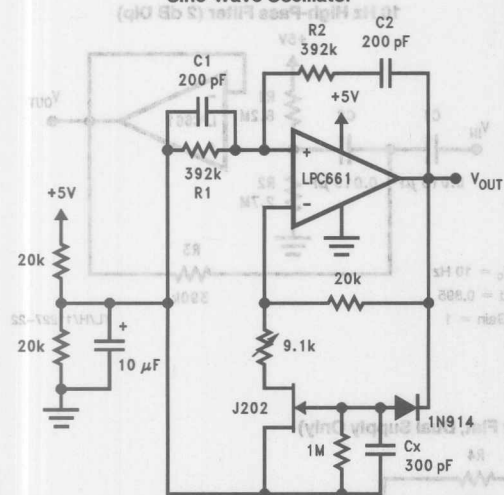
Low-Leakage Sample-and-Hold



TL/H/11227-17

Typical Single-Supply Applications ($V^+ = 5.0 V_{DC}$) (Continued)

Sine-Wave Oscillator



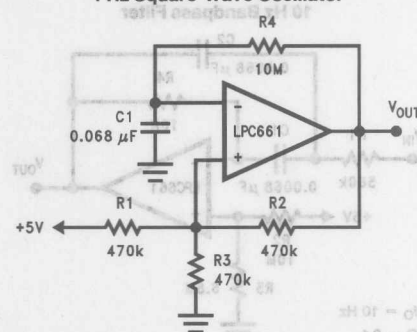
Oscillator frequency is determined by R_1 , R_2 , C_1 , and C_2 :

$$f_{osc} = 1/2\pi RC$$

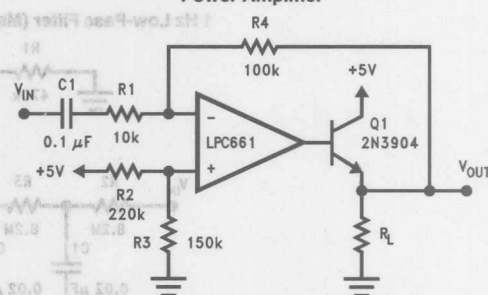
where $R = R_1 = R_2$ and $C = C_1 = C_2$.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator

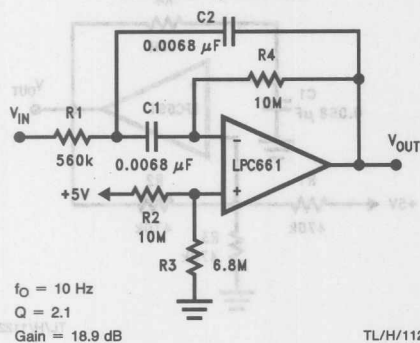


Power Amplifier



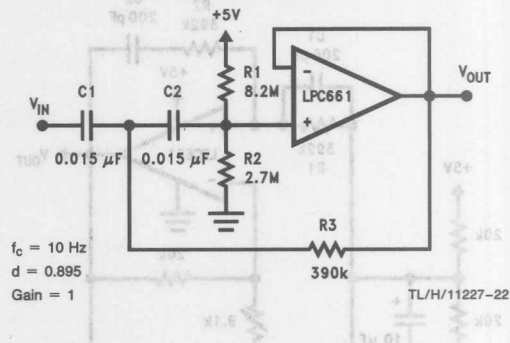
Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

10 Hz Bandpass Filter



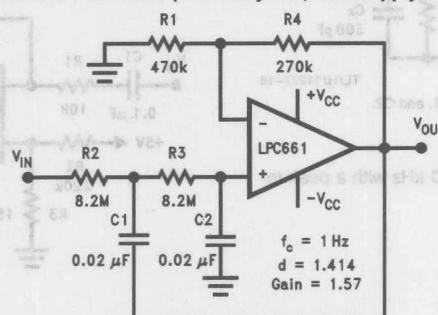
TL/H/11227-21

10 Hz High-Pass Filter (2 dB Dip)



TL/H/11227-22

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



TL/H/11227-23

LPC662

Low Power CMOS Dual Operational Amplifier

General Description

The LPC662 CMOS Dual operational amplifier is ideal for operation from a single supply. It features a wide range of operating voltage from +5V to +15V, rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS} , drift, and broadband noise as well as voltage gain (into 100 k Ω and 5 k Ω) are all equal to or better than widely accepted bipolar equivalents, while the power supply requirement is typically less than 0.5 mW.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LPC660 datasheet for a Quad CMOS operational amplifier and LPC661 for a single CMOS operational amplifier with these same features.

Applications

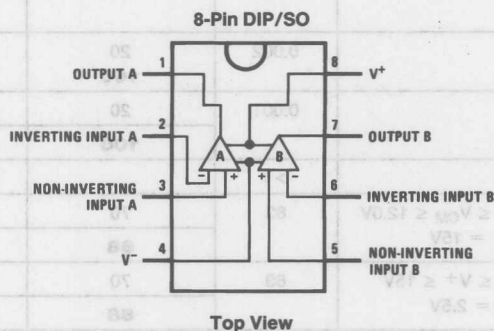
- High-impedance buffer
- Precision current-to-voltage converter

- Long-term integrator
- High-impedance preamplifier
- Active filter
- Sample-and-Hold circuit
- Peak detector

Features

- Rail-to-rail output swing
- Micropower operation (<0.5 mW)
- Specified for 100 k Ω and 5 k Ω loads
- High voltage gain 120 dB
- Low input offset voltage 3 mV
- Low offset voltage drift 1.3 μ V/ $^{\circ}$ C
- Ultra low input bias current 2 fA
- Input common-mode includes GND
- Operating range from +5V to +15V
- Low distortion 0.01% at 1 kHz
- Slew rate 0.11 V/ μ s
- Full military temperature range available

Connection Diagram



Ordering Information

| Package | Temperature Range | | NSC Drawing | Transport Media |
|-------------------------------|-------------------|-----------------------|-------------|--------------------|
| | Military | Industrial | | |
| 8-Pin Side Brazed Ceramic DIP | LPC662AMD | | D08C | Rail |
| 8-Pin Small Outline | | LPC662AIM or LPC662IM | M08A | Rail Tape and Reel |
| 8-Pin Molded DIP | | LPC662AIN or LPC662IN | N08E | Rail |
| 8-Pin Ceramic DIP | LPC662AMJ/883 | | J08A | Rail |

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------|----------------------|
| Differential Input Voltage | \pm Supply Voltage |
| Supply Voltage ($V^+ - V^-$) | 16V |

Output Short Circuit to V^+ (Note 11)

Output Short Circuit to V- (Note 1)

Lead Temperature (Soldering, 10 sec.) 260°C

Storage Temp. Range -65°C to $+150^{\circ}\text{C}$

Junction Temperature 150°C

ESD Rating (C = 100 pF, R = 1.5 k Ω) 1000V

Power Dissipation (Note 2)

Current at Input Pin ± 5 mA

Current at Output Pin $\pm 18 \text{ mA}$

Current at Power Supply Pin 35 mA

Voltage at Input/Output Pin (V⁺) + 0.3V, (V⁻) - 0.3V

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

Operating Ratings (Note 3)

Temperature Range

LPC662AMJ/883 $-55^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$

LPC662AM $-55^{\circ}\text{C} \leq T_J \leq +125^{\circ}\text{C}$ LPC662AI $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$ LPC662I $-40^{\circ}\text{C} \leq T_J \leq +85^{\circ}\text{C}$

Supply Range 4.75V to 15.5V

Power Dissipation (Note 9)

Thermal Resistance (θ_{JA}) (Note 10)

8-Pin Ceramic DIP 100°C/W

8-Pin Molded DIP 101°C/W

8-Pin SO 165°C/W

8-Pin Side Brazed Ceramic DIP 100°C/W

| Parameter | Conditions | Type | LPC662AM LPC662AMJ/883 Limit (Notes 4, 8) | LPC662AI Limit (Note 4) | LPC662I Limit (Note 4) | Units |
|--|--|-------------|--|--|--|------------------------------|
| Input Offset Voltage | | 1 | 3 | 3 | 6 | mV |
| | | | 3.5 | 3.3 | 6.3 | max |
| Input Offset Voltage Average Drift | | 1.3 | | | | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | | 0.002 | 20 100 | 4 | 4 | pA max |
| Input Offset Current | | 0.001 | 20 100 | 2 | 2 | pA max |
| Input Resistance | | > 1 | | | | Tera Ω |
| Common Mode Rejection Ratio | $0\text{V} \leq V_{\text{CM}} \leq 12.0\text{V}$ $V^+ = 15\text{V}$ | 83 | 70 68 | 70 68 | 63 61 | dB min |
| Positive Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 15\text{V}$ $V_O = 2.5\text{V}$ | 83 | 70 68 | 70 68 | 63 61 | dB min |
| Negative Power Supply Rejection Ratio | $0\text{V} \leq V^- \leq -10\text{V}$ | 94 | 84 82 | 84 83 | 74 73 | dB min |
| Input Common-Mode Voltage Range | $V^+ = 5\text{V}$ and 15V For CMRR $\geq 50\text{ dB}$ | -0.4 | -0.1 0 | -0.1 0 | -0.1 0 | V max |
| | | $V^+ - 1.9$ | $V^+ - 2.3$ $V^+ - 2.6$ | $V^+ - 2.3$ $V^+ - 2.5$ | $V^+ - 2.3$ $V^+ - 2.5$ | V min |
| | | | | | | |
| | | | | | | |
| | | | | | | |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified. (Continued)

| Parameter | Conditions | Typ | LPC662AM LPC662AMJ/883 Limit (Notes 4, 8) | LPC662AI Limit (Note 4) | LPC662I Limit (Note 4) | Units |
|--------------------------------------|---|--------|--|-------------------------------|------------------------------|---------------|
| Large Signal Voltage Gain | $R_L = 100\text{ k}\Omega$ (Note 5) Sourcing | 1000 | 400 | 400 | 300 | V/mV |
| | | | 250 | 300 | 200 | min |
| | Sinking | 500 | 180 | 180 | 90 | V/mV |
| | | | 70 | 120 | 70 | min |
| | $R_L = 5\text{ k}\Omega$ (Note 5) | 1000 | 200 | 200 | 100 | V/mV |
| Slew Rate | Sourcing | | 150 | 160 | 80 | min |
| | Sinking | 250 | 100 | 100 | 50 | V/mV |
| | | | 35 | 60 | 40 | min |
| Output Swing | $V^+ = 5\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+ / 2$ | 4.987 | 4.970 | 4.970 | 4.940 | V |
| | | | 4.950 | 4.950 | 4.910 | min |
| | | 0.004 | 0.030 | 0.030 | 0.060 | V |
| | | | 0.050 | 0.050 | 0.090 | max |
| | $V^+ = 5\text{V}$ $R_L = 5\text{ k}\Omega$ to $V^+ / 2$ | 4.940 | 4.850 | 4.850 | 4.750 | V |
| | | | 4.750 | 4.750 | 4.650 | min |
| | | 0.040 | 0.150 | 0.150 | 0.250 | V |
| | | | 0.250 | 0.250 | 0.350 | max |
| | $V^+ = 15\text{V}$ $R_L = 100\text{ k}\Omega$ to $V^+ / 2$ | 14.970 | 14.920 | 14.920 | 14.880 | V |
| | | | 14.880 | 14.880 | 14.820 | min |
| | | 0.007 | 0.030 | 0.030 | 0.060 | V |
| | | | 0.050 | 0.050 | 0.090 | max |
| | $V^+ = 15\text{V}$ $R_L = 5\text{ k}\Omega$ to $V^+ / 2$ | 14.840 | 14.680 | 14.680 | 14.580 | V |
| | | | 14.600 | 14.600 | 14.480 | min |
| | | 0.110 | 0.220 | 0.220 | 0.320 | V |
| | | | 0.300 | 0.300 | 0.400 | max |
| Output Current $V^+ = 5\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 22 | 16 | 16 | 13 | mA |
| | | | 12 | 14 | 11 | min |
| | Sinking, $V_O = 5\text{V}$ | 21 | 16 | 16 | 13 | mA |
| | | | 12 | 14 | 11 | min |
| Output Current $V^+ = 15\text{V}$ | Sourcing, $V_O = 0\text{V}$ | 40 | 19 | 28 | 23 | mA |
| | | | 19 | 25 | 20 | min |
| | Sinking, $V_O = 13\text{V}$ (Note 11) | 39 | 19 | 28 | 23 | mA |
| | | | 19 | 24 | 19 | min |
| Supply Current | Both Amplifiers $V_O = 1.5\text{V}$ | 86 | 120 | 120 | 140 | μA |
| | | | 145 | 140 | 160 | max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}$ unless otherwise specified.

| Parameter | Conditions | Typ | LPC662AM LPC662AMJ/883 Limit (Notes 4, 8) | LPC662AI Limit (Note 4) | LPC662I Limit (Note 4) | Units |
|------------------------------|---|--------|--|-------------------------------|------------------------------|------------------------|
| Slew Rate | (Note 6) | 0.11 | 0.07 | 0.07 | 0.05 | V/ μ s min |
| | | | 0.04 | 0.05 | 0.03 | |
| Gain-Bandwidth Product | | 0.35 | | | | MHz |
| Phase Margin | | 50 | | | | Deg |
| Gain Margin | | 17 | | | | dB |
| Amp-to-Amp Isolation | (Note 7) | 130 | | | | dB |
| Input Referred Voltage Noise | F = 1 kHz | 42 | | | | nV/ $\sqrt{\text{Hz}}$ |
| Input Referred Current Noise | F = 1 kHz | 0.0002 | | | | pA/ $\sqrt{\text{Hz}}$ |
| Total Harmonic Distortion | F = 1 kHz, A _V = -10, V ₊ = 15V R _L = 100 k Ω , V _O = 8 V _{PP} | 0.01 | | | | % |

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ± 30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation of any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to $7.5V$. For Sourcing tests, $7.5V \leq V_O \leq 11.5V$. For Sinking tests, $2.5V \leq V_O \leq 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_I = 100\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ Vpp}$.

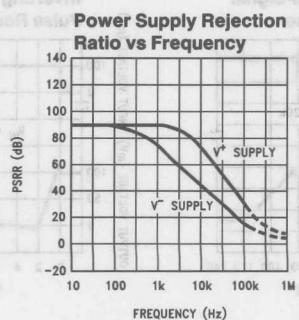
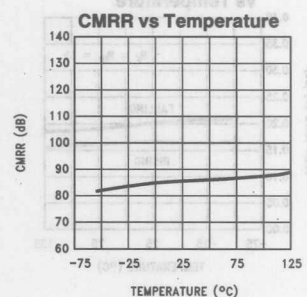
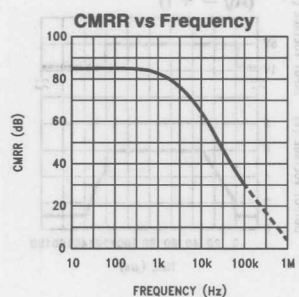
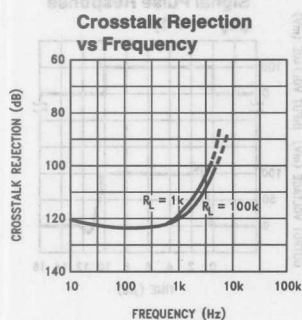
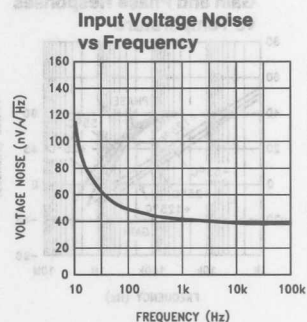
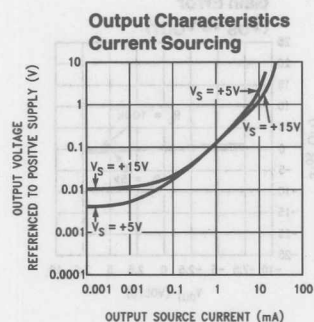
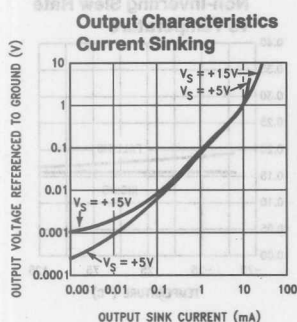
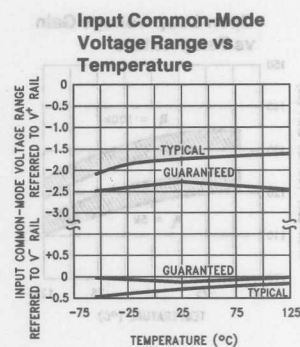
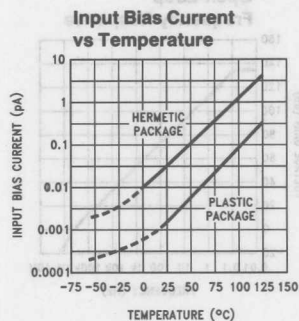
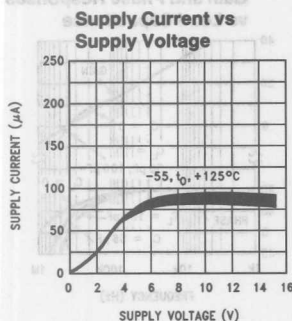
Note 8: A military RETS electrical test specification is available on request. At the time of printing, the LPC662AMJ/883 RETS specification complied fully with the **boldface** limits in this column. The LPC662AMJ/883 may also be procured to a Standard Military Drawing specification.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

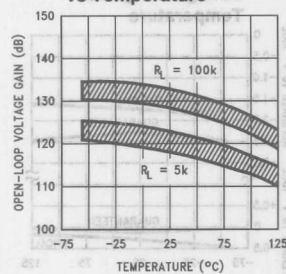
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified

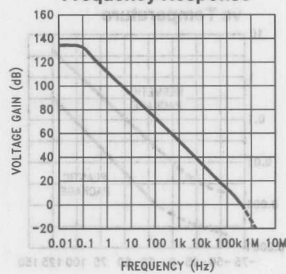


Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified (Continued)

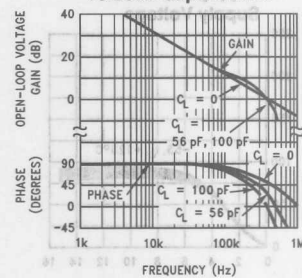
Open-Loop Voltage Gain vs Temperature



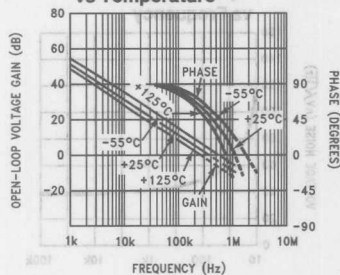
Open-Loop Frequency Response



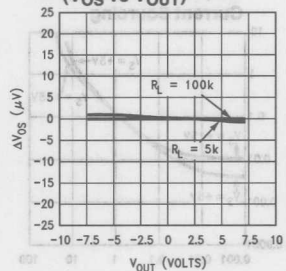
Gain and Phase Responses vs Load Capacitance



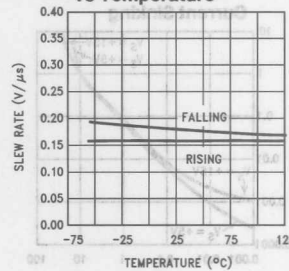
Gain and Phase Responses vs Temperature



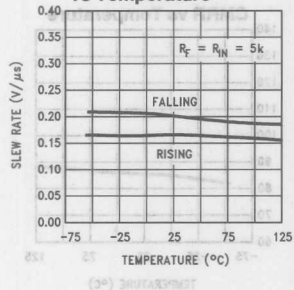
Gain Error (V_{OS} vs V_{OUT})



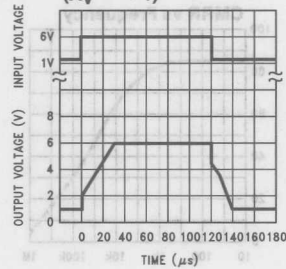
Non-Inverting Slew Rate vs Temperature



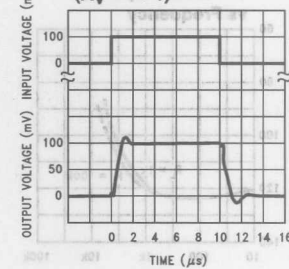
Inverting Slew Rate vs Temperature



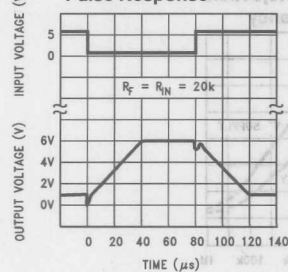
Large-Signal Pulse Non-Inverting Response ($A_V = +1$)



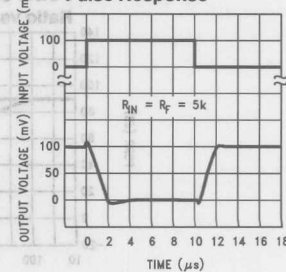
Non-Inverting Small Signal Pulse Response ($A_V = +1$)



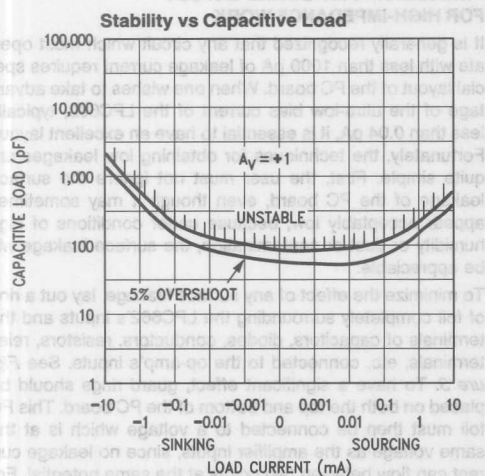
Inverting Large-Signal Pulse Response



Inverting Small-Signal Pulse Response



Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ (Continued)



Note: Avoid resistive loads of less than 500 Ω , as they may cause instability.

Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LPC662 is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

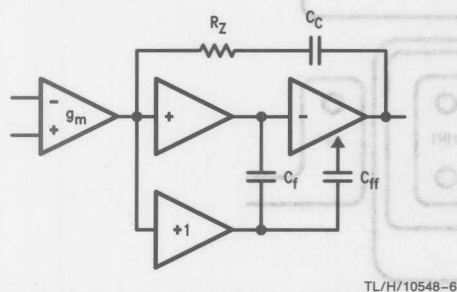
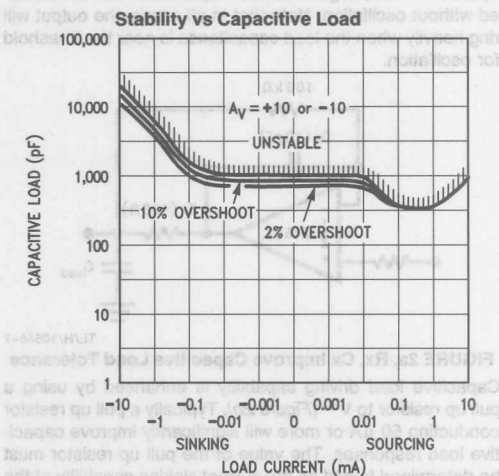


FIGURE 1. LPC662 Circuit Topology (Each Amplifier)



The large signal voltage gain while sourcing is comparable to traditional bipolar op amps for load resistance of at least 5 k Ω . The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, when driving load resistance of 5 k Ω or less, the gain will be reduced as indicated in the Electrical Characteristics. The op amp can drive load resistance as low as 500 Ω without instability.

COMPENSATING INPUT CAPACITANCE

Refer to the LMC660 or LMC662 datasheets to determine whether or not a feedback capacitor will be necessary for compensation and what the value of that capacitor would be.

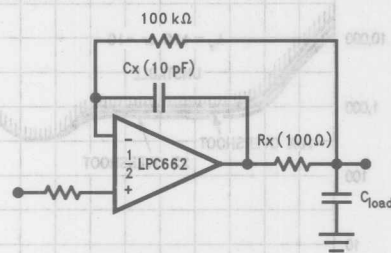
CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LPC662 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See the Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. The addition of a small resistor (50 Ω to 100 Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit

Application Hints (Continued)

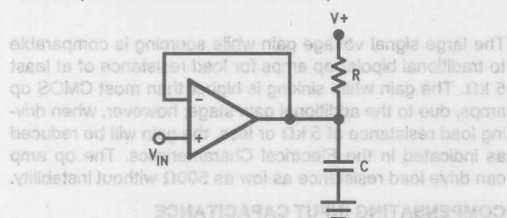
operation. Thus, larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



TL/H/10548-7

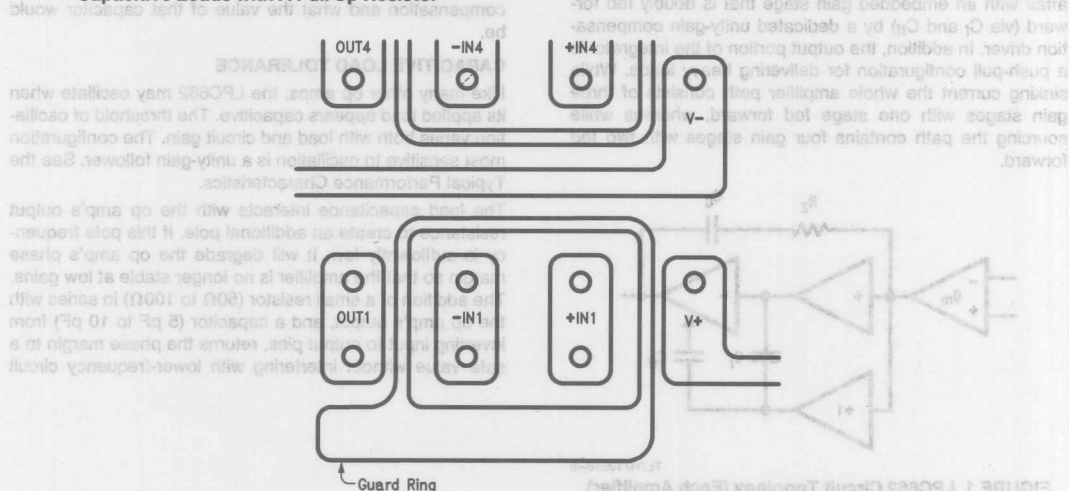
FIGURE 2a. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (Figure 2b). Typically a pull up resistor conducting 50 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



TL/H/10548-26

FIGURE 2b. Compensating for Large Capacitive Loads with A Pull Up Resistor



TL/H/10548-19

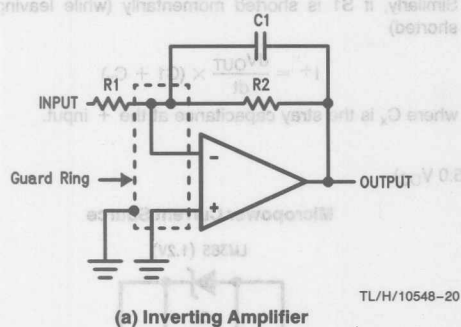
FIGURE 3. Example of Guard Ring in P.C. Board Layout, using the LPC660

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

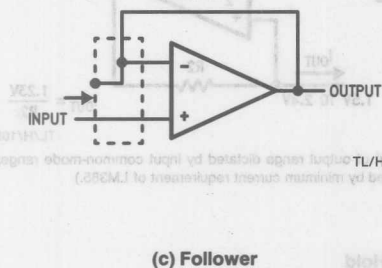
It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LPC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LPC662's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op-amp's inputs. See Figure 3. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of 10^{12} ohms, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LPC662's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of 10^{11} ohms would cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See Figures 4a, 4b, 4c for typical connections of guard rings for standard op-amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see Figure 4d.

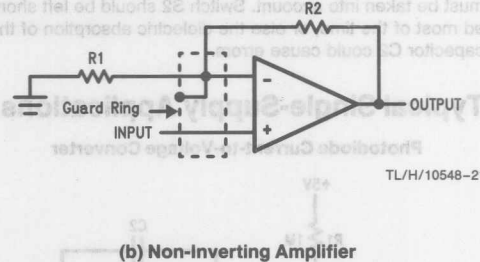
Application Hints (Continued)



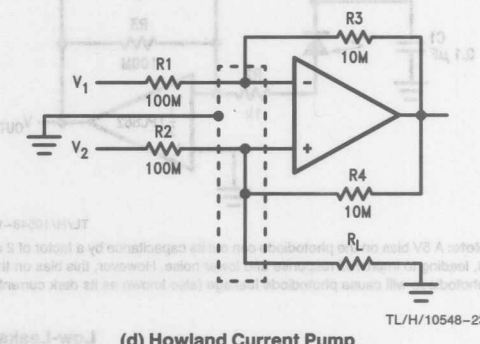
TL/H/10548-20



TL/H/10548-22



TL/H/10548-21



TL/H/10548-23

FIGURE 4. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See Figure 5.

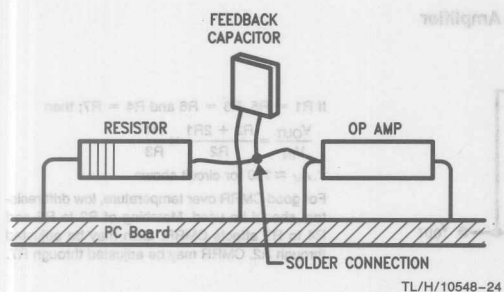


FIGURE 5. Air Wiring

TL/H/10548-24

BIAS CURRENT TESTING

The test method of Figure 6 is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I^- = \frac{dV_{OUT}}{dt} \times C2.$$

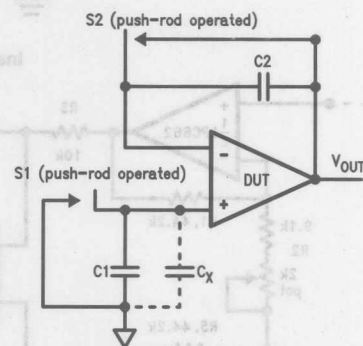


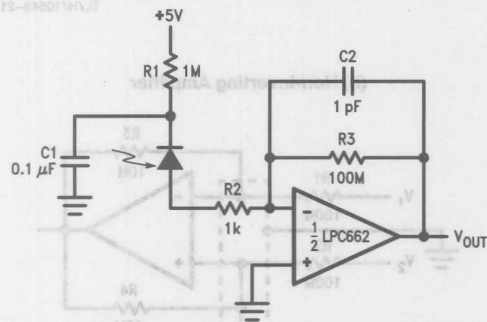
FIGURE 6. Simple Input Bias Current Test Circuit

TL/H/10548-25

media, MnO₂ ceramic, or air-dielectric. When determining the magnitude of I_{-} , the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Typical Single-Supply Applications ($V^{+} = 5.0 \text{ V}_{\text{DC}}$)

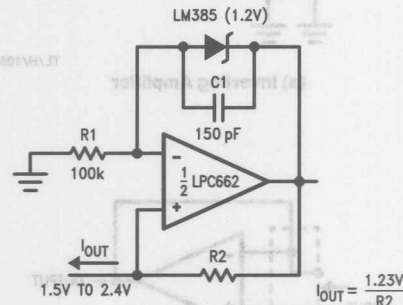
Photodiode Current-to-Voltage Converter



TL/H/10548-17

Note: A 5V bias on the photodiode can cut its capacitance by a factor of 2 or 3, leading to improved response and lower noise. However, this bias on the photodiode will cause photodiode leakage (also known as its dark current).

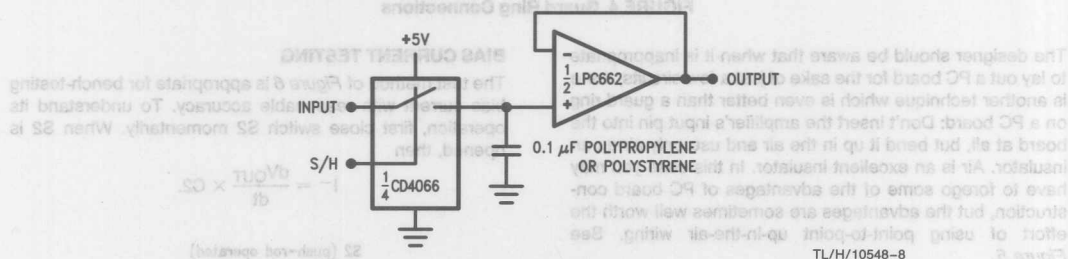
Micropower Current Source



TL/H/10548-18

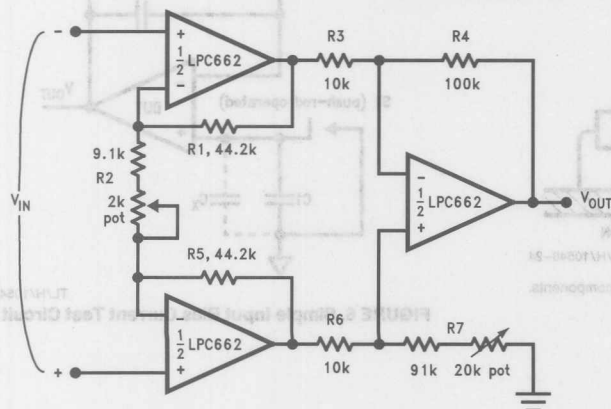
(Upper limit of output range dictated by input common-mode range; lower limit dictated by minimum current requirement of LM385.)

Low-Leakage Sample-and-Hold



TL/H/10548-8

Instrumentation Amplifier



If $R1 = R5$, $R3 = R6$ and $R4 = R7$; then

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

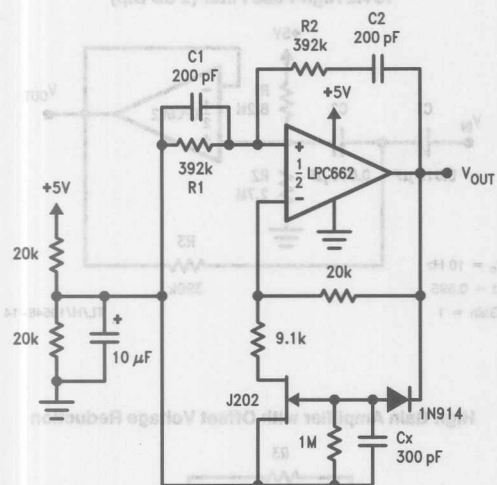
$\therefore A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of $R3$ to $R6$ and $R4$ to $R7$ affects CMRR. Gain may be adjusted through $R2$. CMRR may be adjusted through $R7$.

TL/H/10548-9

Typical Single-Supply Applications ($V^{\pm} = 5.0 V_{DC}$) (Continued)

Sine-Wave Oscillator



TL/H/10548-10

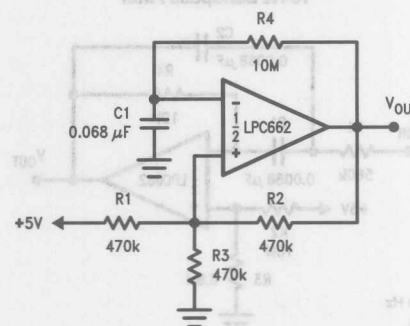
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{OSC} = 1/2\pi RC$$

where $R = R1 = R2$ and $C = C1 = C2$.

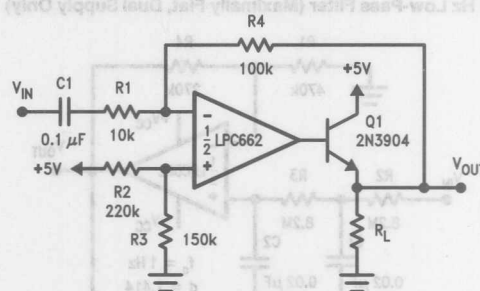
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V

1 Hz Square-Wave Oscillator



TL/H/10548-11

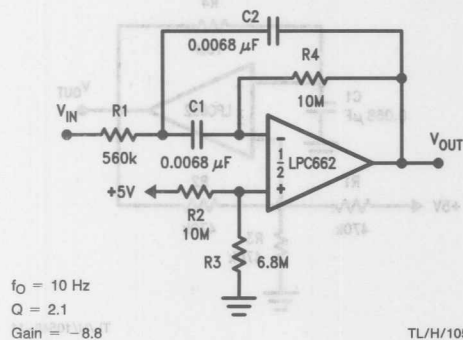
Power Amplifier



TL/H/10548-12

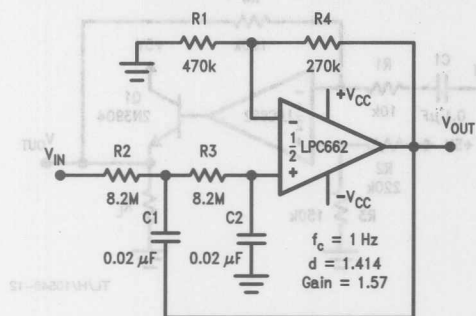
Typical Single-Supply Applications ($V^+ = 5.0\text{ V}_{\text{DC}}$) (Continued)

10 Hz Bandpass Filter



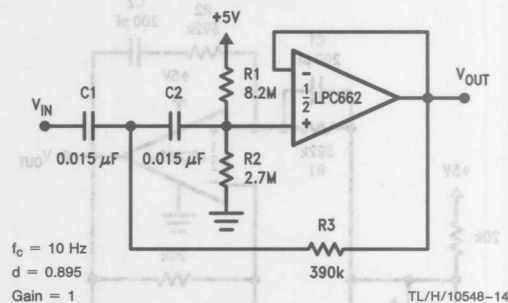
TL/H/10548-13

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



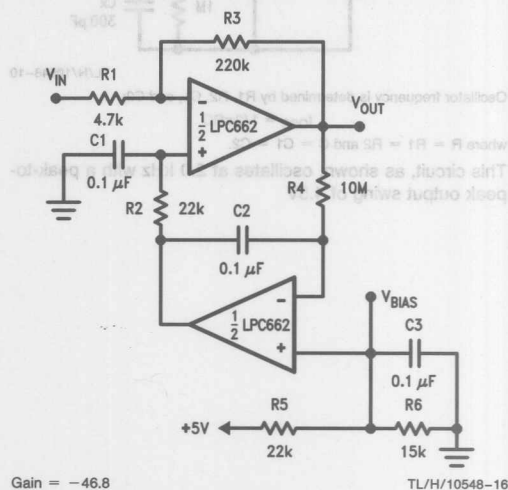
TL/H/10548-15

10 Hz High-Pass Filter (2 dB Dip)



TL/H/10548-14

High Gain Amplifier with Offset Voltage Reduction



TL/H/10548-16

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV), referred to V_{BIAS} .

OP-07 Low Offset, Low Drift Operational Amplifier

General Description

The OP-07 has very low input offset voltage which is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP-07 also features low input bias current and high open-loop gain. The low offsets and high open-loop gain make the OP-07 particularly useful for high-gain applications.

The wide input voltage range of $\pm 13V$ minimum combined with high CMRR of 110 dB and high input impedance provide high accuracy in the non-inverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains.

Stability of offsets and gain with time or variation in temperature is excellent.

The OP-07 is available in TO-99 metal can, ceramic or molded DIP.

For improved specifications, see the LM607.

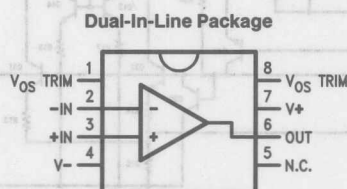
Features

- Low V_{OS} 75 μV Max
- Low V_{OS} Drift 0.6 $\mu V/^{\circ}C$ Max
- Ultra-Stable vs Time 1.0 μV /Month Max
- Low Noise 0.6 μV -p Max
- Wide Input Voltage Range $\pm 14V$
- Wide Supply Voltage Range $\pm 3V$ to $\pm 18V$
- Fits 725/108A/308A, 741, AD510 Sockets
- Replaces the $\mu A714$

Applications

- Strain Gauge Amplifiers
- Thermocouple Amplifiers
- Precision Reference Buffer
- Analog Computing Functions

Connection Diagram



TL/H/10550-1

See NS Package Number N08E

Ordering Information

| $T_A = 25^{\circ}C$ $V_{OS}Max$ (μV) | N08E Plastic | Operating Temperature Range |
|---|-----------------|-----------------------------------|
| 75 | OP07EP | COM |
| 150 | OP07CP | COM |
| 150 | OP07DP | COM |

*Also available per SMD #8203602

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-------------------------------------|------------|
| Supply Voltage | $\pm 22V$ |
| Internal Power Dissipation (Note 5) | 500 mW |
| Differential Input Voltage | $\pm 30V$ |
| Input Voltage (Note 6) | $\pm 22V$ |
| Output Short-Circuit Duration | Continuous |

Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$

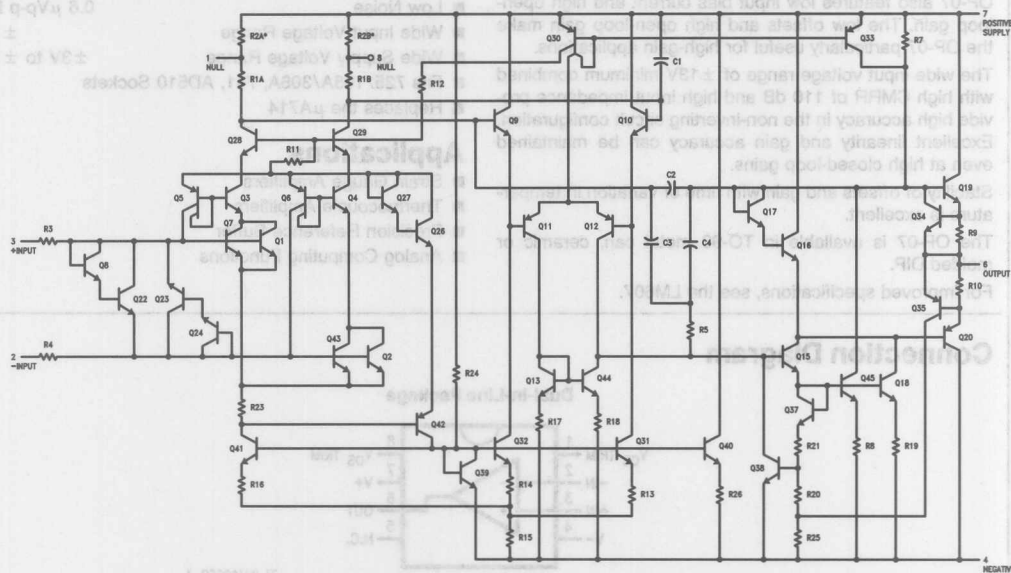
Lead Temperature (Soldering, 60 sec.) $260^{\circ}C$

Junction Temperature $-65^{\circ}C$ to $+150^{\circ}C$

Operating Temperature Range

OP-07E, OP-07C, OP-07D $0^{\circ}C$ to $+70^{\circ}C$

Simplified Schematic



*R2A and R2B are electronically trimmed on chip at the factory for minimum offset voltage.

TL/H/10550-3

| Operating Temperature Range | Model | V_{OS}^{max} (mV) at $T_A = 25^{\circ}C$ |
|-----------------------------|--------|--|
| COM | OP07EP | 75 |
| COM | OP07CP | 150 |
| COM | OP07DP | 150 |

*Also available per SMB & SOIC

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25^\circ C$. **Boldface** type refers to limits over $0^\circ C \leq T_A \leq 70^\circ C$

| Symbol | Parameter | Conditions | OP-07E | | | OP-07C | | | Units |
|-------------|--|--|-------------------|-------------------------------|-------------------------------|-------------------|-------------------------------|-------------------------------|------------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | (Note 1) | | 30 45 | 75 130 | | 60 85 | 150 250 | μV |
| $V_{OS/t}$ | Long-Term V_{OS} Stability | (Note 2) | | 0.3 | 1.5 | | 0.4 | 2.0 | $\mu V/Mo$ |
| I_{OS} | Input Offset Current | | | 0.5 0.9 | 3.8 5.3 | | 0.8 1.6 | 6.0 8.0 | nA |
| I_B | Input Bias Current | | | ± 1.2 \pm 1.5 | ± 4.0 \pm 5.5 | | ± 1.8 \pm 2.2 | ± 7.0 \pm 9.0 | nA |
| e_{n-p} | Input Noise Voltage | 0.1 Hz to 10 Hz (Note 3) | | 0.35 | 0.6 | | 0.38 | 0.65 | μV_{p-p} |
| e_n | Input Noise Voltage Density | $f_O = 10$ Hz | | 10.3 | 18.0 | | 10.5 | 20.0 | nV/\sqrt{Hz} |
| | | $f_O = 100$ Hz (Note 3) | | 10.0 | 13.0 | | 10.2 | 13.5 | |
| | | $f_O = 1000$ Hz | | 9.6 | 11.0 | | 9.8 | 11.5 | |
| i_{n-p} | Input Noise Current | 0.1 Hz to 10 Hz (Note 3) | | 14 | 30 | | 15 | 35 | pA_{p-p} |
| i_n | Input Noise Current Density | $f_O = 10$ Hz | | 0.32 | 0.80 | | 0.35 | 0.90 | pA/\sqrt{Hz} |
| | | $f_O = 100$ Hz (Note 3) | | 0.14 | 0.23 | | 0.15 | 0.27 | |
| | | $f_O = 1000$ Hz | | 0.12 | 0.17 | | 0.13 | 0.18 | |
| R_{IN} | Input Resistance Differential-Mode | (Note 4) | 15 | 50 | | 8 | 33 | | M Ω |
| R_{INCM} | Input Resistance Common-Mode | | | 160 | | | 120 | | G Ω |
| IVR | Input Voltage Range | | ± 13.0 | ± 14.0 | | ± 13 | ± 14 | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM} = \pm 13V$ | 106 103 | 123 123 | | 100 97 | 120 120 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 3V$ to $\pm 18V$ $V_S = \pm 3V$ to $\pm 18V$ | | 5 7 | 20 32 | | 7 10 | 32 51 | $\mu V/V$ |
| A_{VO} | Large Signal Voltage Gain | $R_L \geq 2$ k Ω , $V_O = \pm 10V$ | 200 | 500 | | 120 | 400 | | V/mV |
| | | $R_L \geq 2$ k Ω | 180 | 450 | | 100 | 400 | | |
| | | $R_L \geq 500\Omega$, $V_O = \pm 0.5V$ | 150 | 400 | | 100 | 400 | | |
| | | $V_S = \pm 3V$ (Note 4) | | | | | | | |
| V_O | Output Voltage Swing | $R_L \geq 10$ k Ω | ± 12.5 | ± 13.0 | | ± 12.0 | ± 13.0 | | V |
| | | $R_L \geq 2$ k Ω | ± 12.0 | ± 12.8 | | ± 11.5 | ± 12.8 | | |
| | | $R_L \geq 2$ k Ω | \pm 12.0 | \pm 12.6 | | \pm 11.0 | \pm 12.6 | | |
| | | $R_L \geq 1$ k Ω | ± 10.5 | ± 12.0 | | | ± 12.0 | | |
| SR | Slew Rate | $R_L \geq 2$ k Ω (Note 3) | 0.1 | 0.3 | | 0.1 | 0.3 | | V/ μs |
| BW | Closed-Loop Bandwidth | $A_{VCL} = +1$ (Note 3) | 0.4 | 0.6 | | 0.4 | 0.6 | | MHz |
| R_O | Output Resistance | $V_O = 0$, $I_O = 0$ | | 60 | | | 60 | | Ω |
| P_d | Power Consumption | $V_S = \pm 15V$, No Load | | 75 | 120 | | 80 | 150 | mW |
| | | $V_S = \pm 3V$, No Load | | 4 | 6 | | 4 | 8 | |
| | Offset Adj. Range | $R_P = 20$ k Ω | | ± 4 | | | ± 4 | | mV |
| TCV_{OS} | Average Input Offset Voltage Drift Without External Trim | (Note 4) | | 0.3 | 1.3 | | 0.5 | 1.8 | $\mu V/^\circ C$ |
| TCV_{OSn} | With External Trim | $R_P = 20$ k Ω (Note 4) | | 0.3 | 1.3 | | 0.4 | 1.6 | $\mu V/^\circ C$ |
| TCI_{OS} | Average Input Offset Current Drift | (Note 3) | | 8 | 35 | | 12 | 50 | $pA/^\circ C$ |
| TCI_B | Average Input Bias Current Drift | (Note 3) | | 13 | 35 | | 18 | 50 | $pA/^\circ C$ |

Electrical Characteristics

Unless otherwise specified, $V_S = \pm 15V$, $T_A = 25^\circ C$. **Boldface** type refers to limits over $0^\circ C \leq T_A \leq +70^\circ C$

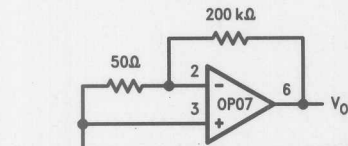
| Symbol | Parameter | Conditions | OP-07D | | | Units |
|-------------|--|---|---|---|---------------------------------|------------------|
| | | | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | (Note 1) | | 60 85 | 150 250 | μV |
| $V_{OS/t}$ | Long-Term V_{OS} Stability | (Note 2) | | 0.5 | 3.0 | $\mu V/Mo$ |
| I_{OS} | Input Offset Current | | | 0.8 1.6 | 6.0 8.0 | nA |
| I_B | Input Bias Current | | | ± 2.0 \pm 3.0 | ± 12.0 \pm 14.0 | nA |
| e_{np-p} | Input Noise Voltage | 0.1 Hz to 10 Hz (Note 3) | | 0.38 | 0.65 | $\mu Vp-p$ |
| e_n | Input Noise Voltage Density | $f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz | | 10.5 10.3 9.8 | 20.0 13.5 11.5 | nV/\sqrt{Hz} |
| i_{np-p} | Input Noise Current | 0.1 Hz to 10 Hz (Note 3) | | 15 | 35 | $pAp-p$ |
| i_n | Input Noise Current Density | $f_O = 10$ Hz $f_O = 100$ Hz (Note 3) $f_O = 1000$ Hz | | 0.35 0.15 0.13 | 0.90 0.27 0.18 | pA/\sqrt{Hz} |
| R_{IN} | Input Resistance Differential-Mode | (Note 4) | 7 | 31 | | $M\Omega$ |
| R_{INCM} | Input Resistance Common-Mode | | | 120 | | $G\Omega$ |
| IVR | Input Voltage Range | | ± 13 | ± 14 | | V |
| CMRR | Common-Mode Rejection Ratio | $V_{CM} = \pm 13V$ | 94 94 | 110 106 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 3V$ to $\pm 18V$ | | 7 10 | 32 51 | $\mu V/V$ |
| A_{VO} | Large Signal Voltage Gain | $R_L \leq 2 k\Omega$, $V_O = \pm 10V$ $R_L = 2 k\Omega$, $V_O = \pm 10V$ $R_L \geq 500\Omega$, $V_O = \pm 0.5V$, $V_S \pm 3V$ (Note 4) | 120 100 | 400 400 400 | | V/mV |
| V_O | Output Voltage Swing | $R_L \geq 10 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 2 k\Omega$ $R_L \geq 1 k\Omega$ | ± 12.0 ± 11.5 \pm 11.0 ± 12.0 | ± 13.0 ± 12.8 \pm 12.6 ± 12.0 | | V |
| SR | Slew Rate | $R_L \geq 2 k\Omega$ (Note 3) | 0.1 | 0.3 | | $V/\mu s$ |
| BW | Closed-Loop Bandwidth | $A_{VCL} = +1$ (Note 3) | 0.4 | 0.6 | | MHz |
| R_O | Output Resistance | $V_O = 0$, $I_O = 0$ | | 60 | | Ω |
| P_d | Power Consumption | $V_S = \pm 15V$, No Load $V_S = \pm 3V$, No Load | | 80 4 | 150 8 | mW |
| | Offset Adj. Range | $R_p = 20 k\Omega$ | | ± 4 | | mV |
| TCV_{OS} | Average Input Offset Voltage Drift Without External Trim | (Note 4) | | 0.7 | 2.5 | $\mu V/^\circ C$ |
| TCV_{OSn} | With External Trim | $R_p = 20 k\Omega$ (Note 4) | | 0.7 | 2.5 | $\mu V/^\circ C$ |
| TCI_{OS} | Average Input Offset Current Drift | (Note 3) | | 12 | 50 | $pA/^\circ C$ |
| TCI_B | Average Input Bias Current Drift | (Note 3) | | 18 | 50 | $pA/^\circ C$ |

Note 1: V_{OS} is measured approximately 0.5 second after application of power.

Note 2: Long-Term Offset Voltage Stability refers to the averaged trend line of V_{OS} vs Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV . Parameter is sample tested.

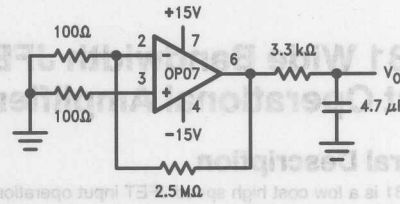
Note 3: Sample Tested.

Note 4: Guaranteed by design.



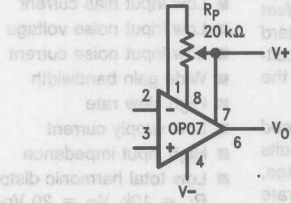
are critical, the LM255 is recommended. If maximum supply current is important, however, the TL081C is a better choice.

TL/H/10550-4



TL/H/10550-5

Optional Offset Nulling Circuit



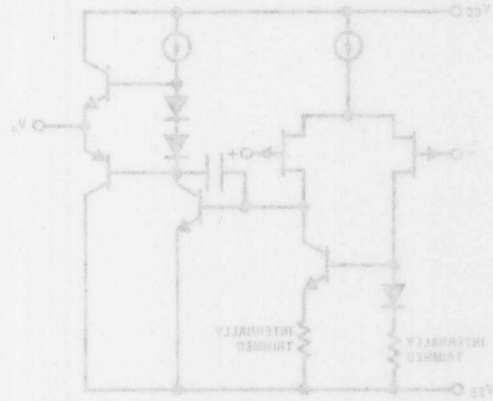
TL/H/10550-6

15 mV
50 pA
25 nV/√Hz
0.01 pA/√Hz
4 MHz
10 V/μs
1.8 mA
10 kΩ
>0.02%

50 Hz
5 μs

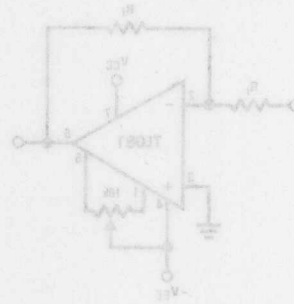
Fast settling time to 0.01%

Simplified Schematic

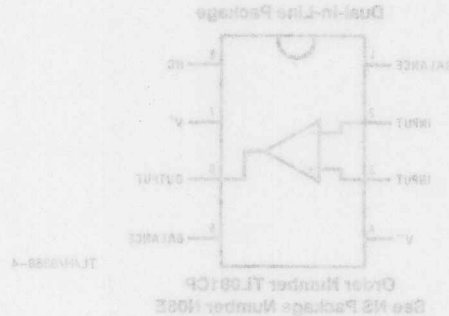


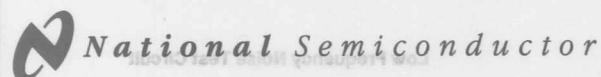
TL081-1

Typical Connection



Connection Diagram





TL081 Wide Bandwidth JFET Input Operational Amplifier

General Description

The TL081 is a low cost high speed JFET input operational amplifier with an internally trimmed input offset voltage (BI-FET IIT[™] technology). The device requires a low supply current and yet maintains a large gain bandwidth product and a fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL081 is pin compatible with the standard LM741 and uses the same offset voltage adjustment circuitry. This feature allows designers to immediately upgrade the overall performance of existing LM741 designs.

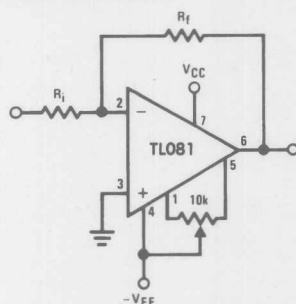
The TL081 may be used in applications such as high speed integrators, fast D/A converters, sample-and-hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The device has low noise and offset voltage drift, but for applications where these requirements

are critical, the LF356 is recommended. If maximum supply current is important, however, the TL081C is the better choice.

Features

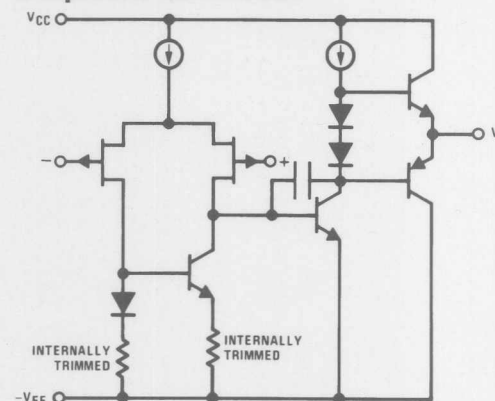
| | |
|---|--------------------|
| ■ Internally trimmed offset voltage | 15 mV |
| ■ Low input bias current | 50 pA |
| ■ Low input noise voltage | 25 nV/√Hz |
| ■ Low input noise current | 0.01 pA/√Hz |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/μs |
| ■ Low supply current | 1.8 mA |
| ■ High input impedance | 10 ¹² Ω |
| ■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20$ Vp-p, $BW = 20$ Hz–20 kHz | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 μs |

Typical Connection



TL/H/8358-1

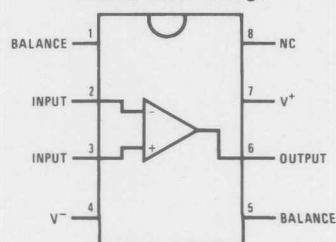
Simplified Schematic



TL/H/8358-2

Connection Diagram

Dual-In-Line Package



TL/H/8358-4

Order Number TL081CP
See NS Package Number N08E

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------------|--|
| Supply Voltage | $\pm 18\text{V}$ |
| Power Dissipation (Notes 1 and 6) | 670 mW |
| Operating Temperature Range | 0°C to $+70^{\circ}\text{C}$ |
| $T_{\text{J(MAX)}}$ | 115°C |
| Differential Input Voltage | $\pm 30\text{V}$ |

| | |
|------------------------------------|---|
| Input Voltage Range (Note 2) | $\pm 15\text{V}$ |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ |
| Lead Temp. (Soldering, 10 seconds) | 260°C |
| θ_{JA} | $120^{\circ}\text{C}/\text{W}$ |
| ESD rating to be determined. | |

DC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | TL081C | | | Units |
|---------------------------------|------------------------------------|--|----------|----------------|----------|--------------------------------|
| | | | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_{\text{S}} = 10\text{ k}\Omega$, $T_{\text{A}} = 25^{\circ}\text{C}$ Over Temperature | | 5 | 15 20 | mV mV |
| $\Delta V_{\text{OS}}/\Delta T$ | Average TC of Input Offset Voltage | $R_{\text{S}} = 10\text{ k}\Omega$ | | 10 | | $\mu\text{V}/^{\circ}\text{C}$ |
| I_{OS} | Input Offset Current | $T_{\text{J}} = 25^{\circ}\text{C}$, (Notes 3, 4) $T_{\text{J}} \leq 70^{\circ}\text{C}$ | | 25 | 100 4 | pA nA |
| I_{B} | Input Bias Current | $T_{\text{J}} = 25^{\circ}\text{C}$, (Notes 3, 4) $T_{\text{J}} \leq 70^{\circ}\text{C}$ | | 50 | 200 8 | pA nA |
| R_{IN} | Input Resistance | $T_{\text{J}} = 25^{\circ}\text{C}$ | | 10^{12} | | Ω |
| A_{VOL} | Large Signal Voltage Gain | $V_{\text{S}} = \pm 15\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$ $V_{\text{O}} = \pm 10\text{V}$, $R_{\text{L}} = 2\text{ k}\Omega$ Over Temperature | 25 15 | 100 | | V/mV V/mV |
| V_{O} | Output Voltage Swing | $V_{\text{S}} = \pm 15\text{V}$, $R_{\text{L}} = 10\text{ k}\Omega$ | ± 12 | ± 13.5 | | V |
| V_{CM} | Input Common-Mode Voltage Range | $V_{\text{S}} = \pm 15\text{V}$ | ± 11 | $+15$ -12 | | V V |
| CMRR | Common-Mode Rejection Ratio | $R_{\text{S}} \leq 10\text{ k}\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 5) | 70 | 100 | | dB |
| I_{S} | Supply Current | | | 1.8 | 2.8 | mA |

AC Electrical Characteristics (Note 3)

| Symbol | Parameter | Conditions | TL081C | | | Units |
|----------------|--------------------------------|--|--------|------|-----|------------------------|
| | | | Min | Typ | Max | |
| SR | Slew Rate | $V_{\text{S}} = \pm 15\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$ | | 13 | | V/ μs |
| GBW | Gain Bandwidth Product | $V_{\text{S}} = \pm 15\text{V}$, $T_{\text{A}} = 25^{\circ}\text{C}$ | | 4 | | MHz |
| e_{n} | Equivalent Input Noise Voltage | $T_{\text{A}} = 25^{\circ}\text{C}$, $R_{\text{S}} = 100\Omega$, $f = 1000\text{ Hz}$ | | 25 | | nV/ $\sqrt{\text{Hz}}$ |
| i_{n} | Equivalent Input Noise Current | $T_{\text{J}} = 25^{\circ}\text{C}$, $f = 1000\text{ Hz}$ | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of $120^{\circ}\text{C}/\text{W}$ junction to ambient for N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: These specifications apply for $V_{\text{S}} = \pm 15\text{V}$ and $0^{\circ}\text{C} \leq T_{\text{A}} \leq +70^{\circ}\text{C}$. V_{OS} , I_{B} and I_{OS} are measured at $V_{\text{CM}} = 0$.

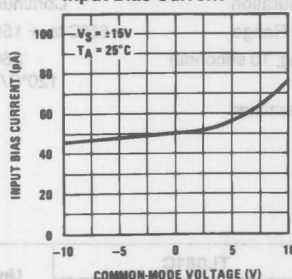
Note 4: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_{J} . Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_{D} . $T_{\text{J}} = T_{\text{A}} + \theta_{\text{JA}} P_{\text{D}}$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 5: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice from $V_{\text{S}} = \pm 5\text{V}$ to $\pm 15\text{V}$.

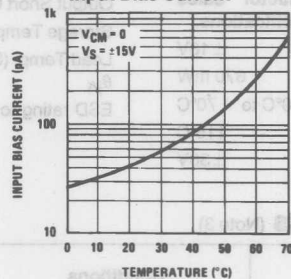
Note 6: Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside guaranteed limits.

Typical Performance Characteristics

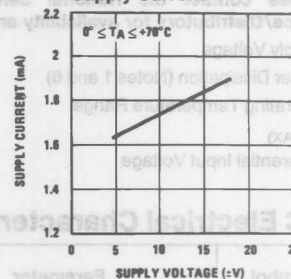
Input Bias Current



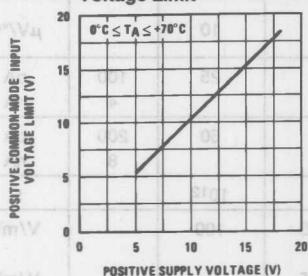
Input Bias Current



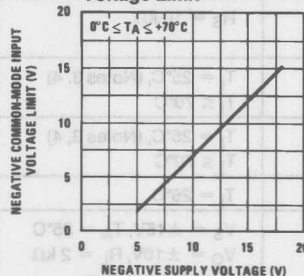
Supply Current



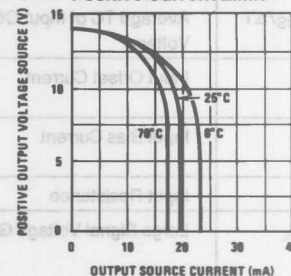
Positive Common-Mode Input Voltage Limit



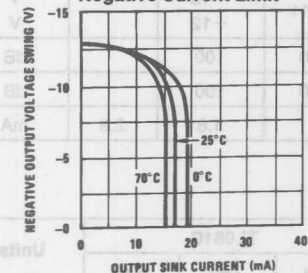
Negative Common-Mode Input Voltage Limit



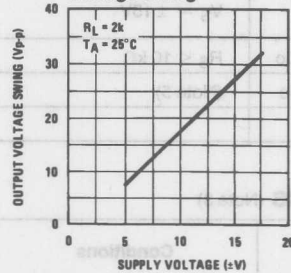
Positive Current Limit



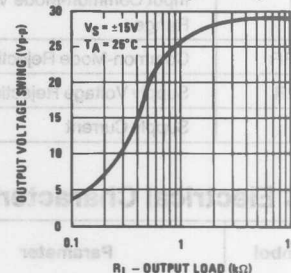
Negative Current Limit



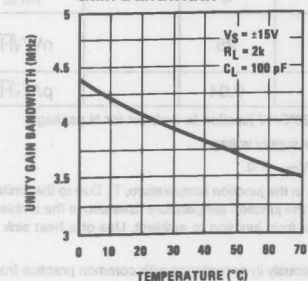
Voltage Swing



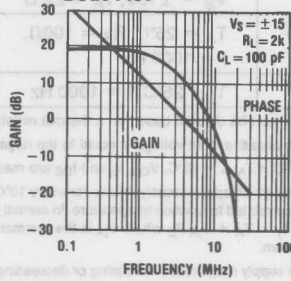
Output Voltage Swing



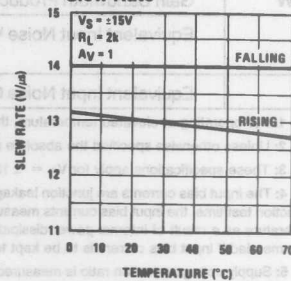
Gain Bandwidth



Bode Plot

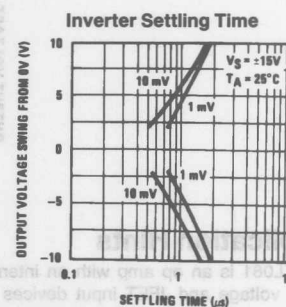
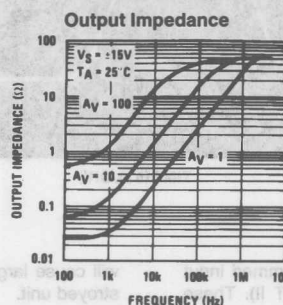
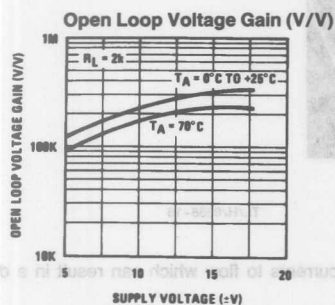
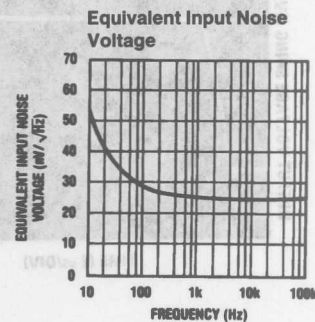
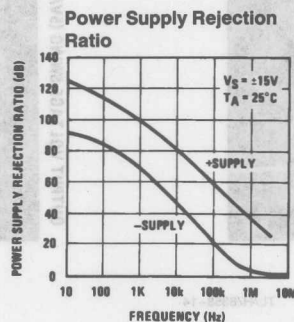
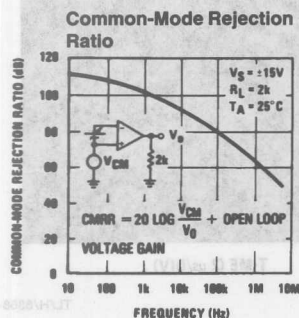
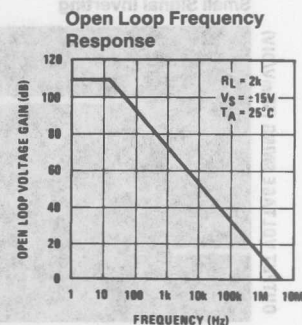
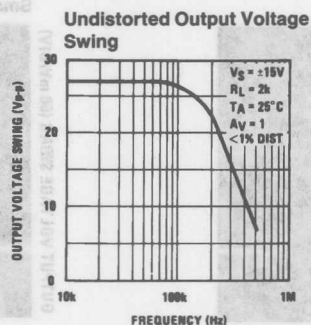
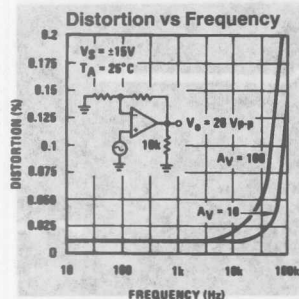


Slew Rate



TL/H/8358-5

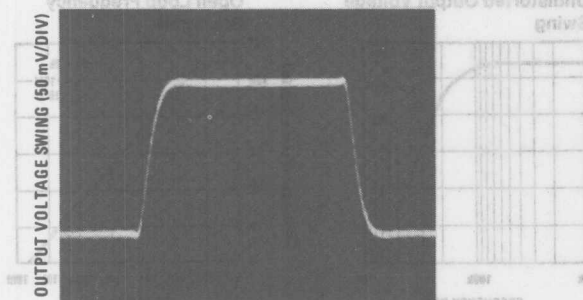
Typical Performance Characteristics (Continued)



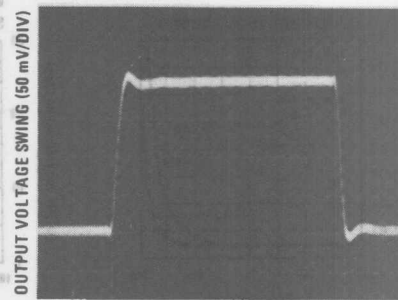
TL/H/8358-6

Pulse Response

Small Signal Inverting

TIME (0.2 μ s/DIV)

Small Signal Non-Inverting

TIME (0.2 μ s/DIV)

TL/H/8358-7

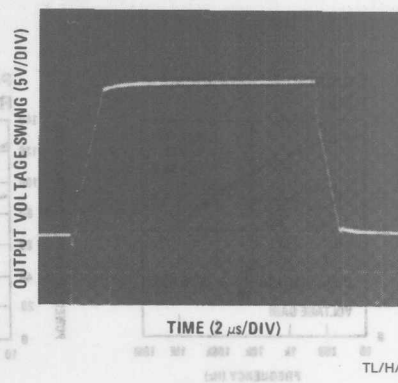
TL/H/8358-13

Large Signal Inverting

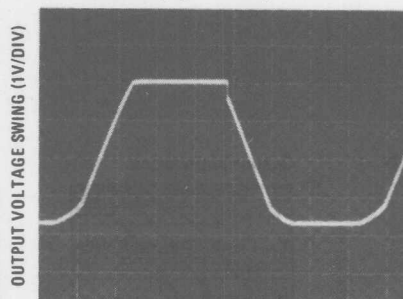
TIME (2 μ s/DIV)

TL/H/8358-14

Large Signal Non-Inverting

TIME (2 μ s/DIV)

TL/H/8358-15

Current Limit ($R_L = 100\Omega$)TIME (5 μ s/DIV)

TL/H/8358-16

Application Hints

The TL081 is an op amp with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this

will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output.

Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the

the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The TL081 is biased by a zener reference which allows normal circuit operation on $\pm 4V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The TL081 will drive a 2 k Ω load resistance to $\pm 10V$ over the full temperature range of 0°C to +70°C. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the

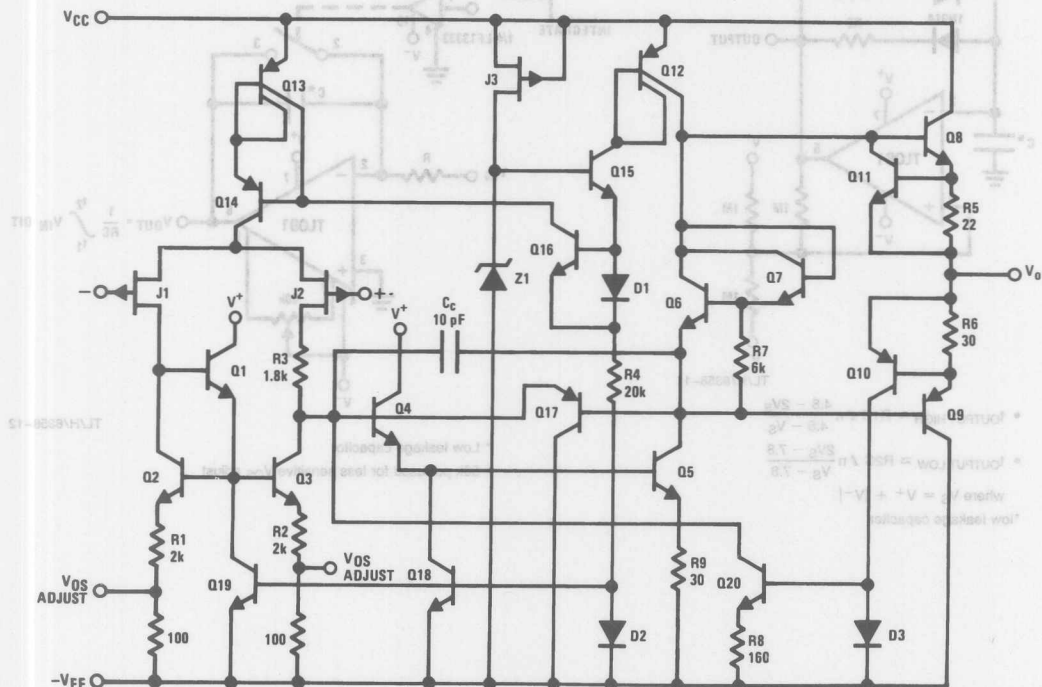
the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

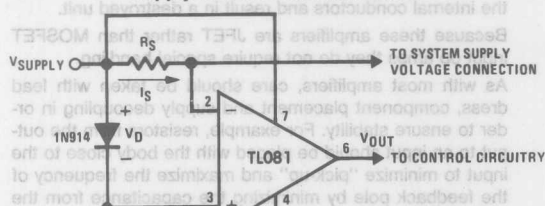
Detailed Schematic



TL/H/8358-8

Typical Applications

Supply Current Indicator/Limiter

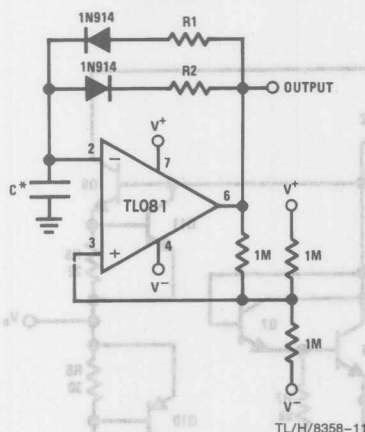


TL/H/8358-9

• V_{OUT} switches high when $R_S I_S > V_D$

However, if the feedback pole is less than approximately 5 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Ultra-Low (or High) Duty Cycle Pulse Generator



$$t_{OUTPUT\ HIGH} \approx R1C \ln \frac{4.8 - 2V_S}{4.8 - V_S}$$

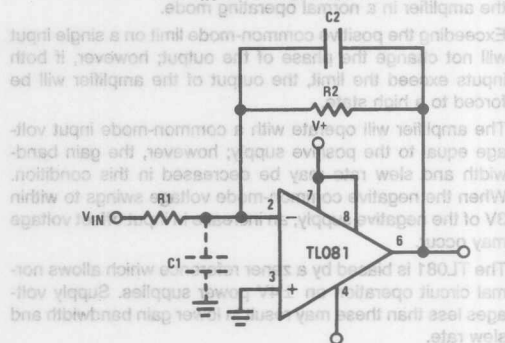
$$t_{OUTPUT\ LOW} \approx R2C \ln \frac{2V_S - 7.8}{V_S - 7.8}$$

where $V_S = V^+ + |V^-|$

*low leakage capacitor

TL/H/8358-11

Hi-Z_{IN} Inverting Amplifier

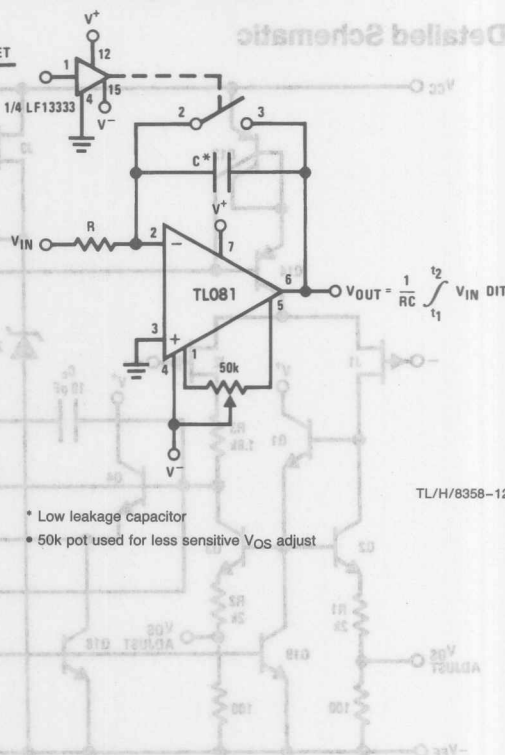


TL/H/8358-10

Parasitic input capacitance $C1 \approx 3$ pF for TL081 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate, add $C2$ such that $R2C2 \approx R1C1$.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unit through the

Long Time Integrator



- * Low leakage capacitor
- * 50k pot used for less sensitive V_{OS} adjust

TL/H/8358-12

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

General Description

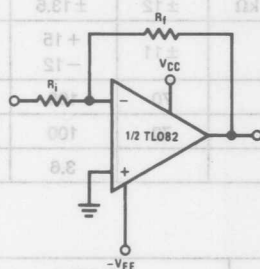
These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

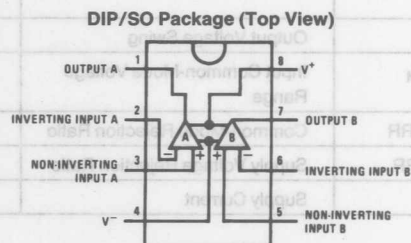
Features

| | |
|---|--------------------|
| ■ Internally trimmed offset voltage | 15 mV |
| ■ Low input bias current | 50 pA |
| ■ Low input noise voltage | 16nV/√Hz |
| ■ Low input noise current | 0.01 pA/√Hz |
| ■ Wide gain bandwidth | 4 MHz |
| ■ High slew rate | 13 V/μs |
| ■ Low supply current | 3.6 mA |
| ■ High input impedance | 10 ¹² Ω |
| ■ Low total harmonic distortion $A_V = 10$, $R_L = 10k$, $V_O = 20 V_p - p$, $BW = 20 Hz - 20 kHz$ | <0.02% |
| ■ Low 1/f noise corner | 50 Hz |
| ■ Fast settling time to 0.01% | 2 μs |

Typical Connection

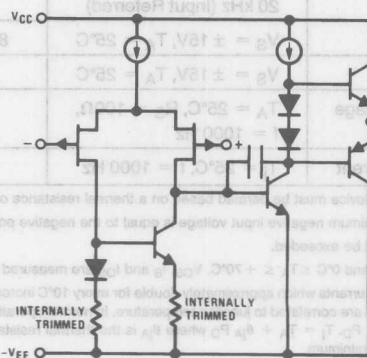


Connection Diagram



Order Number TL082CM or TL082CP
See NS Package Number M08A or N08E

Simplified Schematic



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-----------------------------|--|
| Supply Voltage | $\pm 18\text{V}$ |
| Power Dissipation | (Note 1) |
| Operating Temperature Range | 0°C to $+70^\circ\text{C}$ |
| $T_{j(\text{MAX})}$ | 150°C |

| | |
|------------------------------------|---|
| Differential Input Voltage | $\pm 30\text{V}$ |
| Input Voltage Range (Note 2) | $\pm 15\text{V}$ |
| Output Short Circuit Duration | Continuous |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lead Temp. (Soldering, 10 seconds) | 260°C |
| ESD rating to be determined. | |

DC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | TL082C | | | Units |
|--------------------------|------------------------------------|--|----------|------------|----------|------------------------------|
| | | | Min | Typ | Max | |
| V_{OS} | Input Offset Voltage | $R_S = 10\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ Over Temperature | | 5 | 15 20 | mV mV |
| $\Delta V_{OS}/\Delta T$ | Average TC of Input Offset Voltage | $R_S = 10\text{ k}\Omega$ | | 10 | | $\mu\text{V}/^\circ\text{C}$ |
| I_{OS} | Input Offset Current | $T_j = 25^\circ\text{C}$, (Notes 4, 5) $T_j \leq 70^\circ\text{C}$ | | 25 | 200 4 | pA nA |
| I_B | Input Bias Current | $T_j = 25^\circ\text{C}$, (Notes 4, 5) $T_j \leq 70^\circ\text{C}$ | | 50 | 400 8 | pA nA |
| R_{IN} | Input Resistance | $T_j = 25^\circ\text{C}$ | | 10^{12} | | Ω |
| A_{VOL} | Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ $V_O = \pm 10\text{V}$, $R_L = 2\text{ k}\Omega$ Over Temperature | 25 15 | 100 | | V/mV V/mV |
| V_O | Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{ k}\Omega$ | ± 12 | ± 13.5 | | V |
| V_{CM} | Input Common-Mode Voltage Range | $V_S = \pm 15\text{V}$ | ± 11 | +15 -12 | | V V |
| CMRR | Common-Mode Rejection Ratio | $R_S \leq 10\text{ k}\Omega$ | 70 | 100 | | dB |
| PSRR | Supply Voltage Rejection Ratio | (Note 6) | 70 | 100 | | dB |
| I_S | Supply Current | | | 3.6 | 5.6 | mA |

AC Electrical Characteristics (Note 4)

| Symbol | Parameter | Conditions | TL082C | | | Units |
|--------|---------------------------------|--|--------|------|-----|------------------------|
| | | | Min | Typ | Max | |
| | Amplifier to Amplifier Coupling | $T_A = 25^\circ\text{C}$, $f = 1\text{Hz}$ - 20 kHz (Input Referred) | | -120 | | dB |
| SR | Slew Rate | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | 8 | 13 | | V/ μs |
| GBW | Gain Bandwidth Product | $V_S = \pm 15\text{V}$, $T_A = 25^\circ\text{C}$ | | 4 | | MHz |
| e_n | Equivalent Input Noise Voltage | $T_A = 25^\circ\text{C}$, $R_S = 100\Omega$, $f = 1000\text{ Hz}$ | | 25 | | nV/ $\sqrt{\text{Hz}}$ |
| i_n | Equivalent Input Noise Current | $T_j = 25^\circ\text{C}$, $f = 1000\text{ Hz}$ | | 0.01 | | pA/ $\sqrt{\text{Hz}}$ |

Note 1: For operating at elevated temperature, the device must be derated based on a thermal resistance of $115^\circ\text{C}/\text{W}$ junction to ambient for the N package.

Note 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.

Note 3: The power dissipation limit, however, cannot be exceeded.

Note 4: These specifications apply for $V_S = \pm 15\text{V}$ and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$. V_{OS} , I_B and I_{OS} are measured at $V_{CM} = 0$.

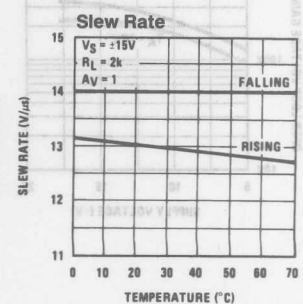
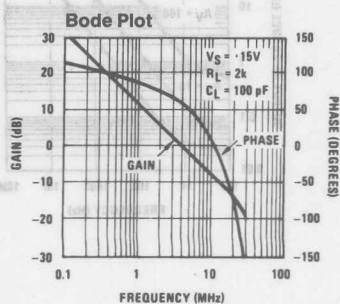
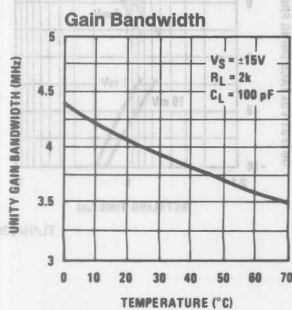
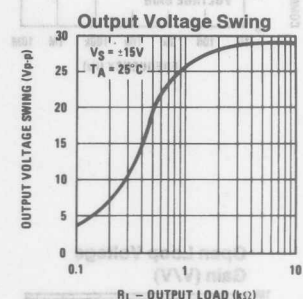
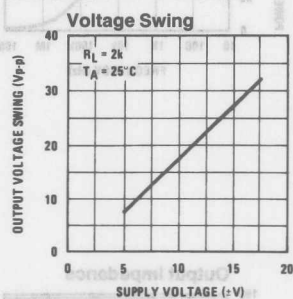
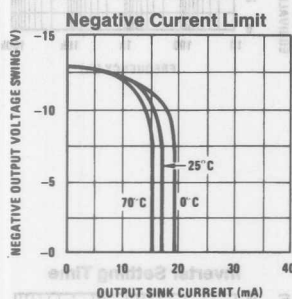
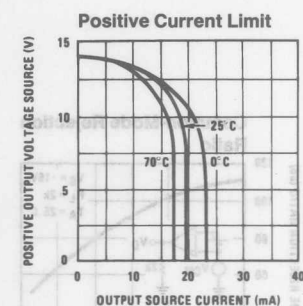
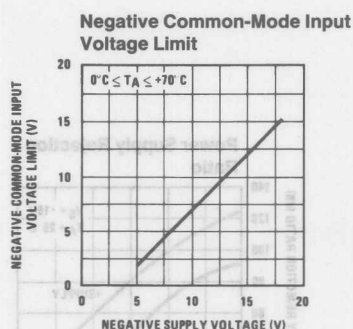
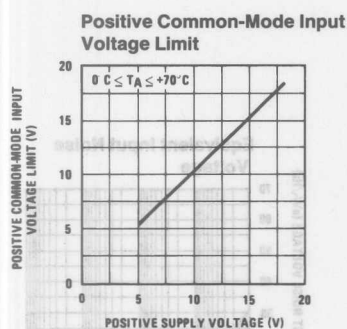
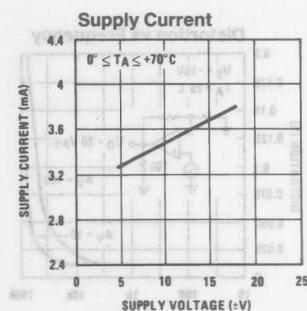
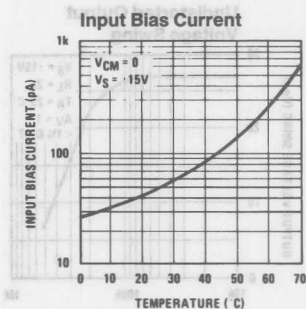
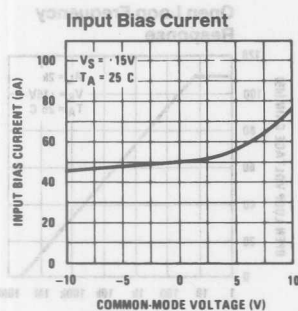
Note 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j . Due to the limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D . $T_j = T_A + \theta_{JA} P_D$ where θ_{JA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.

Note 6: Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

$V_S = \pm 6\text{V}$ to $\pm 15\text{V}$.

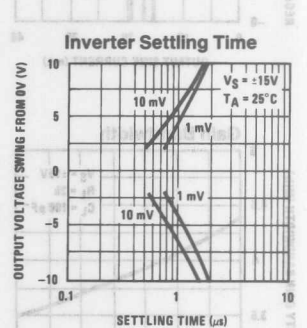
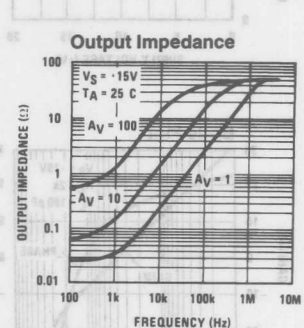
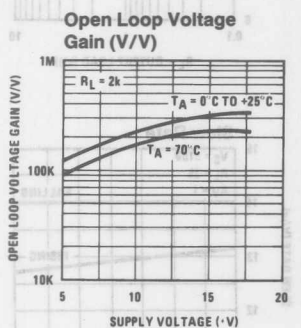
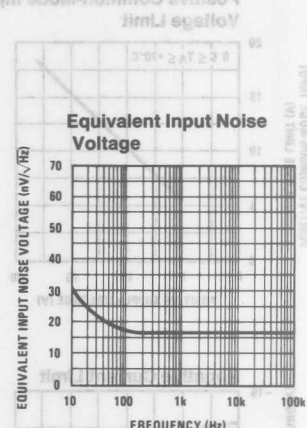
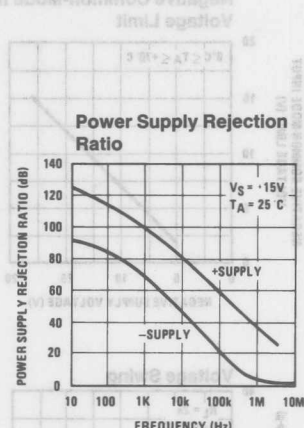
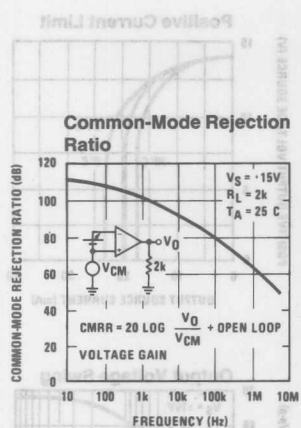
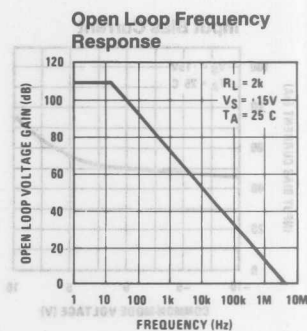
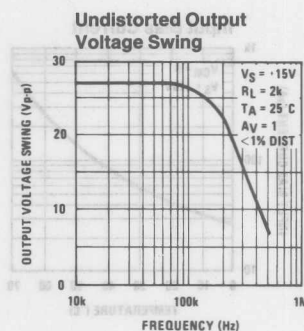
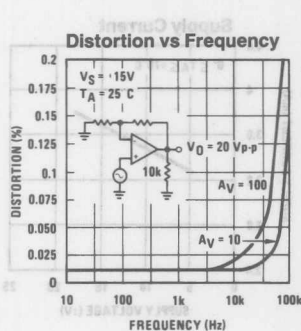
Typical Performance Characteristics

TL082



TL/H/8357-4

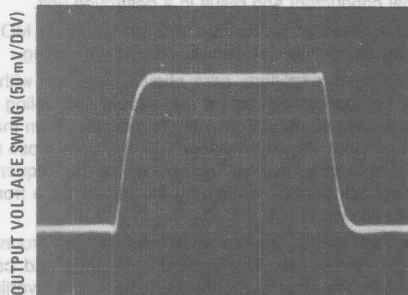
Typical Performance Characteristics (Continued)



TL/H/8357-5

Pulse Response

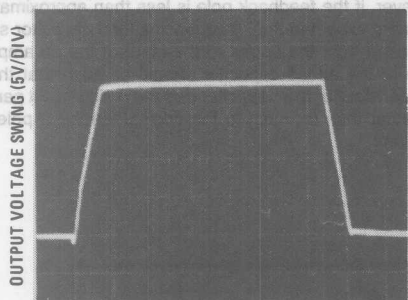
Small Signal Inverting



TIME (0.2 μs/DIV)

TL/H/8357-6

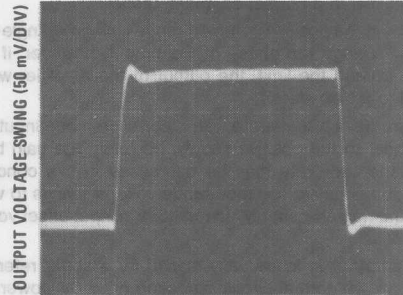
Large Signal Inverting



TIME (2 μs/DIV)

TL/H/8357-8

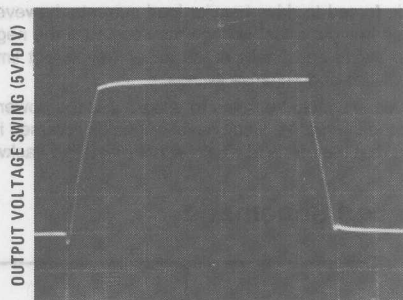
Small Signal Non-Inverting



TIME (0.2 μs/DIV)

TL/H/8357-7

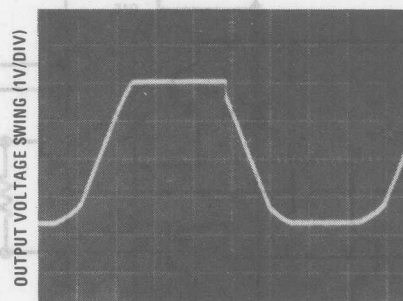
Large Signal Non-Inverting



TIME (2 μs/DIV)

TL/H/8357-9

Current Limit ($R_L = 100\Omega$)



TIME (5 μs/DIV)

TL/H/8357-10

Application Hints

These devices are op amps with an internally trimmed input offset voltage and JFET input devices (BI-FET II). These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages

should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case

Application Hints (Continued)

does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

The amplifiers will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

Each amplifier is individually biased by a zener reference which allows normal circuit operation on $\pm 6V$ power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The amplifiers will drive a $2\text{ k}\Omega$ load resistance to $\pm 10V$ over the full temperature range of 0°C to $+70^\circ\text{C}$. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards

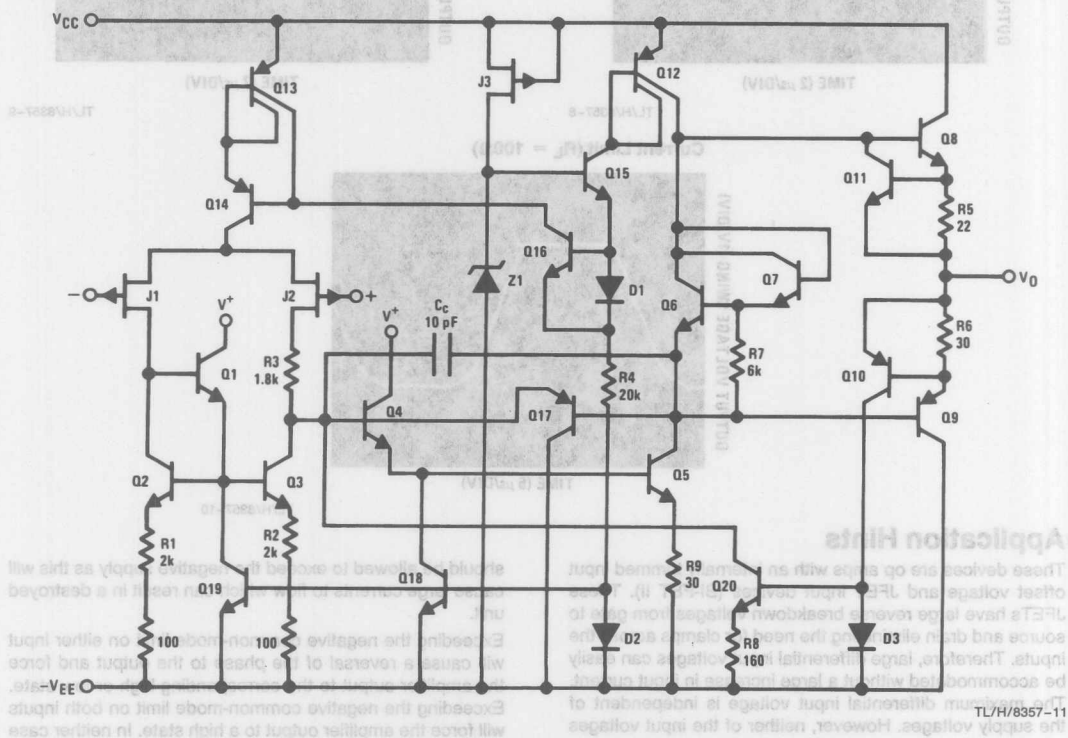
in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pick-up" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

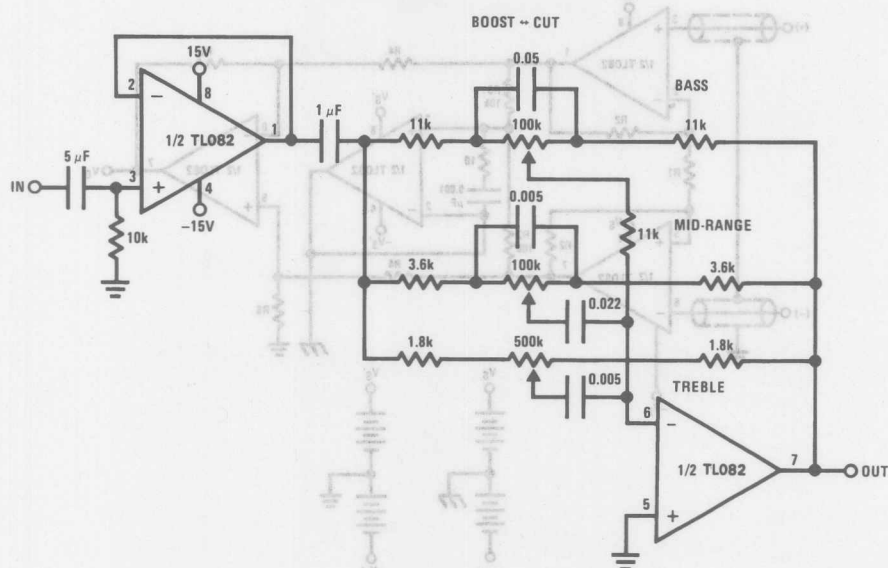
A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Detailed Schematic

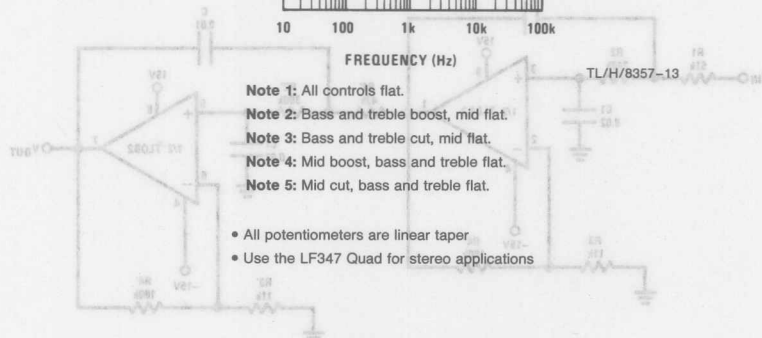
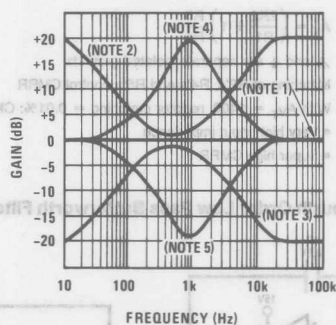


Typical Applications

Three-Band Active Tone Control



TL/H/8357-12



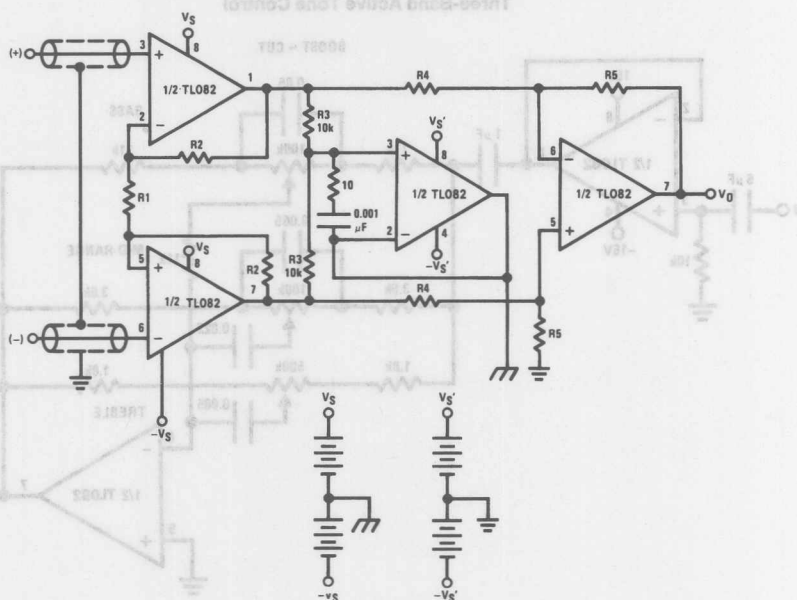
- Note 1: All controls flat.
- Note 2: Bass and treble boost, mid flat.
- Note 3: Bass and treble cut, mid flat.
- Note 4: Mid boost, bass and treble flat.
- Note 5: Mid cut, bass and treble flat.

- All potentiometers are linear taper
- Use the LF347 Quad for stereo applications

- Corner frequency $f_c = \frac{1}{2\pi RC}$
- Passband gain $(H_0) = \frac{R_2}{R_1 + R_2}$
- First stage $Q = 0.5$
- Second stage $Q = 0.5$
- Output shown uses nearest 5% tolerance resistor values for a flat with a corner frequency of 100 Hz and a passband gain of 100
- Circuit not intended for accurate DC performance

Typical Applications (Continued)

Improved CMRR Instrumentation Amplifier



SEPARATE

$$A_V = \left(\frac{2R_2}{R_1} + 1 \right) \frac{R_5}{R_4}$$

\uparrow and \downarrow are separate isolated grounds

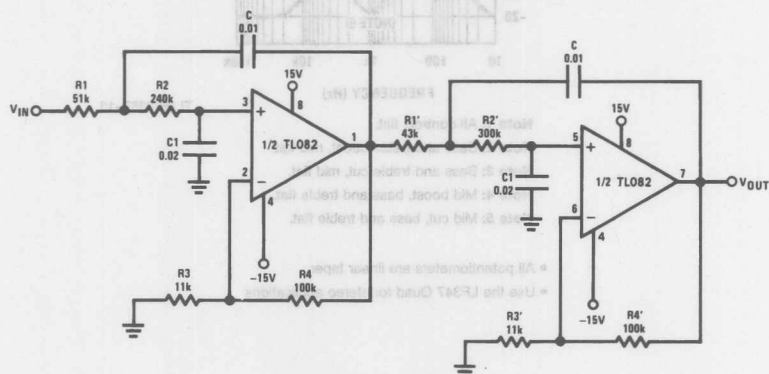
Matching of R2's, R4's and R5's control CMRR

With $A_{VT} = 1400$, resistor matching = 0.01%: CMRR = 136 dB

- Very high input impedance
- Super high CMRR

TL/H/8357-14

Fourth Order Low Pass Butterworth Filter



TL/H/8357-15

$$\bullet \text{ Corner frequency } (f_c) = \sqrt{\frac{1}{R_1 R_2 C C_1}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R_1' R_2' C C_1}} \cdot \frac{1}{2\pi}$$

$$\bullet \text{ Passband gain } (H_0) = (1 + R_4/R_3)(1 + R_4'/R_3')$$

• First stage Q = 1.31

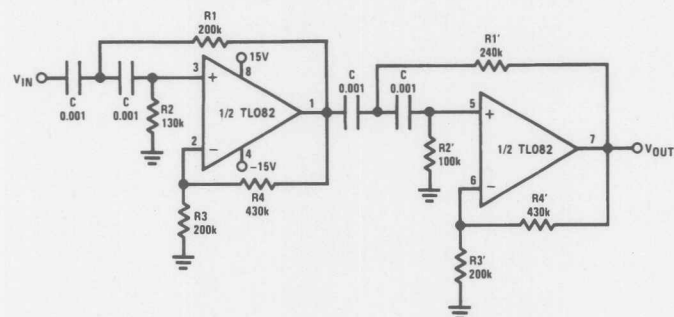
• Second stage Q = 0.541

• Circuit shown uses nearest 5% tolerance resistor values for a filter with a corner frequency of 100 Hz and a passband gain of 100

• Offset nulling necessary for accurate DC performance

Typical Applications (Continued)

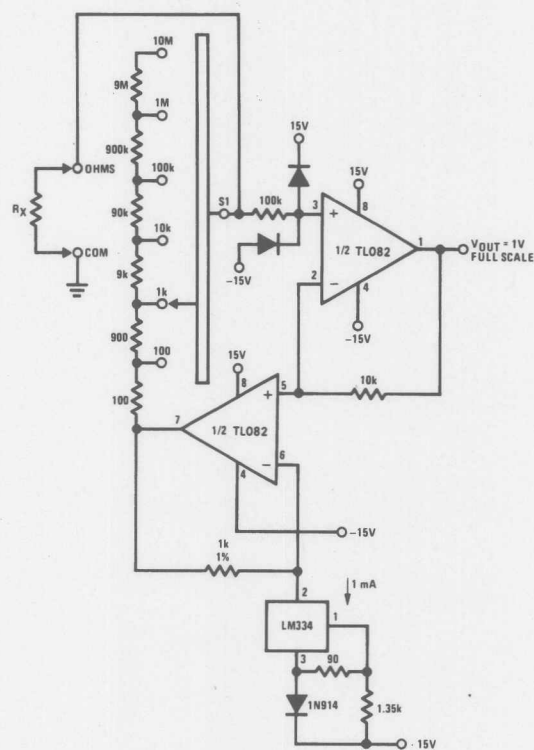
Fourth Order High Pass Butterworth Filter



TL/H/8357-16

- Corner frequency (f_c) = $\sqrt{\frac{1}{R_1 R_2 C^2}} \cdot \frac{1}{2\pi} = \sqrt{\frac{1}{R_1' R_2' C^2}} \cdot \frac{1}{2\pi}$
- Passband gain (H_0) = $(1 + R_4/R_3) (1 + R_4'/R_3')$
- First stage $Q = 1.31$
- Second stage $Q = 0.541$
- Circuit shown uses closest 5% tolerance resistor values for a filter with a corner frequency of 1 kHz and a passband gain of 10

Ohms to Volts Converter



TL/H/8357-17

$$V_O = \frac{1V}{R_{LADDER}} \times R_X$$

Where R_{LADDER} is the resistance from switch S1 pole to pin 7 of the TL082CP.



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| 2-4 | | Buffer Selection Guide |
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| 2-10 | | LH4001 Wideband Current Buffer |
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Section 2 Buffers



Section 2 Contents

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| LM110/LM210/LM310 Voltage Followers | 2-33 |
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| LM6125/LM6225/LM6325 High Speed Buffers | 2-52 |

Buffers Definition of Terms

Bandwidth: That frequency at which the voltage gain is reduced to $1/\sqrt{2}$ times the low frequency value.

Harmonic Distortion: That percentage of harmonic distortion being defined as one-hundred times the ratio of the root-mean-square (rms) sum of the harmonics to the fundamental.

$$\% \text{ harmonic distortion} = \frac{(V_2^2 + V_3^2 + V_4^2 + \dots)^{1/2}}{V_1} (100\%)$$

where V_1 is the rms amplitude of the fundamental and V_2, V_3, V_4, \dots are the rms amplitudes of the individual harmonics.

Input Impedance: The ratio of input voltage to input current under the stated conditions for source resistance (R_S) and load resistance (R_L).

Input Offset Voltage: That voltage which must be applied to the input terminal to obtain zero output voltage.

Input Resistance: The ratio of the change in input voltage to the change in input current.

Input Voltage Range: The range of voltages on the input terminal for which the buffer operates within specifications.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage.

Output Impedance: The ratio of change in output voltage to output current under the stated conditions.

Output Resistance: The small signal resistance seen at the output with the output voltage near zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Offset Voltage Temperature Drift: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

Power Supply Rejection: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

Settling Time: The time between the initiation of the input step function and the time when the output voltage has settled to within a specified error band of the final output voltage.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

Supply Current: The current required from the power supply to operate the buffer with no load and the output midway between the supplies.

Transient Response: The closed-loop step-function response of the amplifier under small-signal conditions.

Voltage Gain: The ratio of output voltage to input voltage under the stated conditions for source resistance (R_S) and load resistance (R_L).



National Semiconductor

Buffer Selection Guide (Notes 1 and 2)

| Device Type | Key Features | Slew Rate (V/ μ s) | Bandwidth \approx 3 dB (MHz) | Gain (A _V) | Output (V, mA) | Full Power BW (MHz @ V _{pp} , R _L) | Test Conditions |
|-----------------|-------------------------|------------------------|--------------------------------|------------------------|------------------------|---|--|
| LH0063 | FET Input, Very Fast | 2400 | 200 | 0.93 | ± 13 , ± 260 | 40 @ 20, 50 | R _L = 50, V _S = ± 15 V |
| LH0033 | FET Input, High Speed | 1500 | 100 | 0.98 | ± 9 , ± 90 | 24 @ 20, 1k | R _L = 1k, V _S = ± 15 V |
| LH4002 | Wideband Video Buffer | 1250 | 200 | 0.97 | ± 2.2 , ± 44 | 100 @ 4, 50 | R _L = 50, V _S = ± 5 V |
| LH2003/2033 | Wideband Video Buffer | 1200 | 100 | 0.9 | ± 11.3 , ± 113 | 2 @ 20, 100 | R _L = 1k, 50, V _S = ± 15 V |
| LM6121/6125 | High Speed VIPTM Buffer | 800 | 50 | 0.90 | ± 12 , ± 240 | 10.6 @ 12, 50 | R _L = 50, V _S = ± 15 V |
| LH0002 | Medium Speed | 200 | 30 | 0.97 | ± 10 , ± 100 | 3 @ 20, 1k | R _L = 1k, V _S = ± 12 V |
| LH4001 | Low Cost LH0002 | 125 | 25 | 0.97 | ± 10 , ± 100 | 4 @ 10, 100 | R _L = 100, V _S = ± 12 V |
| LM110, 210, 310 | Voltage Follower | 30 | 20 | 0.9999 | ± 10 , ± 10 | 0.5 @ 20, 10k | R _L = 10k, V _S = ± 15 V |

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: 200°C Temp Range Parts are available. Consult local sales office for information.



National Semiconductor

LH0002 Buffer

General Description

The LH0002 is a general purpose buffer. Its features make it ideal to integrate with operational amplifiers inside a closed loop configuration to increase current output. The symmetrical output portion of the circuit also provides a low output impedance for both the positive and negative slopes of output pulses.

The LH0002 is available in an 8-lead TO-99 can. The LH0002C is available in an 8-lead TO-99, and a 10-pin molded dual-in-line package.

The LH0002 is specified for operation over the -55°C to $+125^{\circ}\text{C}$ military temperature range. The LH0002C is specified for operation over the 0°C to $+85^{\circ}\text{C}$ temperature range.

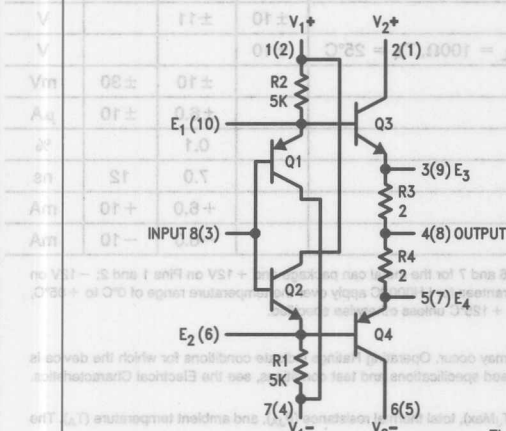
Features

- High input impedance
- Low output impedance
- High power efficiency
- Low harmonic distortion
- DC to 30 MHz bandwidth
- Output voltage swing that approaches supply voltage
- 400 mA pulsed output current
- Slew rate is typically $200 \text{ V}/\mu\text{s}$
- Operation from $\pm 5\text{V}$ to $\pm 20\text{V}$

Applications

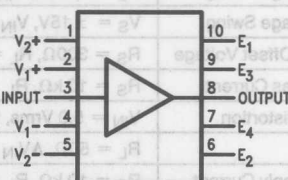
- Line driver
- 30 MHz buffer
- High speed D/A conversion

Schematic and Connection Diagrams



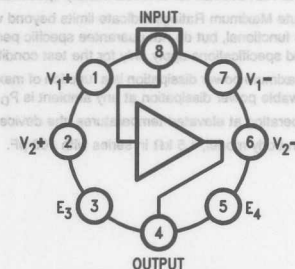
Pin numbers in parentheses denote pin connections for dual-in-line package.

Dual-In-Line Package



Order Number LH0002CN
See NS Package Number N10A

Metal Can Package



Order Number LH0002H,
LH0002H-MIL or LH0002CH
LH0002H/883*
See NS Package Number H08D

*Available per SMD #7801301

Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 2)

| | |
|---|---------------------------------|
| Supply Voltage | ±22V |
| Power Dissipation (Note 4) | 600 mW |
| Input Voltage | (Equal to Power Supply Voltage) |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | |
| N Package | +150°C |
| H Package | +175°C |
| Steady State Output Current | ±100 mA |
| Pulsed Output Current (50 ms On/1 sec. Off) | ±400 mA |
| Lead Temperature Soldering (10 seconds) | 300°C |
| Metal Can | 300°C |
| Plastic | 260°C |
| ESD Rating (Note 6) | 2 kV |

Electrical Characteristics (Note 1)

| Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------|--|------|------|-----|---------------|
| Voltage Gain | $R_S = 10\text{ k}\Omega$, $R_L = 1.0\text{ k}\Omega$, $V_{IN} = \pm 10\text{V}$ | 0.95 | 0.97 | | |
| Input Impedance | $R_S = 200\text{ k}\Omega$, $V_{IN} = \pm 1.0\text{V}$, $R_L = 1.0\text{ k}\Omega$ | 180 | 400 | | k Ω |
| Output Impedance | $V_{IN} = \pm 1.0\text{V}$, $R_L = 50\Omega$, $R_S = 10\text{ k}\Omega$ | | 6.0 | 10 | Ω |
| Output Voltage Swing | $R_L = 1.0\text{ k}\Omega$, $V_{IN} = \pm 12\text{V}$ | ±10 | ±11 | | V |
| Output Voltage Swing | $V_S = \pm 15\text{V}$, $V_{IN} = \pm 12\text{V}$, $R_S = 50\Omega$, $R_L = 100\Omega$, $T_A = 25^\circ\text{C}$ | ±10 | | | V |
| DC Output Offset Voltage | $R_S = 300\Omega$, $R_L = 1.0\text{ k}\Omega$ | | ±10 | ±30 | mV |
| DC Input Bias Current | $R_S = 10\text{ k}\Omega$, $R_L = 1.0\text{ k}\Omega$ | | ±6.0 | ±10 | μA |
| Harmonic Distortion | $V_{IN} = 5.0\text{ Vrms}$, $f = 1.0\text{ kHz}$ | | 0.1 | | % |
| Rise Time | $R_L = 50\Omega$, $\Delta V_{IN} = 100\text{ mV}$ | | 7.0 | 12 | ns |
| Positive Supply Current | $R_S = 10\text{ k}\Omega$, $R_L = 1.0\text{ k}\Omega$ | | +6.0 | +10 | mA |
| Negative Supply Current | $R_S = 10\text{ k}\Omega$, $R_L = 1.0\text{ k}\Omega$ | | −6.0 | −10 | mA |

Note 1: Specification applies for $T_A = 25^\circ\text{C}$ with +12V on Pins 1 and 2; −12V on Pins 6 and 7 for the metal can package and +12V on Pins 1 and 2; −12V on Pins 4 and 5 for the dual-in-line package, unless otherwise specified. The parameter guarantees for LH0002C apply over the temperature range of 0°C to $+85^\circ\text{C}$, while parameters for the LH0002 are guaranteed over the temperature range -55°C to $+125^\circ\text{C}$ unless otherwise specified.

Note 2: Refer to RETS0002X for LH0002 military specifications.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: The maximum power dissipation is a function of maximum junction temperature ($T_{J\text{Max}}$), total thermal resistance (θ_{JA}), and ambient temperature (T_A). The maximum allowable power dissipation at any ambient is $P_D = (T_{J\text{Max}} - T_A)/\theta_{JA}$.

Note 5: For operating at elevated temperatures, the device must be derated based on the thermal resistance θ_{JA} and $T_{J\text{Max}}$. $T_J = T_A + P_D\theta_{JA}$.

Note 6: Human body model, 1.5 k Ω in series with 100 pF.

Operating Ratings (Note 3)

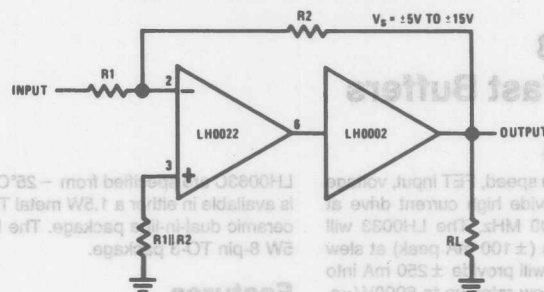
| | |
|-------------------|--|
| Temperature Range | |
| LH0002 | −55°C to +125°C |
| LH0002C | 0°C to $+85^\circ\text{C}$ |

Thermal Resistance (Note 5)

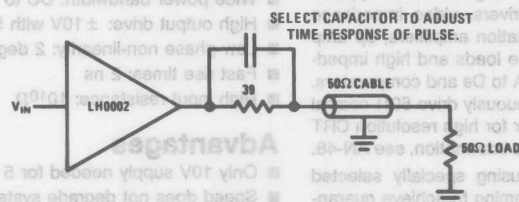
| | |
|---------------------------|----------|
| θ_{JA} , H Package | +125°C/W |
| θ_{JC} , H Package | +75°C/W |
| θ_{JA} , N Package | +120°C/W |

Typical Applications

High Current Operational Amplifier



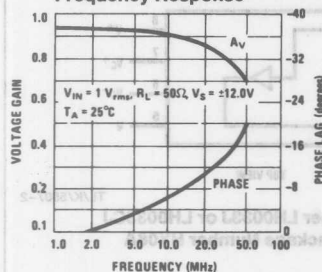
Line Driver



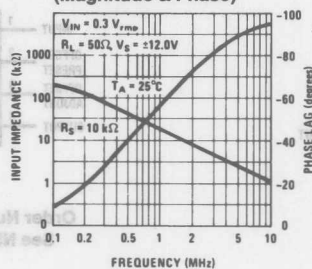
*Previously called NH0002/NH0002C

Typical Performance Characteristics

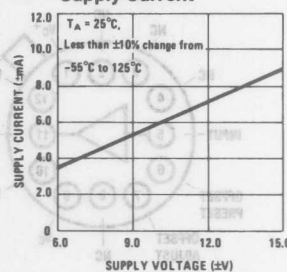
Frequency Response



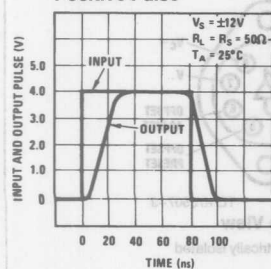
Input Impedance (Magnitude & Phase)



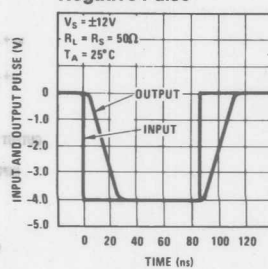
Supply Current



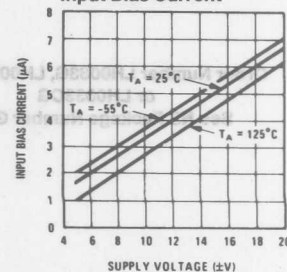
Positive Pulse



Negative Pulse



Input Bias Current



TL/H/5560-7



LH0033/LH0063 Fast and Ultra Fast Buffers

General Description

The LH0033 and LH0063 are high speed, FET input, voltage follower/buffers designed to provide high current drive at frequencies from DC to over 100 MHz. The LH0033 will provide ± 10 mA into 1 k Ω loads (± 100 mA peak) at slew rates of 1500V/ μ s. The LH0063 will provide ± 250 mA into 50 Ω loads (± 500 mA peak) at slew rates up to 6000V/ μ s. In addition, both exhibit excellent phase linearity up to 20 MHz.

Both are intended to fulfill a wide range of buffer applications such as high speed line drivers, video impedance transformation, nuclear instrumentation amplifiers, op amp isolation buffers for driving reactive loads and high impedance input buffers for high speed A to Ds and comparators. In addition, the LH0063 can continuously drive 50 Ω coaxial cables or be used as a yoke driver for high resolution CRT displays. For additional applications information, see AN-48.

These devices are constructed using specially selected junction FETs and active laser trimming to achieve guaranteed performance specifications. The LH0033 is specified for operation from -55°C to $+125^{\circ}\text{C}$; the LH0033C and the

LH0063C are specified from -25°C to $+85^{\circ}\text{C}$. The LH0033 is available in either a 1.5W metal TO-8 package or an 8-pin ceramic dual-in-line package. The LH0063 is available in a 5W 8-pin TO-3 package.

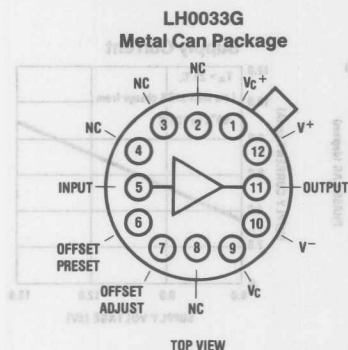
Features

- Ultra fast (LH0063): 6000 V/ μ s
- Wide range single or dual supply operation
- Wide power bandwidth: DC to 100 MHz
- High output drive: ± 10 V with 50 Ω load
- Low phase non-linearity: 2 degrees
- Fast rise times: 2 ns
- High input resistance: $10^{10}\Omega$

Advantages

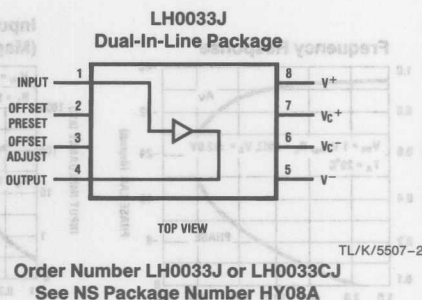
- Only 10V supply needed for 5 Vp-p video out
- Speed does not degrade system performance
- Wide data rate range for phase encoded systems

Connection Diagrams

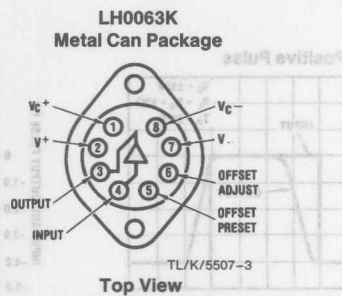


Order Number LH0033G, LH0033G-MIL
or LH0033CG
See NS Package Number G12B

TL/K/5507-1



TL/K/5507-2



Order Number LH0063CK
See NS Package Number K08A

TL/K/5507-3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------|--------------|
| Supply Voltage ($V^+ - V^-$) | 40V |
| Power Dissipation (See Curves) | |
| LH0063C | 5W |
| LH0033/LH0033C | 2.2W |
| Junction Temperature | 175°C |
| Input Voltage | $\pm V_S$ |
| Continuous Output Current | |
| LH0063C | ± 250 mA |
| LH0033/LH0033C | ± 100 mA |

| | |
|------------------------------------|--------------|
| Peak Output Current | |
| LH0063C | ± 500 mA |
| LH0033/LH0033C | ± 250 mA |
| Lead Temp. (Soldering, 10 seconds) | 300°C |

Operating Temperature Range

| | |
|------------------------------|-----------------|
| LH0033 | -55°C to +125°C |
| LH0033C and LH0063C | -25°C to +85°C |
| Storage Temperature Range | -65° to +150°C |
| ESD rating to be determined. | |

DC Electrical Characteristics $V_S = \pm 15V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified, (Note 1)

| Parameter | Conditions | LH0033 | | | LH0033C | | | Units |
|---|--|-----------|-----------|------|-----------|-----------|------|------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Output Offset Voltage | $R_S = 100\Omega$, $T_J = 25^\circ\text{C}$, $V_{IN} = 0V$ (Note 2) $R_S = 100\Omega$ | | 5.0 | 10 | | 12 | 20 | mV |
| | | | | 15 | | | 25 | mV |
| Average Temperature Coefficient of Offset Voltage | $R_S = 100\Omega$, $V_{IN} = 0V$ (Note 3) | | 50 | 100 | | 50 | 100 | $\mu\text{V}/^\circ\text{C}$ |
| Input Bias Current | $V_{IN} = 0V$ $T_J = 25^\circ\text{C}$ (Note 2) $T_A = 25^\circ\text{C}$ (Note 4) $T_J = T_A = T_{MAX}$ | | | 250 | | | 500 | pA |
| | | | | 2.5 | | | 5.0 | nA |
| | | | | 10 | | | 20 | nA |
| | | | | | | | | |
| Voltage Gain | $V_O = \pm 10V$, $R_S = 100\Omega$, $R_L = 1.0k\Omega$ | 0.97 | 0.98 | 1.00 | 0.96 | 0.98 | 1.00 | V/V |
| Input Impedance | $R_L = 1k\Omega$ | 10^{10} | 10^{11} | | 10^{10} | 10^{11} | | Ω |
| Output Impedance | $V_{IN} = \pm 1.0V$, $R_L = 1.0k\Omega$ | | 6.0 | 10 | | 6.0 | 10 | Ω |
| Output Voltage Swing | $V_I = \pm 14V$, $R_L = 1.0k\Omega$ $V_I = \pm 10.5V$, $R_L = 100\Omega$, $T_A = 25^\circ\text{C}$ | ± 12 | | | ± 12 | | | V |
| | | ± 9.0 | | | ± 9.0 | | | V |
| Supply Current | $V_{IN} = 0V$ (Note 5) | | 20 | 22 | | 21 | 24 | mA |
| Power Consumption | $V_{IN} = 0V$ | | 600 | 660 | | 630 | 720 | mW |

AC Electrical Characteristics $T_J = 25^\circ\text{C}$, $V_S = \pm 15V$, $R_S = 50\Omega$, $R_L = 1.0K\Omega$ (Note 6)

| Parameter | Conditions | LH0033 | | | LH0033C | | | Units |
|---------------------|------------------------|--------|------|-----|---------|------|-----|------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Slew Rate | $V_{IN} = \pm 10V$ | 1000 | 1500 | | 1000 | 1400 | | V/ μs |
| Bandwidth | $V_{IN} = 1.0$ Vrms | | 100 | | | 100 | | MHz |
| Phase Non-Linearity | BW = 1.0Hz to 20 MHz | | 2.0 | | | 2.0 | | degrees |
| Rise Time | $\Delta V_{IN} = 0.5V$ | | 2.9 | | | 3.2 | | ns |
| Propagation Delay | $\Delta V_{IN} = 0.5V$ | | 1.2 | | | 1.5 | | ns |
| Harmonic Distortion | $f > 1$ kHz | | <0.1 | | | <0.1 | | % |

Note 1: LH0033 is 100% production tested as specified at 25°C, 125°C, and -55°C. LH0033AC/C are 100% production tested at 25°C only. Specifications at temperature extremes are verified by sample testing, but these limited are not used to calculate outgoing quality level.

Note 2: Specification is at 25°C junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25^\circ\text{C}$. When supply voltages are $\pm 15V$, no-load operating junction temperature may rise 40-60°C above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: LH0033 is 100% production tested for this parameter. LH0033C is sample tested only. Limits are not used to calculate outgoing quality levels. $\Delta V_{OS}/\Delta T$ is the average value calculated from measurements at 25°C and T_{MAX} .

Note 4: Measured in still air 7 minutes after application of power. Guaranteed through correlated automatic pulse testing.

Note 5: Guaranteed through correlated automatic pulse testing at $T_J = 25^\circ\text{C}$.

Note 6: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

Note 7: Refer to RETS0033 for the LH0033G military specifications.

DC Electrical Characteristics $V_S = \pm 15V, T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Note 1)

| Parameter | Conditions | LH0063C | | | Units |
|--|---|----------|----------|-----------|------------------|
| | | Min | Typ | Max | |
| Output Offset Voltage | $R_S \leq 100k\Omega, T_J = 25^\circ C, R_L = 100\Omega$ (Note 2) | | 10 | 50 100 | mV mV |
| Average Temperature Coefficient of Output Offset Voltage | $R_S \leq 100k\Omega$ | | 300 | | $\mu V/^\circ C$ |
| Input Bias Current | $T_J = 25^\circ C$ (Note 2) | | 10 | 30 100 | nA nA |
| Voltage Gain | $V_{IN} = \pm 10V, R_S \leq 100k\Omega, R_L = 1k\Omega$ | 0.94 | 0.96 | 1.0 | V/V |
| Voltage Gain | $V_{IN} = \pm 10V, R_S \leq 100k\Omega, R_L = 50\Omega$ $T_J = 25^\circ C$ | 0.91 | 0.93 | 0.98 | V/V |
| Input Capacitance | Case Shorted to Output | | 8.0 | | pF |
| Output Impedance | $V_{OUT} = \pm 10V, R_S \leq 100k\Omega, R_L = 50\Omega$ | | 1.0 | 4.0 | Ω |
| Output Current Swing | $V_{IN} = \pm 10V, R_S \leq 100k\Omega$ | 0.2 | 0.25 | | A |
| Output Voltage Swing | $R_L = 50\Omega$ | ± 10 | ± 13 | | V |
| Output Voltage Swing | $V_S = \pm 5.0V, R_L = 50\Omega, T_J = 25^\circ C$ | 5.09 | 7.0 | | Vp-p |
| Supply Current | $T_J = 25^\circ C, R_L = \infty, V_S = \pm 15V$ | | 50 | 65 | mA |
| Supply Current | $V_S = \pm 5.0V$ | | 40 | | mA |
| Power Consumption | $T_J = 25^\circ C, R_L = \infty, V_S = \pm 15V$ | | 1.5 | 1.95 | W |
| Power Consumption | $V_S = \pm 5.0V$ | | 400 | | mW |

AC Electrical Characteristics $T_J = 25^\circ C, V_S = \pm 15V, R_S = 50\Omega, R_L = 50\Omega$ (Note 3)

| Parameter | Conditions | LH0063C | | | Units |
|---------------------|--|---------|------|-----|------------|
| | | Min | Typ | Max | |
| Slew Rate | $R_L = 1.0k\Omega, V_{IN} = \pm 10V$ | | 6000 | | V/ μs |
| Slew Rate | $R_L = 50\Omega, V_{IN} = \pm 10V, T_J = 25^\circ C$ | 2000 | 2400 | | V/ μs |
| Bandwidth | $V_{IN} = 1.0V_{rms}$ | | 200 | | MHz |
| Phase Non-Linearity | $BW = 1.0Hz$ to $20MHz$ | | 2.0 | | degrees |
| Rise Time | $\Delta V_{IN} = 0.5V$ | | 1.9 | | ns |
| Propagation Delay | $\Delta V_{IN} = 0.5V$ | | 2.1 | | ns |
| Harmonic Distortion | | | <0.1 | | % |

Note 1: LH0063C is 100% production tested at $25^\circ C$ only. Specifications at temperature extremes are verified by sample testing, but these limits are not used to calculate outgoing quality level.

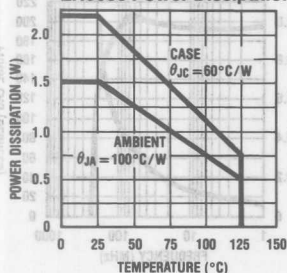
Note 2: Specification is at $25^\circ C$ junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed the value at $T_J = 25^\circ C$. When supply voltages are $\pm 15V$, no-load operating junction temperature may rise $40-60^\circ C$ above ambient, and more under load conditions. Accordingly, V_{OS} may change one to several mV, and I_B will change significantly during warm-up. Refer to I_B vs temperature graph for expected values.

Note 3: Not 100% production tested; verified by sample testing only. Limits are not used to calculate outgoing quality level.

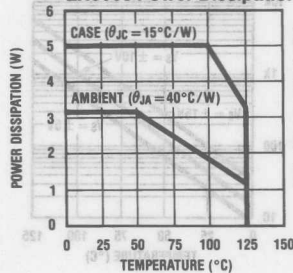
Typical Performance Characteristics

LH0033/LH0063

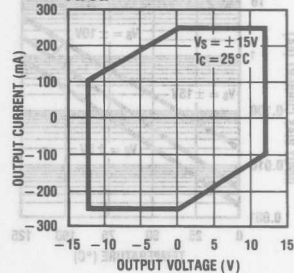
LH0033 Power Dissipation



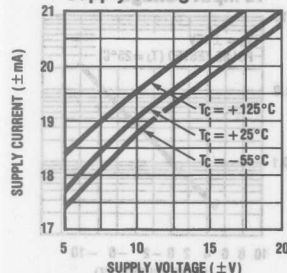
LH0063 Power Dissipation



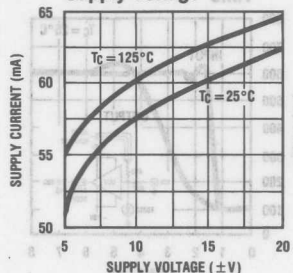
LH0063 DC Safe Operating Area



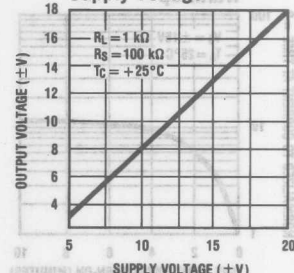
LH0033 Supply Current vs Supply Voltage



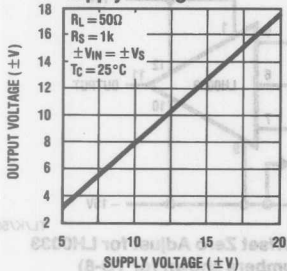
LH0063 Supply Current vs Supply Voltage



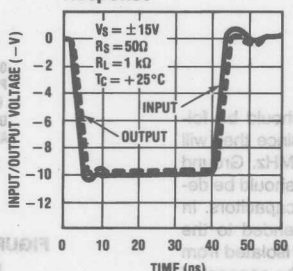
LH0033 Output Voltage vs Supply Voltage



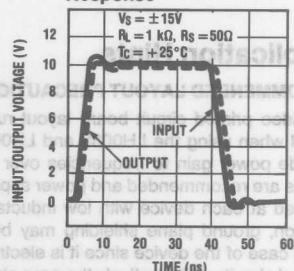
LH0063 Output Voltage vs Supply Voltage



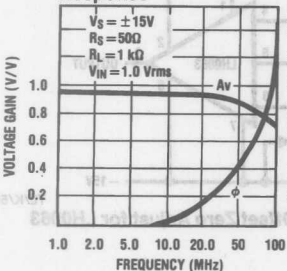
LH0033 Negative Pulse Response



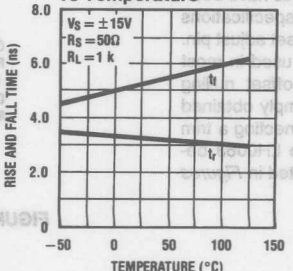
LH0033 Positive Pulse Response



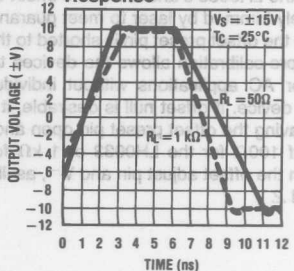
LH0033 Frequency Response



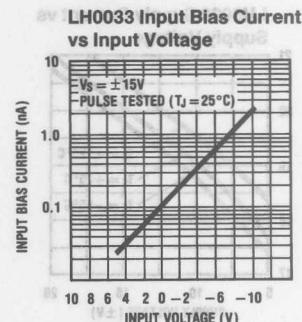
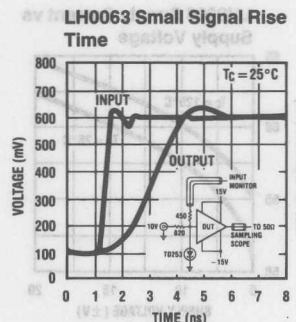
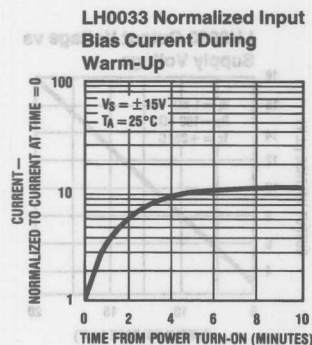
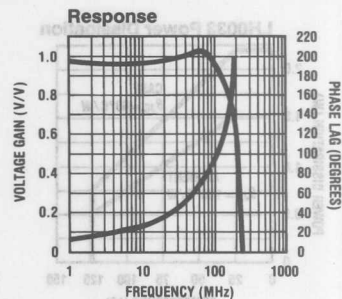
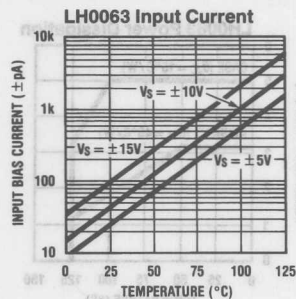
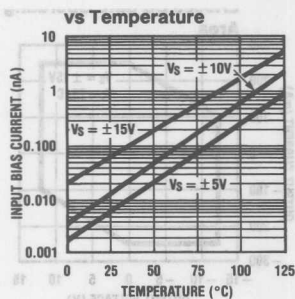
LH0033 Rise and Fall Time vs Temperature



LH0063 Large Signal Pulse Response



TL/K/5507-4



TL/K/5507-5

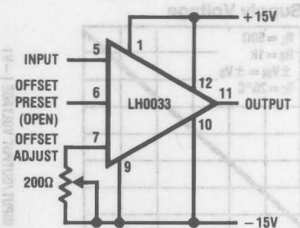
Application Hints

RECOMMENDED LAYOUT PRECAUTIONS

RF/video printed circuit board layout rules should be followed when using the LH0033 and LH0063 since they will provide power gain to frequencies over 100 MHz. Ground planes are recommended and power supplies should be decoupled at each device with low inductance capacitors. In addition, ground plane shielding may be extended to the metal case of the device since it is electrically isolated from internal circuitry. Alternatively the case should be connected to the output to minimize input capacitance.

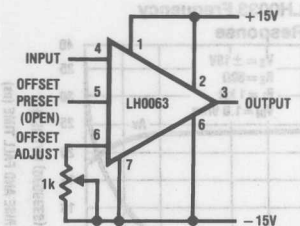
OFFSET VOLTAGE ADJUSTMENT

Both the LH0033's and LH0063's offset voltages have been actively trimmed by laser to meet guaranteed specifications when the offset preset pin is shorted to the offset adjust pin. This pre-calibration allows the devices to be used in most DC or AC applications without individually offset nulling each device. If offset null is desirable, it is simply obtained by leaving the offset preset pin open and connecting a trim pot of 100Ω for the LH0033 or 1 kΩ for the LH0063 between the offset adjust pin and V^- , as illustrated in Figures 1 and 2.



TL/K/5507-6

FIGURE 1. Offset Zero Adjust for LH0033
(Pin numbers shown for TO-8)



TL/K/5507-7

FIGURE 2. Offset Zero Adjust for LH0063

Application Hints (Continued)

OPERATION FROM SINGLE OR ASYMMETRICAL POWER SUPPLIES

Both device types may be readily used in applications where symmetrical supplies are unavailable or not desirable. A typical application might be an interface to a MOS shift register where $V^+ = +5V$ and $V^- = -12V$. In this case, an apparent output offset occurs due to the device's voltage gain of less than unity. This additional output offset error may be predicted by:

$$\Delta V_O \approx (1 - A_V) \frac{(V^+ - V^-)}{2} = 0.005(V^+ - V^-)$$

where:

A_V = No load voltage gain, typically 0.99

V^+ = Positive supply voltage

V^- = Negative supply voltage

For the above example, ΔV_O would be $-35mV$. This may be adjusted to zero as described in Figure 2. For AC coupled applications, no additional offset occurs if the DC input is properly biased as illustrated in the Typical Applications section.

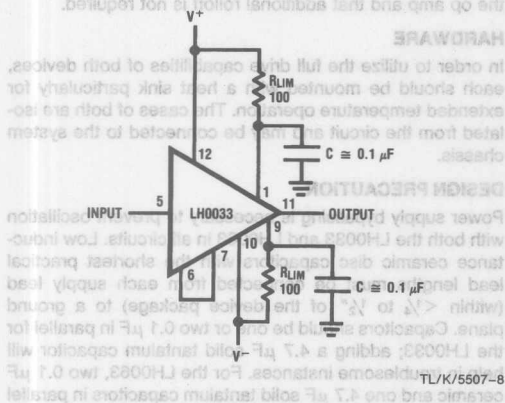


FIGURE 3. LH0033 Using Resistor Current Limiting

SHORT CIRCUIT PROTECTION

In order to optimize transient response and output swing, output current limit has been omitted from the LH0033 and LH0063. Short circuit protection may be added by inserting appropriate value resistors between V^+ and V_C^+ pins and V^- and V_C^- pins as illustrated in Figures 3 and 4. Resistor values may be predicted by:

$$R_{LIM} \approx \frac{V^+ - V^-}{I_{SC}}$$

where:

$I_{SC} \leq 100$ mA for LH0033

$I_{SC} \leq 250$ mA for LH0063

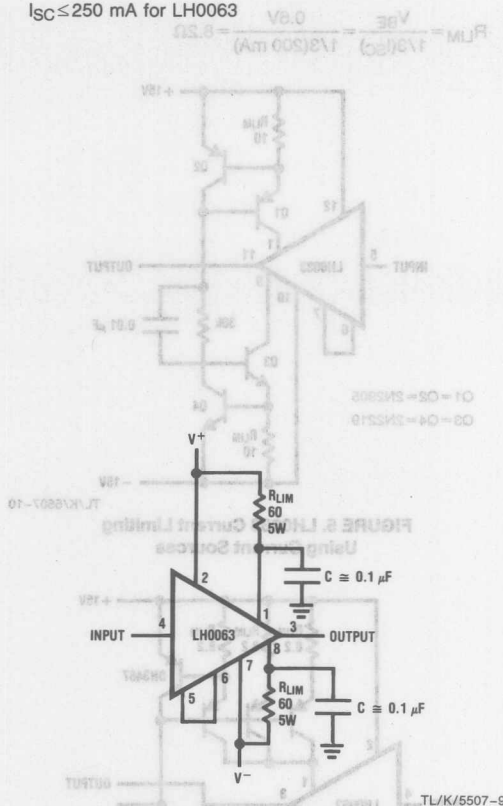


FIGURE 4. LH0063 Using Resistor Current Limiting

Application Hints (Continued)

The inclusion of limiting resistors in the collectors of the output transistors reduces output voltage swing. Decoupling V_{C+} and V_{C-} pins with capacitors to ground will retain full output swing for transient pulses. Alternate active current limit techniques that retain full DC output swing are shown in *Figures 5 and 6*. In *Figures 5 and 6*, the current sources are saturated during normal operation, thus apply full supply voltage to the V_C pins. Under fault conditions, the voltage decreases as required by the overload.

For Figure 5:

$$R_{LIM} = \frac{V_{BE}}{I_{SC}} = \frac{0.6V}{60\text{ mA}} = 10\Omega$$

In *Figure 6*, quad transistor arrays are used to minimize can count and:

$$R_{LIM} = \frac{V_{BE}}{1/3(I_{SC})} = \frac{0.6V}{1/3(200 \text{ mA})} = 8.2\Omega$$

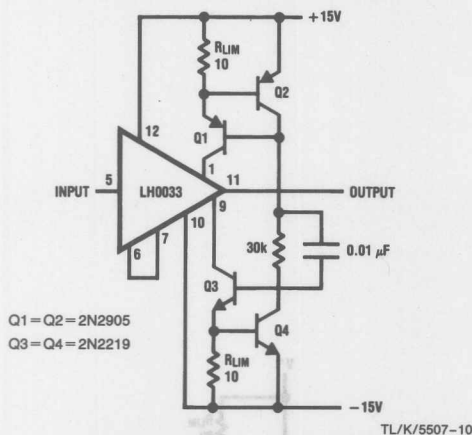


FIGURE 5. LH0033 Current Limiting Using Current Sources

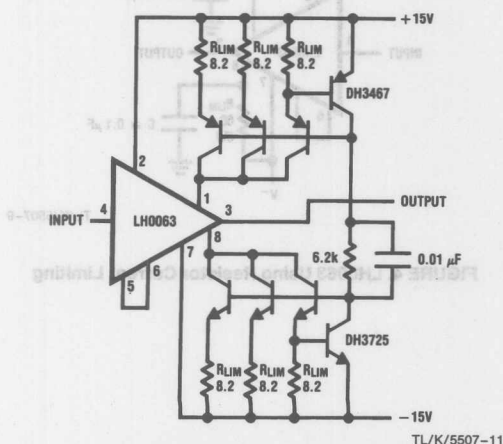


FIGURE 6. LH0063 Current Limiting Using Current Sources

CAPACITIVE LOADING

Both the LH0033 and LH0063 are designed to drive capacitive loads such as coaxial cables in excess of several thousand picofarads without susceptibility to oscillation. However, peak current resulting from $(C \times dV/dt)$ should be limited below absolute maximum peak current ratings for the devices.

Thus for the LH0033:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 250 \text{ mA}$$

and for the LH0063:

$$\left(\frac{\Delta V_{IN}}{\Delta t}\right) \times C_L \leq I_{OUT} \leq \pm 500 \text{ mA}$$

In addition, power dissipation resulting from driving capacitive loads plus standby power should be kept below total package power rating:

$$P_{Dpkg.} \geq P_{DC} + P_{AC}$$

$$P_{Dpkg.} \geq (V^+ - V^-) \times I_S + P_{AC}$$

$$P_{AC} \cong (V_p - p)^2 \times f \times C_l$$

where:

V_{p-p} = Peak-to-peak output voltage swing

f = Frequency

C_l = Load Capacitance

OPERATION WITHIN AN OP AMP LOOP

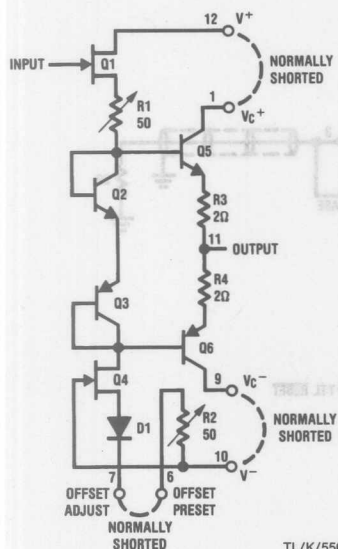
Both devices may be used as a current booster or isolation buffer within a closed loop with op amps such as LM6218, LM6361 or LH0032. An isolation resistor of 47Ω should be used between the op amp output and the input of LH0033. The wide bandwidths and high slew rates of the LH0033 and LH0063 assure that the loop has the characteristics of the op amp and that additional rolloff is not required.

HARDWARE

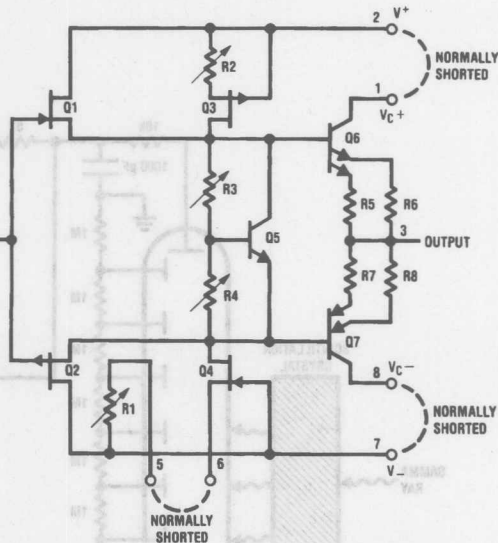
In order to utilize the full drive capabilities of both devices, each should be mounted with a heat sink particularly for extended temperature operation. The cases of both are isolated from the circuit and may be connected to the system chassis.

DESIGN PRECAUTION

Power supply bypassing is necessary to prevent oscillation with both the LH0033 and LH0063 in all circuits. Low inductance ceramic disc capacitors with the shortest practical lead lengths must be connected from each supply lead (within $<1/4$ to $1/2$ " of the device package) to a ground plane. Capacitors should be one or two $0.1 \mu\text{F}$ in parallel for the LH0033; adding a $4.7 \mu\text{F}$ solid tantalum capacitor will help in troublesome instances. For the LH0063, two $0.1 \mu\text{F}$ ceramic and one $4.7 \mu\text{F}$ solid tantalum capacitors in parallel will be necessary on each supply lead.



TL/K/5507-12

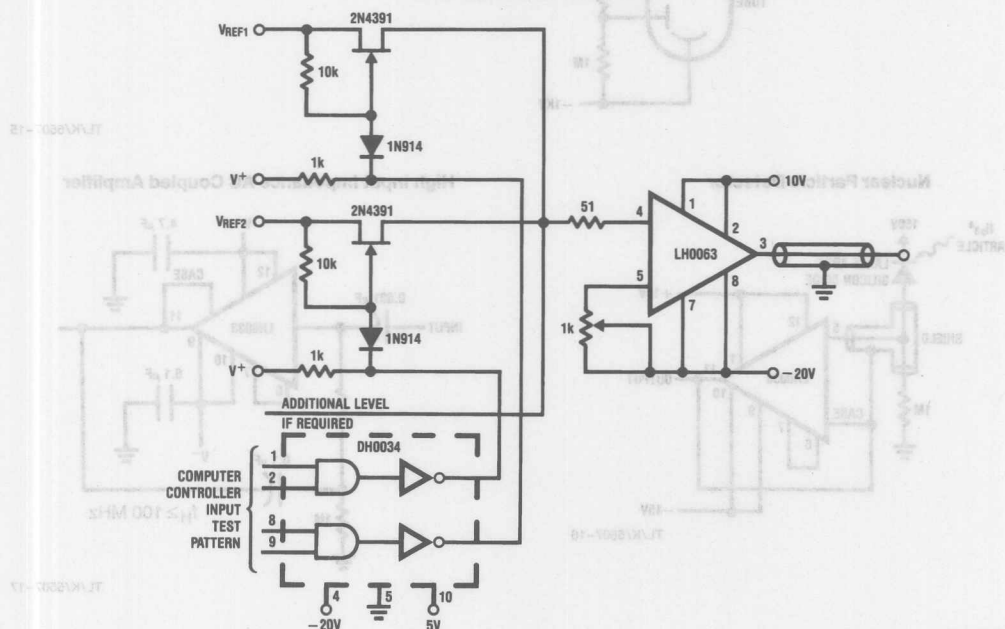


TL/K/5507-13

Pin numbers shown for TO-8 ("G") package.

Typical Applications

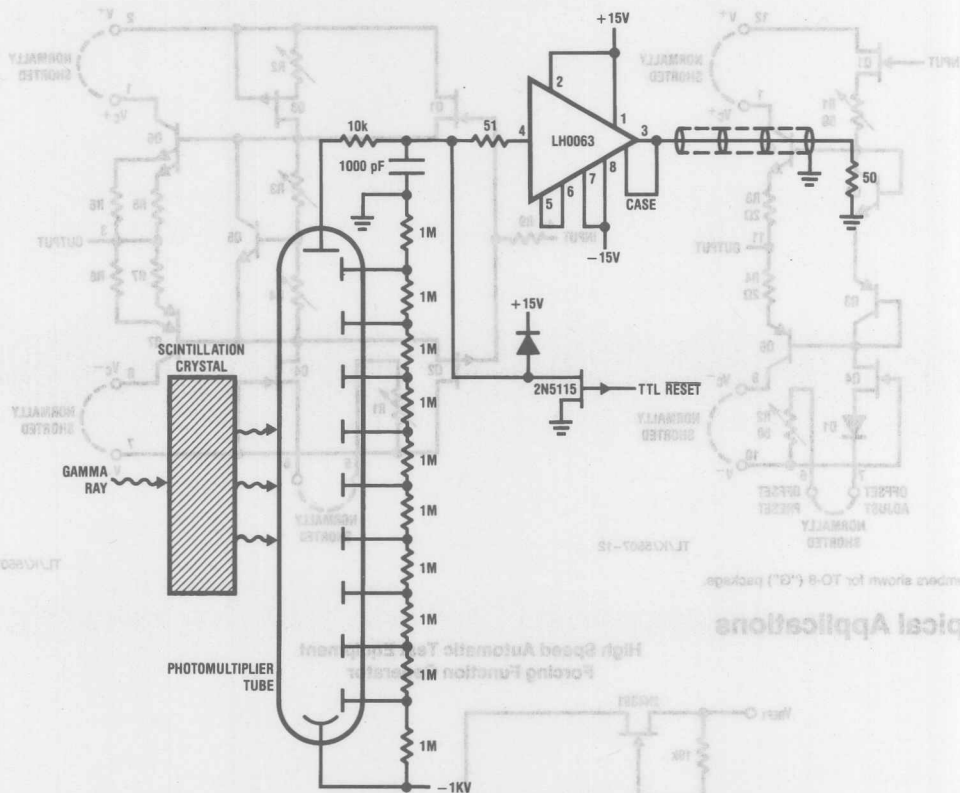
High Speed Automatic Test Equipment Forcing Function Generator



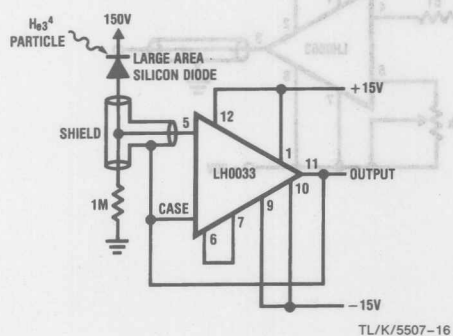
TL/K/5507-14

Typical Applications (Continued)

Gamma Ray Pulse Integrator

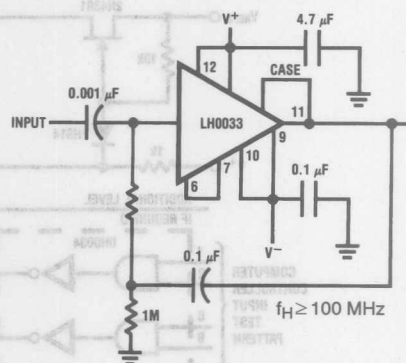


Nuclear Particle Detector



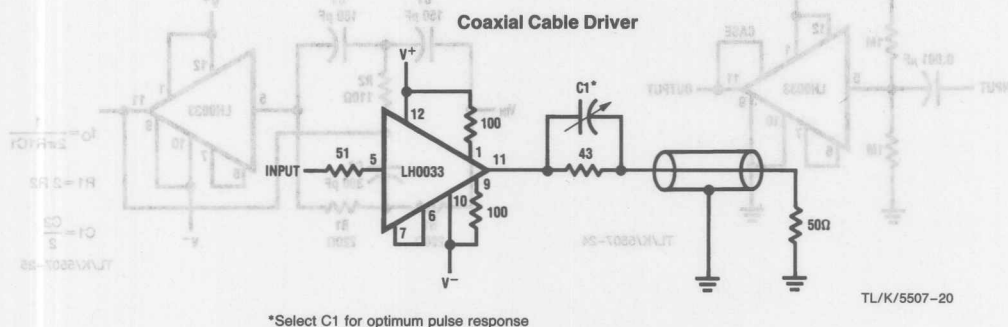
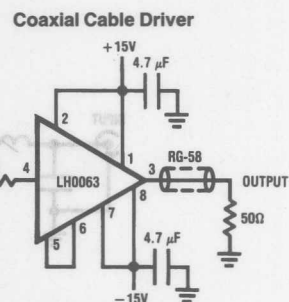
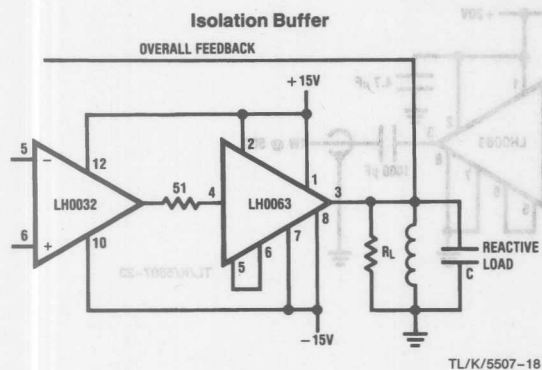
TL/K/5507-16

High Input Impedance AC Coupled Amplifier

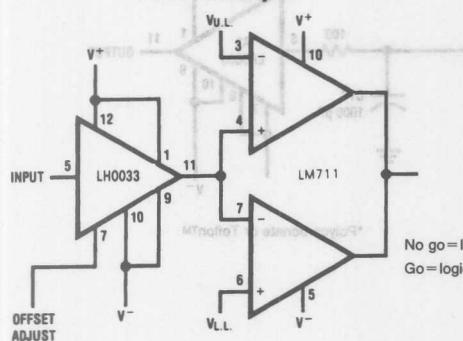


TL/K/5507-17

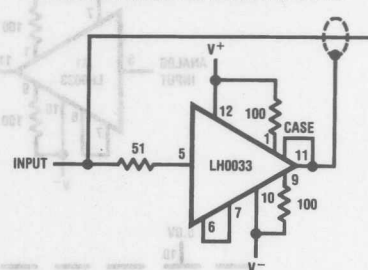
Typical Applications (Continued)



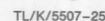
High Input Impedance Comparator with Offset Adjust



Instrumentation Shield/Line Driver



4.5 MHz Notch Filter



LH4001 Wideband Current Buffer

General Description

The LH4001 is a high speed unity gain buffer designed to provide high current drive capability at frequencies from DC to over 25 MHz. It is capable of providing a continuous output current of ± 100 mA and a peak of ± 200 mA.

The LH4001 is designed to fulfill a wide range of applications such as impedance transformation, high impedance input buffers for A/D converters and comparators, as well as high speed line drivers. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased to ± 100 mA.

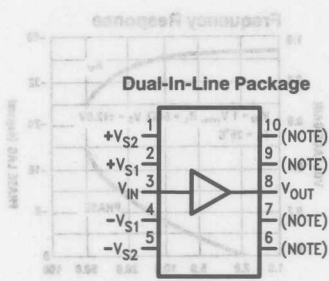
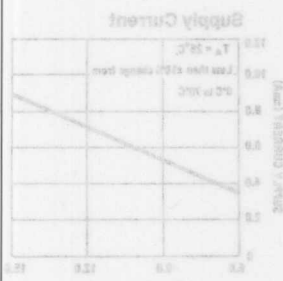
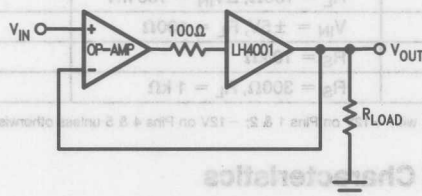
Features

- DC to 25 MHz bandwidth
- 125 V/ μ s slew rate
- Drives ± 10 V into 50 Ω
- Operates from ± 5 to ± 20 V supplies
- Output swing approaches supply voltage

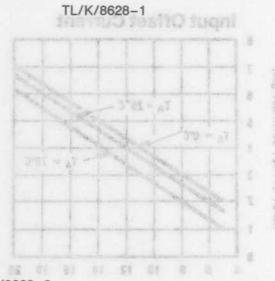
Applications

- Boost op amp output
- Buffer amplifiers
- Isolate capacitive loads
- Drive long cables

Typical Applications and Connection Diagram



Top View



*Note: Electrically connected internally. No connection should be made to these pins.

Order Number LH4001CN
See NS Package Number N10A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|---------------------|
| Supply Voltage, V_S | $\pm 22V$ |
| Continuous Output Current, I_O | $\pm 100\text{ mA}$ |
| Peak Output Current, $I_{O(\text{peak})}$ (50 ms On/1 Sec Off) | $\pm 200\text{ mA}$ |
| Input Voltage Range, V_{IN} | $\pm V_S$ |
| Power Dissipation | 500 mW |

| | |
|--------------------------------------|---|
| Storage Temperature Range, T_{STG} | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature, T_J | 150°C |
| Lead Temp. (Soldering, < 10 seconds) | 260°C |
| ESD rating is to be determined. | |

Operating Ratings

| | |
|----------------------------------|--|
| Temperature Range, T_A | 0°C to $+70^\circ\text{C}$ |
| Thermal Resistance θ_{JA} | 120°C/W |

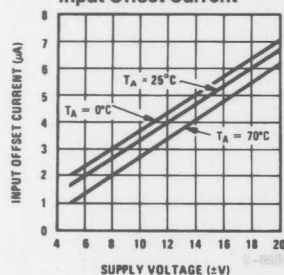
Electrical Characteristics (Note 1)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|--------------------|--|----------|----------|----------|------------------|
| A_V | Voltage Gain | $R_S = 10\text{ k}\Omega$, $R_L = 1\text{ k}\Omega$ $V_{IN} = \pm 10V$ | 0.95 | 0.97 | 1 | V/V |
| R_{IN} | Input Impedance | $R_S = 200\text{ k}\Omega$, $R_L = 1\text{ k}\Omega$ $V_{IN} = \pm 1.0V$ | 180 | 400 | | k Ω |
| R_{OUT} | Output Impedance | $R_S = 10\text{ k}\Omega$, $R_L = 50\Omega$ $V_{IN} = \pm 1.0V$ | | 6 | 10 | Ω |
| V_O | Output Swing | $V_S = \pm 15V$, $R_S = 50\Omega$ $R_L = 100\Omega$, $V_{IN} = \pm 12V$ | ± 10 | ± 11 | | V |
| I_B | Input Bias Current | $R_S = 10\text{ k}\Omega$, $R_L = 1\text{ k}\Omega$ | | ± 10 | ± 50 | μA |
| t_r | Rise Time | $R_L = 100\Omega$, $\Delta V_{IN} = 100\text{ mV}$ | | 7 | | ns |
| SR | Slew Rate | $V_{IN} = \pm 5V$, $R_L = 100\Omega$ | | 125 | | V/ μs |
| I_S | Supply Current | $R_S = 10\text{ k}\Omega$ | | ± 6 | ± 10 | mA |
| V_{OS} | Offset Voltage | $R_S = 300\Omega$, $R_L = 1\text{ k}\Omega$ | | ± 10 | ± 50 | mV |

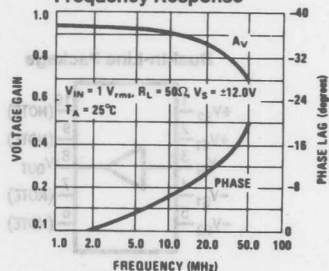
Note 1: Specification applies for $T_A = 25^\circ\text{C}$ with $+12V$ on Pins 1 & 2; $-12V$ on Pins 4 & 5 unless otherwise specified.

Typical Performance Characteristics

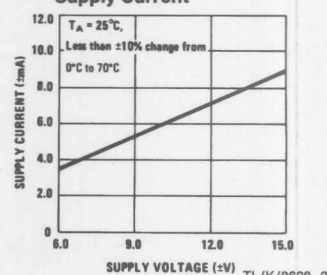
Input Offset Current



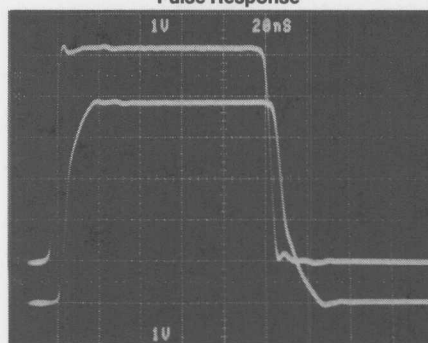
Frequency Response



Supply Current



Pulse Response



TOP TRACE = INPUT

BOTTOM TRACE = OUTPUT

$V_{IN} = \pm 2.5V$, $R_S = R_L = 50\Omega$

TL/K/8628-10

Applications Information

Figure 1 shows a simple implementation of a non-inverting buffer amplifier of unity gain. Popular industry standard operational amplifiers such as LF156, LF351, LF411, LF441, LM11, LM741, etc. can be used in this configuration. Due to the high bandwidth of the LH4001, it is suitable for use with most monolithic op amps.

Figure 2 shows an implementation of an inverting amplifier with output current capability in excess of ± 100 mA. The gain of this amplifier is determined by the values of R_F and R_{IN} . The resistor between the non-inverting input and ground is used to minimize the output offset voltage resulting from the input bias current.

Because of its high current drive capability, the LH4001 buffer amplifier is suitable for driving terminated or unterminated co-axial cables, and high current or reactive loads.

Figure 3 shows a co-axial cable drive circuit. The 43Ω resistor matches the driving source to the cable, however, its inclusion rarely will result in substantial improvement in pulse response into a terminated cable. If the 43Ω resistor is included, the output voltage to the load is about half what it would be without the near end termination.

Figure 4 shows a non-inverting amplifier with gain and output current capability in excess of ± 100 mA. It is capable of providing ± 10 mA into a $1\text{ k}\Omega$ load or ± 100 mA into a 100Ω load ($\pm 10\text{V}$ swing). Figures 5 and 6 show two different methods of providing current limit or short circuit protection for the LH4001. In Figure 6, the 10Ω resistor limits the output current to approximately 70 mA. This circuit is highly recommended if there is a potential for a short circuit to occur.

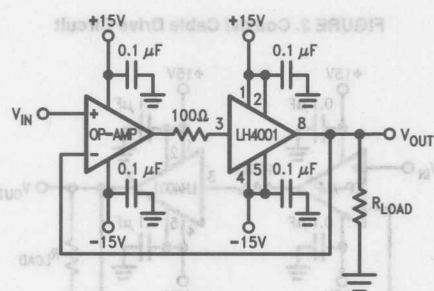


FIGURE 1. Non-Inverting Buffer Amplifier

TL/K/8628-4

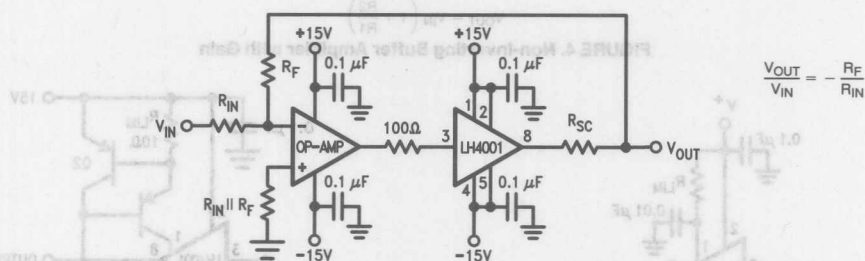


FIGURE 2. Inverting Buffer Amplifier with Current Limit

TL/K/8628-6

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_{IN}}$$

Applications Information (Continued)

Figure 3 shows a coaxial cable drive circuit. The 43Ω resistor is for matching the driving source to the cable. However, its inclusion rarely will result in substantial improvement in signal-to-noise ratio. The 43Ω resistor is used to convert the output voltage to the load is about half what it would be without the resistor and termination.

Figure 4 shows an inverting amplifier with gain and current limiting. The output current capability is in excess of ±100 mA. It is capable of driving a load of ±10 mA into a 1 kΩ load or ±100 mA into a 100 Ω load. The 100 Ω resistor is used to provide current limiting or short circuit protection. Figures 5 and 6 show two different methods of current limiting for the LH4001. In Figure 5, the 10Ω resistor limits the current to approximately 70 mA. This circuit is highly recommended if there is a potential for a short circuit to ground.

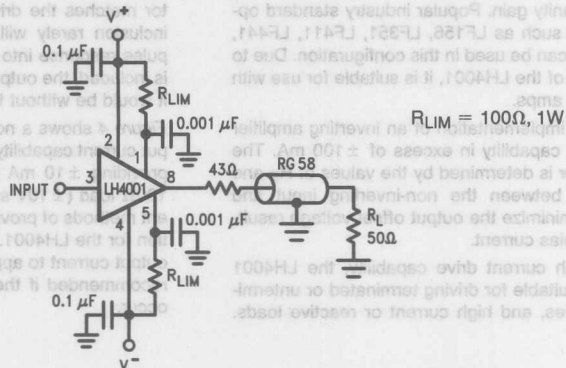
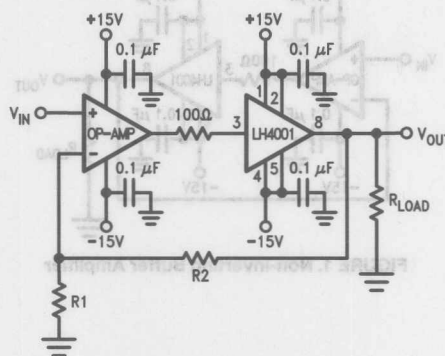
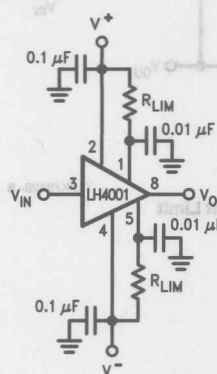


FIGURE 3. Coaxial Cable Drive Circuit

TL/K/8628-7

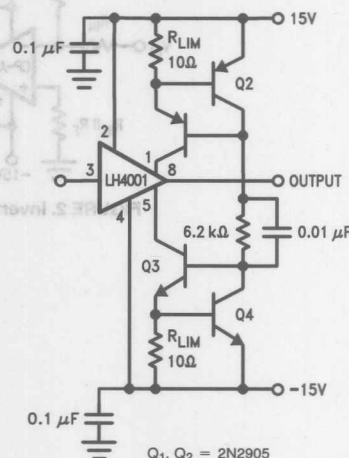


TL/K/8628-5

$$V_{OUT} = V_{IN} \left(1 + \frac{R_2}{R_1} \right)$$
 FIGURE 4. Non-Inverting Buffer Amplifier with Gain


TL/K/8628-8

FIGURE 5. LH4001 Using Resistor Current Limiting



Q₁, Q₂ = 2N2905
Q₃, Q₄ = 2N2219

TL/K/8628-9

FIGURE 6. Current Limit Using Current Sources

LH4002 Wideband Video Buffer

General Description

The LH4002 is a high speed voltage follower designed to drive video signals from DC up to 200 MHz. At voltage supplies of $\pm 5V$, the LH4002 will provide up to 40 mA into 50Ω at slew rates in excess of $1000 V/\mu s$.

The device is intended to fulfill a wide range of high speed applications including video distribution, impedance transformation, and load isolation. It is also suitable for use in current booster applications within an op amp loop. This allows the output current capability of existing op amps to be increased.

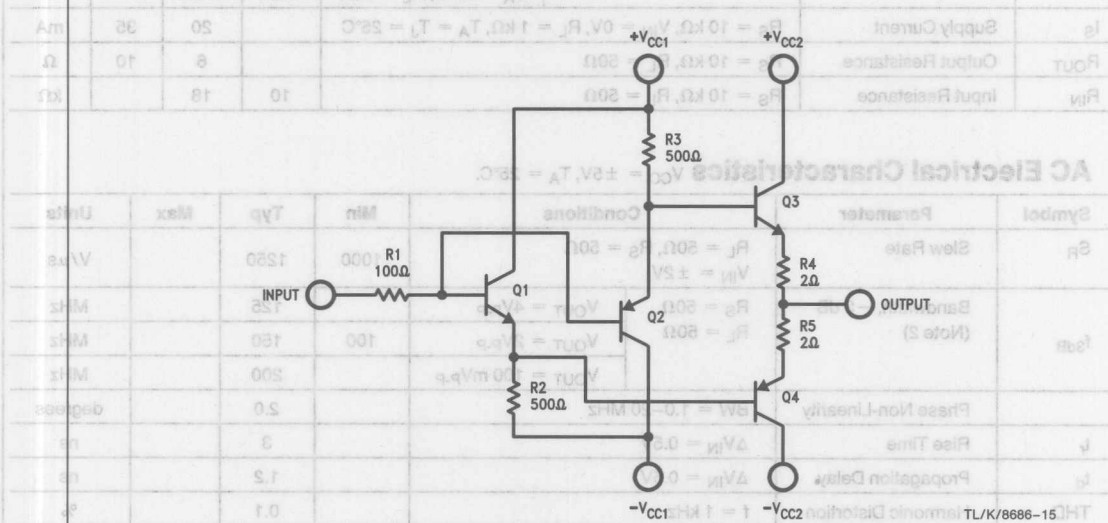
Features

- DC to 200 MHz Bandwidth with $V_S = \pm 5V$
- $1250 V/\mu s$ Slew Rate into 50Ω
- 150 MHz Bandwidth with $V_S = \pm 5V$, $R_L = 50\Omega$ and Voltage Swing = $2 V_{P-P}$

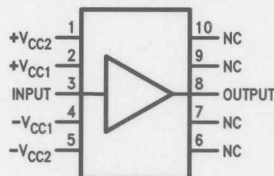
Applications

- Wideband Amplifier Buffer
- Wideband Line Driver

Schematic and Connection Diagrams



Dual-In-Line Package



Top View

Order Number LH4002CN
See NS Package Number N10A

TL/K/8686-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|---|
| Supply Voltage, V_S | $\pm 6V$ |
| Input Voltage Range, V_{IN} | $\pm V_S$ |
| Continuous Output Current, I_O | $\pm 60\text{ mA}$ |
| Storage Temperature Range, T_{STG} | -65°C to $+150^\circ\text{C}$ |

Operating Temperature Range, T_A

LH4002C

-25°C to $+85^\circ\text{C}$

Junction Temperature, T_J

150°C

Lead Temperature (Soldering, 10 sec)

300°C

ESD rating is to be determined.

DC Electrical Characteristics $V_{CC} = \pm 5V$, $T_{min} \leq T_A \leq T_{max}$ unless otherwise stated.

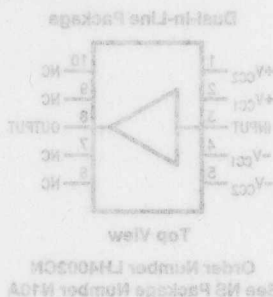
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|----------------------|---|-----------|-----------|-----|---------------|
| V_{OS} | Input Offset Voltage | $T_A = T_J = 25^\circ\text{C}$ $R_S = 150\Omega$, $R_L = 50\Omega$ | | 20 | 50 | mV |
| I_B | Input Bias Current | $R_S = 1\text{ k}\Omega$, $R_L = 50\Omega$ | | 100 | 200 | μA |
| A_V | DC Voltage Gain | $R_S = 10\text{ k}\Omega$, $R_L = 1.0\text{ k}\Omega$, $V_{IN} = \pm 2V$ | 0.95 | 0.97 | | V/V |
| V_O | Output Voltage Swing | $R_S = 150\Omega$, $V_{IN} = \pm 2.5V$ $R_L = 1\text{ k}\Omega$ | ± 2.2 | ± 2.4 | | V |
| | | $T_A = 25^\circ\text{C}$, $R_L = 50\Omega$ | ± 2.0 | ± 2.2 | | V |
| I_S | Supply Current | $R_S = 10\text{ k}\Omega$, $V_{IN} = 0V$, $R_L = 1\text{ k}\Omega$, $T_A = T_J = 25^\circ\text{C}$ | | 20 | 35 | mA |
| R_{OUT} | Output Resistance | $R_S = 10\text{ k}\Omega$, $R_L = 50\Omega$ | | 6 | 10 | Ω |
| R_{IN} | Input Resistance | $R_S = 10\text{ k}\Omega$, $R_L = 50\Omega$ | 10 | 18 | | k Ω |

AC Electrical Characteristics $V_{CC} = \pm 5V$, $T_A = 25^\circ\text{C}$.

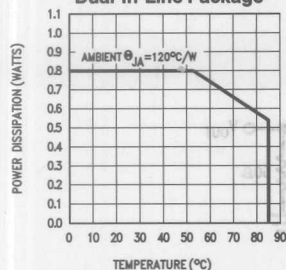
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------|---------------------------------------|--|------|------|-----|------------------|
| S_R | Slew Rate | $R_L = 50\Omega$, $R_S = 50\Omega$ $V_{IN} = \pm 2V$ | 1000 | 1250 | | V/ μs |
| f_{3dB} | Bandwidth, -3 dB (Note 2) | $R_S = 50\Omega$ $R_L = 50\Omega$ $V_{OUT} = 4V_{P-P}$ | | 125 | | MHz |
| | | $V_{OUT} = 2V_{P-P}$ | 100 | 150 | | MHz |
| | | $V_{OUT} = 100\text{ mV}_{P-P}$ | | 200 | | MHz |
| | Phase Non-Linearity | $BW = 1.0\text{--}20\text{ MHz}$ | | 2.0 | | degrees |
| t_r | Rise Time | $\Delta V_{IN} = 0.5V$ | | 3 | | ns |
| t_d | Propagation Delay | $\Delta V_{IN} = 0.5V$ | | 1.2 | | ns |
| THD | Harmonic Distortion | $f = 1\text{ kHz}$ | | 0.1 | | % |

Note 1: Under normal operating conditions $+V_{CC1}$ and $+V_{CC2}$ should be connected together, and $-V_{CC1}$ and $-V_{CC2}$ should be connected together.

Note 2: Guaranteed by design. This parameter is sample tested.

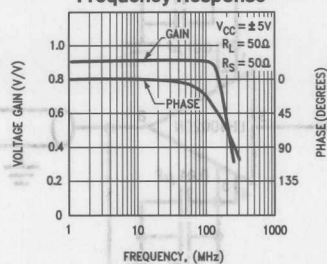


Maximum Power Dissipation Dual-In-Line Package



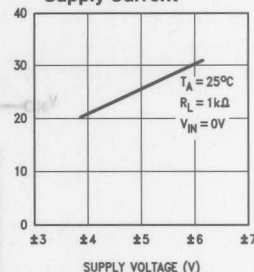
TL/K/8686-12

Frequency Response



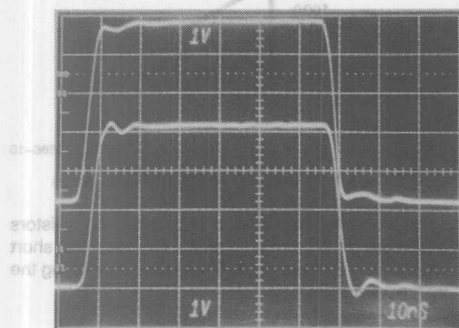
TL/K/8686-5

Supply Current

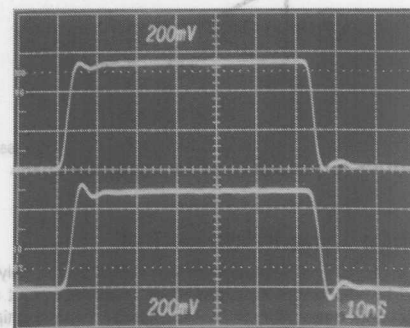


TL/K/8686-6

Pulse Response



TL/K/8686-7



TL/K/8686-8

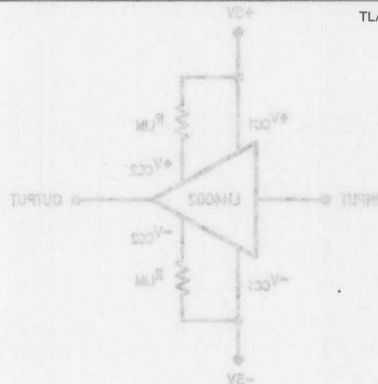


FIGURE 4. LHM02 Using Resistor Current Limiting

Short Circuit Protection

In order to optimize transient response and output swing, output current limits have been omitted from the LHM02. Short circuit protection may be added by inserting appropriate value resistors between V_{CC} and $+V_{CC}$ pins and between $-V_{CC}$ and $-V_{CC}$ pins as illustrated in Figure 4. Resistor values may be predicted by:

$$R_{LIM} = \frac{+V_{CC} - (-V_{CC})}{I_{SC}}$$

Typical Applications

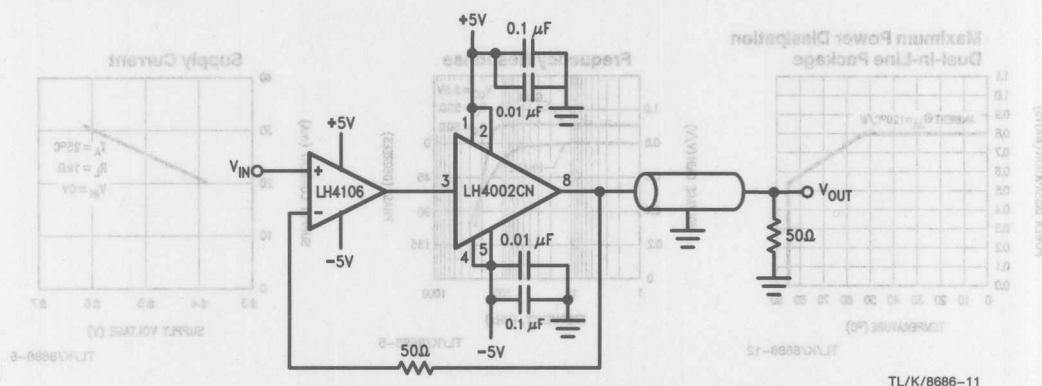


FIGURE 1. Wideband Unity Gain Amplifier Using LH4002CN

TL/K/8686-11

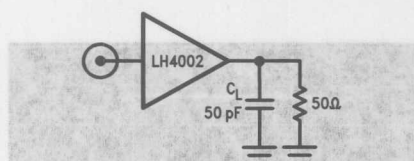


FIGURE 2. Compensation for Capacitive Loads

TL/K/8686-9

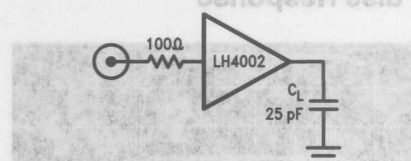


FIGURE 3. Compensation for Capacitive Loads

TL/K/8686-10

Applications Information

The high speed performance of the LH4002 can only be realized by taking certain precautions in circuit layout and power supply decoupling. Low inductance ceramic chip or disc power supply decoupling capacitors of 0.01 μF in parallel with 0.1 μF should be connected with the shortest practical lead length between device supply leads and a ground plane. Failure to follow these rules can result in oscillations. When driving a capacitive load such as inputs to flash converters, the circuits in Figure 2 and 3 can be used to minimize the amount of overshoot and ringing at the outputs. Figure 2 indicates that a 50 Ω should be placed in parallel with the load and Figure 3 recommends that a 100 Ω resistor be placed in series with the input to the LH4002.

Short Circuit Protection

In order to optimize transient response and output swing, output current limits have been omitted from the LH4002. Short circuit protection may be added by inserting appropriate value resistors between $+V_{CC1}$ and $+V_{CC2}$ pins and between $-V_{CC1}$ and $-V_{CC2}$ pins as illustrated in Figure 4. Resistor values may be predicted by:

$$R_{LIM} = \frac{+V_{CC1}}{I_{SC}} = \frac{-V_{CC1}}{I_{SC}}$$

where $I_{SC} \leq 100 \text{ mA}$. The inclusion of 50 Ω limiting resistors in the collectors of the output transistors limits the short circuit current to approximately 100 mA without reducing the output voltage swing.

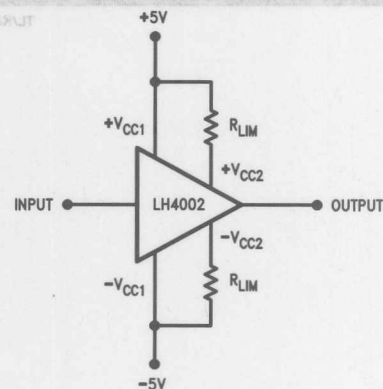


FIGURE 4. LH4002 Using Resistor Current Limiting

TL/K/8686-20

LM102/LM302 Voltage Followers

General Description

The LM102 series are high-gain operational amplifiers designed specifically for unity-gain voltage follower applications. Built on a single silicon chip, the devices incorporate advanced processing techniques to obtain very low input current and high input impedance. Further, the input transistors are operated at zero collector-base voltage to virtually eliminate high temperature leakage currents. It can therefore be operated in a temperature stabilized component oven to get extremely low input currents and low offset voltage drift.

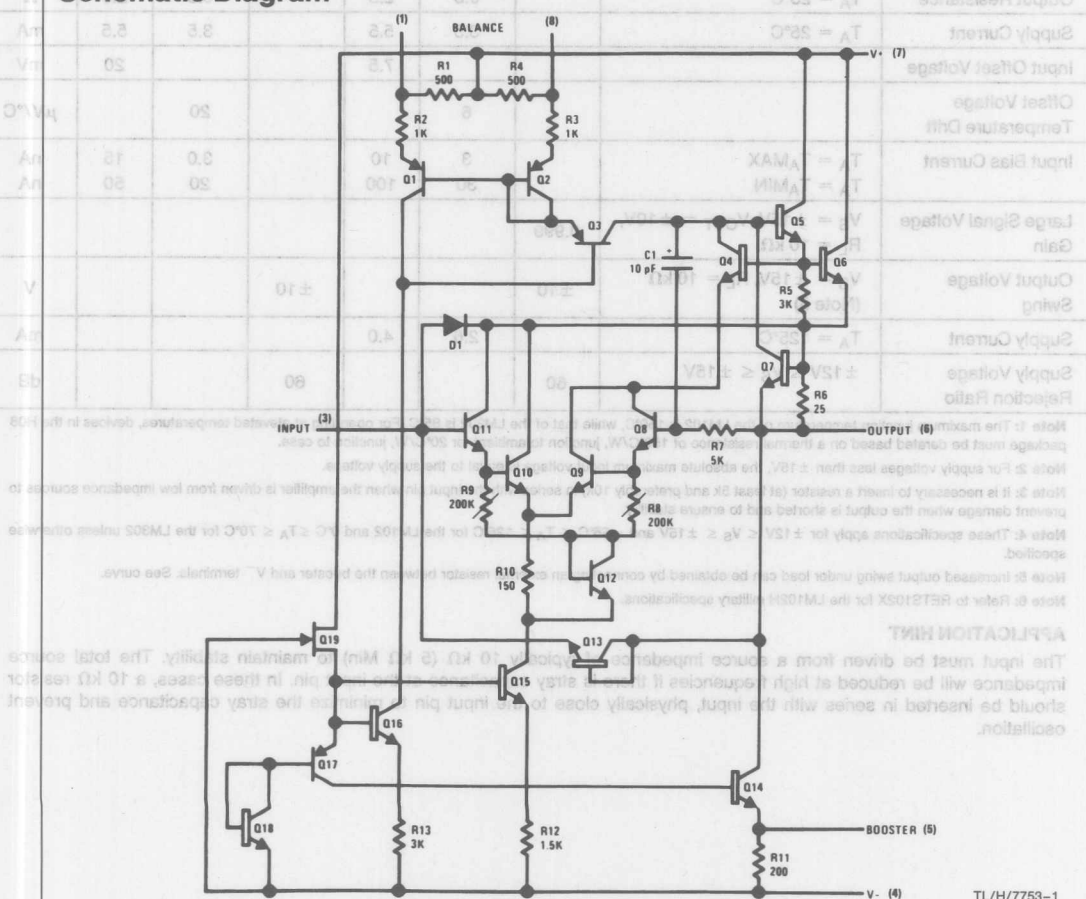
The LM102, which is designed to operate with supply voltages between $\pm 12V$ and $\pm 15V$, also features low input capacitance as well as excellent small signal and large signal frequency response—all of which minimize high fre-

quency gain error. Because of the low wiring capacitances inherent in monolithic construction, this fast operation can be realized without increasing power consumption.

Features

- Fast slewing — $10V/\mu s$
- Low input current — 10 nA (max)
- High input resistance — $10,000\text{ M}\Omega$
- No external frequency compensation required
- Simple offset balancing with optional $1\text{ k}\Omega$ potentiometer
- Plug-in replacement for both the LM101 and LM709 in voltage follower applications

Schematic Diagram



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

| | |
|--|------------------|
| Supply Voltage | $\pm 18\text{V}$ |
| Power Dissipation (Note 1) | 500 mW |
| Input Voltage (Note 2) | $\pm 15\text{V}$ |
| Output Short Circuit Duration (Note 3) | Indefinite |

| | |
|---|---|
| Operating Free Air Temperature Range | |
| LM102 | -55°C to $+125^{\circ}\text{C}$ |
| LM302 | 0°C to $+70^{\circ}\text{C}$ |
| Storage Temperature Range | |
| -65°C to $+150^{\circ}\text{C}$ | |
| Lead Temperature (Soldering, 10 sec.) | |
| 300°C | |
| ESD rating to be determined. | |

Electrical Characteristics (Note 4)

| Parameter | Conditions | LM102 | | | LM302 | | | Units |
|----------------------------------|--|-----------|-----------|-----|----------|-----------|-----|--------------------------------|
| | | Min | Typ | Max | Min | Type | Max | |
| Input Offset Voltage | $T_A = 25^{\circ}\text{C}$ | | 2 | 5 | | 5 | 15 | mV |
| Input Bias Current | $T_A = 25^{\circ}\text{C}$ | | 3 | 10 | | 10 | 30 | nA |
| Input Resistance | $T_A = 25^{\circ}\text{C}$ | 10^{10} | 10^{12} | | 10^9 | 10^{12} | | Ω |
| Input Capacitance | | | | 3.0 | | 3.0 | | pF |
| Large Signal Voltage Gain | $T_A = 25^{\circ}\text{C}$, $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$, $R_L = 8\text{ k}\Omega$ | 0.999 | 0.9996 | | 0.9985 | 0.9995 | 1.0 | V/V |
| Output Resistance | $T_A = 25^{\circ}\text{C}$ | | 0.8 | 2.5 | | 0.8 | 2.5 | Ω |
| Supply Current | $T_A = 25^{\circ}\text{C}$ | | 3.5 | 5.5 | | 3.5 | 5.5 | mA |
| Input Offset Voltage | | | | 7.5 | | | 20 | mV |
| Offset Voltage Temperature Drift | | | 6 | | | 20 | | $\mu\text{V}/^{\circ}\text{C}$ |
| Input Bias Current | $T_A = T_{A\text{MAX}}$ | | 3 | 10 | | 3.0 | 15 | nA |
| | $T_A = T_{A\text{MIN}}$ | | 30 | 100 | | 20 | 50 | nA |
| Large Signal Voltage Gain | $V_S = \pm 15\text{V}$, $V_{OUT} = \pm 10\text{V}$, $R_L = 10\text{ k}\Omega$ | 0.999 | | | | | | |
| Output Voltage Swing | $V_S = \pm 15\text{V}$, $R_L = 10\text{ k}\Omega$ (Note 5) | ± 10 | | | ± 10 | | | V |
| Supply Current | $T_A = 125^{\circ}\text{C}$ | | 2.6 | 4.0 | | | | mA |
| Supply Voltage Rejection Ratio | $\pm 12\text{V} \leq V_S \leq \pm 15\text{V}$ | 60 | | | 60 | | | dB |

Note 1: The maximum junction temperature of the LM102 is 150°C , while that of the LM302 is 85°C . For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of $150^{\circ}\text{C}/\text{W}$, junction to ambient, or $20^{\circ}\text{C}/\text{W}$, junction to case.

Note 2: For supply voltages less than $\pm 15\text{V}$, the absolute maximum input voltage is equal to the supply voltage.

Note 3: It is necessary to insert a resistor (at least $5\text{ k}\Omega$ and preferably $10\text{ k}\Omega$) in series with the input pin when the amplifier is driven from low impedance sources to prevent damage when the output is shorted and to ensure stability.

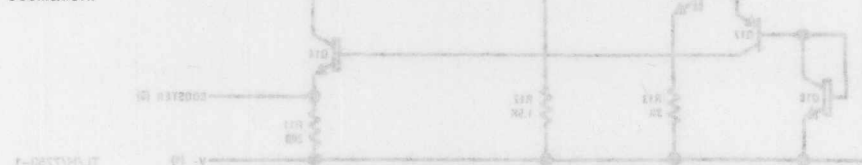
Note 4: These specifications apply for $\pm 12\text{V} \leq V_S \leq \pm 15\text{V}$ and $-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ for the LM102 and $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ for the LM302 unless otherwise specified.

Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

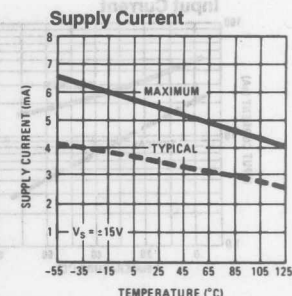
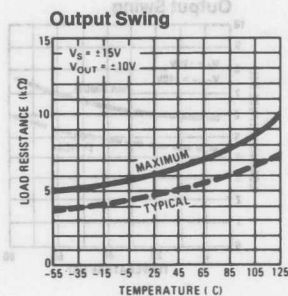
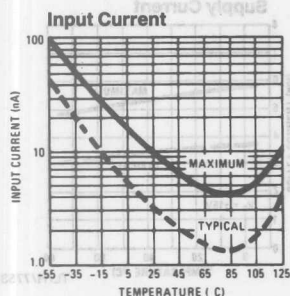
Note 6: Refer to RETS102X for the LM102H military specifications.

APPLICATION HINT

The input must be driven from a source impedance of typically $10\text{ k}\Omega$ ($5\text{ k}\Omega$ Min) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a $10\text{ k}\Omega$ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.

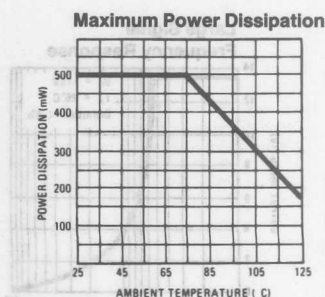
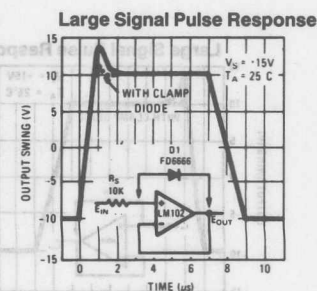
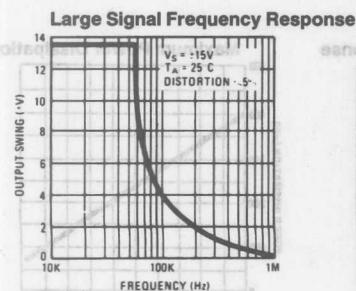
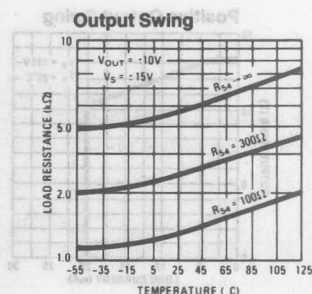
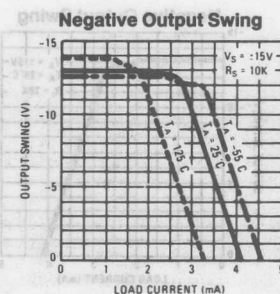
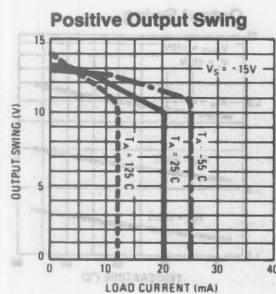
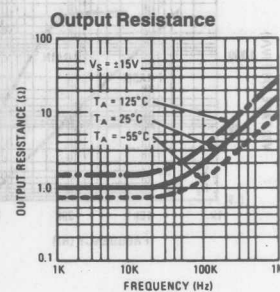
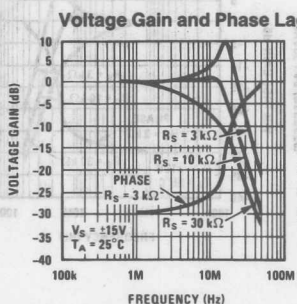
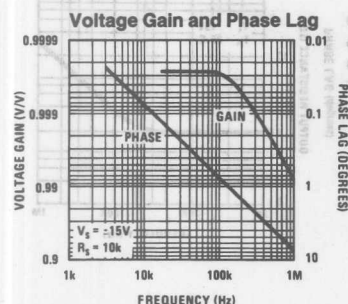


Guaranteed Performance Characteristics LM102

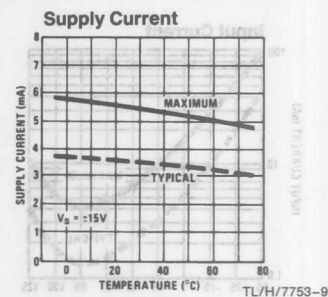
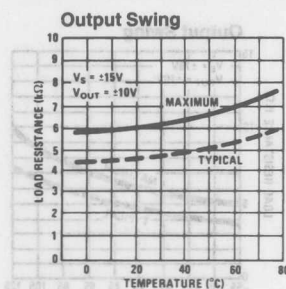
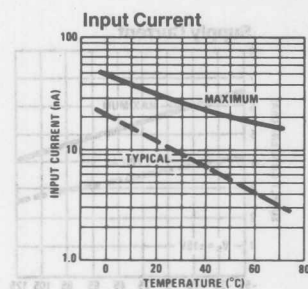


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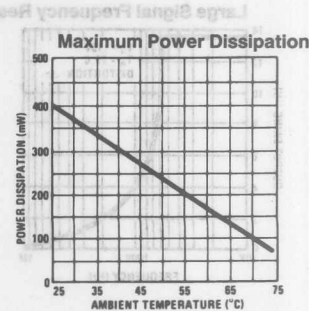
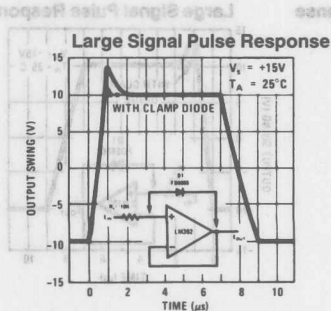
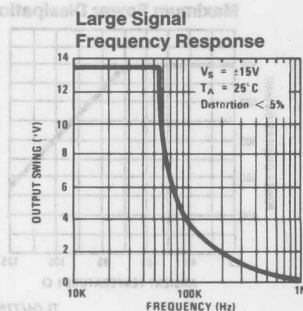
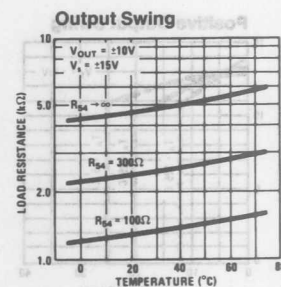
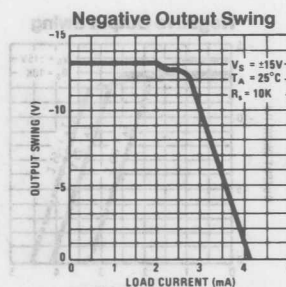
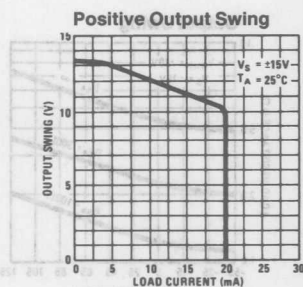
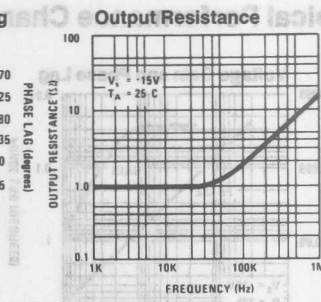
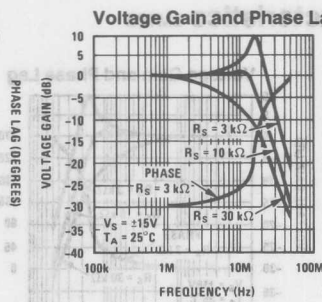
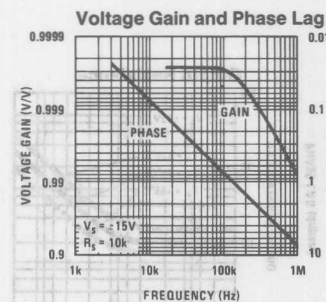
Typical Performance Characteristics LM102

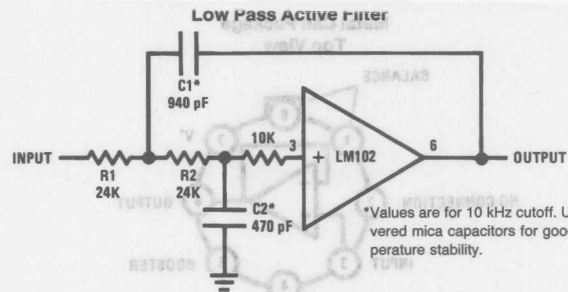


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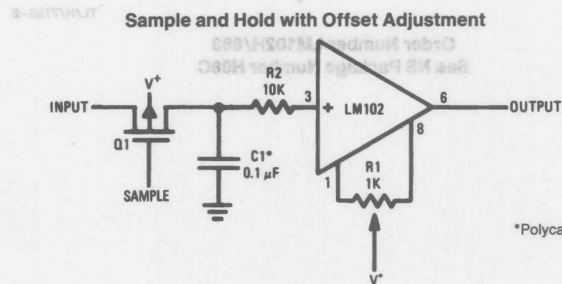


Typical Performance Characteristics LM302

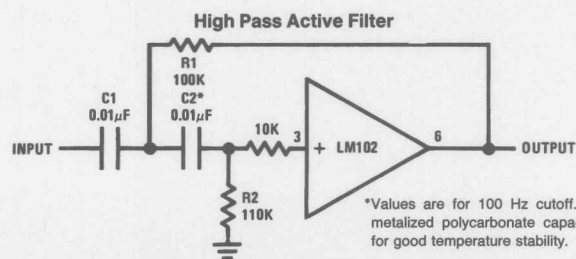




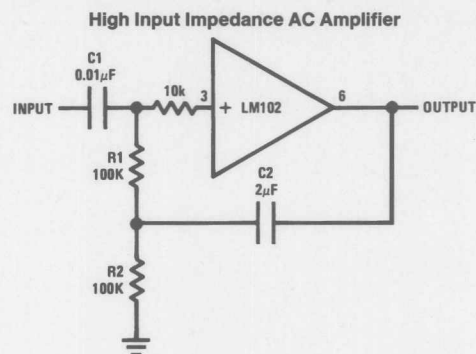
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TL/H/7753-4



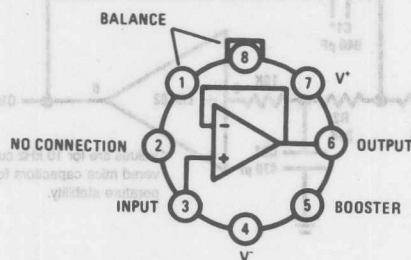
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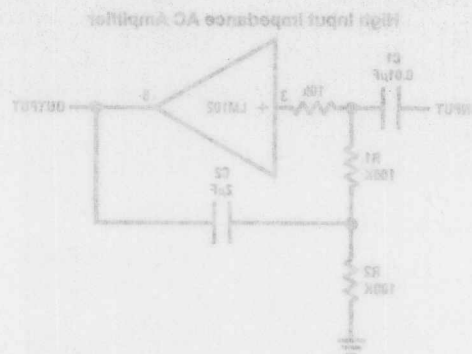
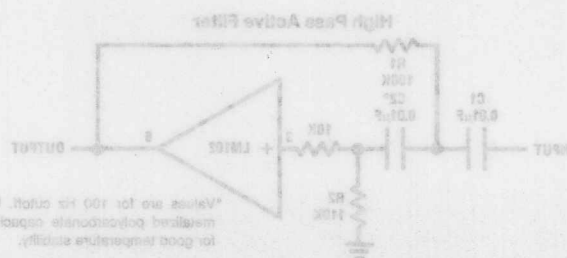
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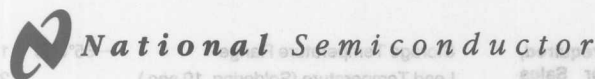
Connection Diagram

Metal Can Package
Top View



Order Number LM102H/883
See NS Package Number H08C





LM110/LM210/LM310 Voltage Follower

General Description

The LM110 series are monolithic operational amplifiers internally connected as unity-gain non-inverting amplifiers. They use super-gain transistors in the input stage to get low bias current without sacrificing speed. Directly interchangeable with 101, 741 and 709 in voltage follower applications, these devices have internal frequency compensation and provision for offset balancing.

The LM110 series are useful in fast sample and hold circuits, active filters, or as general-purpose buffers. Further, the frequency response is sufficiently better than standard IC amplifiers that the followers can be included in the feedback loop without introducing instability. They are plug-in replacements for the LM102 series voltage followers, offer-

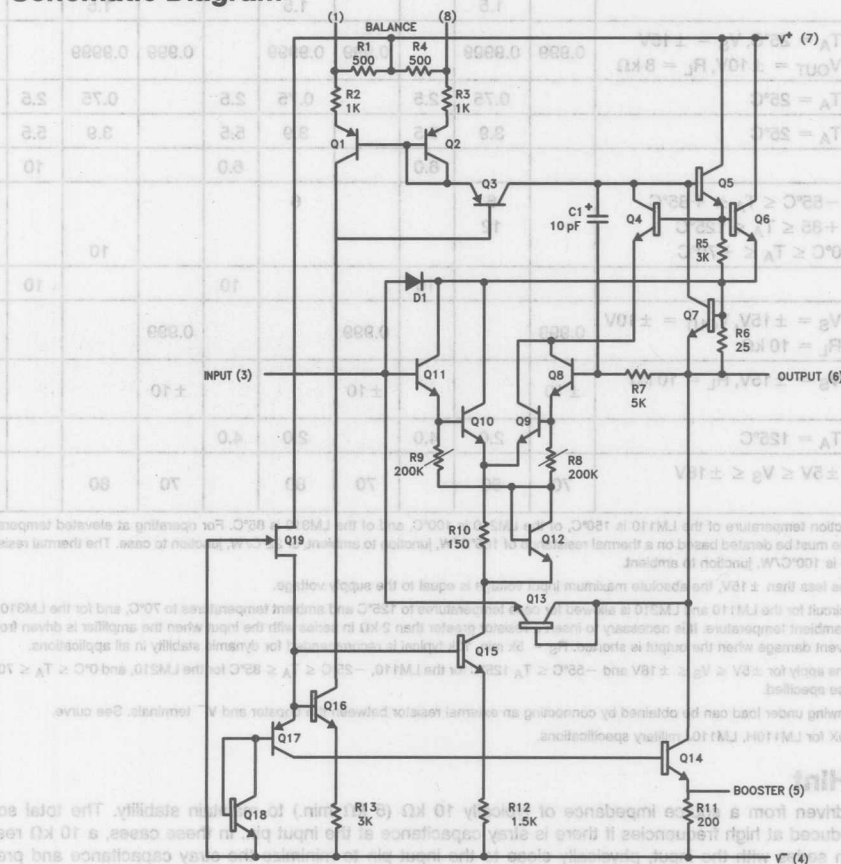
ing lower offset voltage, drift, bias current and noise in addition to higher speed and wider operating voltage range.

The LM110 is specified over a temperature range $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$, the LM210 from $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ and the LM310 from $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$.

Features

- Input current 10 nA max over temperature
- Small signal bandwidth 20 MHz
- Slew rate 30 V/ μs
- Supply voltage range $\pm 5\text{V}$ to $\pm 18\text{V}$

Schematic Diagram



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 6)

| | |
|--|-----------------------------------|
| Supply Voltage | $\pm 18V$ |
| Power Dissipation (Note 1) | 500 mW |
| Input Voltage (Note 2) | $\pm 15V$ |
| Output Short Circuit Duration (Note 3) | Indefinite |
| Operating Temperature Range | |
| LM110 | $-55^{\circ}C$ to $+125^{\circ}C$ |
| LM210 | $-25^{\circ}C$ to $+85^{\circ}C$ |
| LM310 | $0^{\circ}C$ to $+70^{\circ}C$ |

Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$

Lead Temperature (Soldering, 10 sec.) $260^{\circ}C$

Soldering Information

Dual-In-Line Package $260^{\circ}C$

Soldering (10 sec.)

Small Outline Package $215^{\circ}C$

Vapor Phase (60 sec.) $220^{\circ}C$

Infrared (15 sec.)

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating to be determined.

Electrical Characteristics (Note 4)

| Parameter | Conditions | LM110 | | | LM210 | | | LM310 | | | Units |
|----------------------------------|--|-----------|-----------|-----------|-----------|-----------|-----|-----------|-----------|-----|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $T_A = 25^{\circ}C$ | | 1.5 | 4.0 | | 1.5 | 4.0 | | 2.5 | 7.5 | mV |
| Input Bias Current | $T_A = 25^{\circ}C$ | | 1.0 | 3.0 | | 1.0 | 3.0 | | 2.0 | 7.0 | nA |
| Input Resistance | $T_A = 25^{\circ}C$ | 10^{10} | 10^{12} | | 10^{10} | 10^{12} | | 10^{10} | 10^{12} | | Ω |
| Input Capacitance | | | 1.5 | | | 1.5 | | | 1.5 | | pF |
| Large Signal Voltage Gain | $T_A = 25^{\circ}C, V_S = \pm 15V$ $V_{OUT} = \pm 10V, R_L = 8 k\Omega$ | 0.999 | 0.9999 | | 0.999 | 0.9999 | | 0.999 | 0.9999 | | V/V |
| Output Resistance | $T_A = 25^{\circ}C$ | | 0.75 | 2.5 | | 0.75 | 2.5 | | 0.75 | 2.5 | Ω |
| Supply Current | $T_A = 25^{\circ}C$ | | 3.9 | 5.5 | | 3.9 | 5.5 | | 3.9 | 5.5 | mA |
| Input Offset Voltage | | | | 6.0 | | | 6.0 | | | 10 | mV |
| Offset Voltage Temperature Drift | $-55^{\circ}C \leq T_A \leq +85^{\circ}C$ $+85 \leq T_A \leq 125^{\circ}C$ $0^{\circ}C \leq T_A \leq +70^{\circ}C$ | | 6 12 | | | 6 | | | 10 | | $\mu V/^{\circ}C$ $\mu V/^{\circ}C$ $\mu V/^{\circ}C$ |
| Input Bias Current | | | | 10^{-6} | | | 10 | | | 10 | nA |
| Large Signal Voltage Gain | $V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L = 10 k\Omega$ | 0.999 | | | 0.999 | | | 0.999 | | | V/V |
| Output Voltage Swing (Note 5) | $V_S = \pm 15V, R_L = 10 k\Omega$ | ± 10 | | | ± 10 | | | ± 10 | | | V |
| Supply Current | $T_A = 125^{\circ}C$ | | 2.0 | 4.0 | | 2.0 | 4.0 | | | | mA |
| Supply Voltage Rejection Ratio | $\pm 5V \leq V_S \leq \pm 18V$ | 70 | 80 | | 70 | 80 | | 70 | 80 | | dB |

Note 1: The maximum junction temperature of the LM110 is $150^{\circ}C$, of the LM210 is $100^{\circ}C$, and of the LM310 is $85^{\circ}C$. For operating at elevated temperatures, devices in the HO8 package must be derated based on a thermal resistance of $165^{\circ}C/W$, junction to ambient, or $22^{\circ}C/W$, junction to case. The thermal resistance of the dual-in-line package is $100^{\circ}C/W$, junction to ambient.

Note 2: For supply voltages less than $\pm 15V$, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit for the LM110 and LM210 is allowed for case temperatures to $125^{\circ}C$ and ambient temperatures to $70^{\circ}C$, and for the LM310, $70^{\circ}C$ case temperature or $55^{\circ}C$ ambient temperature. It is necessary to insert a resistor greater than $2 k\Omega$ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted. $R_S = 5k \Omega$ min, $10k \Omega$ typical is recommended for dynamic stability in all applications.

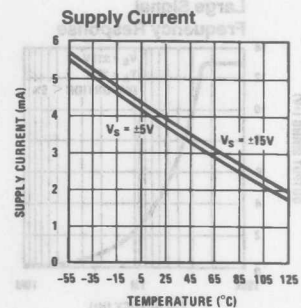
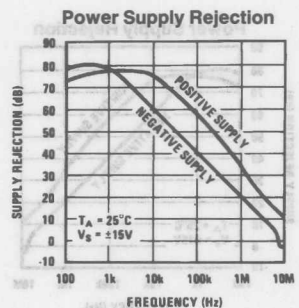
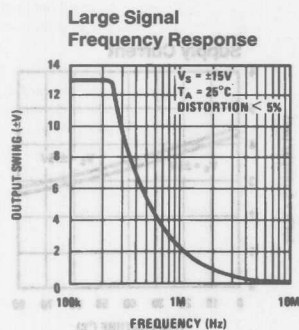
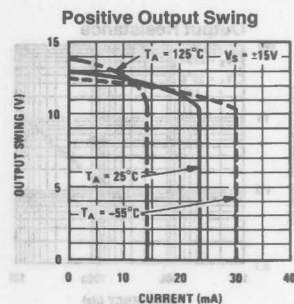
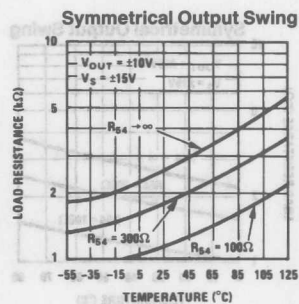
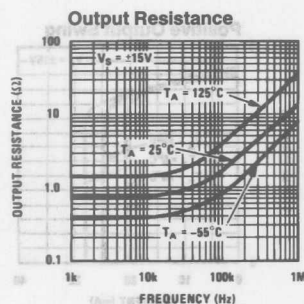
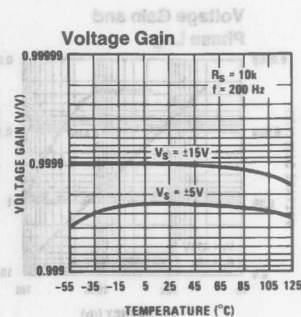
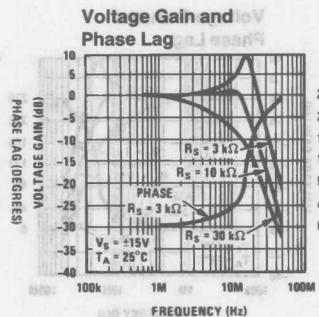
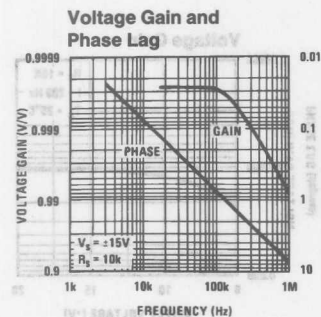
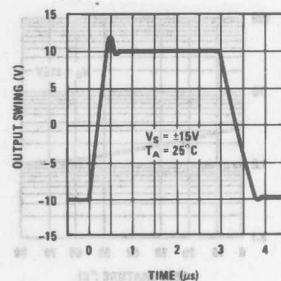
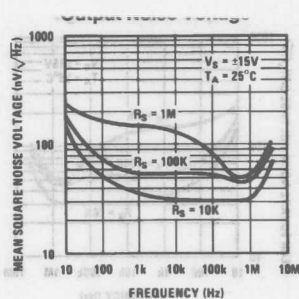
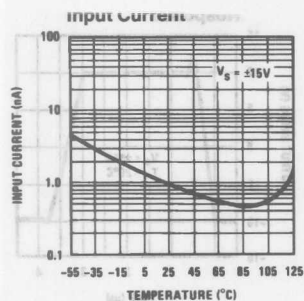
Note 4: These specifications apply for $\pm 5V \leq V_S \leq \pm 18V$ and $-55^{\circ}C \leq T_A \leq 125^{\circ}C$ for the LM110, $-25^{\circ}C \leq T_A \leq 85^{\circ}C$ for the LM210, and $0^{\circ}C \leq T_A \leq 70^{\circ}C$ for the LM310 unless otherwise specified.

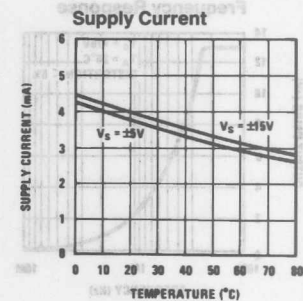
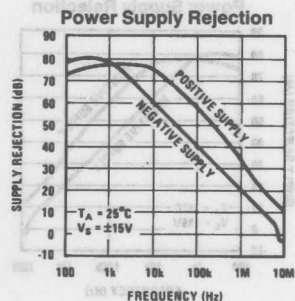
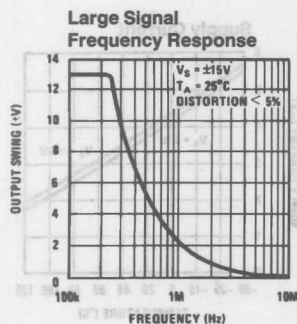
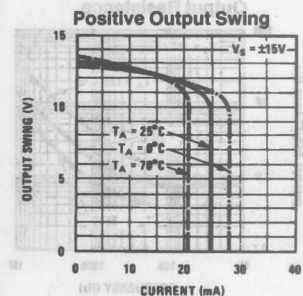
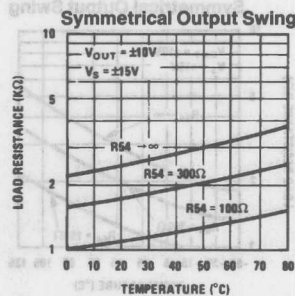
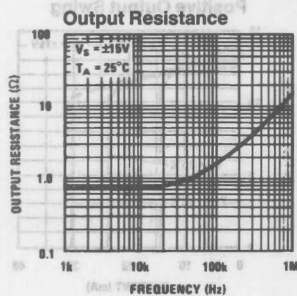
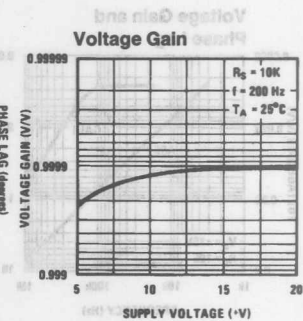
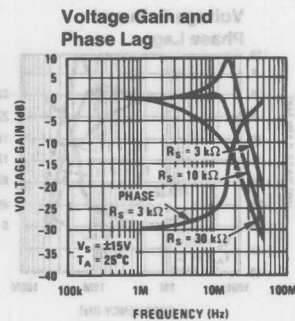
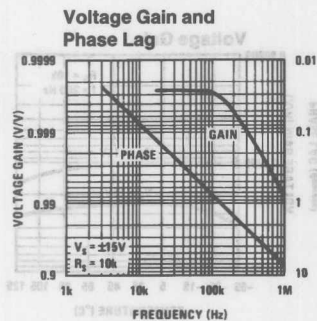
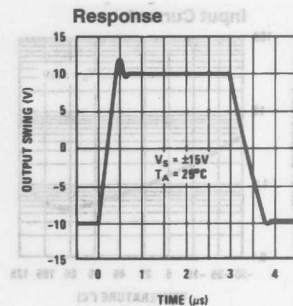
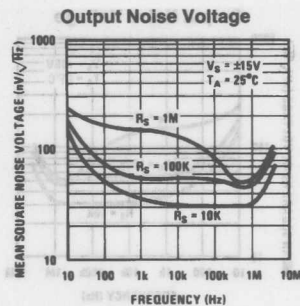
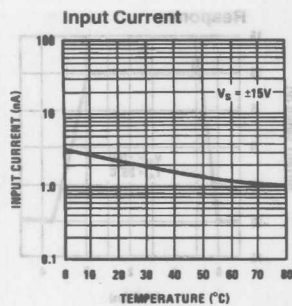
Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

Note 6: Refer to RETS110X for LM110H, LM110J military specifications.

Application Hint

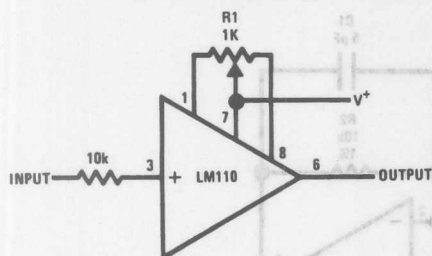
The input must be driven from a source impedance of typically $10 k\Omega$ ($5 k\Omega$ min.) to maintain stability. The total source impedance will be reduced at high frequencies if there is stray capacitance at the input pin. In these cases, a $10 k\Omega$ resistor should be inserted in series with the input, physically close to the input pin to minimize the stray capacitance and prevent oscillation.





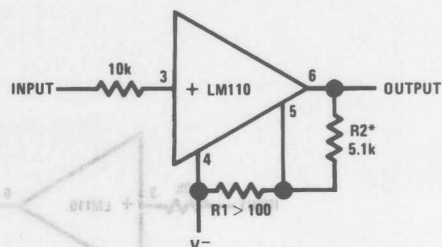
Auxiliary Circuits

Offset Balancing Circuit



TL/H/7761-2

Increasing Negative Swing Under Load

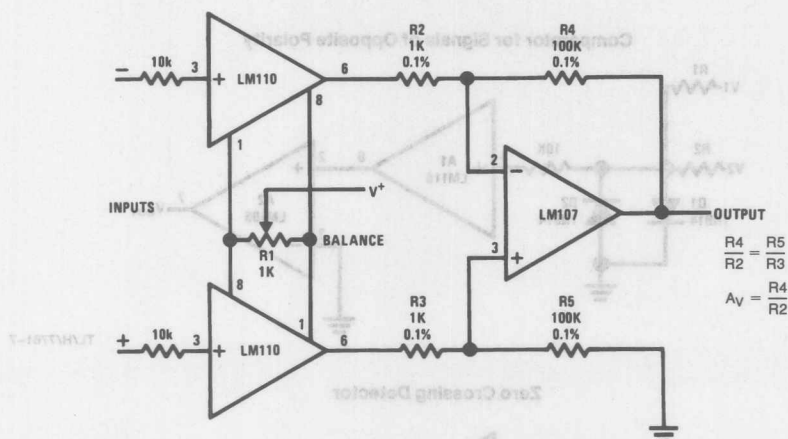


TL/H/7761-3

*May be added to reduce internal dissipation

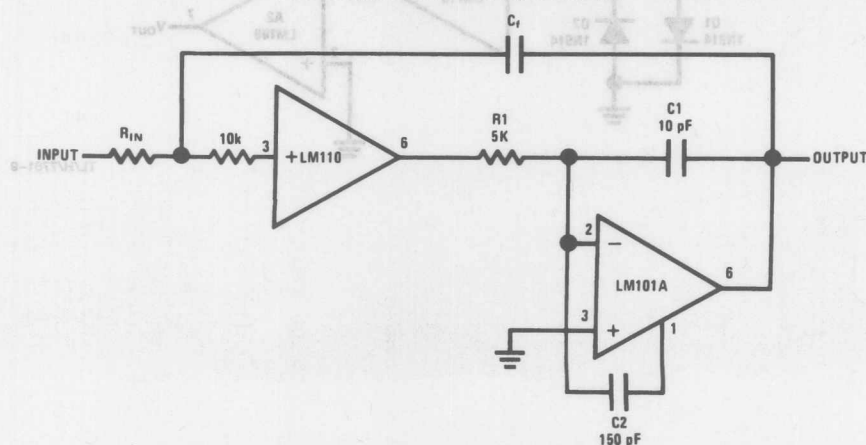
Typical Applications

Differential Input Instrumentation Amplifier



TL/H/7761-4

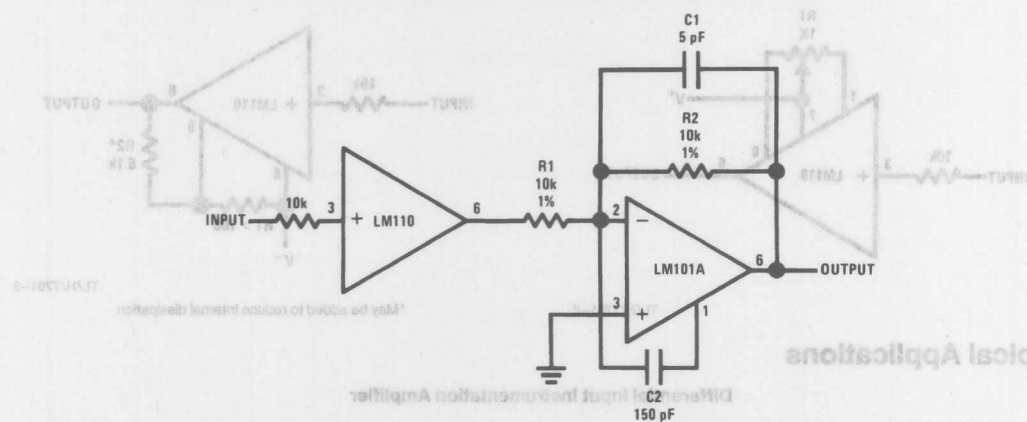
Fast Integrator with Low Input Current



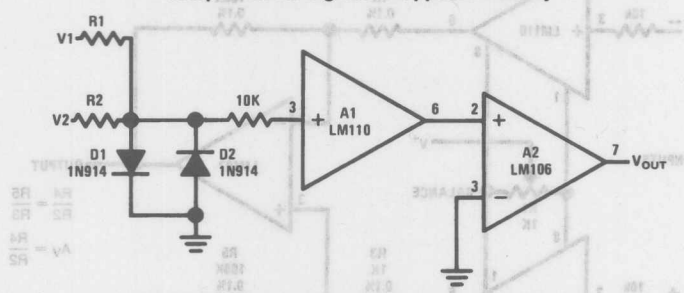
TL/H/7761-5

Typical Applications (Continued)

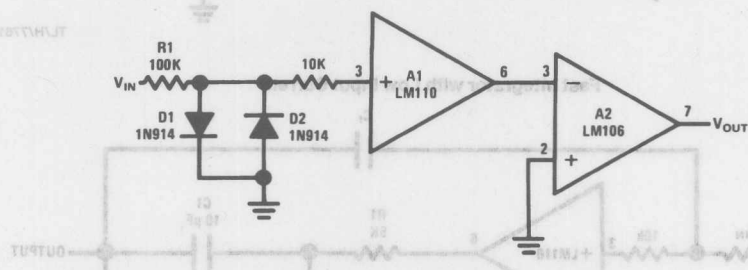
Fast Inverting Amplifier with High Input Impedance



Comparator for Signals of Opposite Polarity

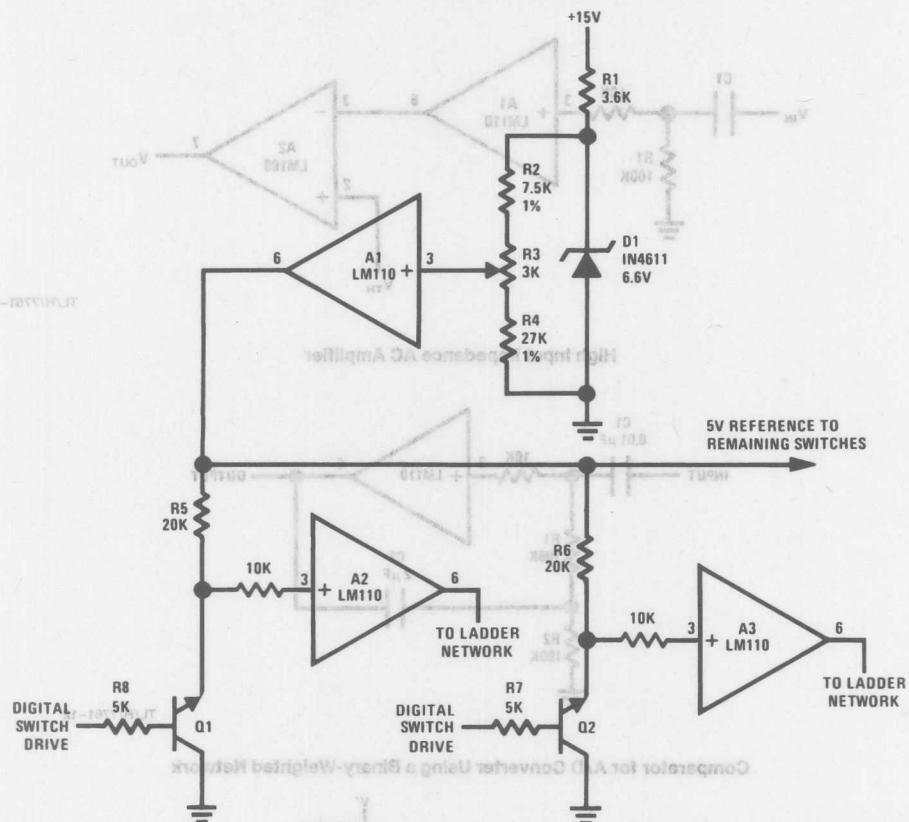


Zero Crossing Detector



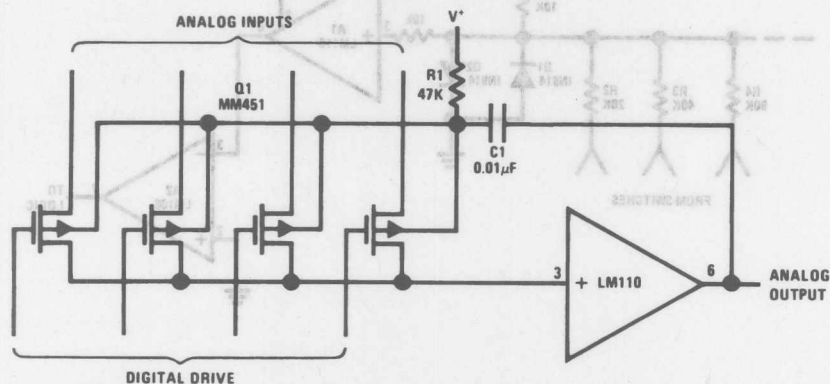
Typical Applications (Continued)

Driver for A/D Ladder Network



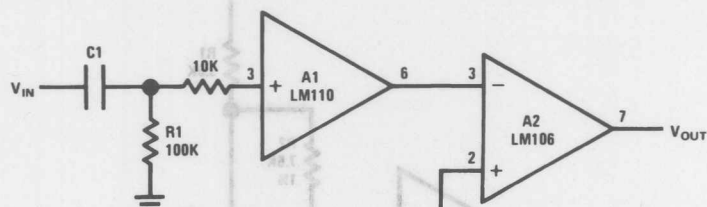
TL/H/7761-8

Buffer for Analog Switch*



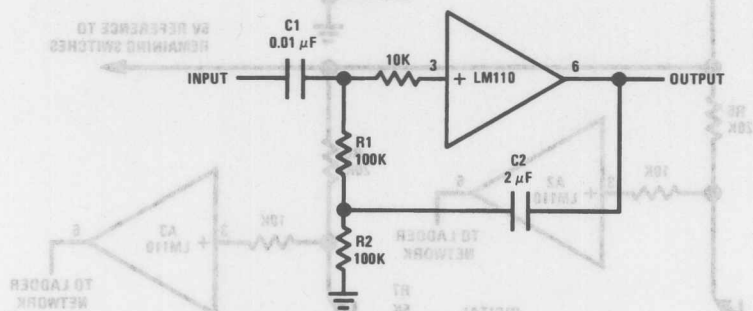
*Switch substrates are boot-strapped to reduce output capacitance of switch.

TL/H/7761-10



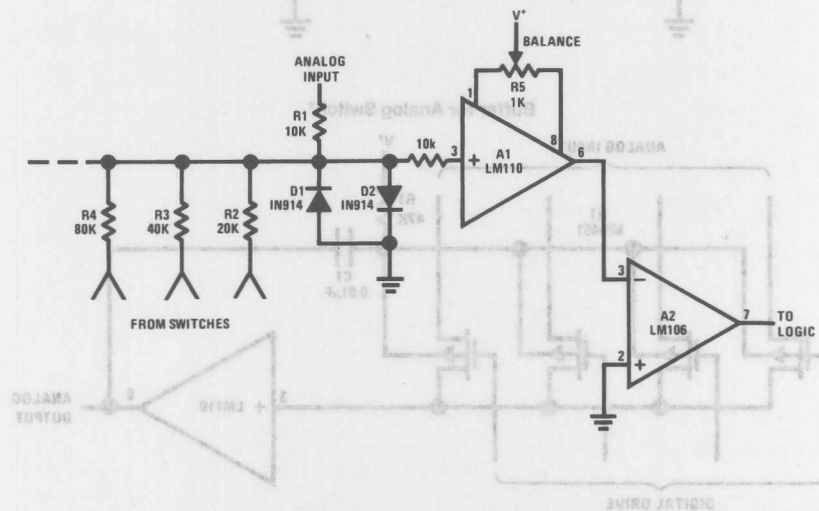
TL/H/7761-11

High Input Impedance AC Amplifier

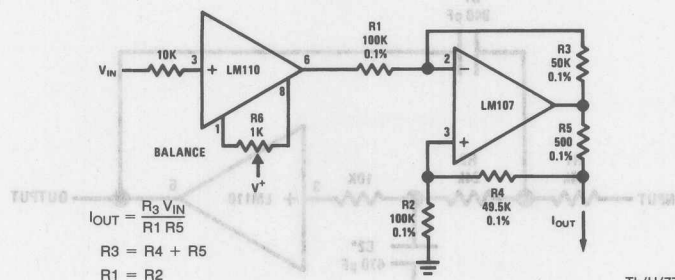


TL/H/7761-12

Comparator for A/D Converter Using a Binary-Weighted Network

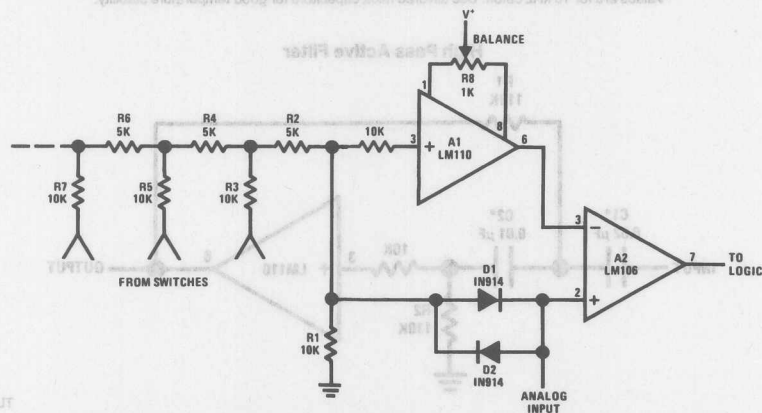


TL/H/7761-13



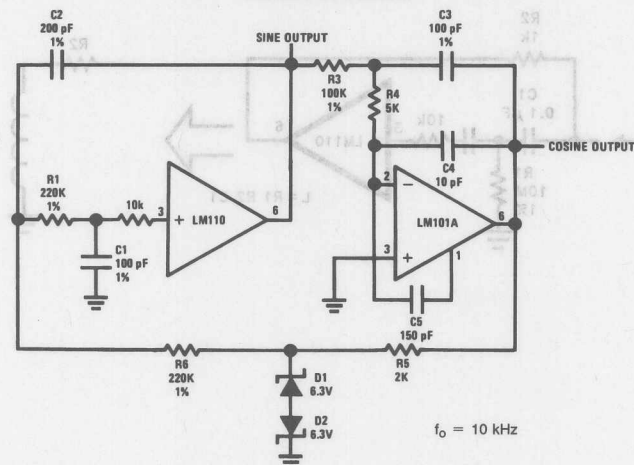
TL/H/7761-14

Comparator for A/D Converter Using a Ladder Network



TL/H/7761-15

Sine Wave Oscillator

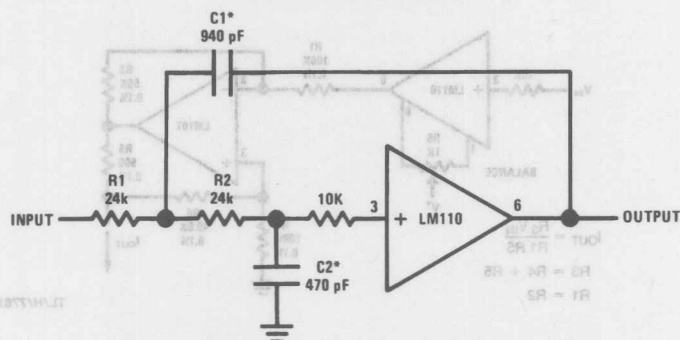


TL/H/7761-16

Typical Applications (Continued)

Typical Applications (Continued)

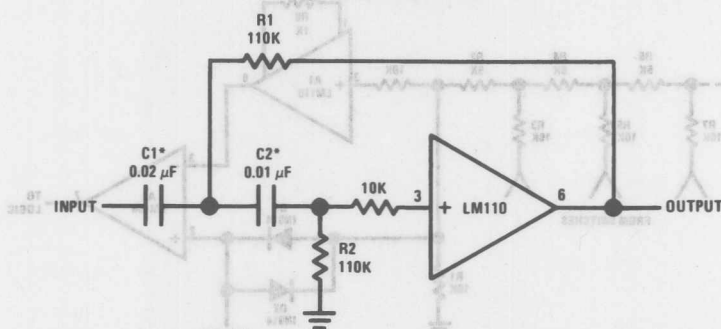
Low Pass Active Filter



*Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

TL/H/7761-18

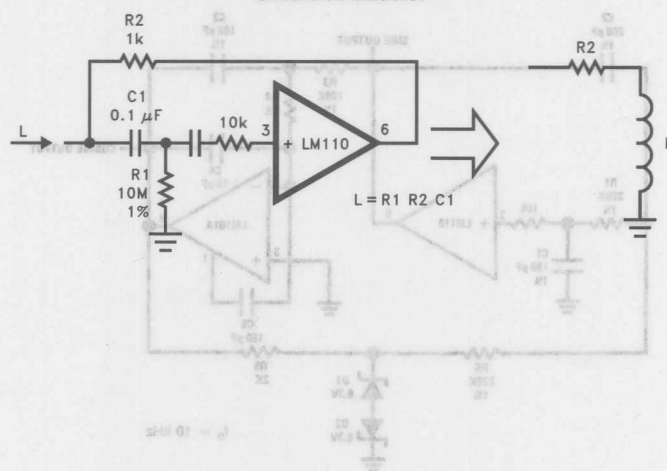
High Pass Active Filter



*Values are for 100 Hz cutoff. Use metalized polycarbonate capacitors for good temperature stability.

TL/H/7761-19

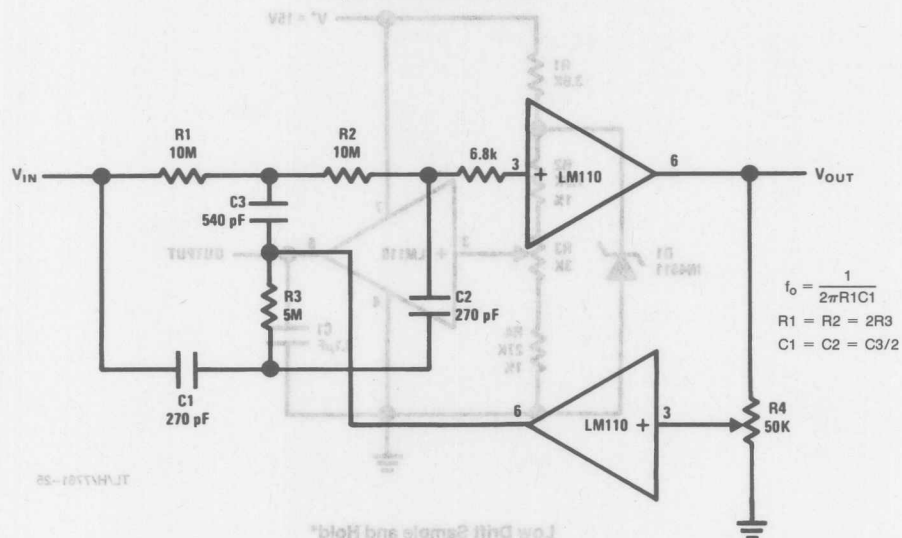
Simulated Inductor



TL/H/7761-21

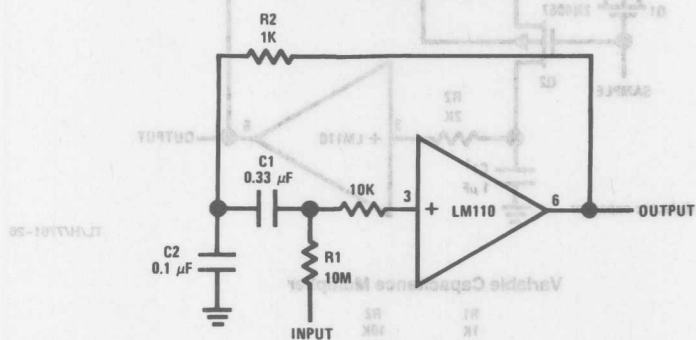
Typical Applications (Continued)

Adjustable Q Notch Filter



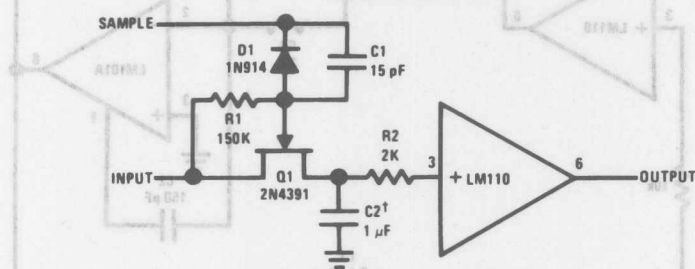
TL/H/7761-22

Bandpass Filter



TL/H/7761-23

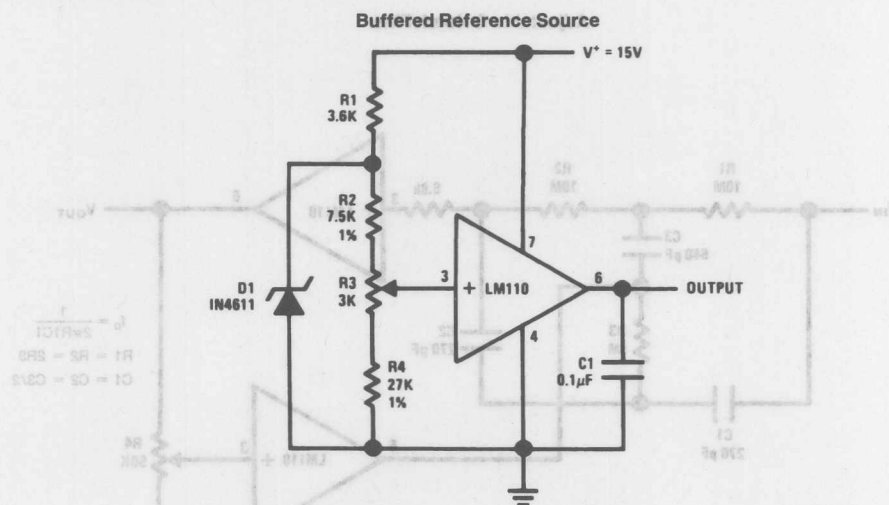
Sample and Hold



TL/H/7761-24

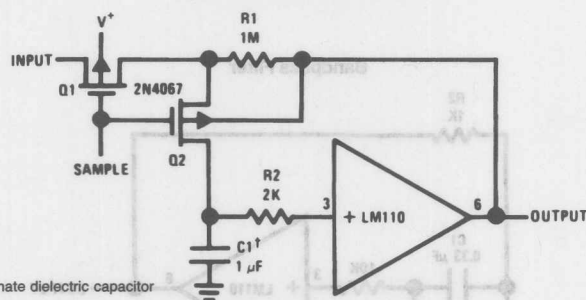
†Use capacitor with polycarbonate teflon or polyethylene dietic

Typical Applications (Continued)



TL/H/7761-25

Low Drift Sample and Hold*

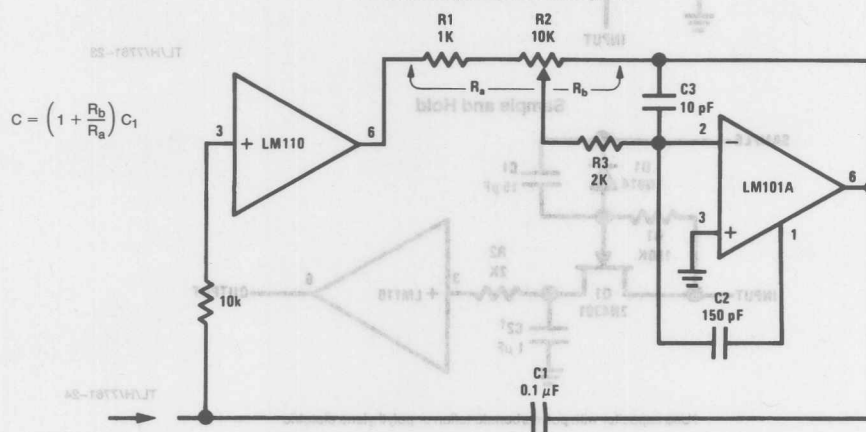


†Teflon polyethylene or polycarbonate dielectric capacitor

*Worst case drift less than 3 mV/sec

TL/H/7761-26

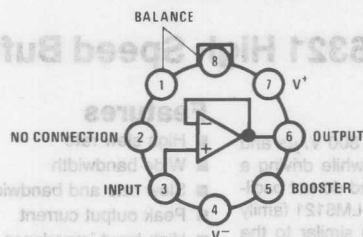
Variable Capacitance Multiplier



TL/H/7761-27

Connection Diagrams

Metal Can Package



Package is connected to Pin 4 (V^-)

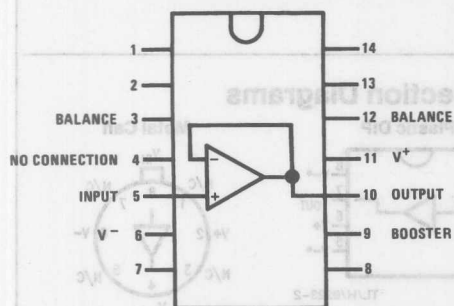
Top View

Order Number LM110H, LM210H or LM310H

LM110H/883*

See NS Package Number H08C

Dual-In-Line Package



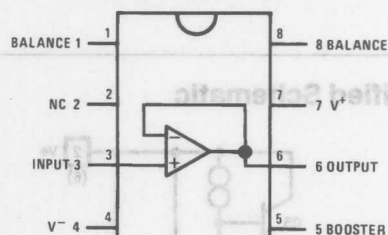
Top View

Order Number LM110J, LM210J,

LM310J or LM110J/883*

See NS Package Number J14A

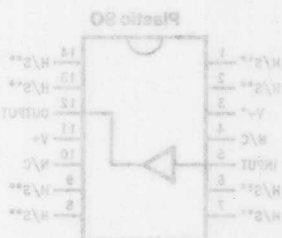
Dual-In-Line Package



Top View

Order Number LM310M, LM310N or LM110J-8/883*

See NS Package Number J08A, M08A or N08E



*Available per SMD # 5962-8760601

LM6121/LM6221/LM6321 High Speed Buffer

General Description

These high speed unity gain buffers slew at $800 \text{ V}/\mu\text{s}$ and have a small signal bandwidth of 50 MHz while driving a 50Ω load. They can drive $\pm 300 \text{ mA}$ peak and do not oscillate while driving large capacitive loads. The LM6121 family are monolithic ICs which offer performance similar to the LH0002 with the additional features of current limit and thermal shutdown.

These buffers are built with National's VIPTM (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

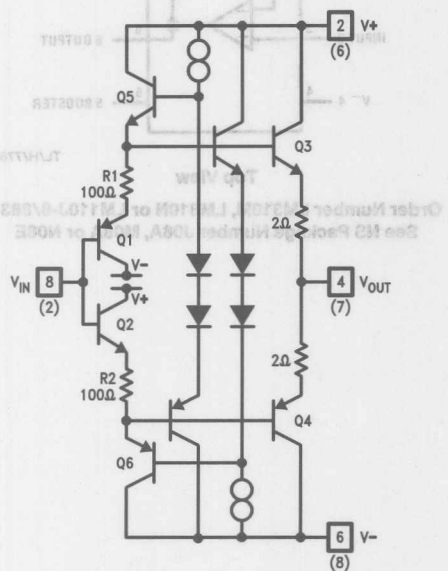
Features

- High slew rate $800 \text{ V}/\mu\text{s}$
- Wide bandwidth 50 MHz
- Slew rate and bandwidth 100% tested
- Peak output current $\pm 300 \text{ mA}$
- High input impedance $5 \text{ M}\Omega$
- LH0002H pin compatible
- No oscillations with capacitive loads
- 5V to $\pm 15\text{V}$ operation guaranteed
- Current and thermal limiting
- Fully specified to drive 50Ω lines

Applications

- Line Driving
- Radar
- Sonar

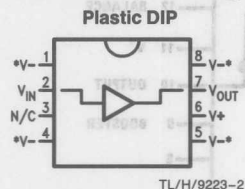
Simplified Schematic



Numbers in () are for 8-pin N DIP.

TL/H/9223-1

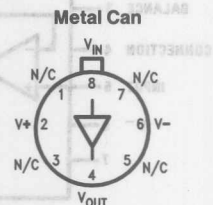
Connection Diagrams



TL/H/9223-2

*Heat-sinking pins. See Application section on heat sinking requirements.

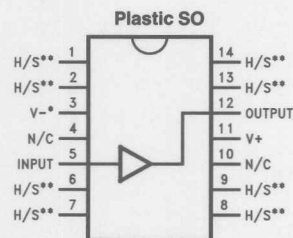
Order Number LM6221N,
LM6321N or LM6121J/883
See NS Package
Number J08A or N08E



TL/H/9223-3

Top View

Note: Pin 6 connected to case.
Order Number LM6221H or
LM6121H/883
See NS Package
Number H08C



TL/H/9223-7

*Pin 3 must be connected to the negative supply.

**Heat-sinking pins. See Application section on heat-sinking requirements. These pins are at V^- potential.

Order Number LM6321M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|---|
| Supply Voltage | 36V (± 18) |
| Input to Output Voltage (Note 2) | $\pm 7V$ |
| Input Voltage | $\pm V_{supply}$ |
| Output Short-Circuit to GND (Note 3) | Continuous |
| Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ |
| Lead Temperature (Soldering, 10 seconds) | 260°C |
| Power Dissipation | (Note 10) |

ESD Tolerance (Note 8)

 $\pm 2000V$ Junction Temperature ($T_{J(max)}$) 150°C **Operating Ratings**

Operating Temperature Range

LM6121H/883

 -55°C to $+125^{\circ}\text{C}$

LM6221

 -40°C to $+85^{\circ}\text{C}$

LM6321

 0°C to $+70^{\circ}\text{C}$

Operating Supply Range

 4.75 to $\pm 16V$ Thermal Resistance (θ_{JA}), (Note 4)

H Package

 150°C/W

N Package

 47°C/W

M Package

 69°C/W Thermal Resistance (θ_{JC}), H Package 17°C/W **DC Electrical Characteristics**

The following specifications apply for Supply Voltage = $\pm 15V$, $V_{CM} = 0$, $R_L \geq 100\text{ k}\Omega$ and $R_S = 50\Omega$ unless otherwise noted.

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Typ | LM6121 | LM6221 | LM6321 | Units |
|----------|------------------------------|---|-------|-----------------------|-----------------------|-----------------------|----------------------|
| | | | | Limit (Notes 5, 9) | Limit (Note 5) | Limit (Note 5) | |
| A_{V1} | Voltage Gain 1 | $R_L = 1\text{ k}\Omega$, $V_{IN} = \pm 10V$ | 0.990 | 0.980 0.970 | 0.980 0.950 | 0.970 0.950 | V/V Min |
| A_{V2} | Voltage Gain 2 | $R_L = 50\Omega$, $V_{IN} = \pm 10V$ | 0.900 | 0.860 0.800 | 0.860 0.820 | 0.850 0.820 | |
| A_{V3} | Voltage Gain 3 (Note 6) | $R_L = 50\Omega$, $V^+ = 5V$ $V_{IN} = 2 V_{pp}$ ($1.5 V_{pp}$) | 0.840 | 0.780 0.750 | 0.780 0.700 | 0.750 0.700 | |
| V_{OS} | Offset Voltage | $R_L = 1\text{ k}\Omega$ | 15 | 30 50 | 30 60 | 50 100 | mV Max |
| I_B | Input Bias Current | $R_L = 1\text{ k}\Omega$, $R_S = 10\text{ k}\Omega$ | 1 | 4 7 | 4 7 | 5 7 | μA Max |
| R_{IN} | Input Resistance | $R_L = 50\Omega$ | 5 | | | | M Ω |
| C_{IN} | Input Capacitance | | 3.5 | | | | pF |
| R_{O1} | Output Resistance | $I_{OUT} = \pm 10\text{ mA}$ | 3 | 5 10 | 5 10 | 5 6 | Ω Max |
| I_{S1} | Supply Current 1 | $R_L = \infty$ | 15 | 18 20 | 18 20 | 20 22 | mA Max |
| I_{S2} | Supply Current 2 | $R_L = \infty$, $V^+ = 5V$ | 14 | 16 18 | 16 18 | 18 20 | |
| V_{O1} | Output Swing 1 | $R_L = 1\text{ k}$ | 13.5 | 13.3 13 | 13.3 13 | 13.2 13 | $\pm V$ Min |
| V_{O2} | Output Swing 2 | $R_L = 100\Omega$ | 12.7 | 11.5 10 | 11.5 10 | 11 10 | |
| V_{O3} | Output Swing 3 | $R_L = 50\Omega$ | 12 | 11 9 | 11 9 | 10 9 | |
| V_{O4} | Output Swing 4 | $R_L = 50\Omega$, $V^+ = 5V$ (Note 6) | 1.8 | 1.6 1.3 | 1.6 1.4 | 1.6 1.5 | V_{pp} Min |
| PSSR | Power Supply Rejection Ratio | $V^{\pm} = \pm 5V$ to $\pm 15V$ | 70 | 60 55 | 60 50 | 60 50 | dB Min |

AC Electrical Characteristics

The following specifications apply for Supply Voltage = $\pm 15\text{V}$, $V_{\text{CM}} = 0$, $R_{\text{L}} \geq 100\text{ k}\Omega$ and $R_{\text{S}} = 50\Omega$ unless otherwise noted.

Boldface limits apply for $T_{\text{A}} = T_{\text{J}} = T_{\text{MIN}}$ to T_{MAX} ; all other limits $T_{\text{A}} = T_{\text{J}} = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Typ | LM6121 | LM6221 | LM6321 | Units |
|---------------------------------|---------------------------|---|------|-------------------|-------------------|-------------------|-------------------------|
| | | | | Limit (Note 5) | Limit (Note 5) | Limit (Note 5) | |
| SR ₁ | Slew Rate 1 | $V_{\text{IN}} = \pm 11\text{V}$, $R_{\text{L}} = 1\text{ k}\Omega$ | 1200 | 550 | 550 | 550 | V/ μs Min |
| SR ₂ | Slew Rate 2 | $V_{\text{IN}} = \pm 11\text{V}$, $R_{\text{L}} = 50\Omega$ (Note 7) | 800 | 550 | 550 | 550 | |
| SR ₃ | Slew Rate 3 | $V_{\text{IN}} = 2\text{ V}_{\text{PP}}$, $R_{\text{L}} = 50\Omega$ $V_{+} = 5\text{V}$ (Note 6) | 50 | 550 | 550 | 550 | |
| BW | -3 dB Bandwidth | $V_{\text{IN}} = \pm 100\text{ mV}_{\text{PP}}$, $R_{\text{L}} = 50\Omega$ $C_{\text{L}} \leq 10\text{ pF}$ | 50 | 30 | 30 | 30 | MHz Min |
| t_{r} , t_{f} | Rise Time Fall Time | $R_{\text{L}} = 50\Omega$, $C_{\text{L}} \leq 10\text{ pF}$ $V_{\text{O}} = 100\text{ mV}_{\text{PP}}$ | 7.0 | | | | ns |
| t_{pd} | Propagation Delay Time | $R_{\text{L}} = 50\Omega$, $C_{\text{L}} \leq 10\text{ pF}$ $V_{\text{O}} = 100\text{ mV}_{\text{PP}}$ | 4.0 | | | | ns |
| OS | Overshoot | $R_{\text{L}} = 50\Omega$, $C_{\text{L}} \leq 10\text{ pF}$ $V_{\text{O}} = 100\text{ mV}_{\text{PP}}$ | 10 | | | | % |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit or thermal limit, the input current will increase if the input to output differential voltage exceeds 8V. For input to output differential voltages in excess of 8V the input current should be limited to $\pm 20\text{ mA}$.

Note 3: The LM6121 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: The thermal resistance θ_{JA} of the device in the N package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 4, 5 and 8) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal resistance θ_{JA} of the N package is 84°C/W . The thermal resistance θ_{JA} of the device in the M package is measured when soldered directly to a printed circuit board, and the heat-sinking pins (pins 1, 2, 6, 7, 8, 9, 13, 14) are connected to 1 square inch of 2 oz. copper.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to 2.5V and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_y3 test at -55°C where it is reduced to 1.5 V_{PP} .

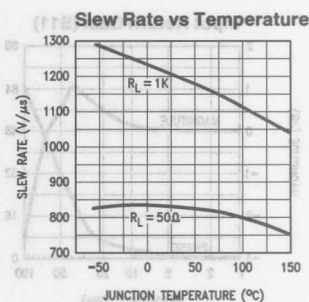
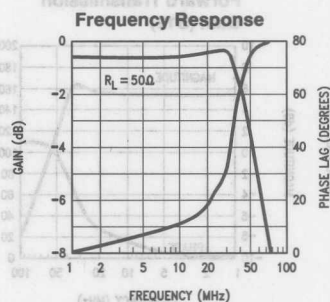
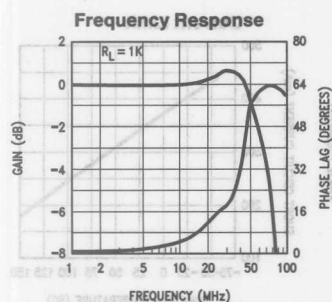
Note 7: Slew rate is measured with a $\pm 11\text{V}$ input pulse and 50 Ω source impedance at 25°C . Since voltage gain is typically 0.9 driving a 50 Ω load, the output swing will be approximately $\pm 10\text{V}$. Slew rate is calculated for transitions between $\pm 5\text{V}$ levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to $\pm 10\text{V}$ for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/ μs .

Note 8: The test circuit consists of the human body model of 120 pF in series with 1500 Ω .

Note 9: For specification limits over the full Military Temperature Range, see RETS6121X.

Note 10: The maximum power dissipation is a function of $T_{\text{J(max)}}$, θ_{JA} , and T_{A} . The maximum allowable power dissipation at any ambient temperature is $P_{\text{D}} = (T_{\text{J(max)}} - T_{\text{A}}) / \theta_{\text{JA}}$.

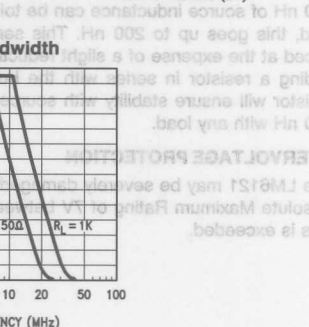
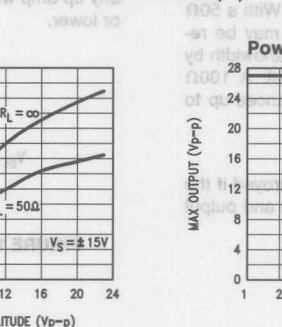
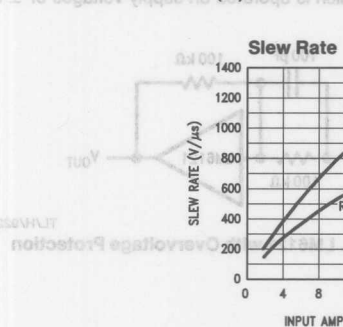
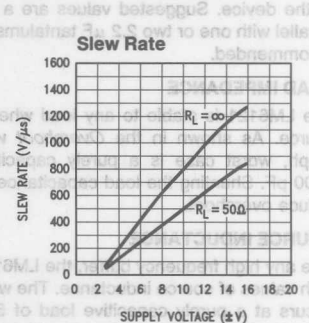
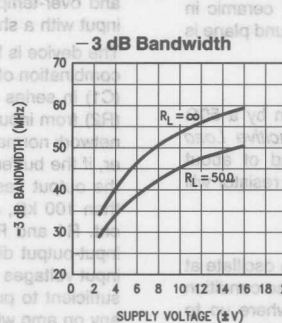
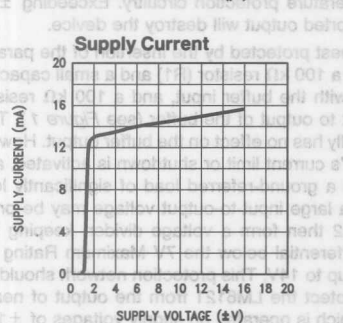
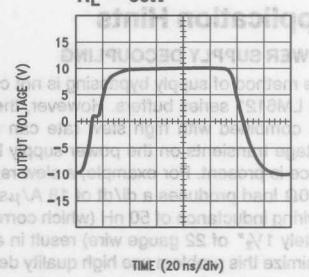
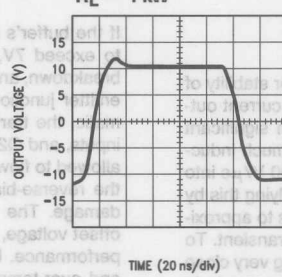
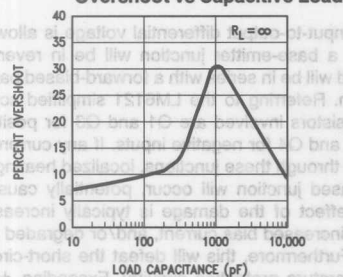
Typical Performance Characteristics, $T_J = 25^\circ\text{C}$, unless otherwise specified



Frequency Response

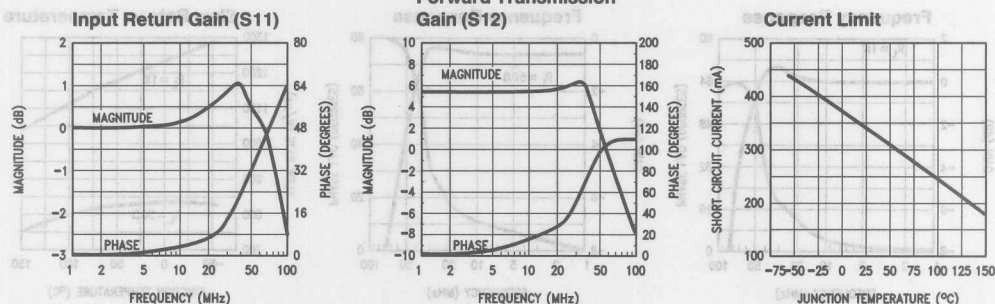
Frequency Response

Slew Rate vs Temperature



TL/H/9223-4

Typical Performance Characteristics $T_J = 25^\circ\text{C}$, unless otherwise specified (Continued)



TL/H/9223-5

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6121 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of $900\text{ V}/\mu\text{s}$ into a 50Ω load produces a di/dt of $18\text{ A}/\mu\text{s}$. Multiplying this by a wiring inductance of 50 nH (which corresponds to approximately $1\frac{1}{2}$ " of 22 gauge wire) result in a 0.9V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a $0.1\text{ }\mu\text{F}$ ceramic in parallel with one or two $2.2\text{ }\mu\text{F}$ tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6121 is stable to any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF . Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

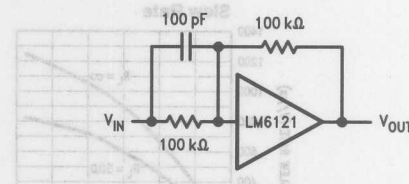
Like any high frequency buffer, the LM6121 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH . This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

OVERVOLTAGE PROTECTION

The LM6121 may be severely damaged or destroyed if the Absolute Maximum Rating of 7V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7V , a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6121 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. Furthermore, this will defeat the short-circuit and over-temperature protection circuitry. Exceeding $\pm 7\text{V}$ input with a shorted output will destroy the device.

The device is best protected by the insertion of the parallel combination of a $100\text{ k}\Omega$ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a $100\text{ k}\Omega$ resistor (R2) from input to output of the buffer (see Figure 1). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than $100\text{ k}\Omega$, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7V Maximum Rating for input voltages up to 14V . This protection network should be sufficient to protect the LM6121 from the output of nearly any op amp which is operated on supply voltages of $\pm 15\text{V}$ or lower.



TL/H/9223-6

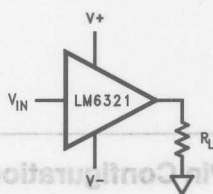
FIGURE 1. LM6121 with Overvoltage Protection

Application Hints

HEATSINK REQUIREMENTS

A heatsink may be required with the LM6321 depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible operating conditions, the junction temperature must be within the range specified under Absolute Maximum Ratings.

To determine if a heatsink is required, the maximum power dissipated by the buffer, $P(\max)$, must be calculated. The formula for calculating the maximum allowable power dissipation in any application is $P_D = (T_J(\max) - T_A)/\theta_{JA}$. For the simple case of a buffer driving a resistive load as in Figure 2, the maximum DC power dissipation occurs when the output is at half the supply. Assuming equal supplies, the formula is $P_D = I_S(2V^+) + V^+/2 R_L$.



TL/H/9223-8

FIGURE 2

The next parameter which must be calculated is the maximum allowable temperature rise, $T_R(\max)$. This is calculated by using the formula:

$$T_R(\max) = T_J(\max) - T_A(\max)$$

where: $T_J(\max)$ is the maximum allowable junction temperature

$T_A(\max)$ is the maximum ambient temperature

Using the calculated values for $T_R(\max)$ and $P(\max)$, the required value for junction-to-ambient thermal resistance, θ_{JA} , can now be found:

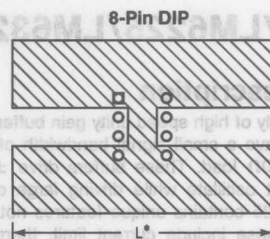
$$\theta_{JA} = T_R(\max)/P(\max)$$

The heatsink for the LM6321 is made using the PC board copper. The heat is conducted from the die, through the lead frame (inside the part), and out the pins which are soldered to the PC board. The pins used for heat conduction are:

TABLE I

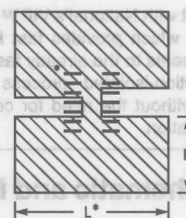
| Part | Package | Pins |
|---------|-----------|-----------------------------|
| LM6321N | 8-Pin DIP | 1, 4, 5, 8 |
| LM6321M | 14-Pin SO | 1, 2, 3, 6, 7, 8, 9, 13, 14 |

Figure 3 shows copper patterns which may be used to dissipate heat from the LM6321.



TL/H/9223-9

14-Pin SO



TL/H/9223-10

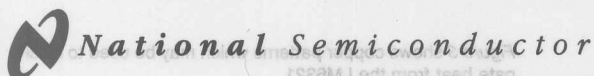
*For best results, use $L = 2H$

FIGURE 3. Copper Heatsink Patterns

Table II shows some values of junction-to-ambient thermal resistance (θ_{JA}) for values of L and W for 2 oz. copper:

TABLE II

| Package | L (in.) | H (in.) | θ_{JA} ($^{\circ}\text{C}/\text{W}$) |
|-----------|---------|---------|---|
| 8-Pin DIP | 2 | 0.5 | 47 |
| 14-Pin SO | 1 | 0.5 | 69 |
| | 2 | 1 | 57 |



LM6125/LM6225/LM6325 High Speed Buffer

General Description

The LM6125 family of high speed unity gain buffers slew at $800 \text{ V}/\mu\text{s}$ and have a small signal bandwidth of 50 MHz while driving a 50Ω load. These buffers drive $\pm 300 \text{ mA}$ peak and do not oscillate while driving large capacitive loads. The LM6125 contains unique features not found in power buffers; these include current limit, thermal shutdown, electronic shutdown, and an error flag that warns of fault conditions.

These buffers are built with National's VIPTM (Vertically Integrated PNP) process which provides fast PNP transistors that are true complements to the already fast NPN devices. This advanced junction-isolated process delivers high speed performance without the need for complex and expensive dielectric isolation.

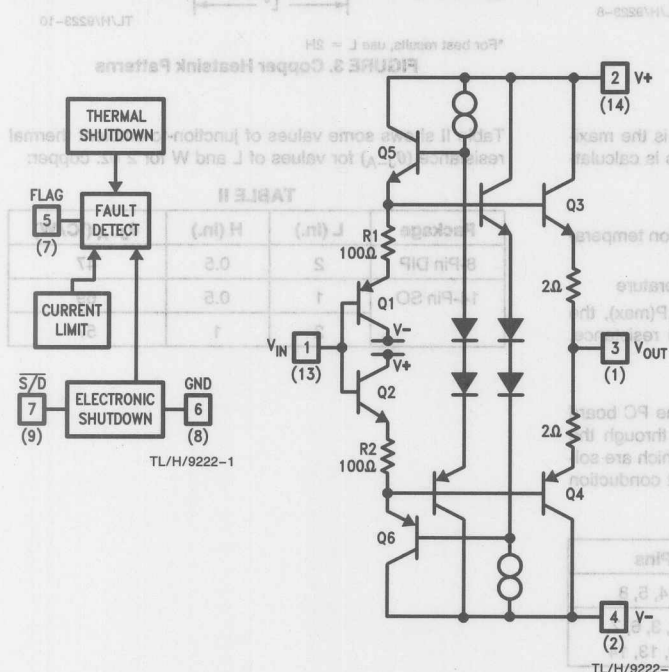
Features

- High slew rate $800 \text{ V}/\mu\text{s}$
- High output current $\pm 300 \text{ mA}$
- Stable with large capacitive loads
- Current and thermal limiting
- Electronic shutdown
- 5 V to $\pm 15 \text{ V}$ operation guaranteed
- Fully specified to drive 50Ω lines

Applications

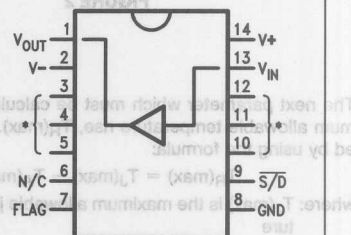
- Line Driving
- Radar
- Sonar

Simplified Schematic and Block Diagram



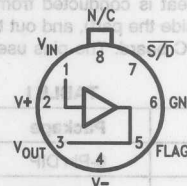
Numbers in () are for 14-pin N DIP.

Pin Configurations



*Heat sinking pins.
Internally connected to V-.

**Order Number LM6225N
or LM6325N**
See NS Package Number N14A



Top View

Note: Pin 4 connected to case

**Order Number LM6125H/883*
or LM6125H**
See NS Package Number H08C

*Available per 5962-9081501

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|--|
| Supply Voltage | 36V (± 18 V) |
| Input to Output Voltage (Note 2) | ± 7 V |
| Input Voltage | $\pm V_{\text{supply}}$ |
| Output Short-Circuit to GND (Note 3) | Continuous |
| Flag Output Voltage | $GND \leq V_{\text{flag}} \leq +V_{\text{supply}}$ |
| Storage Temperature Range | -65°C to $+150^{\circ}\text{C}$ |
| Lead Temperature (Soldering, 10 seconds) | 260°C |

ESD Tolerance (Note 9)

 ± 1500 V θ_{JA} (Note 4)

H Package

 150°C/W

N Package

 40°C/W Maximum Junction Temperature (T_J) 150°C

Operating Temperature Range

LM6125

 -55°C to $+125^{\circ}\text{C}$

LM6225

 -40°C to $+85^{\circ}\text{C}$

LM6325

 0°C to $+70^{\circ}\text{C}$

Operating Supply Voltage Range

 4.75 V to ± 16 V**DC Electrical Characteristics**

The following specifications apply for Supply Voltage = ± 15 V, $V_{CM} = 0$, $R_L \geq 100$ k Ω and $R_S = 50$ Ω unless otherwise noted. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX} ; all other limits $T_A = T_J = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Typ | LM6125 | LM6225 | LM6325 | Units |
|-----------|---------------------------------|--|-------|------------------------|-------------------|-------------------|------------------------|
| | | | | Limit (Notes 5, 10) | Limit (Note 5) | Limit (Note 5) | |
| A_{V1} | Voltage Gain 1 | $R_L = 1$ k Ω , $V_{IN} = \pm 10$ V | 0.990 | 0.980 0.970 | 0.980 | 0.970 | V/V Min |
| A_{V2} | Voltage Gain 2 | $R_L = 50$ Ω , $V_{IN} = \pm 10$ V | 0.900 | 0.860 0.800 | 0.860 | 0.850 | |
| A_{V3} | Voltage Gain 3 (Note 6) | $R_L = 50$ Ω , $V^+ = 5$ V $V_{IN} = 2 V_{PP}$ (1.5 V_{PP}) | 0.840 | 0.780 0.750 | 0.780 | 0.750 | |
| V_{OS} | Offset Voltage | $R_L = 1$ k Ω | 15 | 30 50 | 30 60 | 50 100 | mV Max |
| I_B | Input Bias Current | $R_L = 1$ k Ω , $R_S = 10$ k Ω | 1 | 4 7 | 4 7 | 5 7 | μ A Max |
| R_{IN} | Input Resistance | $R_L = 50$ Ω | 5 | | | | M Ω |
| C_{IN} | Input Capacitance | | 3.5 | | | | pF |
| R_O | Output Resistance | $I_{OUT} = \pm 10$ mA | 3 | 5 10 | 5 10 | 5 6 | Ω Max |
| I_{S1} | Supply Current 1 | $R_L = \infty$ | 15 | 18 20 | 18 20 | 20 22 | mA Max |
| I_{S2} | Supply Current 2 | $R_L = \infty$, $V^+ = 5$ V | 14 | 16 18 | 16 18 | 18 20 | |
| $I_{S/D}$ | Supply Current in Shutdown | $R_L = \infty$, $V^{\pm} = \pm 15$ V | 1.1 | 1.5 2.0 | 1.5 2.0 | 1.5 2.0 | |
| V_{O1} | Output Swing 1 | $R_L = 1$ k Ω | 13.5 | 13.3 13 | 13.3 13 | 13.2 13 | \pm V Min |
| V_{O2} | Output Swing 2 | $R_L = 100$ Ω | 12.7 | 11.5 10 | 11.5 10 | 11 10 | |
| V_{O3} | Output Swing 3 | $R_L = 50$ Ω | 12 | 11 9 | 11 9 | 10 9 | |
| V_{O4} | Output Swing 4 | $R_L = 50$ Ω | 1.8 | 1.6 1.3 | 1.6 1.4 | 1.6 1.5 | V _{PP} Min |
| PSRR | Power Supply Rejection Ratio | $V^+ = 5$ V (Note 6) | 70 | 60 55 | 60 50 | 60 50 | dB Min |
| V_{OL} | Flag Pin Output Low Voltage | $V^{\pm} = \pm 5$ V to ± 15 V $V_{S/D} = 0$ V | | 300 400 | 300 400 | 340 400 | mV Max |
| I_{OH} | Flag Pin Output High Current | V_{OH} Flag Pin = 15V (Note 7) | 0.01 | 10 20 | 10 20 | 10 20 | μ A Max |

$R_L \geq 100 \text{ k}\Omega$ and $R_S = 50 \Omega$ unless otherwise noted.

 $T_J = 25^\circ\text{C}$

| | LM6125 | LM6225 | LM6325 | Units |
|---|------------------------|-------------------|-------------------|-------|
| | Limit (Notes 5, 10) | Limit (Note 5) | Limit (Note 5) | |
| | 2.0 | 2.0 | 2.0 | V |
| | 2.0 | 2.0 | 2.0 | Min |
| | 0.8 | 0.8 | 0.8 | V |
| | 0.8 | 0.8 | 0.8 | Max |
| 7 | -10 | -10 | -10 | μA |
| | -20 | -20 | -20 | Max |
| 5 | -10 | -10 | -10 | μA |
| | -20 | -20 | -20 | Max |
| | 50 | 50 | 100 | μA |
| | 2000 | 100 | 200 | |

$R_{CM} = 0$, $R_L \geq 100 \text{ k}\Omega$ and $R_S = 50 \Omega$ unless otherwise noted.

 $T_A = T_J = 25^\circ\text{C}.$

| | | LM6125 | LM6225 | LM6325 | Units |
|------|---------------------------|----------|----------|----------|-------------------|
| Typ | Limit | Limit | Limit | Limit | |
| | (Note 5) | (Note 5) | (Note 5) | (Note 5) | |
| 1200 | | | | | V _{OS} |
| 800 | 550 | 550 | 550 | | V/ μ s Min |
| 50 | | | | | Min |
| 50 | 30 | 30 | 30 | | MHz Min |
| 8.0 | $R_L = \infty$ | | | | ns |
| 4.0 | $R_L = \infty, V_I = 0$ | | | | ns |
| 10 | $R_L = \infty, V_I = 15V$ | | | | % |
| -50 | $R_L = 1k\Omega$ | | | | dB |
| 30 | | | | | pF |
| 700 | | | | | ns |

Electrical Characteristics (Continued)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: During current limit, thermal limit, or electronic shutdown the input current will increase if the input to output differential voltage exceeds 8V. See Overvoltage Protection in Application Hints.

Note 3: The LM6125 series buffers contain current limit and thermal shutdown to protect against fault conditions.

Note 4: For operation at elevated temperature, these devices must be derated based on a thermal resistance of θ_{JA} and $T_J \text{ max}$, $T_J = T_A + \theta_{JA} P_D$. θ_{JC} for the LM6125H and LM6225H is 17°C/W. The thermal impedance θ_{JA} of the device in the N package is 40°C/W when soldered directly to a printed circuit board, and the heat-sinking pins (pins 3, 4, 5, 10, 11, and 12) are connected to 2 square inches of 2 oz. copper. When installed in a socket, the thermal impedance θ_{JA} of the N package is 60°C/W.

Note 5: Limits are guaranteed by testing or correlation.

Note 6: The input is biased to +2.5V, and V_{IN} swings V_{PP} about this value. The input swing is 2 V_{PP} at all temperatures except for the A_V3 test at -55°C where it is reduced to 1.5 V_{PP} .

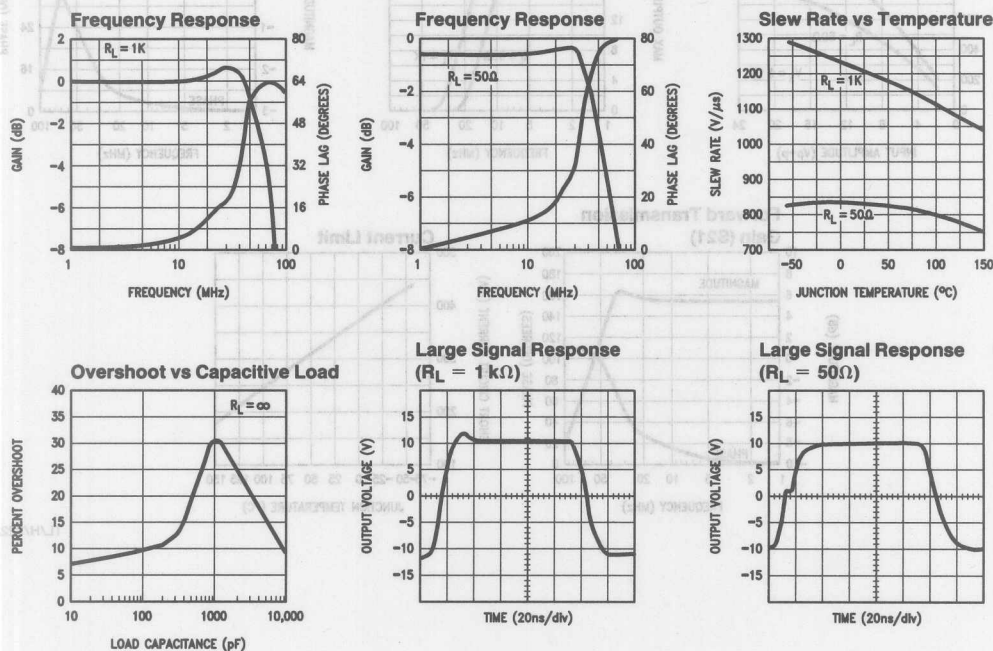
Note 7: The Error Flag is set (low) during current limit or thermal fault detection in addition to being set by the Shutdown pin. It is an open-collector output which requires an external pullup resistor.

Note 8: Slew rate is measured with a $\pm 11V$ input pulse and 50 Ω source impedance at 25°C. Since voltage gain is typically 0.9 driving a 50 Ω load, the output swing will be approximately $\pm 10V$. Slew rate is calculated for transitions between $\pm 5V$ levels on both rising and falling edges. A high speed measurement is done to minimize device heating. For slew rate versus junction temperature see typical performance curves. The input pulse amplitude should be reduced to $\pm 10V$ for measurements at temperature extremes. For accurate measurements, the input slew rate should be at least 1700 V/ μs .

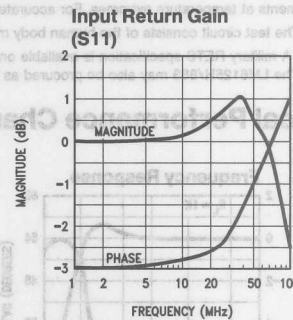
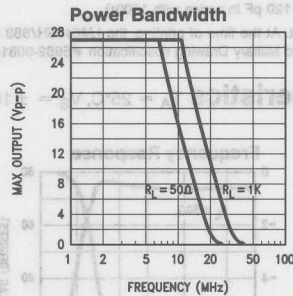
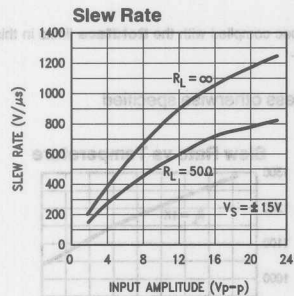
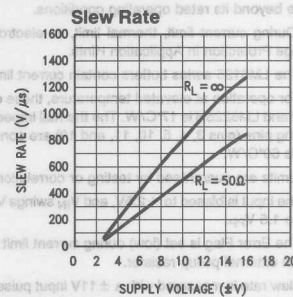
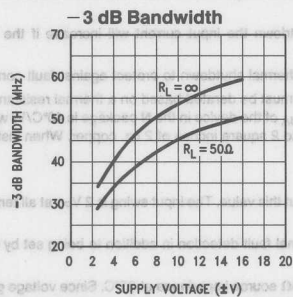
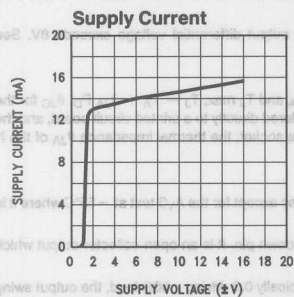
Note 9: The test circuit consists of the human body model of 120 pF in series with 1500 Ω .

Note 10: A military RETS specification is available on request. At the time of printing, the LM6125H/883 RETS spec complied with the **Boldface** limits in this column. The LM6125H/883 may also be procured as Standard Military Drawing specification #5962-9081501MX.

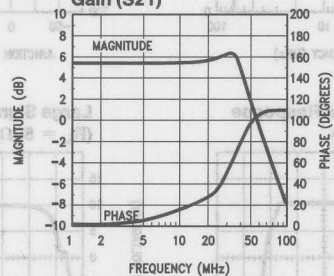
Typical Performance Characteristics $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$, unless otherwise specified



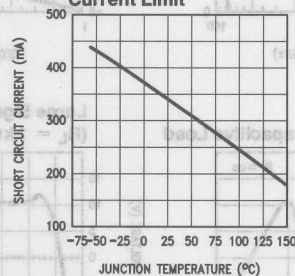
TL/H/9222-5



Forward Transmission Gain (S21)

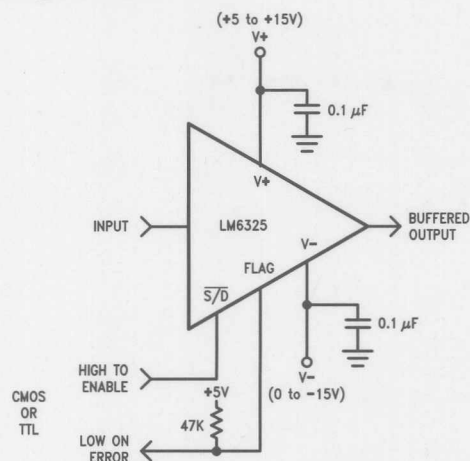


Current Limit



TL/H/9222-7

Typical Connection Diagram



TL/H/9222-6

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6125 series buffers. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of $900 \text{ V}/\mu\text{s}$ into a 50Ω load produces a di/dt of $18 \text{ A}/\mu\text{s}$. Multiplying this by a wiring inductance of 50 nH results in a 0.9 V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a $0.1 \mu\text{F}$ ceramic in parallel with one or two $2.2 \mu\text{F}$ tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6125 is stable into any load when driven by a 50Ω source. As shown in the *Overshoot vs Capacitive Load* graph, worst case is a purely capacitive load of about 1000 pF . Shunting the load capacitance with a resistor will reduce overshoot.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6125 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50Ω load, this goes up to 200 nH . This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation, and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (S/D) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

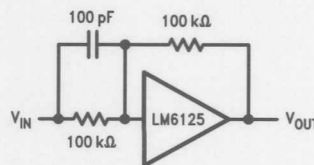
If the S/D pin is not to be used, it should be connected to V^+ .

OVERVOLTAGE PROTECTION

The LM6125 may be severely damaged or destroyed if the Absolute Maximum Rating of 7 V between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed 7 V , a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6125 simplified schematic, the transistors involved are Q1 and Q3 for positive inputs, and Q2 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

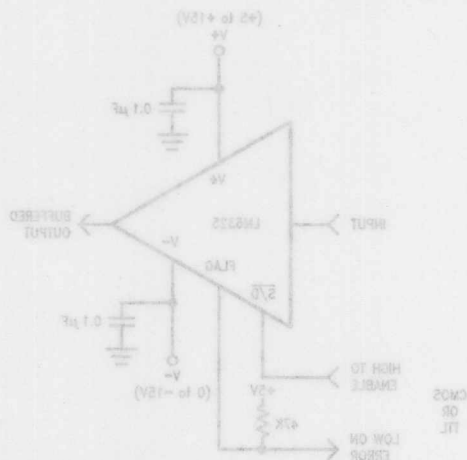
The device is best protected by the insertion of the parallel combination of a $100 \text{ k}\Omega$ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a $100 \text{ k}\Omega$ resistor (R2) from input to output of the buffer (see Figure 1). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referred load of significantly less than $100 \text{ k}\Omega$, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-output differential below the 7 V Maximum Rating for input voltages up to 14 V . This protection network should be sufficient to protect the LM6125 from the output of nearly any op amp which is operated on supply voltages of $\pm 15 \text{ V}$ or lower.



TL/H/9222-8

FIGURE 1. LM6125 with Overvoltage Protection

Typical Connection Diagram



TLV16025-B

Application Hints

POWER SUPPLY DECOUPLING

The method of supply bypassing is not critical for stability of the LM6152 series buffer. However, their high current output combined with high slew rate can result in significant voltage transients on the power supply lines if much inductance is present. For example, a slew rate of 800 V/μs into a 50 Ω load produces a dV/dt of 16 A/μs. Multiplying this by a wiring inductance of 50 nH results in a 0.8 V transient. To minimize this problem use high quality decoupling very close to the device. Suggested values are a 0.1 μF ceramic in parallel with one or two 2.2 μF tantalums. A ground plane is recommended.

LOAD IMPEDANCE

The LM6152 is stable into any load when driven by a 50 Ω source. As shown in the Overvoltage Protection graph, worst case is a purely capacitive load of about 1000 pF. Shunting the load capacitance with a resistor will reduce overvoltage.

SOURCE INDUCTANCE

Like any high-frequency buffer, the LM6152 can oscillate at high values of source inductance. The worst case condition occurs at a purely capacitive load of 50 pF where up to 100 nH of source inductance can be tolerated. With a 50 Ω load, this goes up to 200 nH. This sensitivity may be reduced at the expense of a slight reduction in bandwidth by adding a resistor in series with the buffer input. A 100 Ω resistor will ensure stability with source inductances up to 400 nH with any load.

ERROR FLAG LOGIC

The Error Flag pin is an open-collector output which requires an external pull-up resistor. Flag voltage is HIGH during operation and is LOW during a fault condition. A fault condition occurs if either the internal current limit or the thermal shutdown is activated, or the shutdown (SVD) pin is driven low by external logic. Flag voltage returns to its HIGH state when normal operation resumes.

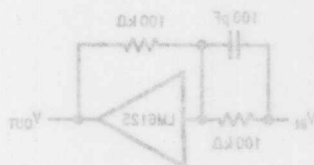
If the SVD pin is not to be used, it should be connected to V+.

OVERVOLTAGE PROTECTION

The LM6152 may be severely damaged or destroyed if the Absolute Maximum Rating of TV between input and output pins is exceeded.

If the buffer's input-to-output differential voltage is allowed to exceed TV, a base-emitter junction will be in reverse-breakdown, and will be in series with a forward-biased base-emitter junction. Referring to the LM6152 simplified schematic, the transistors involved are Q1 and Q2 for positive inputs, and Q3 and Q4 for negative inputs. If any current is allowed to flow through these junctions, localized heating of the reverse-biased junction will occur, potentially causing damage. The effect of the damage is typically increased offset voltage, increased bias current, and/or degraded AC performance. The damage is cumulative, and may eventually result in complete device failure.

The device is best protected by the insertion of the parallel combination of a 100 kΩ resistor (R1) and a small capacitor (C1) in series with the buffer input, and a 100 kΩ resistor (R2) from input to output of the buffer (see Figure 7). This network normally has no effect on the buffer output. However, if the buffer's current limit or shutdown is activated, and the output has a ground-referenced load of significantly less than 100 kΩ, a large input-to-output voltage may be present. R1 and R2 then form a voltage divider, keeping the input-to-output differential below the TV Maximum Rating for input voltages up to 14 V. This protection network should be sufficient to protect the LM6152 from the output of nearly any op amp which is operated on supply voltages of ±12 V or lower.



TLV16025-B

FIGURE 7. LM6152 with Overvoltage Protection



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| 3-107 | LM710 Voltage Comparator |
| 3-111 | LM780 High Speed Differential Comparator |
| 3-118 | LM1801 Battery Operated Power Comparator |
| 3-126 | LM651 180 ns 3V Comparator |
| 3-131 | LMC6782 Dual/LMC6784 Quad Micropower Rail-to-Rail Input and Output CMOS Comparator |
| 3-135 | LMC6725 Dual, LMC6724 Quad, Micropower Rail-to-Rail Input and Open Drain Output CMOS Comparator |
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| 3-144 | LMC722 Tiny CMOS Comparator with Rail-to-Rail Input and Open Drain Output |
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Section 3 Voltage Comparators



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Voltage Comparators Definition of Terms

Input Bias Current: The average of the two input currents.

Input Offset Current: The absolute value of the difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

Input Offset Voltage: The absolute value of the voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

Input Voltage Range: The range of voltage on the input terminals (common-mode) over which the offset specifications apply.

Logic Threshold Voltage: The voltage at the output of the comparator at which the loading logic circuitry changes its digital state.

Negative Output Level: The negative DC output voltage with the comparator saturated by a differential input equal to or greater than a specified voltage.

Output Leakage Current: The current into the output terminal with the output voltage within a given range and the input drive equal to or greater than a given value.

Output Resistance: The resistance seen looking into the output terminal with the DC output level at the logic threshold voltage.

Output Sink Current: The maximum negative current that can be delivered by the comparator.

Positive Output Level: The high output voltage level with a given load and the input drive equal to or greater than a specified value.

Power Consumption: The power required to operate the comparator with no output load. The power will vary with signal level, but is specified as a maximum for the entire range of input signal conditions.

Response Time: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

Saturation Voltage: The low-output voltage level with the input drive equal to or greater than a specified value.

Strobe Current: The current out of the strobe terminal when it is at the zero logic level.

Strobe Output Level: The DC output voltage, independent of input conditions, with the voltage on the strobe terminal equal to or less than the specified low state.

Strobe "ON" Voltage: The maximum voltage on either strobe terminal required to force the output to the specified high state independent of the input voltage.

Strobe "OFF" Voltage: The minimum voltage on the strobe terminal that will guarantee that it does not interfere with the operation of the comparator.

Strobe Release Time: The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from zero to the one logic level.

Supply Current: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

Voltage Gain: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

| | | | | | |
|---------|------|----|-----------|---------------|--|
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | TinyPak SOT23-5 MicroPower Comparator, Open Drain Output |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | TinyPak SOT23-5 MicroPower Comparator |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | Output |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | MicroPower Quad, Open Drain |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | MicroPower Quad, Open Drain Output |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | MicroPower Quad |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | MicroPower Dual |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | Output CMOS Comparator |
| LMC2521 | 4000 | 12 | 7 μ A | 0.02 pA (typ) | MicroPower Rail-to-Rail Input & Output CMOS Comparator |

Note 1: Data sheet should be referred to for test conditions and more detailed information.
Note 2: This section guide should be used to select for Response Time, Input Bias Current, Input Offset Current, Input Offset Voltage, Input Voltage Range, Output Level, Output Resistance, Output Sink Current, Output Leakage Current, Power Consumption, Strobe Current, Strobe Output Level, Strobe "ON" Voltage, Strobe "OFF" Voltage, Strobe Release Time, and Voltage Gain. The DC specifications are for the power Commercial Grade available.



Voltage Comparators Selection Guide

| | Response Time (Typ) ns | V _{OS} mV(Max) | I _S mA(Max) | I _B nA(Max) | Special Features |
|---------------------------------------|------------------------------|----------------------------|---------------------------|---------------------------|--|
| T _A = 25°C (Notes 1 and 2) | | | | | |
| LM6685 | 2.6 | 1.9 | 23 | 9,000 | Single, Very High Speed ECL Output |
| LM6687 | 2.6 | 1.9 | 38 | 9,000 | Dual, Very High Speed ECL Output |
| LM360 | 14 | 5 | 32 | 20,000 | High Speed, Complementary Outputs |
| LM361 | 14 | 5 | 20 | 30,000 | High Speed w/Strobes |
| LM306 | 28 | 5 | 10 | 25,000 | High Speed, High Drive |
| LM319 | 80 | 8 | 12.5 | 1000 | High Speed Dual |
| LM6511 | 180 | 5 | 3.5 | 130 | |
| LF311 | 200 | 10 | 7.5 | 0.15 | FET Input |
| LM311 | 200 | 7.5 | 7.5 | 250 | General Purpose Single |
| LH2311 | 200 | 7.5 | 7.5 | 250 | Dual LM311 |
| LP311 | 1200 | 7.5 | 0.3 | 100 | Low Power Single |
| LM339 | 1300 | 5 | 2.5 | 250 | General Purpose Quad |
| LM392 | 1300 | 10 | 1 | 400 | One Comparator Plus One Op Amp |
| LM393 | 1300 | 5 | 2.5 | 250 | General Purpose Dual |
| LM2901 | 1300 | 7 | 2.5 | 250 | Automotive Quad |
| LM612 | 1500 | 5 | 0.250 | 35 | Super-Block™ |
| LM613 | 1500 | 5 | 1 | 35 | Dual Comparator + Reference Super-Block™ |
| LM615 | 1500 | 5 | 0.600 | 35 | Dual Comparator + Dual Op Amp + Reference Super-Block™ |
| LM2903 | 1500 | 7 | 2.5 | 250 | Quad Comparator + Reference Automotive Dual |
| LP365 | 4000 | 6 | 0.275 | 75 | Programmable Quad |
| LP339 | 8000 | 5 | 0.1 | 25 | Low Power Quad |
| LMC676214 | 4000 | 5 | 0.01 | | MicroPower Rail-to-Rail Input & Output CMOS Comparator |
| LMC6762 | 4000 | 5 | 20 µA | 0.02 pA (typ) | MicroPower Dual |
| LMC6764 | 4000 | 5 | 40 µA | 0.02 pA (typ) | MicroPower Quad |
| LMC6772 | 4000 | 5 | 20 µA | 0.02 pA (typ) | MicroPower Dual, Open Drain Output |
| LMC6774 | 4000 | 5 | 40 µA | 0.02 pA (typ) | MicroPower Quad, Open Drain Output |
| LMC7211 | 4000 | 15 | 7 µA | 0.02 pA (typ) | TinyPak™ SOT23-5 MicroPower Comparator |
| LMC7221 | 4000 | 15 | 7 µA | 0.02 pA (typ) | TinyPak SOT23-5 MicroPower Comparator, Open Drain Output |

Note 1: Datasheet should be referred to for test conditions and more detailed information.

Note 2: This selection guide should be used to select for Response Time required. Industrial and Military Temperature Range types are available. The DC specs are for the lowest Commercial Grade available.

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to $\pm 15V$ range the LF111 can be used in the most critical applications.

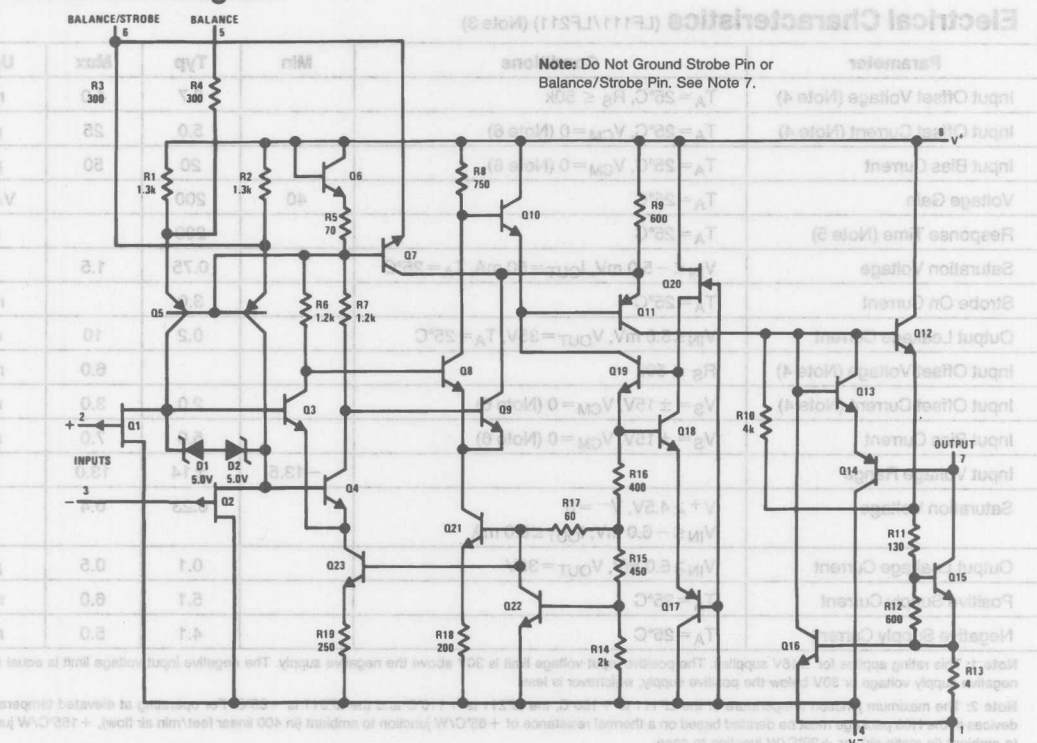
The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done.

Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

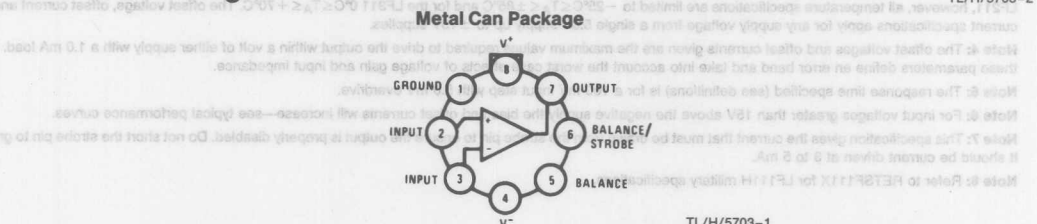
Features

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Schematic Diagram



Connection Diagram



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 8)

| | LF111/LF211 | LF311 |
|--|-------------|------------|
| Total Supply Voltage (V_{84}) | 36V | 36V |
| Output to Negative Supply Voltage (V_{74}) | 50V | 40V |
| Ground to Negative Supply Voltage (V_{14}) | 30V | 30V |
| Differential Input Voltage | $\pm 30V$ | $\pm 30V$ |
| Input Voltage (Note 1) | $\pm 15V$ | $\pm 15V$ |
| Power Dissipation (Note 2) | 500 mW | 500 mW |
| Output Short Circuit Duration | 10 seconds | 10 seconds |

Operating Temp.

Range

LF111

-55°C to $+125^{\circ}\text{C}$

LF211

-25°C to $+85^{\circ}\text{C}$

LF311

0°C to $+70^{\circ}\text{C}$

Storage Temp.

Range

-65°C to $+150^{\circ}\text{C}$

-65°C to $+150^{\circ}\text{C}$

Lead Temp.

(Soldering,

10 seconds)

260°C

260°C

ESD rating to be determined.

Electrical Characteristics (LF111/LF211) (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------|--|-------|----------|------|---------------|
| Input Offset Voltage (Note 4) | $T_A = 25^{\circ}\text{C}$, $R_S \leq 50k$ | | 0.7 | 4.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25^{\circ}\text{C}$, $V_{CM} = 0$ (Note 6) | | 5.0 | 25 | pA |
| Input Bias Current | $T_A = 25^{\circ}\text{C}$, $V_{CM} = 0$ (Note 6) | | 20 | 50 | pA |
| Voltage Gain | $T_A = 25^{\circ}\text{C}$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25^{\circ}\text{C}$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -5.0 \text{ mV}$, $I_{OUT} = 50 \text{ mA}$, $T_A = 25^{\circ}\text{C}$ | | 0.75 | 1.5 | V |
| Strobe On Current | $T_A = 25^{\circ}\text{C}$ | | 3.0 | | mA |
| Output Leakage Current | $V_{IN} \leq 5.0 \text{ mV}$, $V_{OUT} = 35V$, $T_A = 25^{\circ}\text{C}$ | | 0.2 | 10 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50k$ | | | 6.0 | mV |
| Input Offset Current (Note 4) | $V_S = \pm 15V$, $V_{CM} = 0$ (Note 6) | | 2.0 | 3.0 | nA |
| Input Bias Current | $V_S = \pm 15V$, $V_{CM} = 0$ (Note 6) | | 5.0 | 7.0 | nA |
| Input Voltage Range | | -13.5 | ± 14 | 13.0 | V |
| Saturation Voltage | $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6.0 \text{ mV}$, $I_{OUT} \leq 8.0 \text{ mA}$ | | 0.23 | 0.4 | V |
| Output Leakage Current | $V_{IN} \geq 5.0 \text{ mV}$, $V_{OUT} = 35V$ | | 0.1 | 0.5 | μA |
| Positive Supply Current | $T_A = 25^{\circ}\text{C}$ | | 5.1 | 6.0 | mA |
| Negative Supply Current | $T_A = 25^{\circ}\text{C}$ | | 4.1 | 5.0 | mA |

Note 1: This rating applies for $\pm 15V$ supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is $+150^{\circ}\text{C}$, the LF211 is $+110^{\circ}\text{C}$ and the LF311 is $+85^{\circ}\text{C}$. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of $+65^{\circ}\text{C}/\text{W}$ junction to ambient (in 400 linear feet/min air flow), $+165^{\circ}\text{C}/\text{W}$ junction to ambient (in static air), or $+20^{\circ}\text{C}/\text{W}$ junction to case.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ and for the LF311 $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0V supply up to $\pm 15V$ supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 8: Refer to RETSF111X for LF111H military specifications.

Electrical Characteristics (LF311) (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------|---|-----|--------------|-----|--------|
| Input Offset Voltage (Note 4) | $T_A = 25^\circ\text{C}$, $R_S \leq 50\text{k}$ | | 2.0 | 10 | mV |
| Input Offset Current (Note 4) | $T_A = 25^\circ\text{C}$, $V_{CM} = 0$ (Note 6) | | 5.0 | 75 | pA |
| Input Bias Current | $T_A = 25^\circ\text{C}$, $V_{CM} = 0$ (Note 6) | | 25 | 150 | pA |
| Voltage Gain | $T_A = 25^\circ\text{C}$ | | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25^\circ\text{C}$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -10\text{ mV}$, $I_{OUT} = 50\text{ mA}$, $T_A = 25^\circ\text{C}$ | | 0.75 | 1.5 | V |
| Strobe On Current | $T_A = 25^\circ\text{C}$ | | 3.0 | | mA |
| Output Leakage Current | $V_{IN} \geq 10\text{ mV}$, $V_{OUT} = 35\text{ V}$, $T_A = 25^\circ\text{C}$ | | 0.2 | 10 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50\text{k}$ | | | 15 | mV |
| Input Offset Current (Note 4) | $V_S = \pm 15\text{ V}$, $V_{CM} = 0$ (Note 6) | | 1.0 | | nA |
| Input Bias Current | $V_S = 15\text{ V}$, $V_{CM} = 0$ (Note 6) | | 3.0 | | nA |
| Input Voltage Range | | | +14 -13.5 | | V V |
| Saturation Voltage | $V^+ \geq 4.5\text{ V}$, $V^- = 0$ $V_{IN} \leq -10\text{ mV}$, $I_{OUT} \leq 8.0\text{ mA}$ | | 0.23 | 0.4 | V |
| Positive Supply Current | $T_A = 25^\circ\text{C}$ | | 5.1 | 7.5 | mA |
| Negative Supply Current | $T_A = 25^\circ\text{C}$ | | 4.1 | 5.0 | mA |

Note 1: This rating applies for $\pm 15\text{ V}$ supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LF111 is $+150^\circ\text{C}$, the LF211 is $+110^\circ\text{C}$ and the LF311 is $+85^\circ\text{C}$. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of $+165^\circ\text{C/W}$, junction to ambient, or $+20^\circ\text{C/W}$, junction to case.

Note 3: These specifications apply for $V_S = \pm 15\text{ V}$ and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the LF111, unless otherwise stated. With the LF211, however, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ and for the LF311 $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5.0 mV supply up to $\pm 15\text{ V}$ supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1.0 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

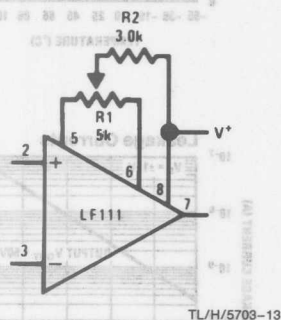
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5.0 mV overdrive.

Note 6: For input voltages greater than 15V above the negative supply the bias and offset currents will increase—see typical performance curves.

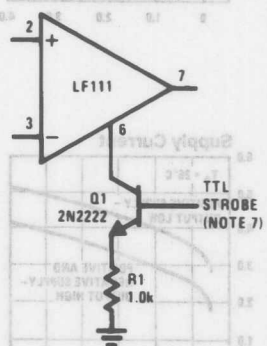
Note 7: This specification gives the current that must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Auxiliary Circuits

Offset Balancing

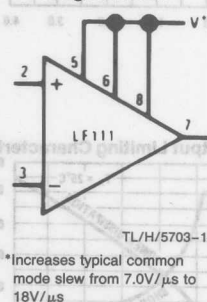


Strobing

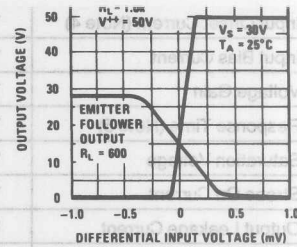
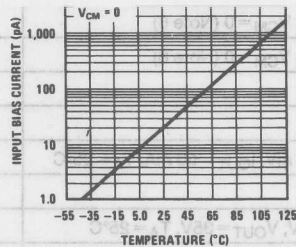
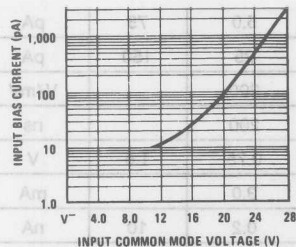


Note: Do Not Ground Strobe Pin.

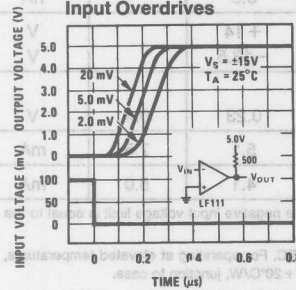
Increasing Input Stage Current*



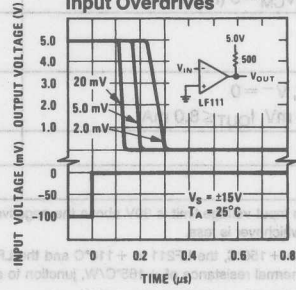
*Increases typical common mode slew from 7.0V/ μs to 18V/ μs



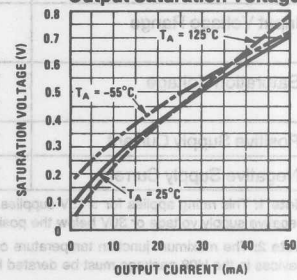
Response Time for Various Input Overdrives



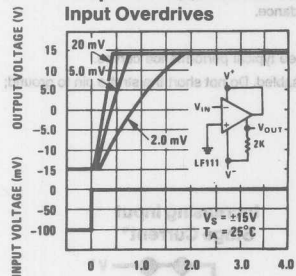
Response Time for Various Input Overdrives



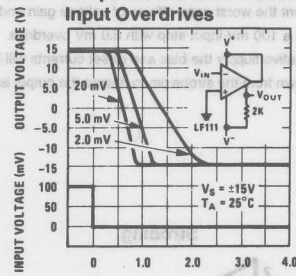
Output Saturation Voltage



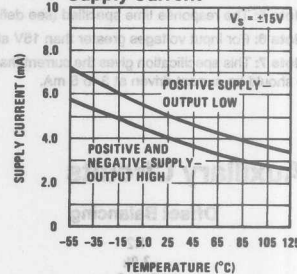
Response Time for Various Input Overdrives



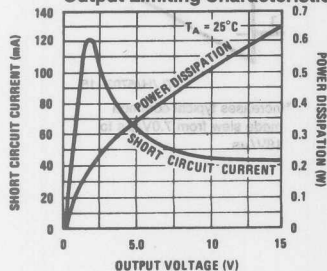
Response Time for Various Input Overdrives



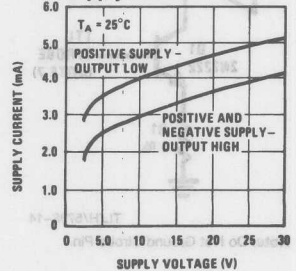
Supply Current



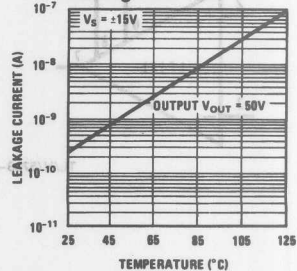
Output Limiting Characteristics



Supply Current

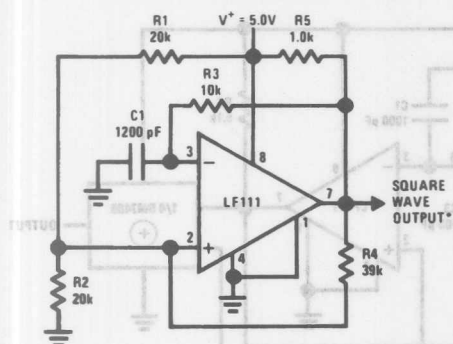


Leakage Currents



Typical Applications

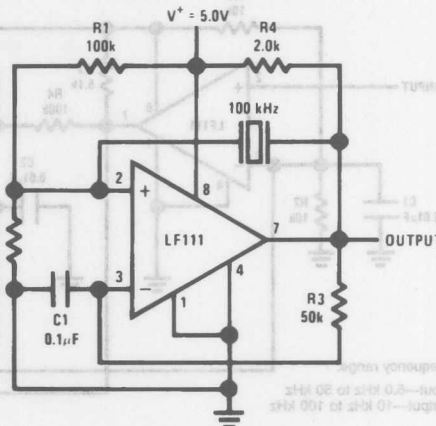
100 kHz Free Running Multivibrator



*TTL or DTL fanout of two.

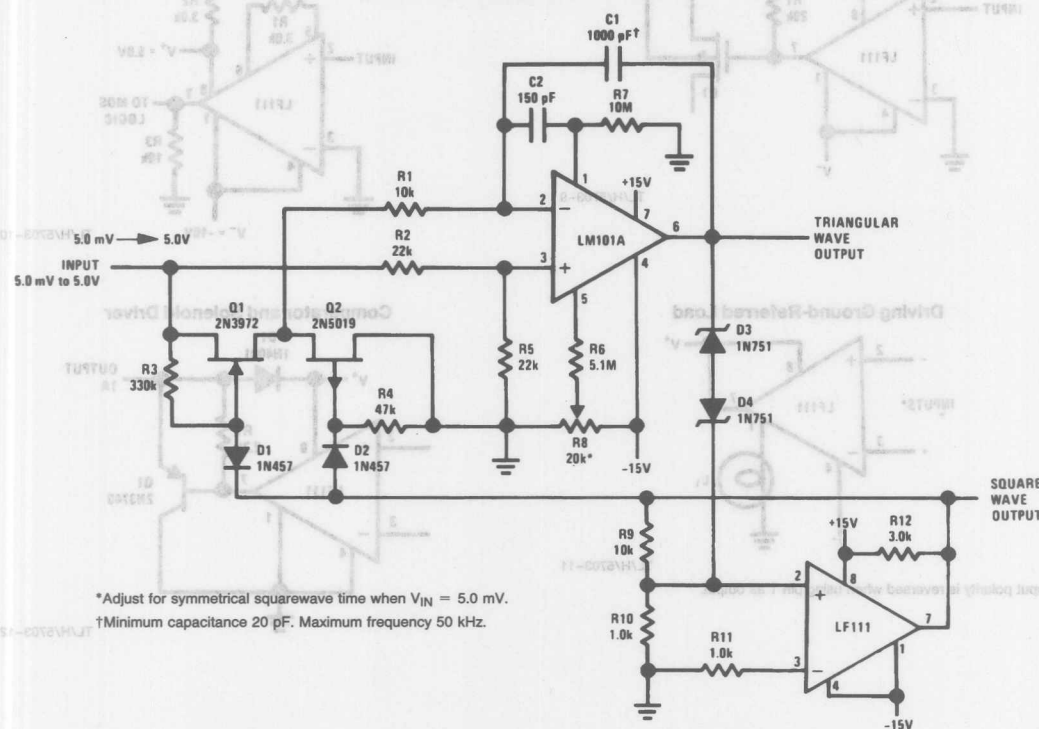
TL/H/5703-7

Crystal Oscillator



TL/H/5703-3

10 Hz to 10 kHz Voltage Controlled Oscillator



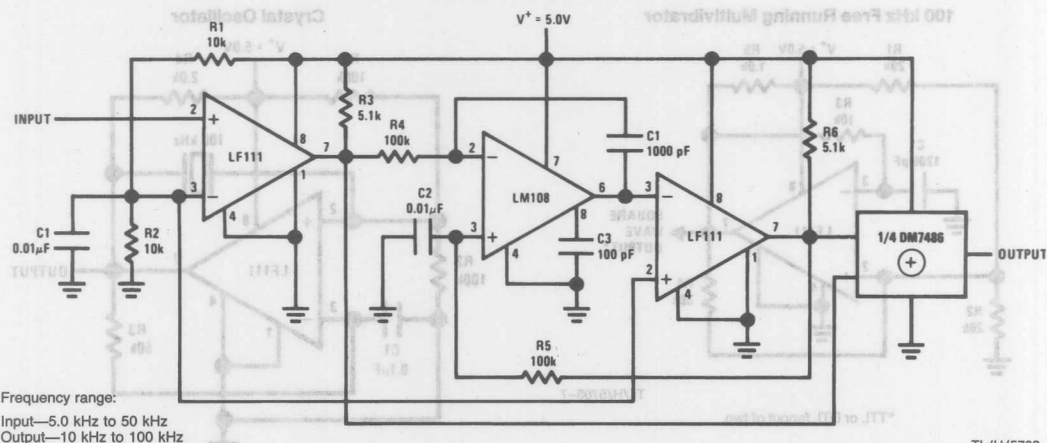
*Adjust for symmetrical squarewave time when $V_{IN} = 5.0$ mV.

†Minimum capacitance 20 pF. Maximum frequency 50 kHz.

TL/H/5703-5

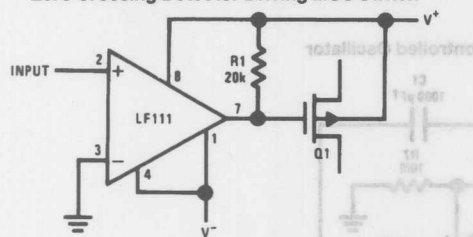
Typical Applications (Continued)

Frequency Doubler



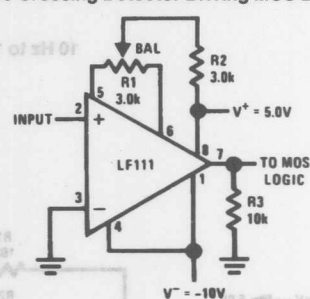
TL/H/5703-8

Zero Crossing Detector Driving MOS Switch



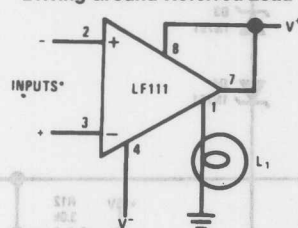
TL/H/5703-9

Zero Crossing Detector Driving MOS Logic



TL/H/5703-10

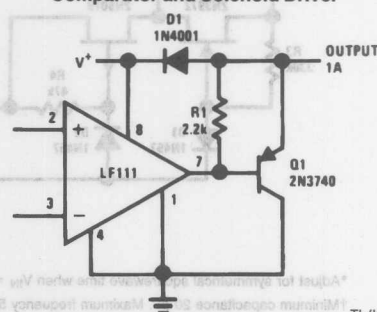
Driving Ground-Referred Load



TL/H/5703-11

*Input polarity is reversed when using pin 1 as output.

Comparator and Solenoid Driver



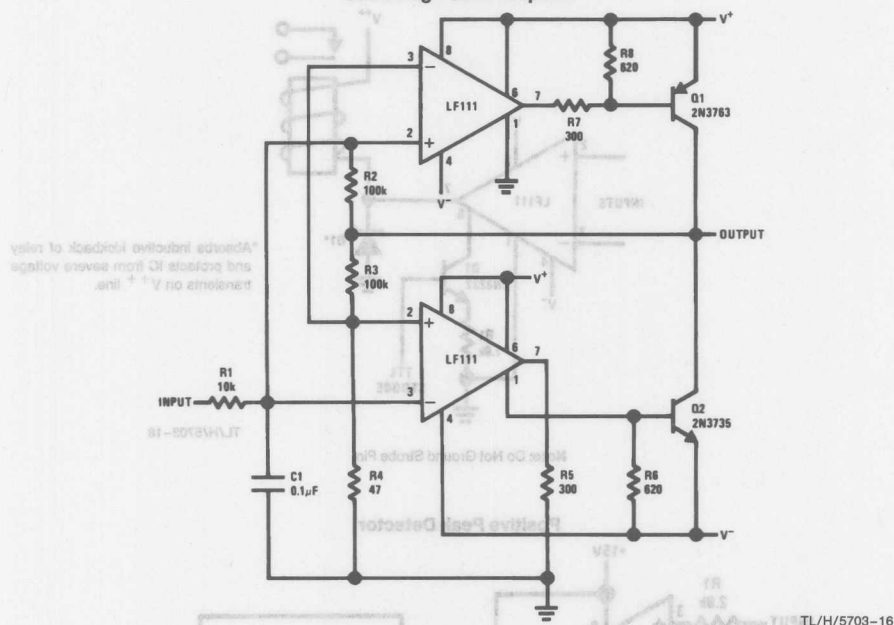
TL/H/5703-12

Typical Applications (Continued)

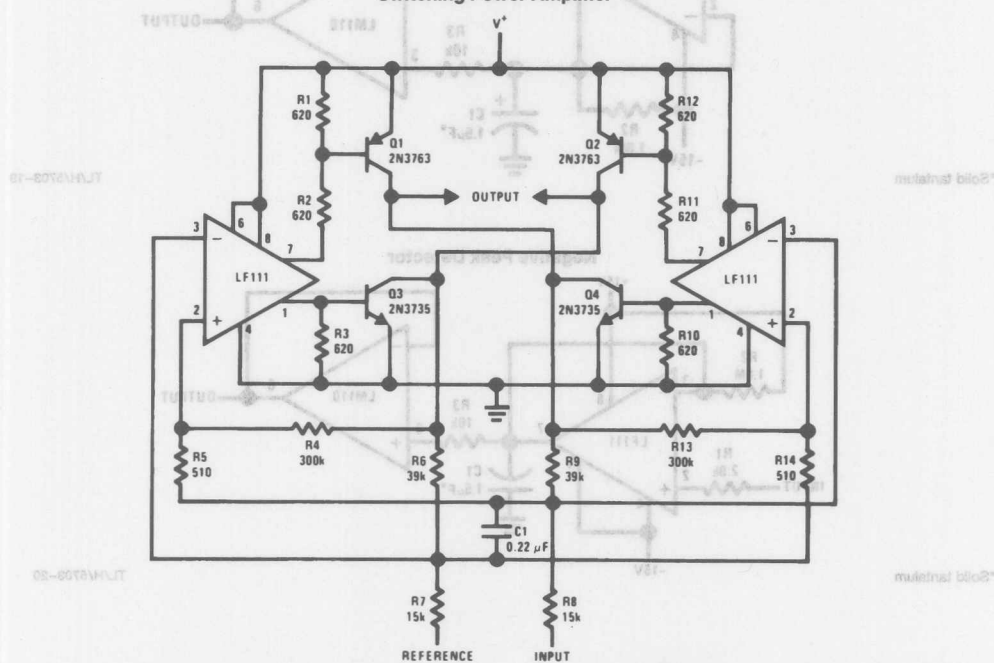
Typical Applications (Continued)

LF111/LF211/LF311

Switching Power Amplifier

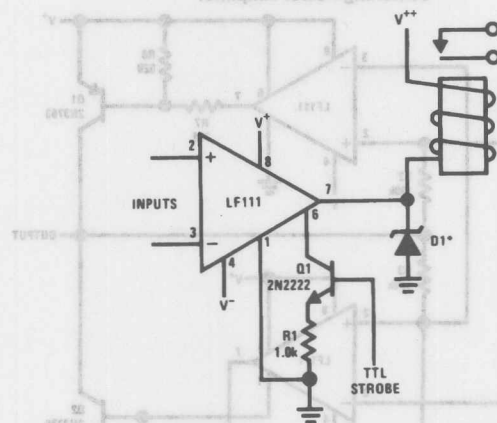


Switching Power Amplifier



Typical Applications (Continued)

Relay Driver with Strobe

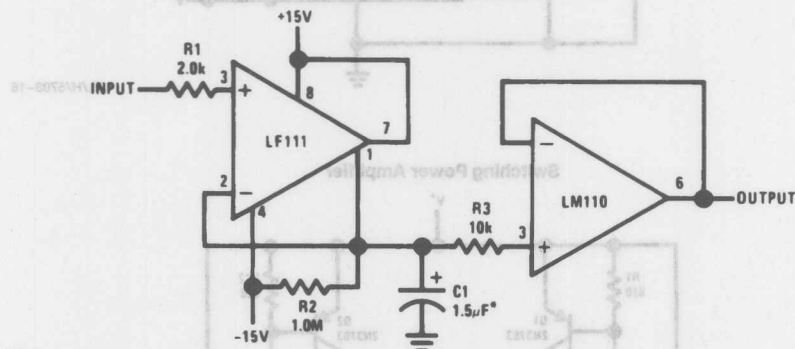


*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V^{++} line.

TL/H/5703-18

Note: Do Not Ground Strobe Pin.

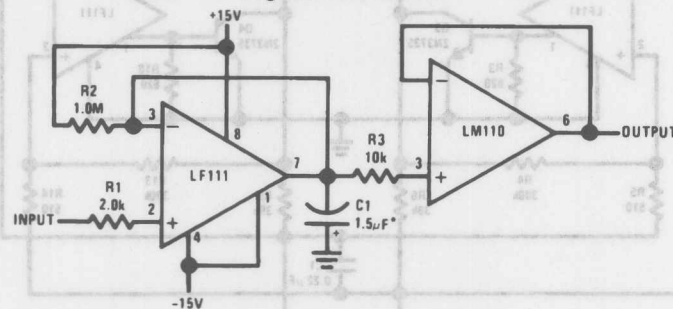
Positive Peak Detector



*Solid tantalum

TL/H/5703-19

Negative Peak Detector

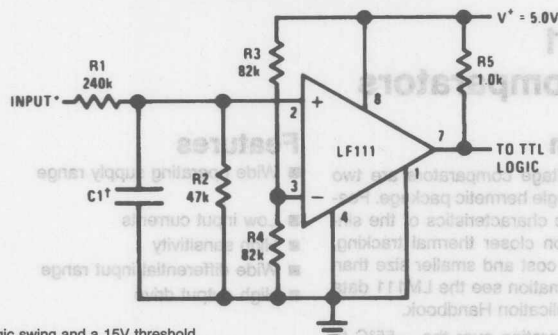


*Solid tantalum

TL/H/5703-20

Typical Applications (Continued)

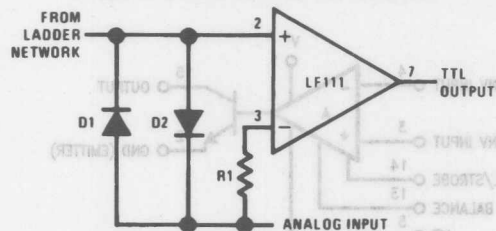
TTL Interface with High Level Logic



*Values shown are for a 0 to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes

Using Clamp Diodes to Improve Response



TL/H/5703-6



LH2111/LH2311 Dual Voltage Comparators

General Description

The LH2111 series of dual voltage comparators are two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, reduced insertion cost and smaller size than two singles. For additional information see the LM111 data sheet and National's Linear Application Handbook.

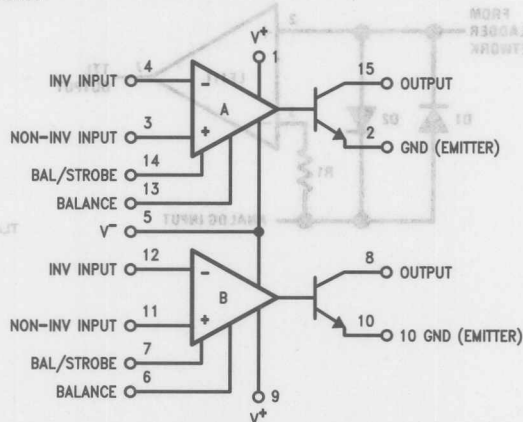
The LH2111 is specified for operation over the -55°C to $+125^{\circ}\text{C}$ military temperature range. The LH2311 is specified for operation over the 0°C to 70°C temperature range.

Features

- Wide operating supply range
- Low input currents
- High sensitivity
- Wide differential input range
- High output drive

$\pm 15\text{V}$ to a
single $+5\text{V}$
 6 nA
 $10\text{ }\mu\text{V}$
 $\pm 30\text{V}$
 50 mA , 50V

Connection Diagram



Order Number LH2111D, LH2111D/883 or LH2311D
See NS Package Number D16C

TL/K/10116-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-----------|
| Total Supply Voltage ($V^+ - V^-$) | 36V |
| Output to Negative Supply Voltage ($V_{OUT} - V^-$) | 50V |
| Ground to Negative Supply Voltage ($GND - V^-$) | 30V |
| Differential Input Voltage | $\pm 30V$ |

| | |
|--------------------------------------|---|
| Input Voltage (Note 1) | $\pm 15V$ |
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range LH2111 | -55°C to $+125^\circ\text{C}$ |
| LH2311 | 0°C to $+70^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Electrical Characteristics Each Side (Note 3)

| Parameter | Conditions | Limits | | Units |
|-------------------------------|---|----------|----------|----------|
| | | LH2111 | LH2311 | |
| Input Offset Voltage (Note 4) | $T_A = 25^\circ\text{C}$, $R_S \leq 50k$ | 3.0 | 7.5 | mV Max |
| Input Offset Current (Note 4) | $T_A = 25^\circ\text{C}$ | 10 | 50 | nA Max |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | 100 | 250 | nA Max |
| Voltage Gain | $T_A = 25^\circ\text{C}$ | 200 | 200 | V/mV Typ |
| Response Time (Note 5) | $T_A = 25^\circ\text{C}$ | 200 | 200 | ns Typ |
| Saturation Voltage | $V_{IN} \leq -5\text{ mV}$, $I_{OUT} = 50\text{ mA}$ $T_A = 25^\circ\text{C}$ | 1.5 | 1.5 | V Max |
| Strobe On Current | $T_A = 25^\circ\text{C}$ | 3.0 | 3.0 | mA Typ |
| Output Leakage Current | $V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35V$ $T_A = 25^\circ\text{C}$ | 10 | 50 | nA Max |
| Input Offset Voltage (Note 4) | $R_S \leq 50k$ | 4.0 | 10 | mV Max |
| Input Offset Current (Note 4) | | 20 | 70 | nA Max |
| Input Bias Current | | 150 | 300 | nA Max |
| Input Voltage Range | | ± 14 | ± 14 | V Typ |
| Saturation Voltage | $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5\text{ mV}$, $I_{SINK} \leq 8\text{ mA}$ | 0.4 | 0.4 | V Max |
| Positive Supply Current | $T_A = 25^\circ\text{C}$ | 6.0 | 7.5 | mA Max |
| Negative Supply Current | $T_A = 25^\circ\text{C}$ | 5.0 | 5.0 | mA Max |

Note 1: This rating applies for $\pm 15V$ supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

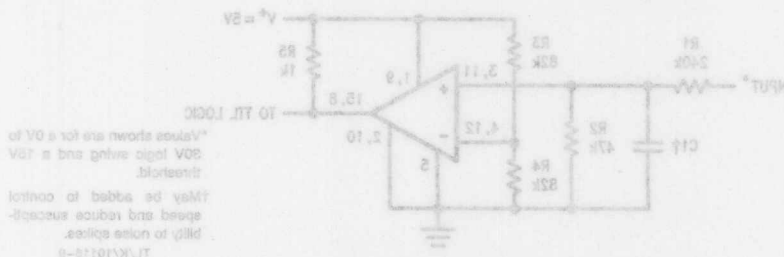
Note 2: The maximum junction temperature is 150°C . For operating at elevated temperatures, devices in the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a $1/16$ -inch-thick epoxy glass board with 0.03-inch-wide, 2 ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W , junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$ for the LH2111, and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to $\pm 15V$ supplies. For the LH2311, $V_{IN} = \pm 10\text{ mV}$.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

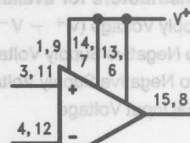
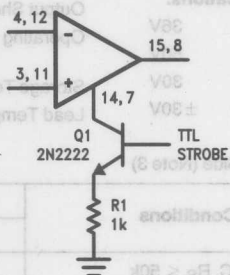
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

Note 6: RETS2111X for the LH2111D and LH2111F military specifications.



Strobing

Increasing Input Stage Current*



TL/K/10116-4

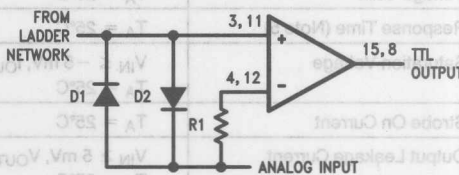
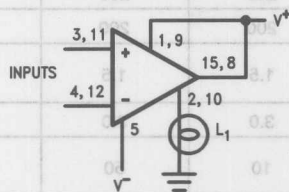
*Increases typical common mode slew from 7.0 V/ μ s to 18 V/ μ s

TI /K/10116-2

TI /K/10116-3

Driving Ground-Referenced Load

Using Clamp Diodes to Improve Responses

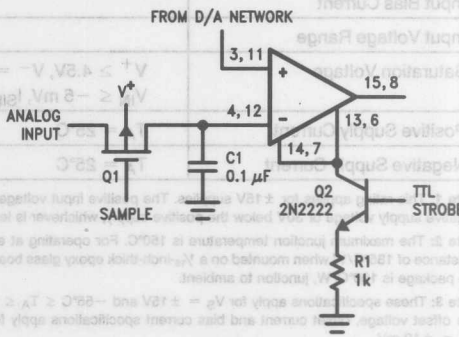
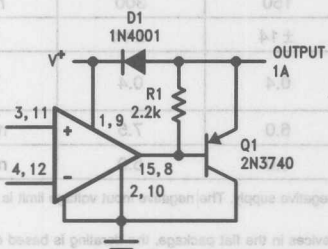


TL/K/10116-5

TL/K/10116-6

Comparator and Solenoid Driver

Strobing off Both Input* and Output Stages

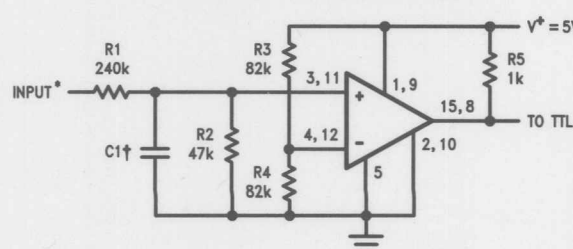


TL/K/10116-7

TL/K/10116-8

*Typical input current is 50 pA with inputs strobed off

TTL Interface with High Level Logic



*Values shown are for a 0V to 30V logic swing and a 15V threshold.

†May be added to control speed and reduce susceptibility to noise spikes.

TL/K/10116-9



LM106/LM306 Voltage Comparator

General Description

The LM106 series are high-speed voltage comparators designed to accurately detect low-level analog signals and drive a digital load. They are equivalent to an LM710, combined with a two input NAND gate and an output buffer. The circuits can drive RTL, DTL or TTL integrated circuits directly. Furthermore, their outputs can switch voltages up to 24V at currents as high as 10 mA.

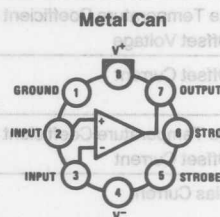
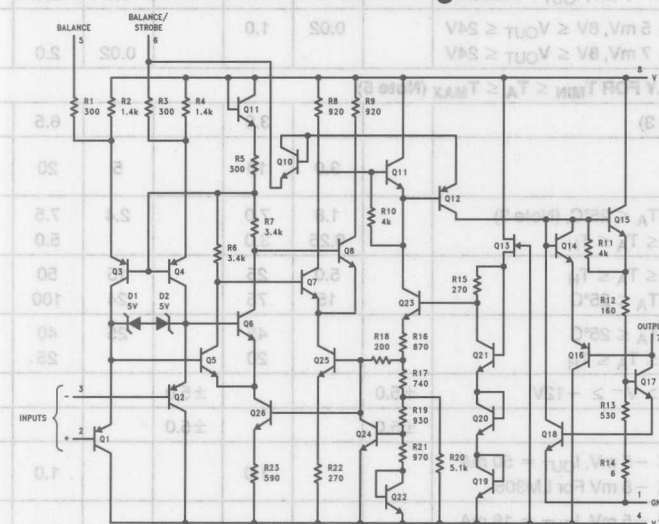
The devices have short-circuit protection which limits the inrush current when it is used to drive incandescent lamps, in addition to preventing damage from accidental shorts to the positive supply. The speed is equivalent to that of an LM710. However, they are even faster where buffers and additional logic circuitry can be eliminated by the increased flexibility of the LM106 series. They can also be operated from any negative supply voltage between -3V and -12V with little effect on performance.

The LM106 is specified for operation over the -55°C to +125°C military temperature range. The LM306 is specified for operation over 0°C to +70°C temperature range.

Features

- Improved accuracy
- Fan-out of 10 with DTL or TTL
- Added logic or strobe capability
- Useful as a relay or lamp driver
- Plug-in replacement for the LM710
- 40 ns maximum response time

Schematic and Connection Diagrams



Top View

Note: Pin 4 connected to case.

Order Number LM106H,
LM106H/883† or LM306H
See NS Package Number H08A

†Available per SMD# 8003701

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 6)

| | |
|-----------------------------------|------|
| Positive Supply Voltage | 15V |
| Negative Supply Voltage | -15V |
| Output Voltage | 24V |
| Output to Negative Supply Voltage | 30V |
| Differential Input Voltage | ±5V |
| Input Voltage | ±7V |

Power Dissipation (Note 1) 600 mW
Output Short Circuit Duration 10 seconds

Operating Temperature Range
LM106 T_{MIN} T_{MAX}
LM306 -55°C to +125°C
0°C to +70°C

Storage Temperature Range -65°C to +150°C

Lead Temperature (Soldering, 10 sec.) 300°C

ESD rating to be determined.

Electrical Characteristics (Note 2)

| Parameter | Conditions | LM106 | | | LM306 | | | Units |
|------------------------|--|-------|------|-----|-------|-----|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 3) | | 0.5 | 2.0 | 1.6 | 5.0 | | mV |
| Input Offset Current | (Note 3) | | 0.7 | 3.0 | 1.8 | 5.0 | | μA |
| Input Bias Current | | | 10 | 20 | 16 | 25 | | μA |
| Response Time | $R_L = 390\Omega$ to 5V $C_L = 15$ pF, (Note 4) | | 28 | 40 | 28 | 40 | | ns |
| Saturation Voltage | $V_{IN} \leq -5$ mV, $I_{OUT} = 100$ mA $V_{IN} \leq -7$ mV, $I_{OUT} = 100$ mA | | 1.0 | 1.5 | 0.8 | 2.0 | | V |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$ $V_{IN} \geq 7$ mV, $8V \leq V_{OUT} \leq 24V$ | | 0.02 | 1.0 | 0.02 | 2.0 | | μA |

THE FOLLOWING SPECIFICATIONS APPLY FOR $T_{MIN} \leq T_A \leq T_{MAX}$ (Note 5)

| | | | | | | | | |
|---|---|------|-------------|------------|------|----------|------------|----------------|
| Input Offset Voltage | (Note 3) | | | 3.0 | | | 6.5 | mV |
| Average Temperature Coefficient of Input Offset Voltage | | | 3.0 | 10 | | 5 | 20 | μV/°C |
| Input Offset Current | $T_L \leq T_A \leq 25^\circ\text{C}$, (Note 3) $25^\circ\text{C} \leq T_A \leq T_H$ | | 1.8 0.25 | 7.0 3.0 | | 2.4 | 7.5 5.0 | μA μA |
| Average Temperature Coefficient of Input Offset Current | $25^\circ\text{C} \leq T_A \leq T_H$ $T_L \leq T_A \leq 25^\circ\text{C}$ | | 5.0 15 | 25 75 | | 15 24 | 50 100 | nA/°C nA/°C |
| Input Bias Current | $T_L \leq T_A \leq 25^\circ\text{C}$ $25^\circ\text{C} \leq T_A \leq T_H$ | | | 45 20 | | 25 | 40 25 | μA μA |
| Input Voltage Range | $-7V \geq V^- \geq -12V$ | ±5.0 | | | ±5.0 | | | V |
| Differential Input Voltage Range | | ±5.0 | | | ±5.0 | | | V |
| Saturation Voltage | $V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $V_{IN} \leq -8$ mV For LM306 | | | 1.0 | | | 1.0 | V |
| Saturation Voltage | $V_{IN} \leq -5$ mV, $I_{OUT} = 16$ mA $V_{IN} \leq -8$ mV For LM306 | | | 0.4 | | | 0.4 | V |
| Positive Output Level | $V_{IN} \geq 5$ mV, $I_{OUT} = -400\mu\text{A}$ $V_{IN} \geq 8$ mV For LM306 | 2.5 | | 5.5 | 2.5 | | 5.5 | V |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $8V \leq V_{OUT} \leq 24V$ $V_{IN} \geq 8$ mV For LM306 $T_L \leq T_A \leq 25^\circ\text{C}$ $25^\circ\text{C} < T_A \leq T_H$ | | | 1.0 100 | | | 2.0 100 | μA μA |
| Strobe Current | $V_{STROBE} = 0.4V$ | | -1.7 | -3.2 | | -1.7 | -3.2 | mA |

Electrical Characteristics (Note 2) (Continued)

| Parameter | Conditions | LM106 | | | LM306 | | | Units |
|-------------------------|--|-------|------|-----|-------|------|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Strobe "ON" Voltage | | 0.9 | 1.4 | | 0.9 | 1.4 | | V |
| Strobe "OFF" Voltage | $I_{SINK} \leq 16 \text{ mA}$ | | 1.4 | 2.2 | | 1.4 | 2.2 | V |
| Positive Supply Current | $V_{IN} = -5 \text{ mV}$ $V_{IN} = -8 \text{ mV}$ for LM306 | | 5.5 | 10 | | 5.5 | 10 | mA |
| Negative Supply Current | | -1.5 | -3.6 | | -1.5 | -3.6 | | mA |

Note 1: The maximum junction temperature of LM106 is 150°C, LM306 is 85°C. For operating at elevated temperatures, devices must be derated based on a thermal resistance of 170°C/W, junction to ambient, or 23°C/W, junction to case.

Note 2: These specifications apply for $-3V \geq V^- \geq -12V$, $V^+ = 12V$ and $T_A = 25^\circ\text{C}$ unless otherwise specified. All currents into device pins are considered positive.

Note 3: The offset voltages and offset currents given are the maximum values required to drive the output down to 0.5V or up to 4.4V (0.5V or up to 4.8V for the LM306). Thus, these parameters actually define an error band and take into account the worst-case effects of voltage gain, specified supply voltage variations, and common mode voltage variations.

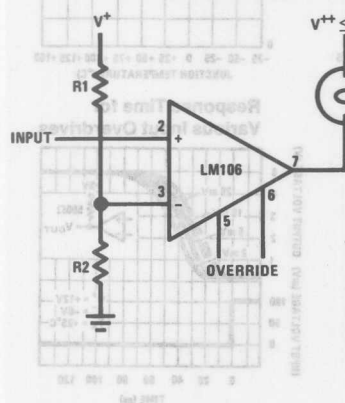
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 5: All currents into device pins are considered positive.

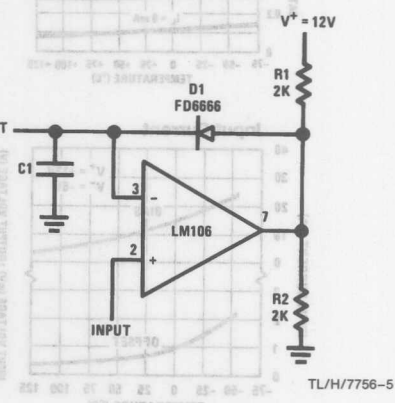
Note 6: Refer to RETS106X for LM106 military specifications.

Typical Applications

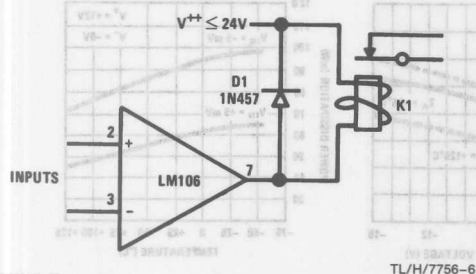
Level Detector and Lamp Driver



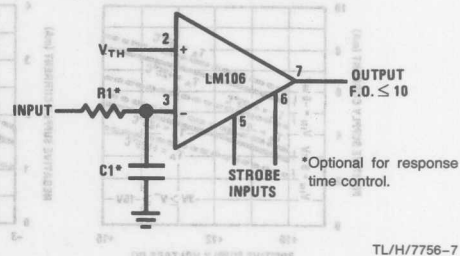
Fast Response Peak Detector



Relay Driver

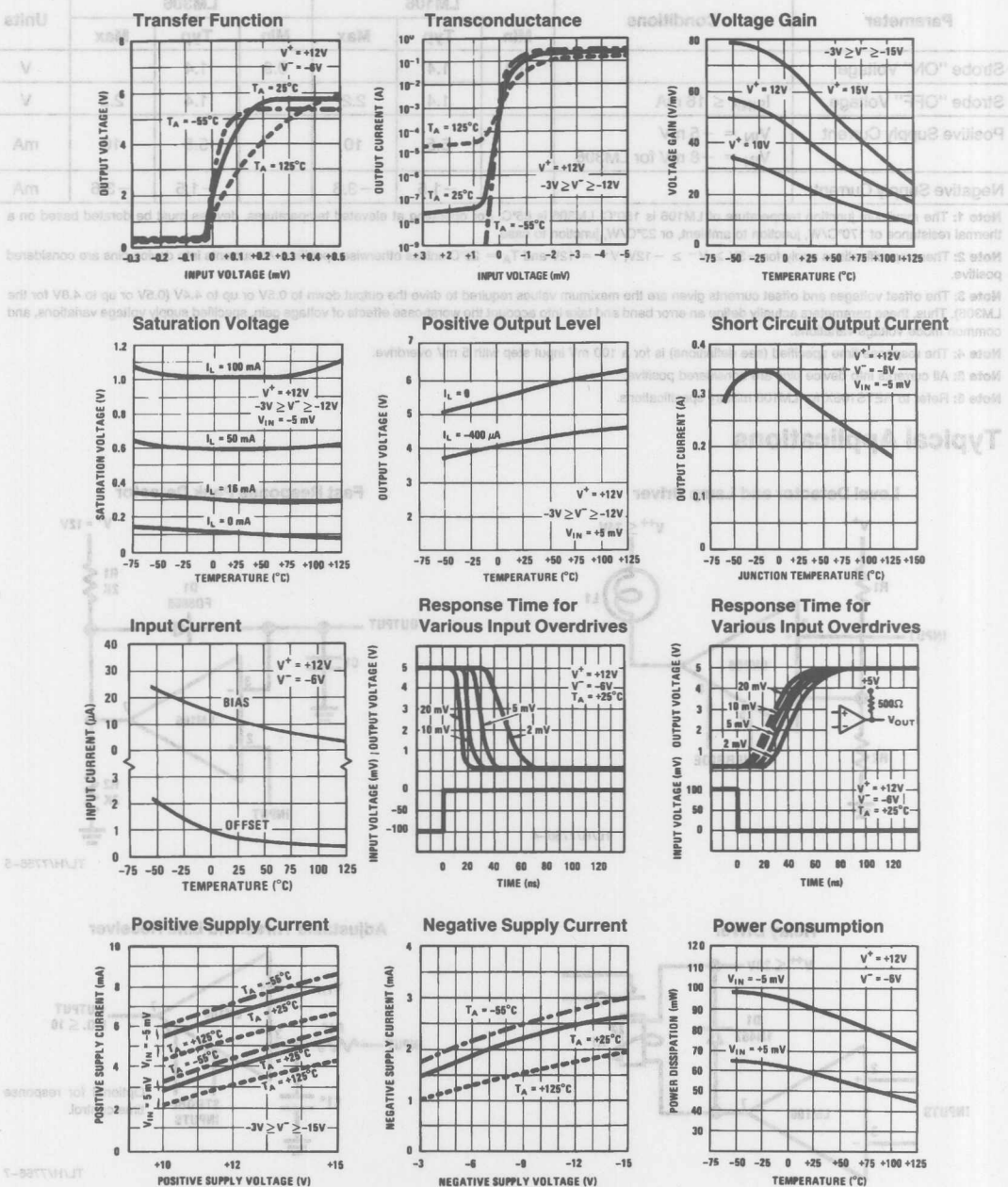


Adjustable Threshold Line Receiver



*Optional for response time control.

Typical Performance Characteristics



TL/H/7756-8

LM111/LM211/LM311 Voltage Comparator

General Description

The LM111, LM211 and LM311 are voltage comparators that have input currents nearly a thousand times lower than devices like the LM106 or LM710. They are also designed to operate over a wider range of supply voltages: from standard $\pm 15V$ op amp supplies down to the single 5V supply used for IC logic. Their output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, they can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the outputs of the LM111, LM211 or the LM311 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs

40 ns) the devices are also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

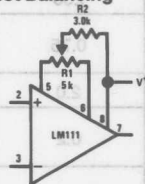
The LM211 is identical to the LM111, except that its performance is specified over a $-25^{\circ}C$ to $+85^{\circ}C$ temperature range instead of $-55^{\circ}C$ to $+125^{\circ}C$. The LM311 has a temperature range of $0^{\circ}C$ to $+70^{\circ}C$.

Features

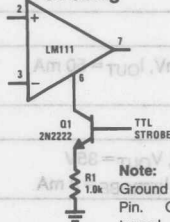
- Operates from single 5V supply
- Input current: 150 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: $\pm 30V$
- Power consumption: 135 mW at $\pm 15V$

Typical Applications**

Offset Balancing

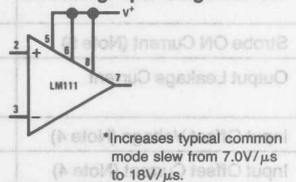


Strobing

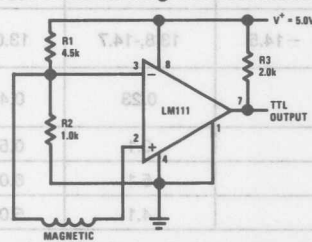


**Note: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

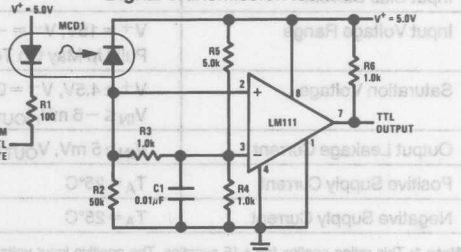
Increasing Input Stage Current*



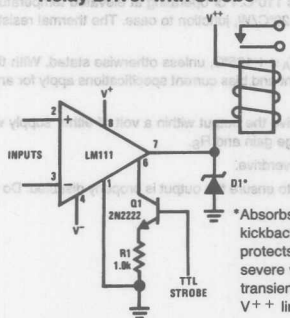
Detector for Magnetic Transducer



Digital Transmission Isolator

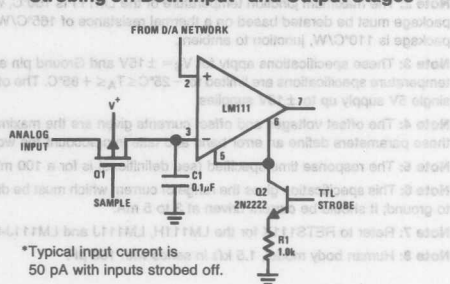


Relay Driver with Strobe



Note: Do Not Ground Strobe Pin.

Strobing off Both Input* and Output Stages



Note: Do Not Ground Strobe Pin.

TL/H/5704-1

Absolute Maximum Ratings for the LM111/LM211

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

| | |
|--|----------------------------------|
| Total Supply Voltage (V_{S4}) | 36V |
| Output to Negative Supply Voltage (V_{74}) | 50V |
| Ground to Negative Supply Voltage (V_{14}) | 30V |
| Differential Input Voltage | $\pm 30V$ |
| Input Voltage (Note 1) | $\pm 15V$ |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range LM111 | $-55^{\circ}C$ to $125^{\circ}C$ |
| LM211 | $-25^{\circ}C$ to $85^{\circ}C$ |

Lead Temperature (Soldering, 10 sec) $260^{\circ}C$
Voltage at Strobe Pin $V^{+} - 5V$

Soldering Information
Dual-In-Line Package

Soldering (10 seconds) $260^{\circ}C$

Small Outline Package

Vapor Phase (60 seconds) $215^{\circ}C$

Infrared (15 seconds) $220^{\circ}C$

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Rating (Note 8) 300V

Electrical Characteristics for the LM111 and LM211 (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------|--|-------|------------|------|---------|
| Input Offset Voltage (Note 4) | $T_A = 25^{\circ}C$, $R_S \leq 50k$ | | 0.7 | 3.0 | mV |
| Input Offset Current | $T_A = 25^{\circ}C$ | | 4.0 | 10 | nA |
| Input Bias Current | $T_A = 25^{\circ}C$ | | 60 | 100 | nA |
| Voltage Gain | $T_A = 25^{\circ}C$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25^{\circ}C$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA $T_A = 25^{\circ}C$ | | 0.75 | 1.5 | V |
| Strobe ON Current (Note 6) | $T_A = 25^{\circ}C$ | | 2.0 | 5.0 | mA |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ $T_A = 25^{\circ}C$, $I_{STROBE} = 3$ mA | | 0.2 | 10 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50$ k | | | 4.0 | mV |
| Input Offset Current (Note 4) | | | | 20 | nA |
| Input Bias Current | | | | 150 | nA |
| Input Voltage Range | $V^{+} = 15V$, $V^{-} = -15V$, Pin 7 Pull-Up May Go To 5V | -14.5 | 13.8, 14.7 | 13.0 | V |
| Saturation Voltage | $V^{+} \geq 4.5V$, $V^{-} = 0$ $V_{IN} \leq -6$ mV, $I_{OUT} \leq 8$ mA | | 0.23 | 0.4 | V |
| Output Leakage Current | $V_{IN} \geq 5$ mV, $V_{OUT} = 35V$ | | 0.1 | 0.5 | μA |
| Positive Supply Current | $T_A = 25^{\circ}C$ | | 5.1 | 6.0 | mA |
| Negative Supply Current | $T_A = 25^{\circ}C$ | | 4.1 | 5.0 | mA |

Note 1: This rating applies for ± 15 supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM111 is $150^{\circ}C$, while that of the LM211 is $110^{\circ}C$. For operating at elevated temperatures, devices in the H08 package must be derated based on a thermal resistance of $165^{\circ}C/W$, junction to ambient, or $20^{\circ}C/W$, junction to case. The thermal resistance of the dual-in-line package is $110^{\circ}C/W$, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Ground pin at ground, and $-55^{\circ}C \leq T_A \leq +125^{\circ}C$, unless otherwise stated. With the LM211, however, all temperature specifications are limited to $-25^{\circ}C \leq T_A \leq +85^{\circ}C$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to $\pm 15V$ supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S .

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

Note 7: Refer to RETS111X for the LM111H, LM111J and LM111J-8 military specifications.

Note 8: Human body model, 1.5 k Ω in series with 100 pF.

Absolute Maximum Ratings for the LM311

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------|
| Total Supply Voltage (V_{84}) | 36V |
| Output to Negative Supply Voltage (V_{74}) | 40V |
| Ground to Negative Supply Voltage (V_{14}) | 30V |
| Differential Input Voltage | $\pm 30V$ |
| Input Voltage (Note 1) | $\pm 15V$ |
| Power Dissipation (Note 2) | 500 mW |
| ESD Rating (Note 7) | 300V |

| | |
|--------------------------------------|----------------|
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range | 0° to 70°C |
| Storage Temperature Range | -65°C to 150°C |
| Lead Temperature (soldering, 10 sec) | 260°C |
| Voltage at Strobe Pin | $V^+ - 5V$ |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics for the LM311 (Note 3)

| Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------|---|-------|-------------|------|-------|
| Input Offset Voltage (Note 4) | $T_A = 25^\circ\text{C}$, $R_S \leq 50k$ | | 2.0 | 7.5 | mV |
| Input Offset Current (Note 4) | $T_A = 25^\circ\text{C}$ | | 6.0 | 50 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 100 | 250 | nA |
| Voltage Gain | $T_A = 25^\circ\text{C}$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25^\circ\text{C}$ | | 200 | | ns |
| Saturation Voltage | $V_{IN} \leq -10 \text{ mV}$, $I_{OUT} = 50 \text{ mA}$ $T_A = 25^\circ\text{C}$ | | 0.75 | 1.5 | V |
| Strobe ON Current (Note 6) | $T_A = 25^\circ\text{C}$ | | 2.0 | 5.0 | mA |
| Output Leakage Current | $V_{IN} \geq 10 \text{ mV}$, $V_{OUT} = 35V$ $T_A = 25^\circ\text{C}$, $I_{STROBE} = 3 \text{ mA}$ $V^- = \text{Pin 1} = -5V$ | | 0.2 | 50 | nA |
| Input Offset Voltage (Note 4) | $R_S \leq 50K$ | | | 10 | mV |
| Input Offset Current (Note 4) | | | | 70 | nA |
| Input Bias Current | | | | 300 | nA |
| Input Voltage Range | | -14.5 | 13.8, -14.7 | 13.0 | V |
| Saturation Voltage | $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10 \text{ mV}$, $I_{OUT} \leq 8 \text{ mA}$ | | 0.23 | 0.4 | V |
| Positive Supply Current | $T_A = 25^\circ\text{C}$ | | 5.1 | 7.5 | mA |
| Negative Supply Current | $T_A = 25^\circ\text{C}$ | | 4.1 | 5.0 | mA |

Note 1: This rating applies for $\pm 15V$ supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LM311 is 110°C. For operating at elevated temperature, devices in the H08 package must be derated based on a thermal resistance of 165°C/W, junction to ambient, or 20°C/W, junction to case. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$ and Pin 1 at ground, and $0^\circ\text{C} < T_A < +70^\circ\text{C}$, unless otherwise specified. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to $\pm 15V$ supplies.

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and R_S .

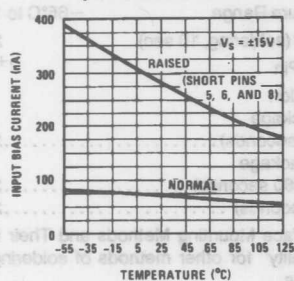
Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 to 5 mA.

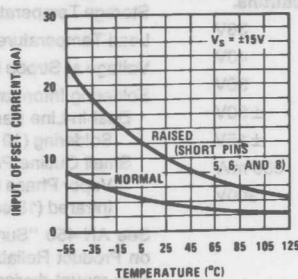
Note 7: Human body model, 1.5 k Ω in series with 100 pF.

LM111/LM211 Typical Performance Characteristics

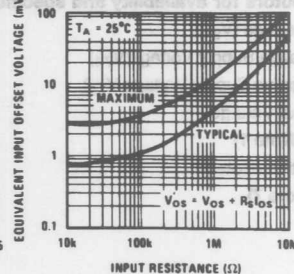
Input Bias Current



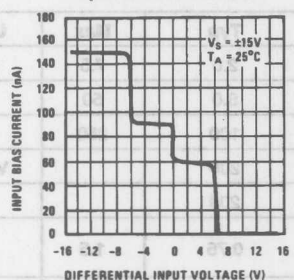
Input Offset Current



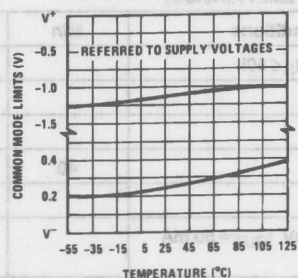
Offset Error



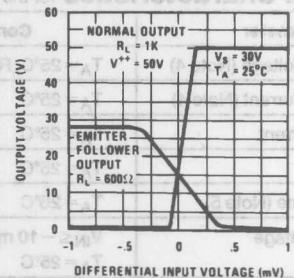
Input Characteristics



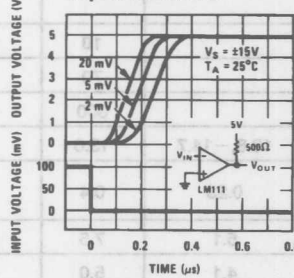
Common Mode Limits



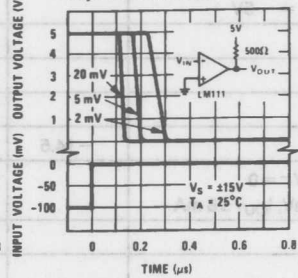
Transfer Function



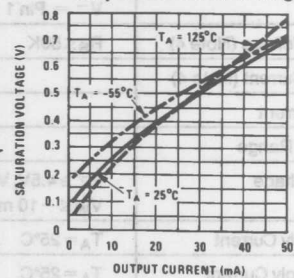
Response Time for Various Input Overdrives



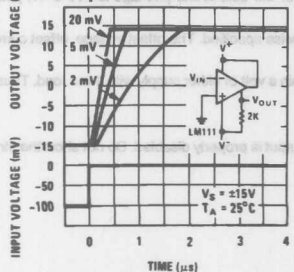
Response Time for Various Input Overdrives



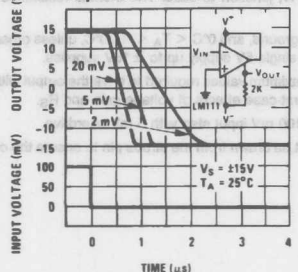
Output Saturation Voltage



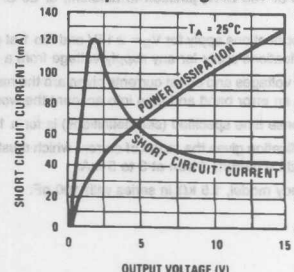
Response Time for Various Input Overdrives



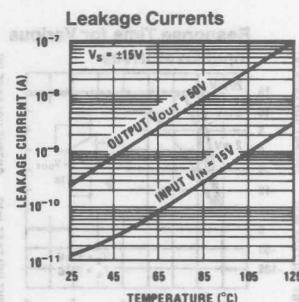
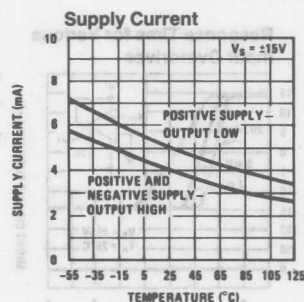
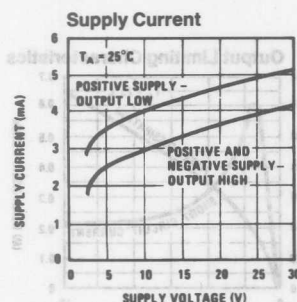
Response Time for Various Input Overdrives



Output Limiting Characteristics

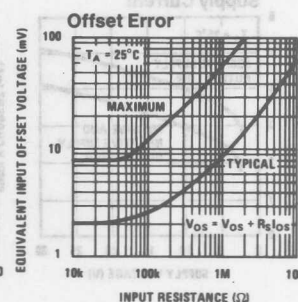
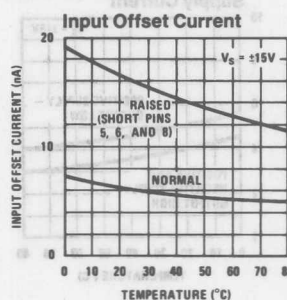
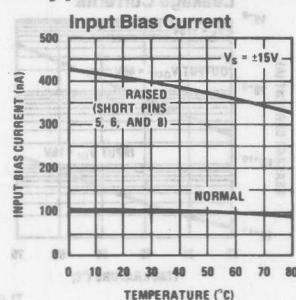


LM111/LM211 Typical Performance Characteristics (Continued)

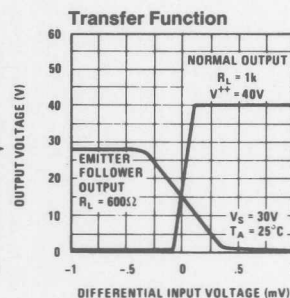
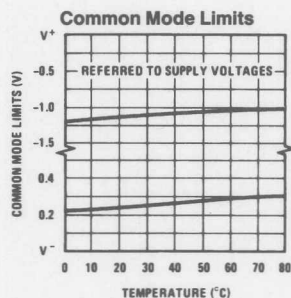
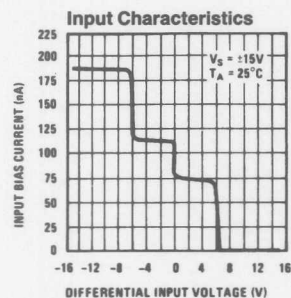


TL/H/5704-3

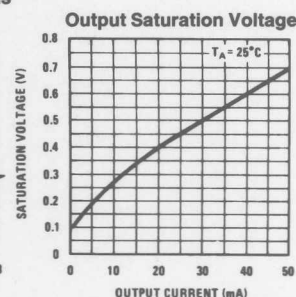
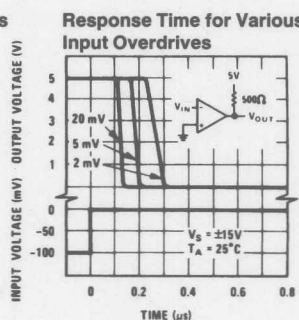
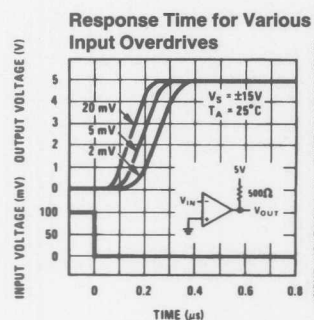
LM311 Typical Performance Characteristics



TL/H/5704-8

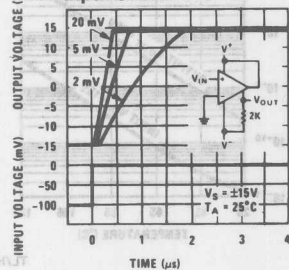


TL/H/5704-9

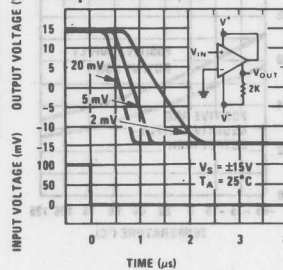


TL/H/5704-10

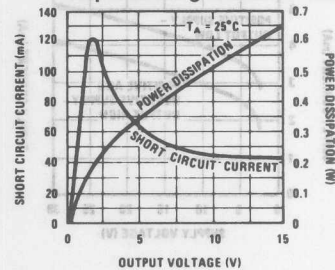
Response Time for Various Input Overdrives



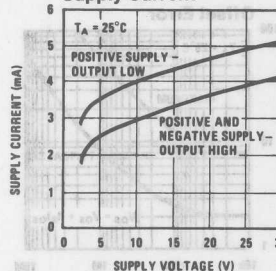
Response Time for Various Input Overdrives



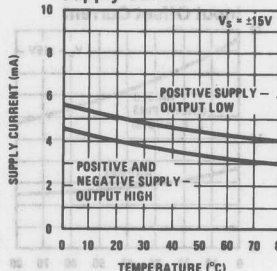
Output Limiting Characteristics



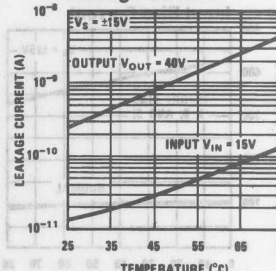
Supply Current



Supply Current



Leakage Currents



TL/H/5704-11

TL/H/5704-12

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

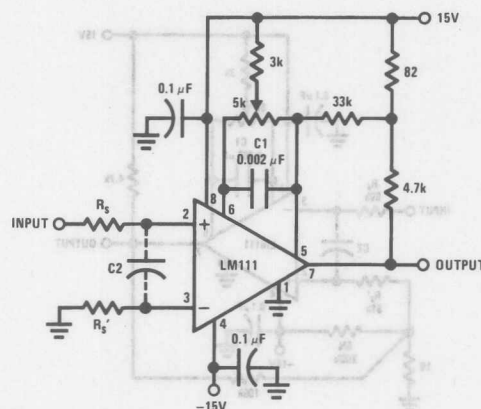
When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 μ F disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 k Ω to 100 k Ω), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in Figure 1 below.

1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 μ F capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in Figure 1.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S , it is usually advantageous to choose an R_S' of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wirewound resistors are not suitable.

4. When comparator circuits use input resistors (eg. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if $R_S = 10$ k Ω , as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.

5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a groundplane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 μ F capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)



Pin connections shown are for LM111H in the H08 hermetic package

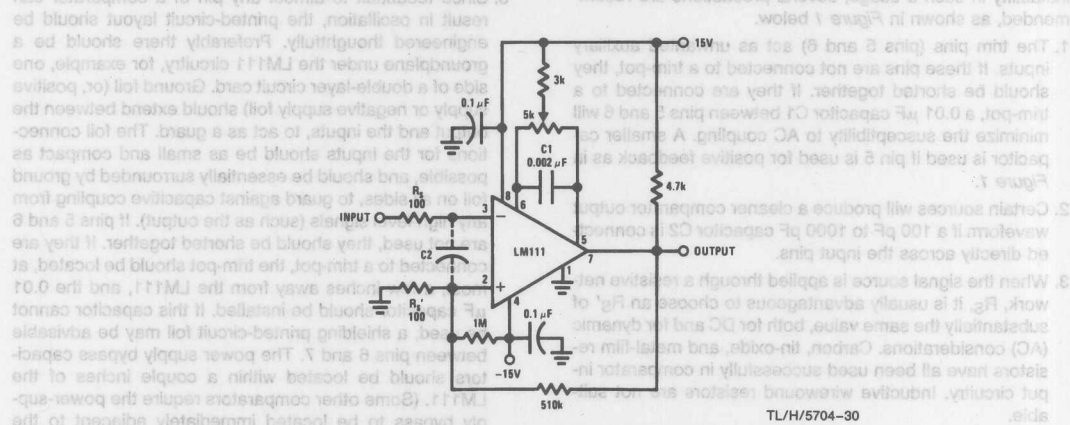
FIGURE 1. Improved Positive Feedback

Application Hints (Continued)

6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω , such as $50\text{ k}\Omega$, it would not be reasonable to simply increase the value of the positive feedback resistor above $510\text{ k}\Omega$. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive

feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the $5\text{ k}\Omega$ pot and $3\text{ k}\Omega$ resistor as shown.

8. These application notes apply specifically to the LM111, LM211, LM311, and LF111 families of comparators, and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

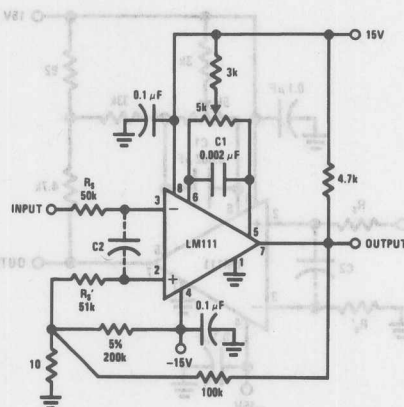
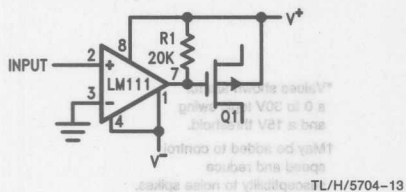


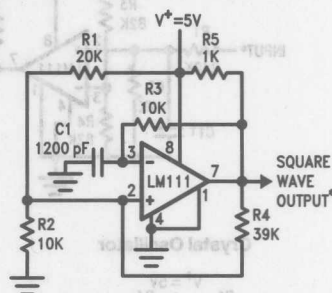
FIGURE 3. Positive Feedback with High Source Resistance

Typical Applications (Continued) (Pin numbers refer to H08 package)

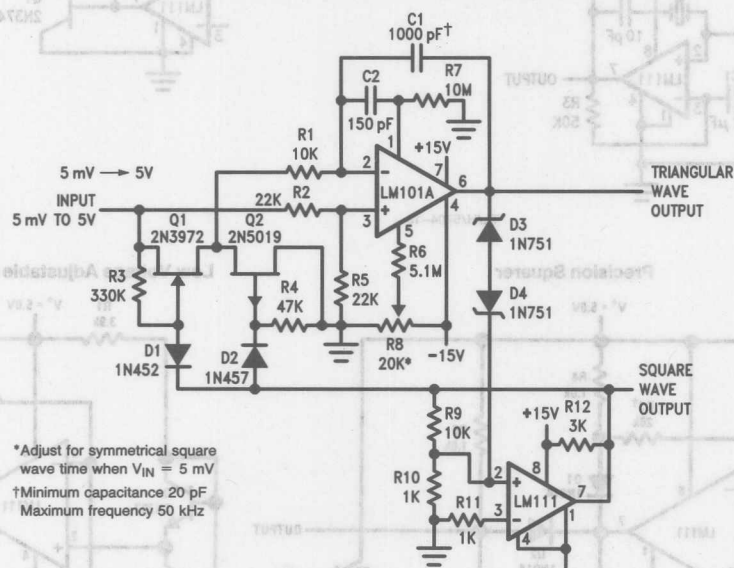
Zero Crossing Detector Driving MOS Switch



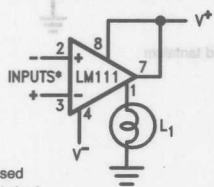
100 kHz Free Running Multivibrator



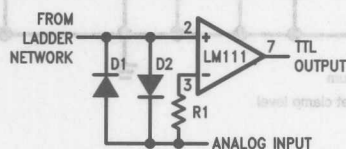
10 Hz to 10 kHz Voltage Controlled Oscillator

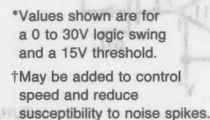


Driving Ground-Referred Load

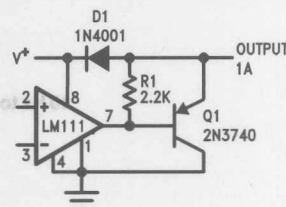


Using Clamp Diodes to Improve Response



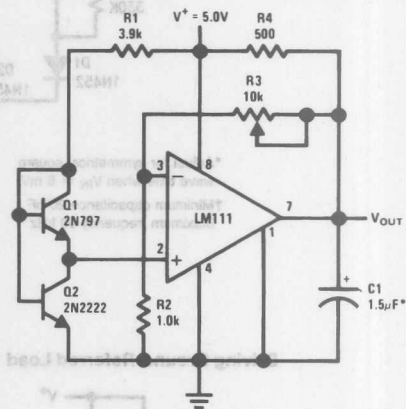


Comparator and Solenoid Driver



TL/H/5704-19

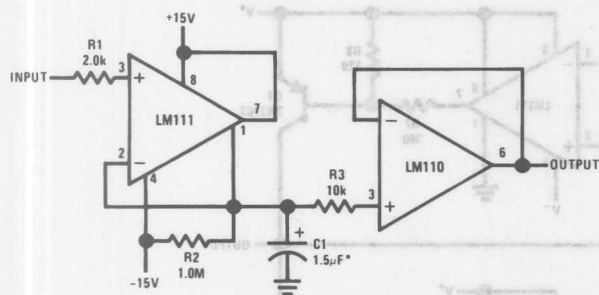
Low Voltage Adjustable Reference Supply



*Solid tantalum

TL/H/5704-22

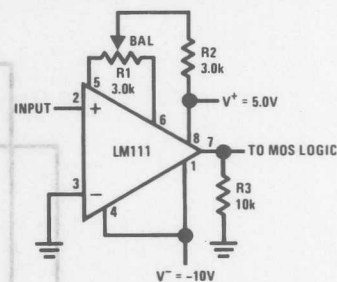
Positive Peak Detector



*Solid tantalum

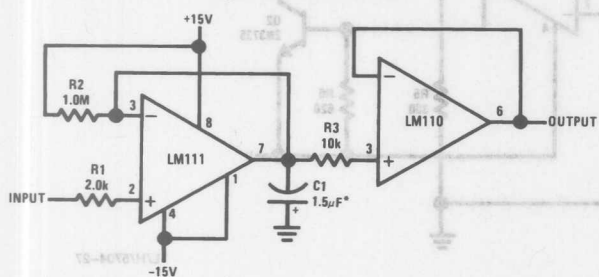
TL/H/5704-23

Zero Crossing Detector Driving MOS Logic



TL/H/5704-24

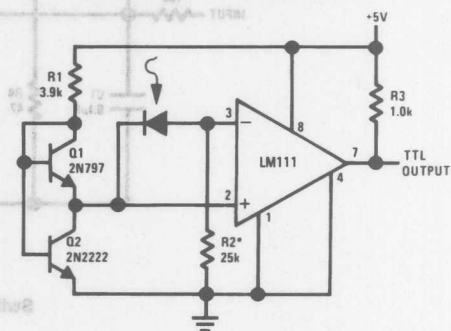
Negative Peak Detector



*Solid tantalum

TL/H/5704-25

Precision Photodiode Comparator

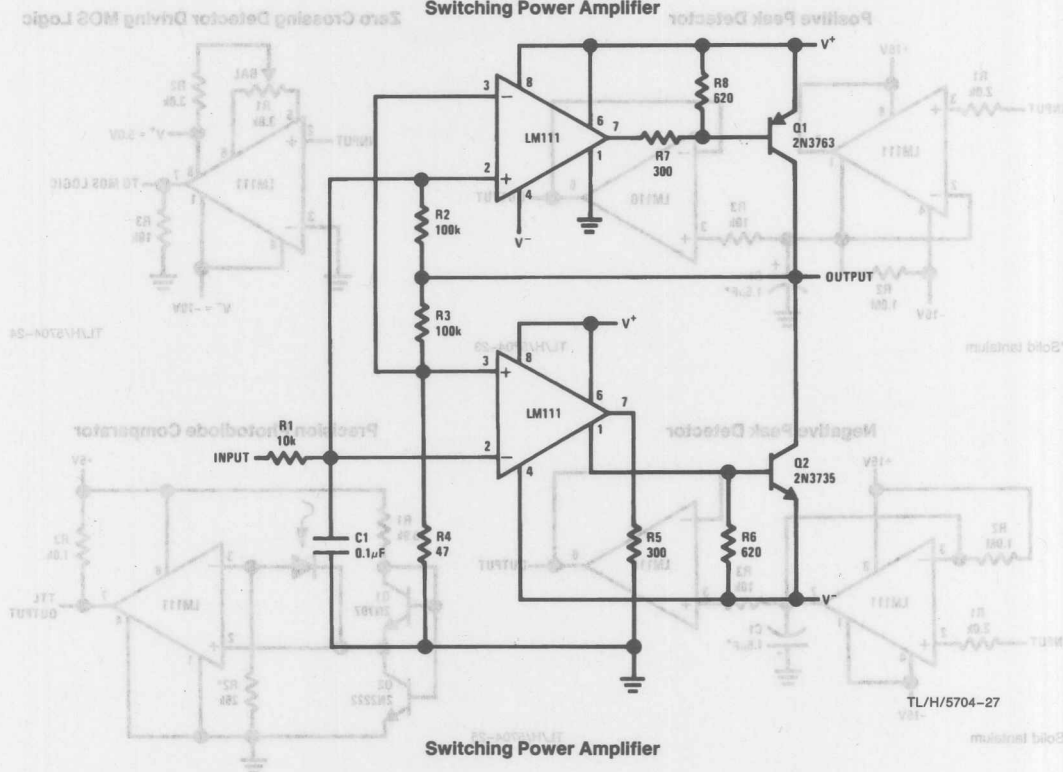


TL/H/5704-26

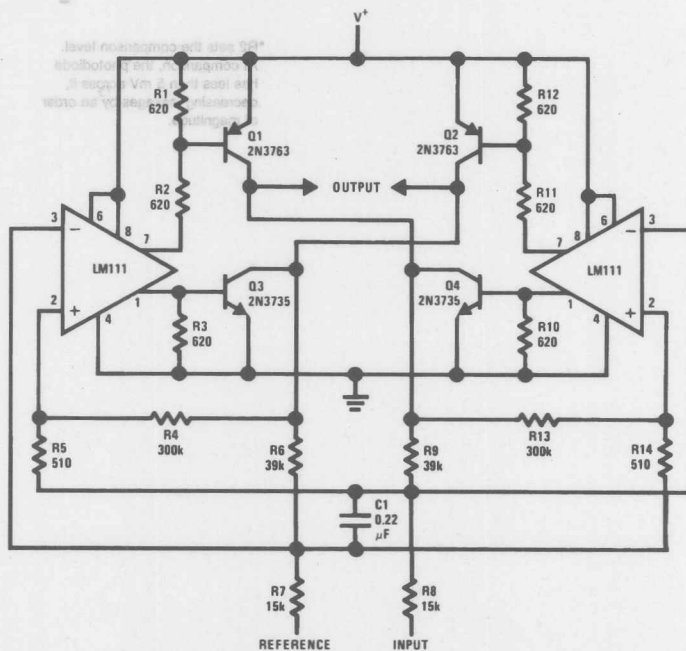
*R2 sets the comparison level.
At comparison, the photodiode
has less than 5 mV across it,
decreasing leakages by an order
of magnitude.

Typical Applications (Continued) (Pin numbers refer to H08 package)

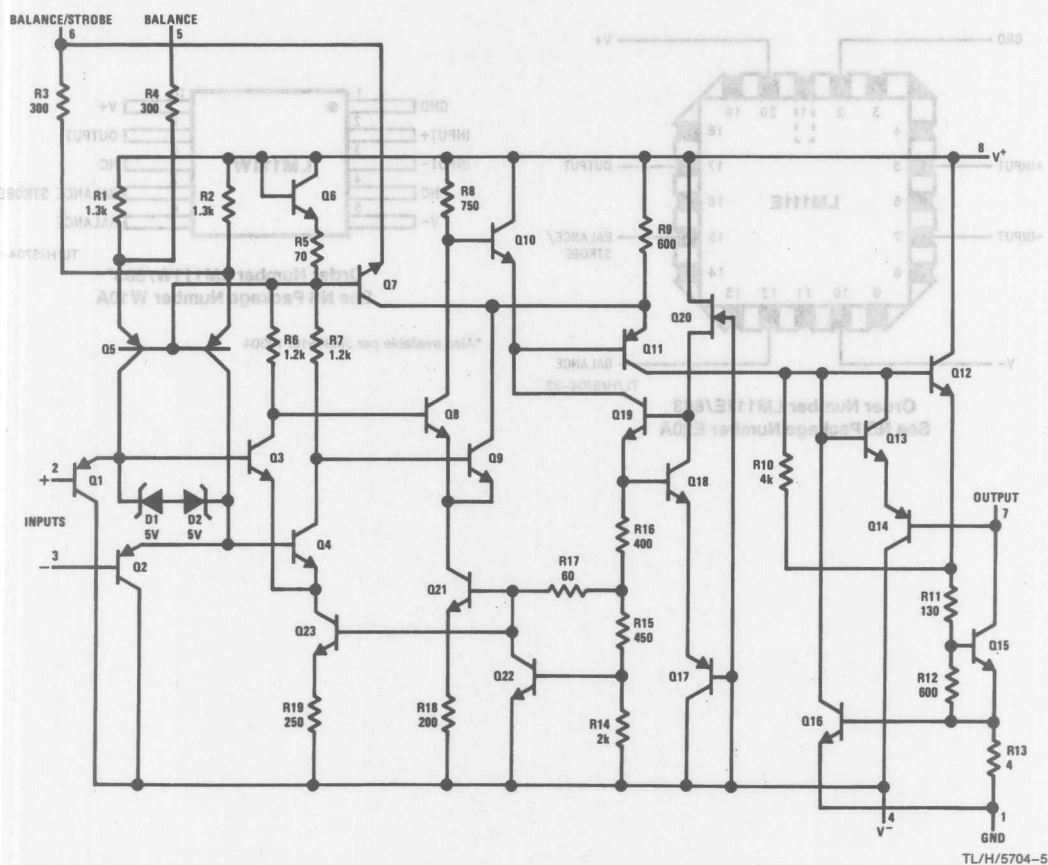
Switching Power Amplifier



Switching Power Amplifier



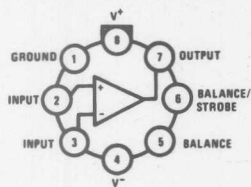
Schematic Diagram**



**Pin connections shown on schematic diagram are for H08 package.

Connection Diagrams*

Metal Can Package

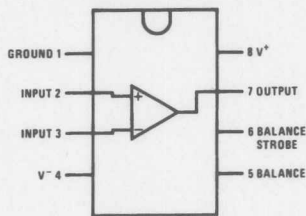


Top View

Note: Pin 4 connected to case

Order Number LM111H,
LM111H/883*, LM211H or LM311H
See NS Package Number H08C

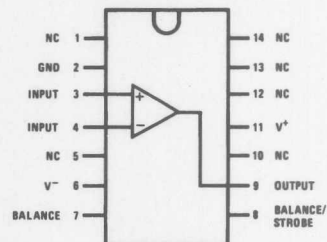
Dual-In-Line Package



Top View

Order Number LM111J-8, LM111J-
8/883*, LM211J-8, LM211M,
LM311M or LM311N
See NS Package Number J08A,
M08A or N08E

Dual-In-Line Package

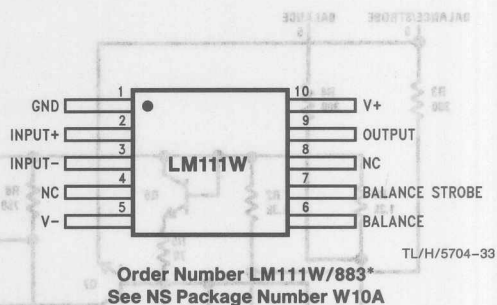
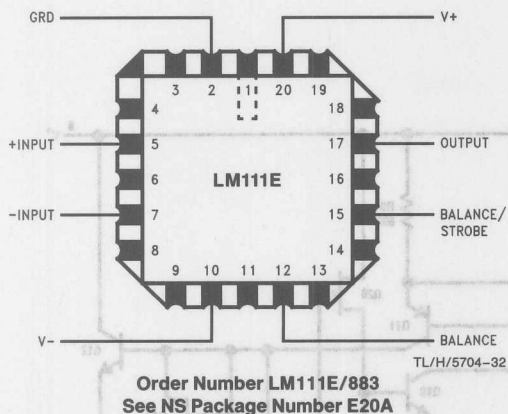


Top View

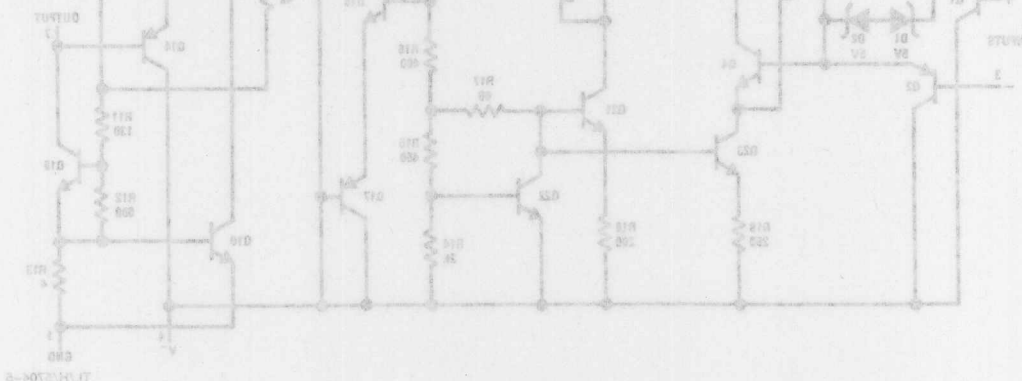
Order Number LM111J/883* or
LM311N-14
See NS Package Number
J14A or N14A

*Also available per JM38510/10304

Connection Diagrams (Continued)

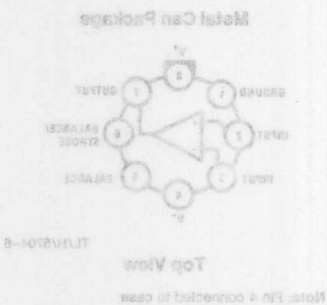


*Also available per JM38510/10304

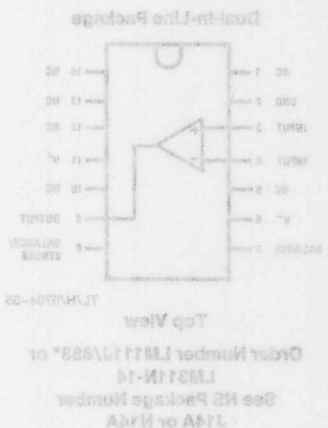
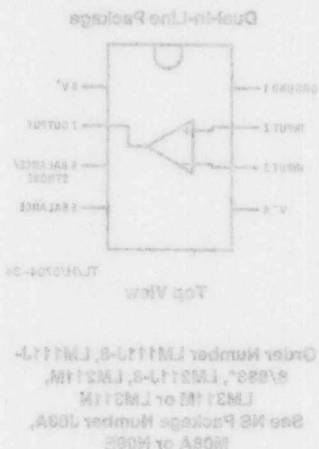


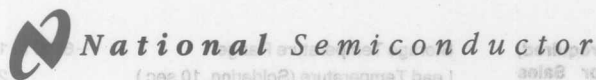
*Pin connections shown on schematic diagram are for HCB package.

Connection Diagrams



*Also available per JM38510/10304





LM119/LM219/LM319 High Speed Dual Comparator

General Description

The LM119 series are precision high speed dual comparators fabricated on a single monolithic chip. They are designed to operate over a wide range of supply voltages down to a single 5V logic supply and ground. Further, they have higher gain and lower input currents than devices like the LM710. The uncommitted collector of the output stage makes the LM119 compatible with RTL, DTL and TTL as well as capable of driving lamps and relays at currents up to 25 mA.

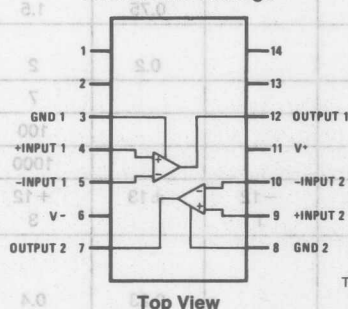
The LM319A offers improved precision over the standard LM319, with tighter tolerances on offset voltage, offset current, and voltage gain.

Features

- Two independent comparators
- Operates from a single 5V supply

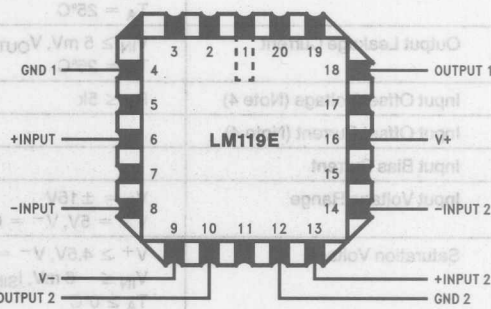
Connection Diagrams

Dual-In-Line-Package



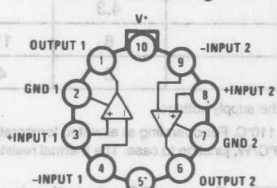
Top View

Order Number LM119J, LM119J/883*, LM219J,
LM319J, LM319AM, LM319M, LM319AN or LM319N
See NS Package Number J14A, M14A or N14A



Order Number LM119E/883
See NS Package Number E20A

Metal Can Package



Top View

Order Number LM119H, LM119H/883*, or LM319H
See NS Package Number H10C

*Also available per SMD # 8601401 or JM38510/10306

- Typically 80 ns response time at $\pm 15V$
- Minimum fan-out of 2 each side
- Maximum input current of $1 \mu A$ over temperature
- Inputs and outputs can be isolated from system ground
- High common mode slew rate

Although designed primarily for applications requiring operation from digital logic supplies, the LM119 series are fully specified for power supplies up to $\pm 15V$. It features faster response than the LM111 at the expense of higher power dissipation. However, the high speed, wide operating voltage range and low package count make the LM119 much more versatile than older devices like the LM711.

The LM119 is specified from $-55^\circ C$ to $+125^\circ C$, the LM219 is specified from $-25^\circ C$ to $+85^\circ C$, and the LM319A and LM319 are specified from $0^\circ C$ to $+70^\circ C$.

LM119/LM219/LM319

please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 7)

| | |
|---|-----------|
| Total Supply Voltage | 36V |
| Output to Negative Supply Voltage | 36V |
| Ground to Negative Supply Voltage | 25V |
| Ground to Positive Supply Voltage | 18V |
| Differential Input Voltage | $\pm 5V$ |
| Input Voltage (Note 1) | $\pm 15V$ |
| ESD rating (1.5 k Ω in series with 100 pF) | 800V |
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |

Lead Temperature (Soldering, 10 sec.)

260°C

Soldering Information

Dual-In-Line Package

Soldering (10 seconds)

260°C

Small Outline Package

Vapor Phase (60 seconds)

215°C

Infrared (15 seconds)

220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Operating Temperature Range

LM119

-55°C to 125°C

LM219

-25°C to 85°C

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM119/LM219 | | | Units |
|-------------------------------|---|-------------|----------|------------|---------------|
| | | Min | Typ | Max | |
| Input Offset Voltage (Note 4) | $T_A = 25^\circ\text{C}$, $R_S \leq 5k$ | | 0.7 | 4.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25^\circ\text{C}$ | | 30 | 75 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 150 | 500 | nA |
| Voltage Gain | $T_A = 25^\circ\text{C}$ (Note 6) | 10 | 40 | | V/mV |
| Response Time (Note 5) | $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$ | | 80 | | ns |
| Saturation Voltage | $V_{IN} \leq -5\text{ mV}$, $I_{OUT} = 25\text{ mA}$ $T_A = 25^\circ\text{C}$ | | 0.75 | 1.5 | V |
| Output Leakage Current | $V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35V$ $T_A = 25^\circ\text{C}$ | | 0.2 | 2 | μA |
| Input Offset Voltage (Note 4) | $R_S \leq 5k$ | | | 7 | mV |
| Input Offset Current (Note 4) | | | | 100 | nA |
| Input Bias Current | | | | 1000 | nA |
| Input Voltage Range | $V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$ | -12 1 | ± 13 | +12 3 | V |
| Saturation Voltage | $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -6\text{ mV}$, $I_{SINK} \leq 3.2\text{ mA}$ $T_A \geq 0^\circ\text{C}$ $T_A \leq 0^\circ\text{C}$ | | 0.23 | 0.4 0.6 | V |
| Output Leakage Current | $V_{IN} \geq 5\text{ mV}$, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$ | | 1 | 10 | μA |
| Differential Input Voltage | | | | ± 5 | V |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0$ | | 4.3 | | mA |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$ | | 8 | 11.5 | mA |
| Negative Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$ | | 3 | 4.5 | mA |

Note 1: For supply voltages less than $\pm 15V$ the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM119 is 150°C , while that of the LM219 is 110°C . For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W , junction to ambient, or 19°C/W , junction to case. The thermal resistance of the J14 and N14 packages is 100°C/W , junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and the Ground pin at ground, and $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise stated. With the LM219, however, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to $\pm 15V$ supplies. Do not operate the device with more than 16V from ground to V_S .

Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

Note 6: Output is pulled up to 15V through a 1.4 k Ω resistor.

Note 7: Refer to RETS119X for LM119H/883 and LM119J/883 specifications.

Absolute Maximum Ratings LM319A/319

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-----------|
| Total Supply Voltage | 36V |
| Output to Negative Supply Voltage | 36V |
| Ground to Negative Supply Voltage | 25V |
| Ground to Positive Supply Voltage | 18V |
| Differential Input Voltage | $\pm 5V$ |
| Input Voltage (Note 1) | $\pm 15V$ |
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| ESD rating (1.5 k Ω in series with 100 pF) | 800V |

| | |
|---|----------------|
| Storage Temperature Range | -65°C to 150°C |
| Lead Temperature (Soldering, 10 sec.) | 260°C |
| Soldering Information | |
| Dual-In-Line Package | |
| Soldering (10 sec.) | 260°C |
| Small Outline Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | |

Operating Temperature Range

| | |
|---------------|-------------|
| LM319A, LM319 | 0°C to 70°C |
|---------------|-------------|

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM319A | | | LM319 | | | Units |
|-------------------------------|---|--------|----------|---------|-------|----------|---------|---------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage (Note 4) | $T_A = 25^\circ\text{C}$, $R_S \leq 5k$ | | 0.5 | 1.0 | | 2.0 | 8.0 | mV |
| Input Offset Current (Note 4) | $T_A = 25^\circ\text{C}$ | | 20 | 40 | | 80 | 200 | nA |
| Input Bias Current | $T_A = 25^\circ\text{C}$ | | 150 | 500 | | 250 | 1000 | nA |
| Voltage Gain | $T_A = 25^\circ\text{C}$ (Note 6) | 20 | 40 | | 8 | 40 | | V/mV |
| Response Time (Note 5) | $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$ | | 80 | | | 80 | | ns |
| Saturation Voltage | $V_{IN} \leq -10\text{ mV}$, $I_{OUT} = 25\text{ mA}$ $T_A = 25^\circ\text{C}$ | | 0.75 | 1.5 | | 0.75 | 1.5 | V |
| Output Leakage Current | $V_{IN} \geq 10\text{ mV}$, $V_{OUT} = 35V$, $V^- = V_{GND} = 0V$, $T_A = 25^\circ\text{C}$ | | 0.2 | 10 | | 0.2 | 10 | μA |
| Input Offset Voltage (Note 4) | $R_S \leq 5k$ | | | 10 | | | 10 | mV |
| Input Offset Current (Note 4) | | | | 300 | | | 300 | nA |
| Input Bias Current | | | | 1000 | | | 1200 | nA |
| Input Voltage Range | $V_S = \pm 15V$ $V^+ = 5V$, $V^- = 0$ | 1 | ± 13 | 3 | 1 | ± 13 | 3 | V |
| Saturation Voltage | $V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -10\text{ mV}$, $I_{SINK} \leq 3.2\text{ mA}$ | | 0.3 | 0.4 | | 0.3 | 0.4 | V |
| Differential Input Voltage | | | | ± 5 | | | ± 5 | V |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V^+ = 5V$, $V^- = 0$ | | 4.3 | | | 4.3 | | mA |
| Positive Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$ | | 8 | 12.5 | | 8 | 12.5 | mA |
| Negative Supply Current | $T_A = 25^\circ\text{C}$, $V_S = \pm 15V$ | | 3 | 5 | | 3 | 5 | mA |

Note 1: For supply voltages less than ± 15 the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum junction temperature of the LM319A and LM319 is 85°C . For operating at elevated temperatures, devices in the H10 package must be derated based on a thermal resistance of 160°C/W , junction to ambient, or 19°C/W , junction to case. The thermal resistance of the N14 and J14 package is 100°C/W , junction to ambient. The thermal resistance of the M14 package is 115°C/W , junction to ambient.

Note 3: These specifications apply for $V_S = \pm 15V$, and $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to $\pm 15V$ supplies. Do not operate the device with more than 16V from ground to V_S .

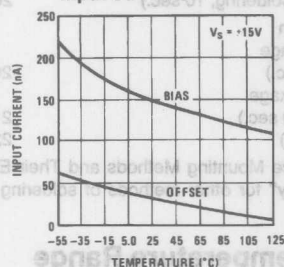
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

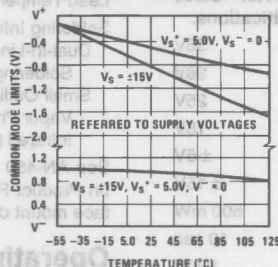
Note 6: Output is pulled up to 15V through a 1.4 k Ω resistor.

Typical Performance Characteristics LM119A/LM119/LM219

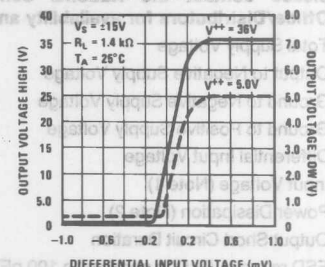
Input Currents



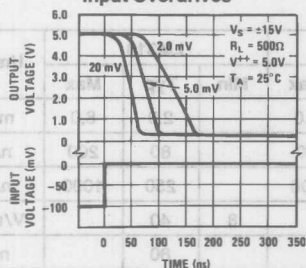
Common Mode Limits



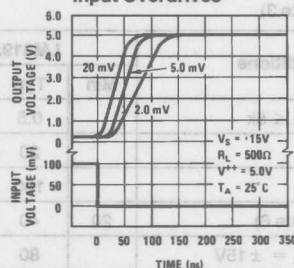
Transfer Function



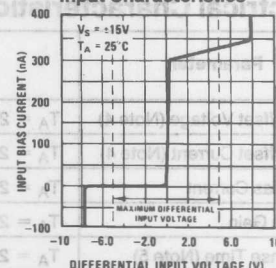
Response Time for Various Input Overdrives



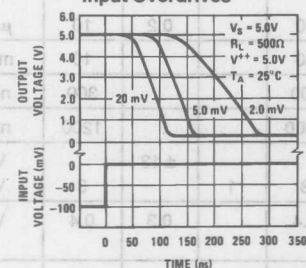
Response Time for Various Input Overdrives



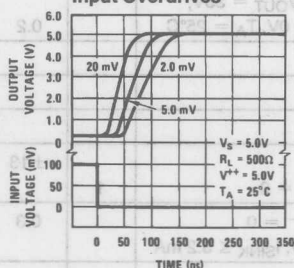
Input Characteristics



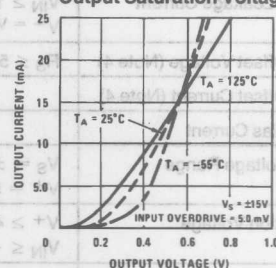
Response Time for Various Input Overdrives



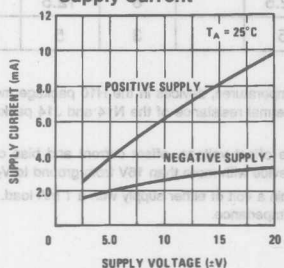
Response Time for Various Input Overdrives



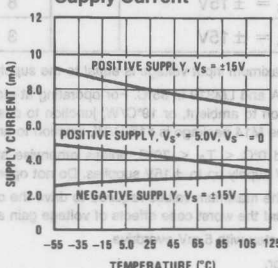
Output Saturation Voltage



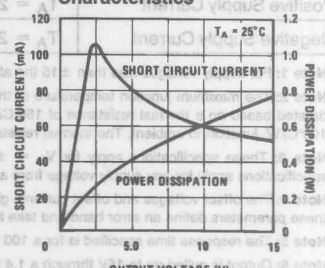
Supply Current



Supply Current



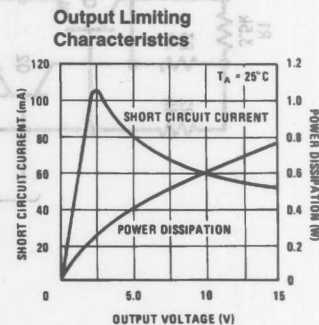
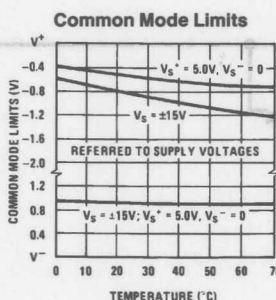
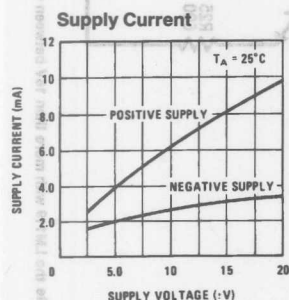
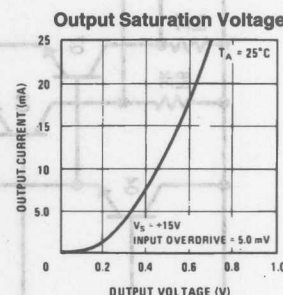
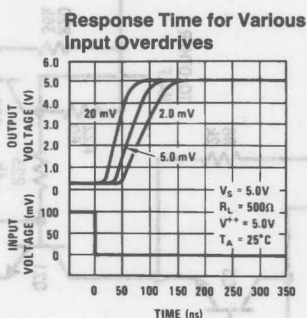
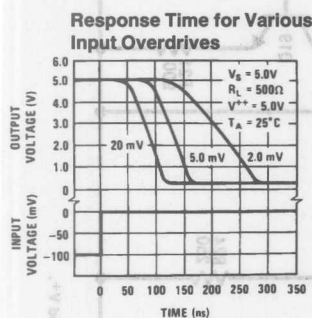
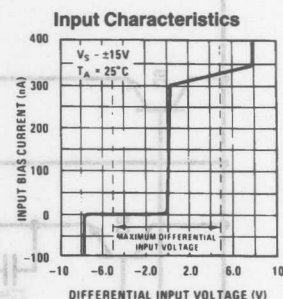
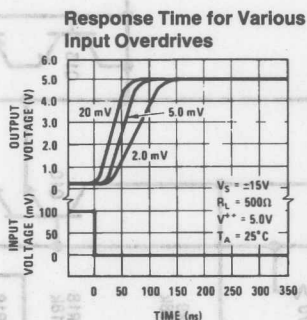
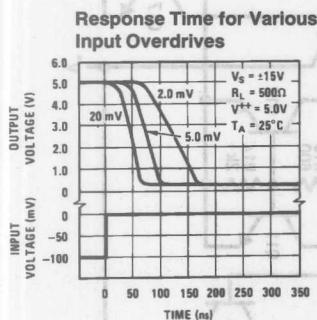
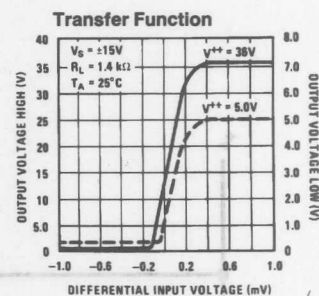
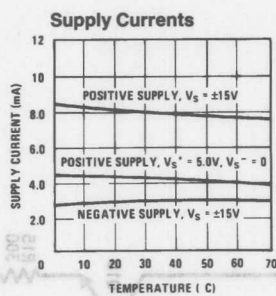
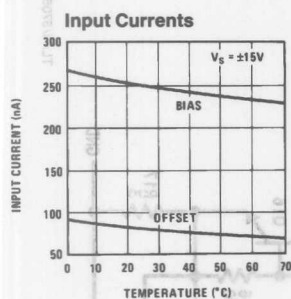
Output Limiting Characteristics



TL/H/5705-2

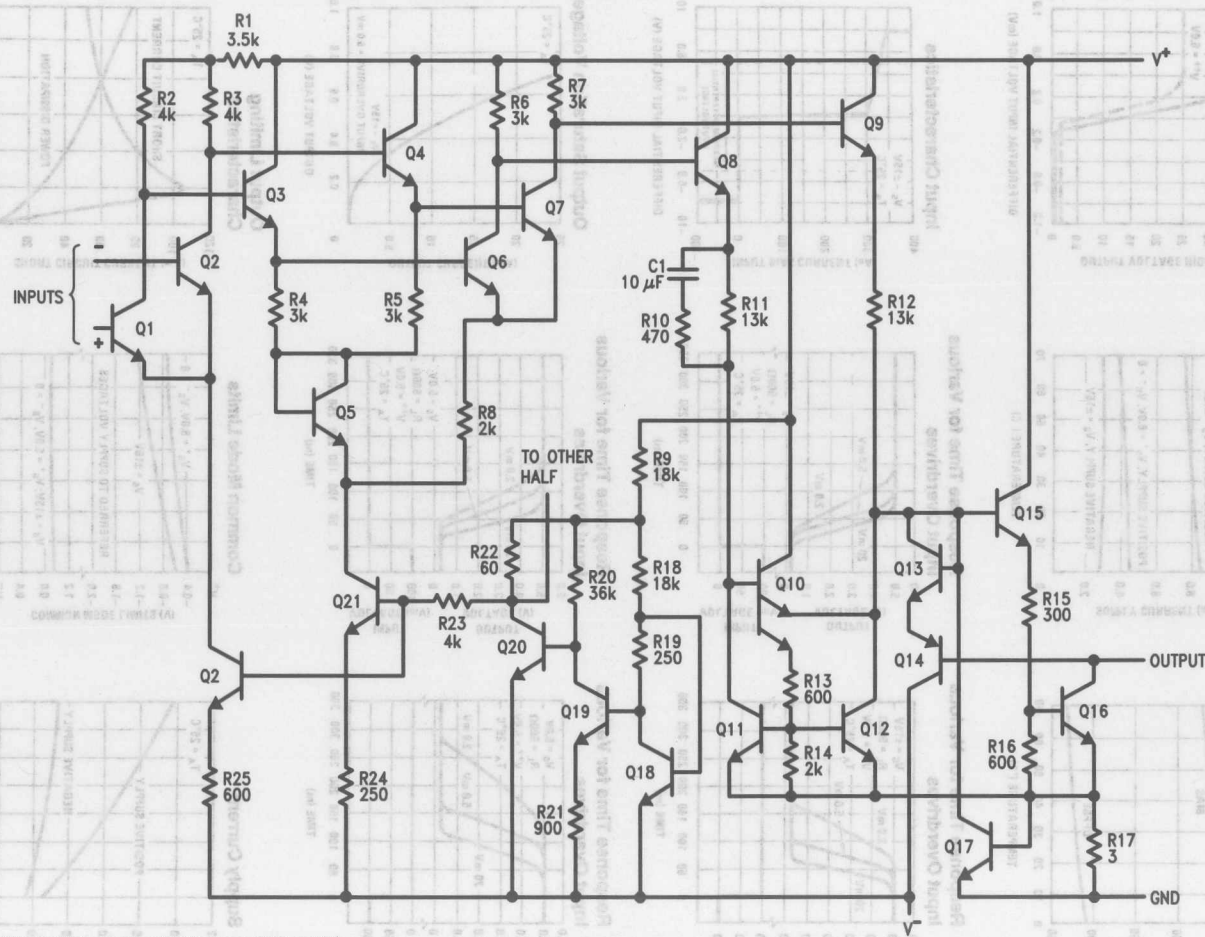
Typical Performance Characteristics LM319A, LM319

LM119/LM219/LM319



TL/H/5705-3

Schematic Diagram

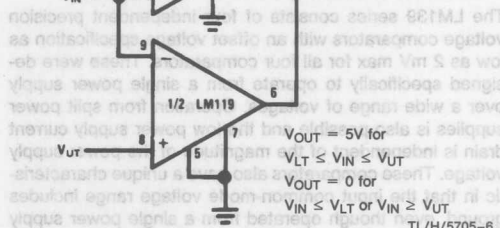


*Do not operate the LM119 with more than 16V between GND and V+.

TL/H/5705-1

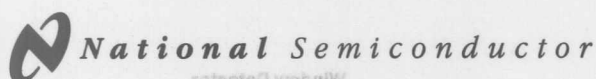


5V



numbers are for metal can

$V_{UT} = 5V$ for
 $V_{LT} \leq V_{IN} \leq V_{UT}$
 $V_{OUT} = 0$ for
 $V_{IN} \leq V_{LT}$ or $V_{IN} \geq V_{UT}$



LM139/LM239/LM339/LM2901/LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

Advantages

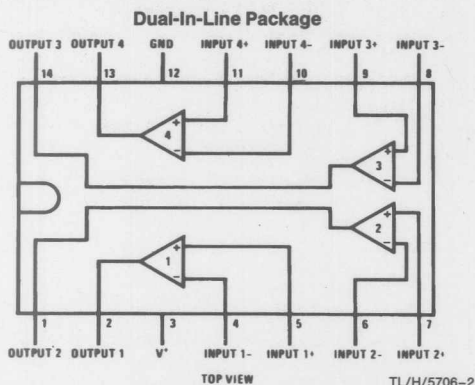
- High precision comparators
- Reduced V_{OS} drift over temperature

- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

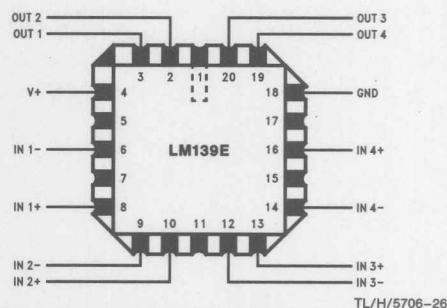
- Wide supply voltage range
LM139 series, 2 V_{DC} to 36 V_{DC} or ± 1 V_{DC} to ± 18 V_{DC}
LM139A series, LM2901 2 V_{DC} to 28 V_{DC}
LM3302 or ± 1 V_{DC} to ± 14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ± 5 nA
and offset voltage ± 3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Connection Diagrams

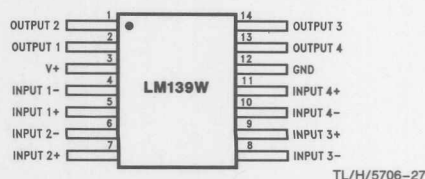


Order Number LM139J, LM139J/883*, LM139AJ,
LM139AJ/883**, LM239J, LM239AJ, LM339J,
See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN,
LM2901N or LM3302N
See NS Package Number N14A

*Available per JM38510/11201
**Available per SMD # 5962-8873901



Order Number LM139AE/883 or LM139E/883
See NS Package Number E20A



Order Number LM139AW/883 or LM139W/883*
See NS Package Number W14B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | LM139/LM239/LM339 | LM139A/LM239A/LM339A | LM3302 | LM139/LM239/LM339 | LM139A/LM239A/LM339A | LM2901 |
|--|--|--|---|-------------------|----------------------|--------|
| Supply Voltage, V^+ | 36 V _{DC} or ± 18 V _{DC} | 28 V _{DC} or ± 14 V _{DC} | Operating Temperature Range | -40°C | | |
| Differential Input Voltage (Note 8) | 36 V _{DC} | 28 V _{DC} | LM339/LM339A | 0°C to +70°C | | |
| Input Voltage | -0.3 V _{DC} to +36 V _{DC} | -0.3 V _{DC} to +28 V _{DC} | LM239/LM239A | -25°C to +85°C | | |
| Input Current ($V_{IN} < 0.3$ V _{DC}), (Note 3) | 50 mA | 50 mA | LM2901 | -40°C to +85°C | | |
| Power Dissipation (Note 1) | | | LM139/LM139A | -55°C to +125°C | | |
| Molded DIP | 1050 mW | 1050 mW | Soldering Information | | | |
| Cavity DIP | 1190 mW | | Dual-In-Line Package | | | |
| Small Outline Package | 760 mW | | Soldering (10 seconds) | 260°C | | |
| Output Short-Circuit to GND, (Note 8) | Continuous | Continuous | Small Outline Package | | | |
| Storage Temperature Range | -65°C to +150°C | -65°C to +150°C | Vapor Phase (60 seconds) | 215°C | | |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C | Infrared (15 seconds) | 220°C | | |
| | | | See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | |
| | | | ESD rating (1.5 k Ω in series with 100 pF) | 600V | | |

Electrical Characteristics ($V^+ = 5$ V_{DC}, $T_A = 25^\circ\text{C}$, unless otherwise stated)

| Parameter | Conditions | LM139A | | LM239A, LM339A | | | LM139 | | LM239, LM339 | | | LM2901 | | LM3302 | |
|---------------------------------|---|--------|-------------|----------------|-----|-------------|-------|-----|--------------|-----|-----|-------------|-----|--------|-------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ |
| Input Offset Voltage | (Note 9) | 1.0 | 2.0 | | 1.0 | 2.0 | | 2.0 | 5.0 | | 2.0 | 5.0 | | 2.0 | 7.0 |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), $V_{CM} = 0$ V | 25 | 100 | | 25 | 250 | | 25 | 100 | | 25 | 250 | | 25 | 250 |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0$ V | 3.0 | 25 | | 5.0 | 50 | | 3.0 | 25 | | 5.0 | 50 | | 5 | 50 |
| Input Common-Mode Voltage Range | $V^+ = 30$ V _{DC} (LM3302, $V^+ = 28$ V _{DC}) (Note 6) | 0 | $V^+ - 1.5$ | 0 | 0 | $V^+ - 1.5$ | 0 | 0 | $V^+ - 1.5$ | 0 | 0 | $V^+ - 1.5$ | 0 | 0 | $V^+ - 1.5$ |
| Supply Current | $R_L = \infty$ on all Comparators, $R_L = \infty$, $V^+ = 36$ V, (LM3302, $V^+ = 28$ V _{DC}) | 0.8 | 2.0 | | 0.8 | 2.0 | | 0.8 | 2.0 | | 0.8 | 2.0 | | 0.8 | 2.0 |
| Voltage Gain | $R_L \geq 15$ k Ω , $V^+ = 15$ V _{DC} , $V_O = 1$ V _{DC} to 11 V _{DC} | 50 | 200 | | 50 | 200 | | 50 | 200 | | 50 | 200 | | 25 | 100 |
| Large Signal Response Time | $V_{IN} = \text{TTL Logic Swing}$, $V_{REF} = 1.4$ V _{DC} , $V_{RL} = 5$ V _{DC} , $R_L = 5.1$ k Ω | 300 | | | 300 | | | 300 | | | 300 | | | 300 | |
| Response Time | $V_{RL} = 5$ V _{DC} , $R_L = 5.1$ k Ω , (Note 7) | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | |
| Output Sink Current | $V_{IN(-)} = 1$ V _{DC} , $V_{IN(+)} = 0$, $V_O \leq 1.5$ V _{DC} | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 | | 6.0 | 16 |

LM139/LM239/LM339/LM3302



LM139/LM239/LM339/LM2901/LM3302

Electrical Characteristics ($V^+ = 5\text{ V}_{\text{DC}}$, $T_A = 25^\circ\text{C}$, unless otherwise stated) (Continued)

| Parameter | Conditions | LM139A | | | LM239A, LM339A | | | LM139 | | | LM239, LM339 | | | LM2901 | | | LM3302 | | | Units | |
|------------------------|--|--------|-----|-----|----------------|-----|-----|-------|-----|-----|--------------|-----|-----|--------|-----|-----|--------|-----|-----|-------|------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| Saturation Voltage | $V_{\text{IN}(-)} = 1\text{ V}_{\text{DC}}, V_{\text{IN}(+)} = 0, I_{\text{SINK}} \leq 4\text{ mA}$ | 250 | | 400 | | 250 | | 400 | | 250 | | 400 | | 250 | | 400 | | 250 | | 500 | mV _{DC} |
| Output Leakage Current | $V_{\text{IN}(+)} = 1\text{ V}_{\text{DC}}, V_{\text{IN}(-)} = 0, V_{\text{O}} = 5\text{ V}_{\text{DC}}$ | 0.1 | | | | 0.1 | | | | 0.1 | | | | 0.1 | | | | 0.1 | | | nA _{DC} |

Electrical Characteristics ($V^+ = 5.0\text{ V}_{\text{DC}}$, Note 4)

| Parameter | Conditions | LM139A | | LM239A, LM339A | | LM139 | | LM239, LM339 | | LM2901 | | LM3302 | | Units | | | | | | | | |
|---------------------------------|---|--------|-----|----------------|-----|-------|-------------|--------------|-----|-------------|-----|--------|-------------|-------|-----|-------------|-----|--|-------------|--|-------------|------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | Min | Typ | Max | | | | | |
| Input Offset Voltage | (Note 9) | | | 4.0 | | | 4.0 | | | 9.0 | | | 9.0 | | | 9 | | | 15 | | 40 | mV _{DC} |
| Input Offset Current | $I_{\text{IN}(+)} - I_{\text{IN}(-)}$, $V_{\text{CM}} = 0\text{V}$ | | | 100 | | | 150 | | | 100 | | | 150 | | | 50 | | | 200 | | 300 | nA _{DC} |
| Input Bias Current | $I_{\text{IN}(+)}$ or $I_{\text{IN}(-)}$ with Output in Linear Range, $V_{\text{CM}} = 0\text{V}$ (Note 5) | | | 300 | | | 400 | | | 300 | | | 400 | | | 200 | | | 500 | | 1000 | nA _{DC} |
| Input Common-Mode Voltage Range | $V^+ = 30\text{ V}_{\text{DC}}$ (LM3302, $V^+ = 28\text{ V}_{\text{DC}}$) (Note 6) | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | 0 | | $V^+ - 2.0$ | | $V^+ - 2.0$ | V _{DC} |
| Saturation Voltage | $V_{\text{IN}(-)} = 1\text{ V}_{\text{DC}}$, $V_{\text{IN}(+)} = 0$, $I_{\text{SINK}} \leq 4\text{ mA}$ | | | 700 | | | 700 | | | 700 | | | 700 | | | 400 | | | 700 | | 700 | mV _{DC} |
| Output Leakage Current | $V_{\text{IN}(+)} = 1\text{ V}_{\text{DC}}$, $V_{\text{IN}(-)} = 0$, $V_{\text{O}} = 30\text{ V}_{\text{DC}}$, (LM3302, $V_{\text{O}} = 28\text{ V}_{\text{DC}}$) | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | | 1.0 | | 1.0 | μA _{DC} |
| Differential Input Voltage | Keep all $V_{\text{IN}}\text{'s} \geq 0\text{ V}_{\text{DC}}$ (or V^- , if used), (Note 8) | | | 36 | | | 36 | | | 36 | | | 36 | | | 36 | | | 36 | | 28 | V _{DC} |

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of $95^\circ\text{C}/\text{W}$ which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100\text{ mW}$), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+ .

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\text{ V}_{\text{DC}}$ (at 25°C).

Note 4: These specifications are limited to $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$, the LM339/LM339A temperature specifications are limited to $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$, and the LM2901, LM3302 temperature range is $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V . The upper end of the common-mode voltage range is $V^+ - 1.5\text{ V}$ at 25°C , but either or both inputs can go to $+30\text{ V}_{\text{DC}}$ without damage (25 V for LM3302), independent of the magnitude of V^+ .

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

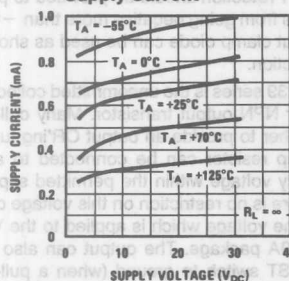
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\text{ V}_{\text{DC}}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O \approx 1.4\text{ V}_{\text{DC}}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} to 30 V_{DC} ; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\text{ V}_{\text{DC}}$), at 25°C . For LM3302, V^+ from 5 V_{DC} to 28 V_{DC} .

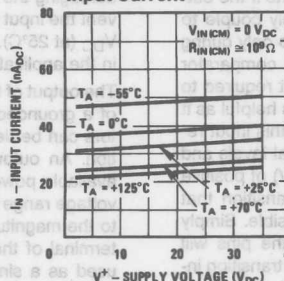
Note 10: Refer to RETS139AX for LM139A military specifications and to RETS139X for LM139 military specifications.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

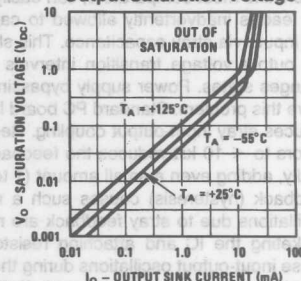
Supply Current



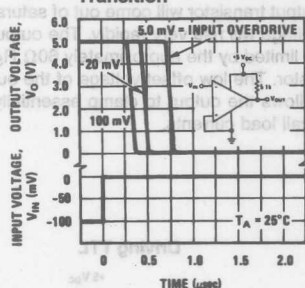
Input Current



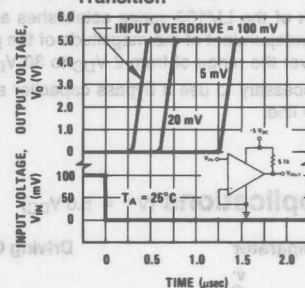
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



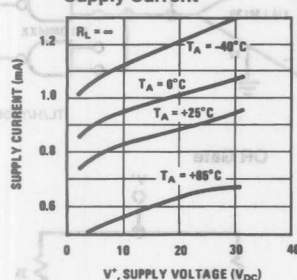
Response Time for Various Input Overdrives—Positive Transition



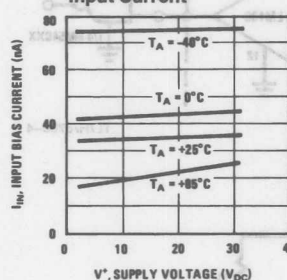
TL/H/5706-6

Typical Performance Characteristics LM2901

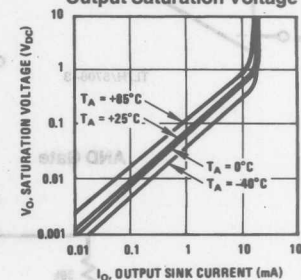
Supply Current



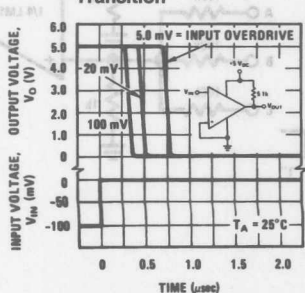
Input Current



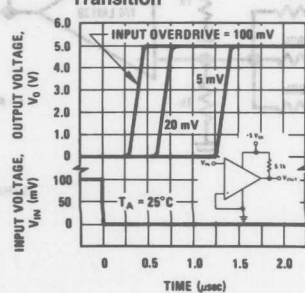
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



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which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing this input resistors to $< 10 \text{ k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2 V_{DC}$ to $30 V_{DC}$.

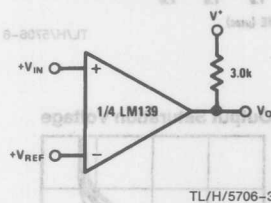
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3 V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

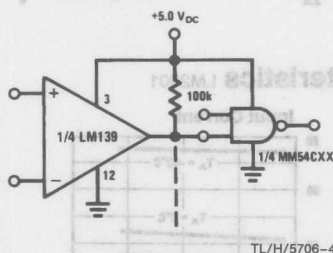
The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately $60\Omega R_{SAT}$ of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0 V_{DC}$)

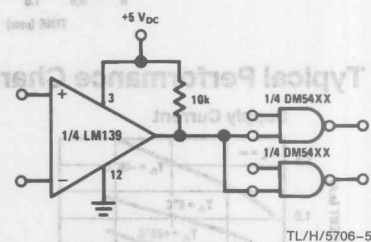
Basic Comparator



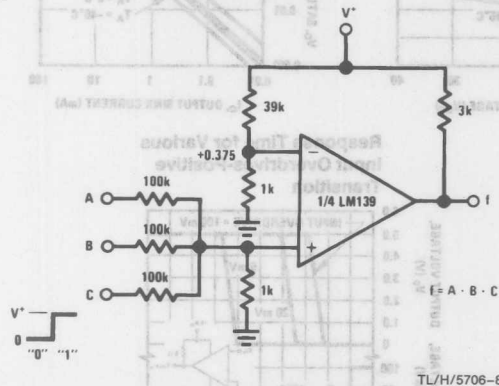
Driving CMOS



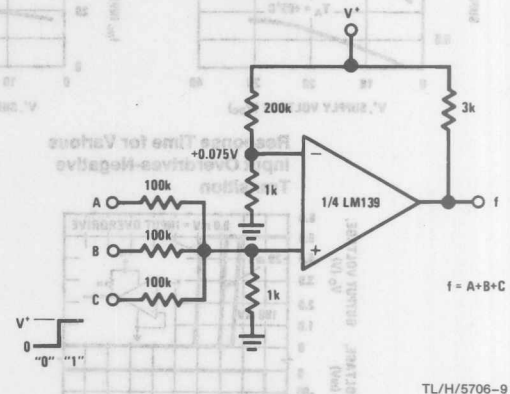
Driving TTL



AND Gate

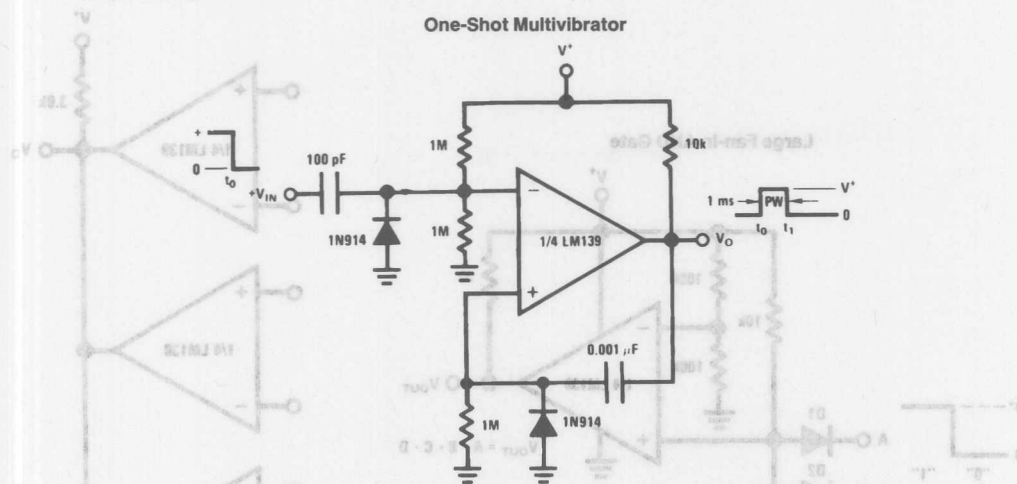


OR Gate

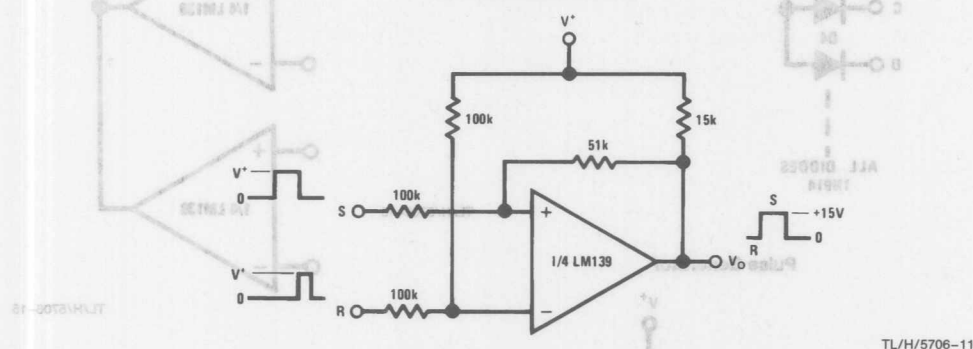


Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

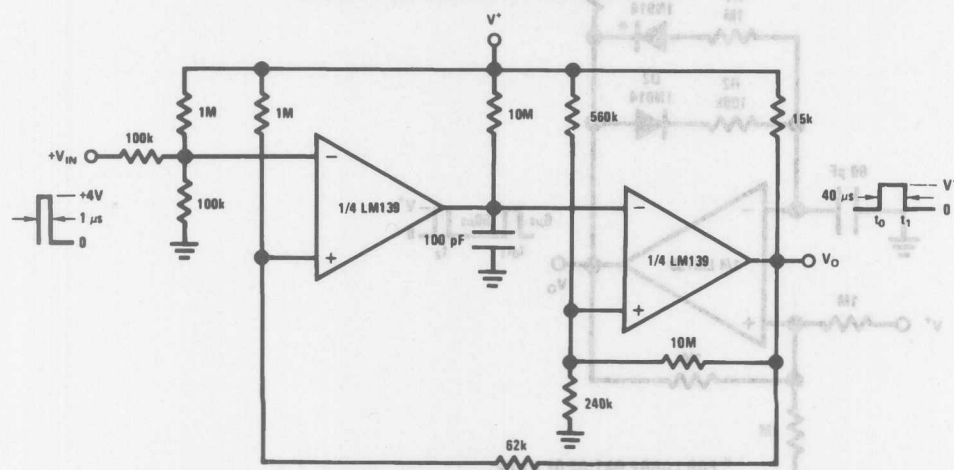
One-Shot Multivibrator



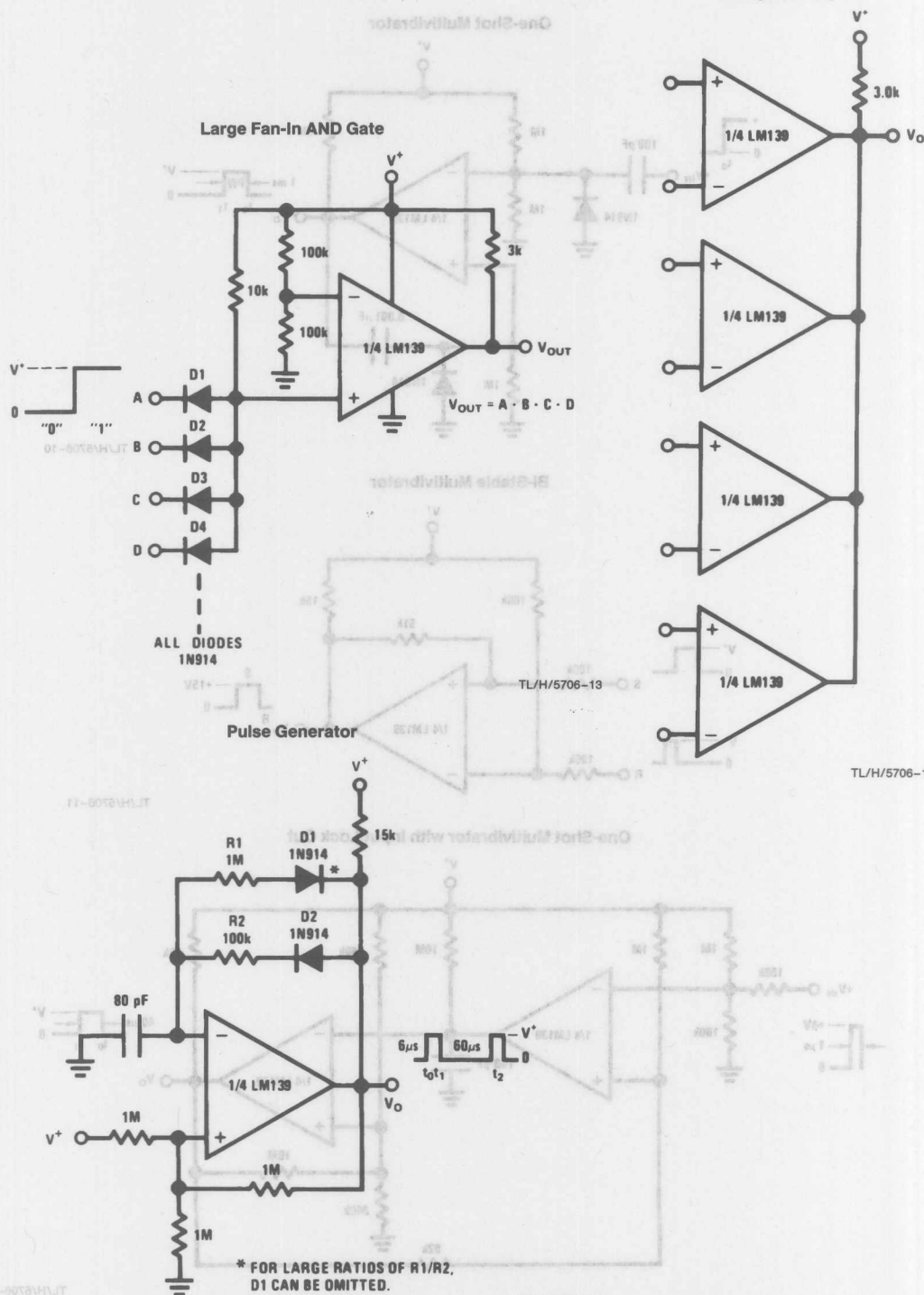
Bi-Stable Multivibrator



One-Shot Multivibrator with Input Lock Out

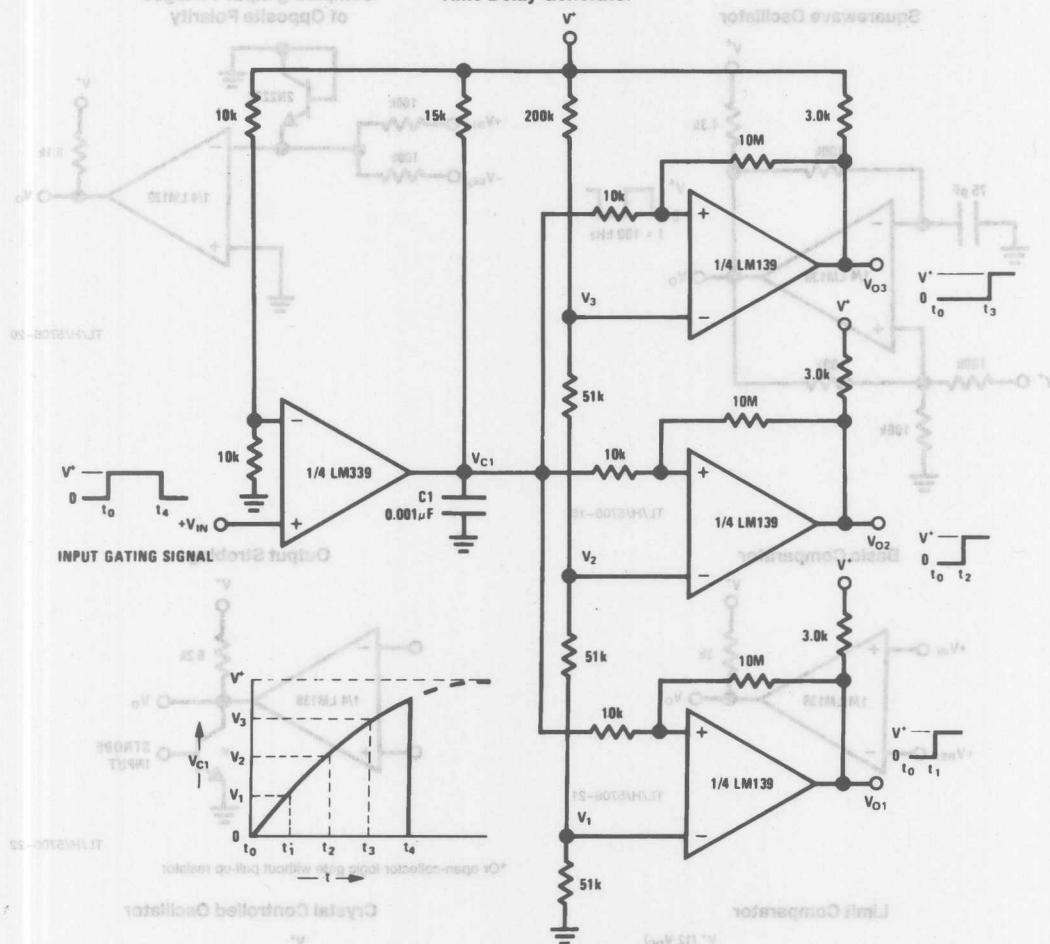


Typical Applications (V⁺ = 15 V_{DC}) (Continued)



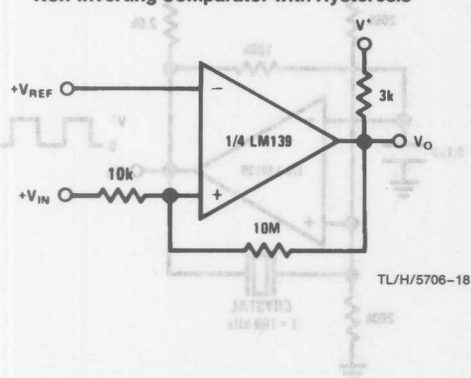
Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

Time Delay Generator



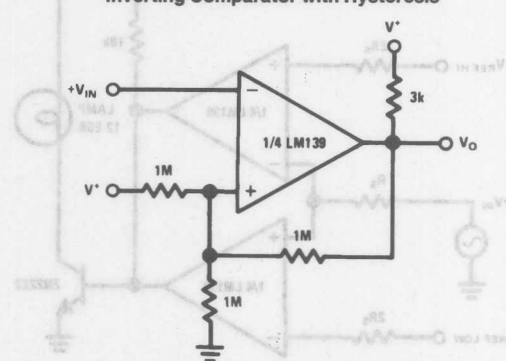
TL/H/5706-14

Non-Inverting Comparator with Hysteresis



TL/H/5706-18

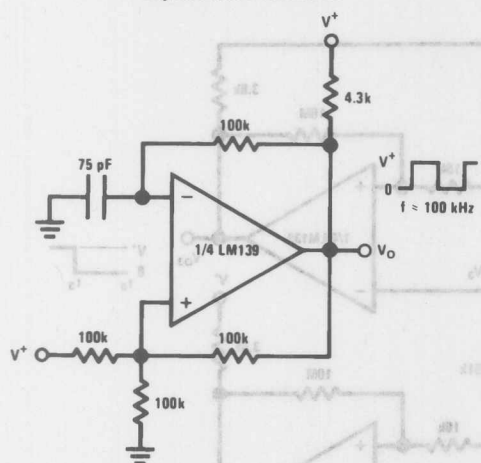
Inverting Comparator with Hysteresis



TL/H/5706-19

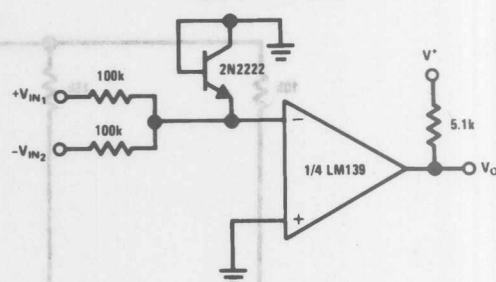
Typical Applications ($V^+ = 15\text{ V}_{\text{DC}}$) (Continued)

Squarewave Oscillator



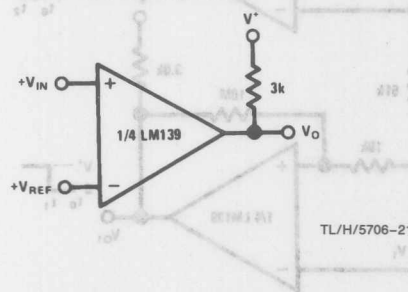
TL/H/5706-16

Comparing Input Voltages of Opposite Polarity



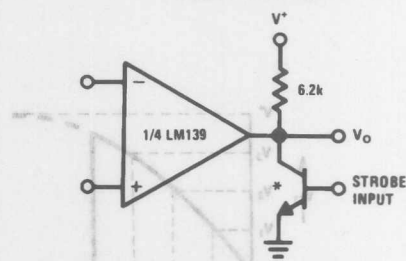
TL/H/5706-20

Basic Comparator



TL/H/5706-21

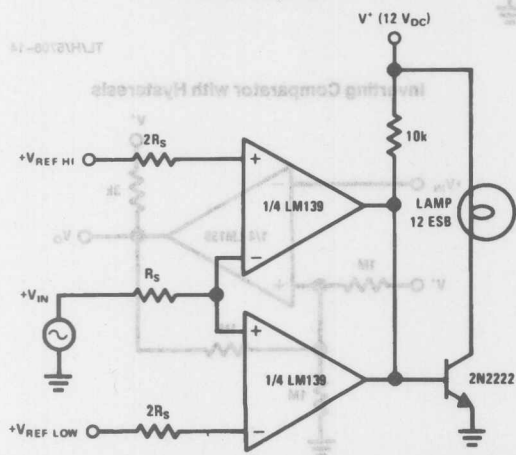
Output Strobing



TL/H/5706-22

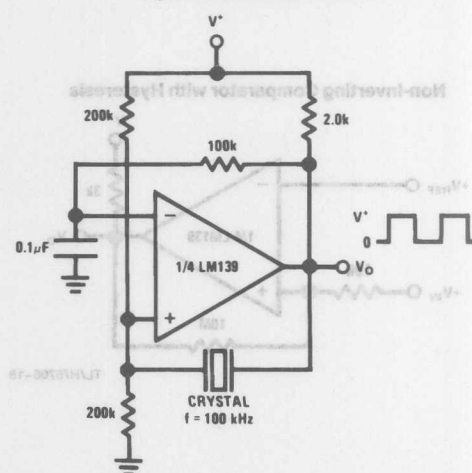
*Or open-collector logic gate without pull-up resistor

Limit Comparator



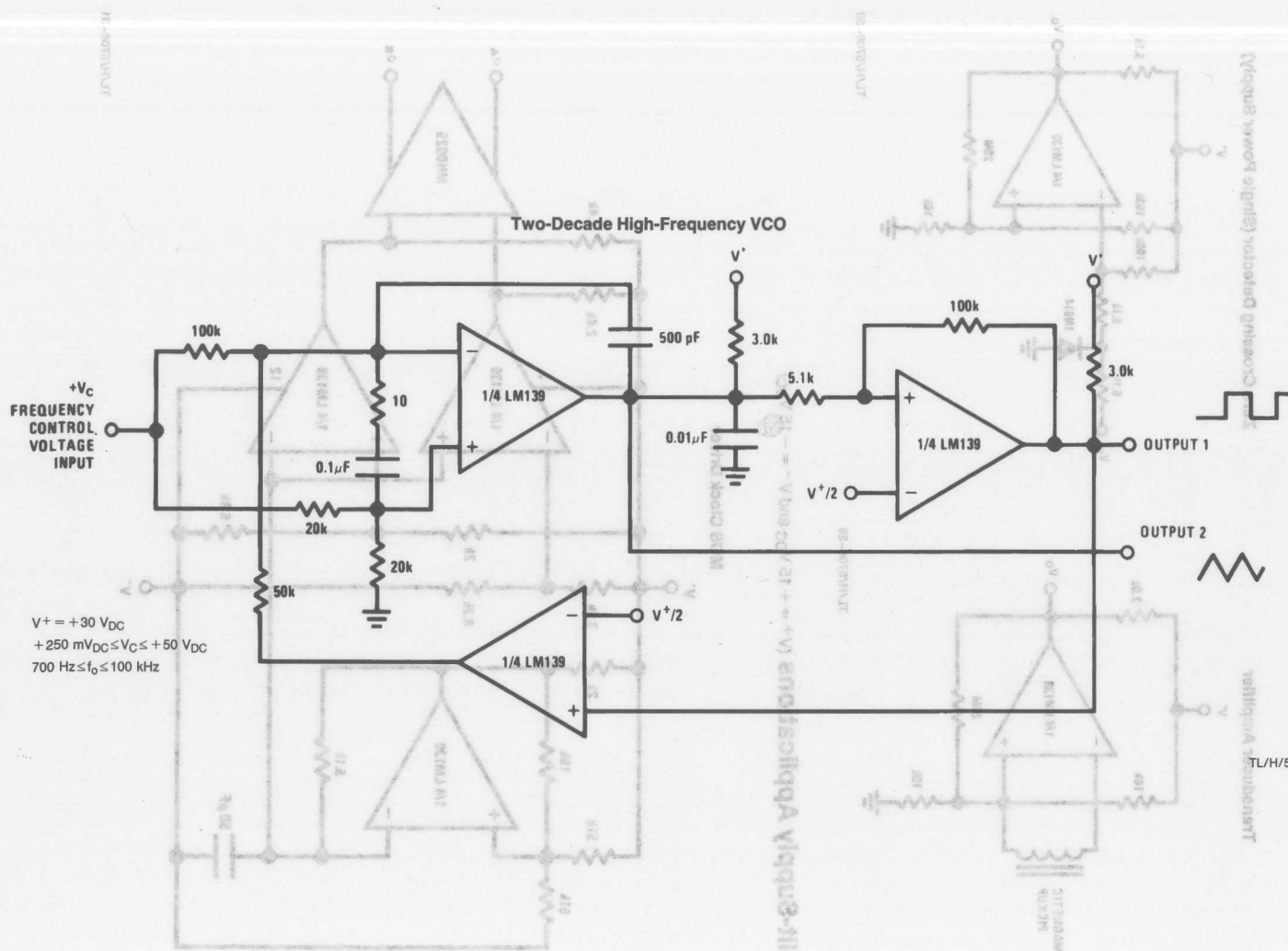
TL/H/5706-24

Crystal Controlled Oscillator



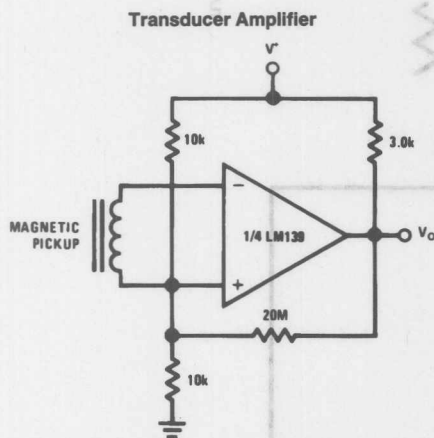
TL/H/5706-25

Typical Applications ($V^+ = 15\text{ V}_{DC}$) (Continued)

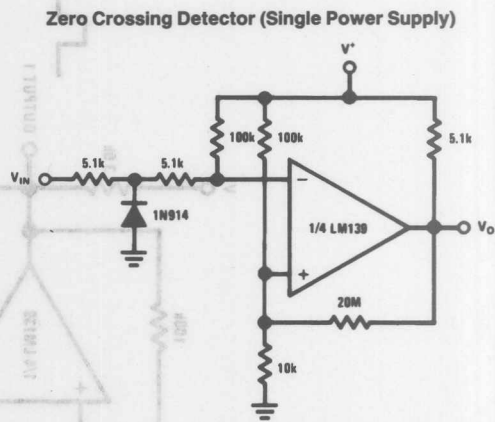


TL/H/5706-23

LM139/LM239/LM339/LM2901/LM3302

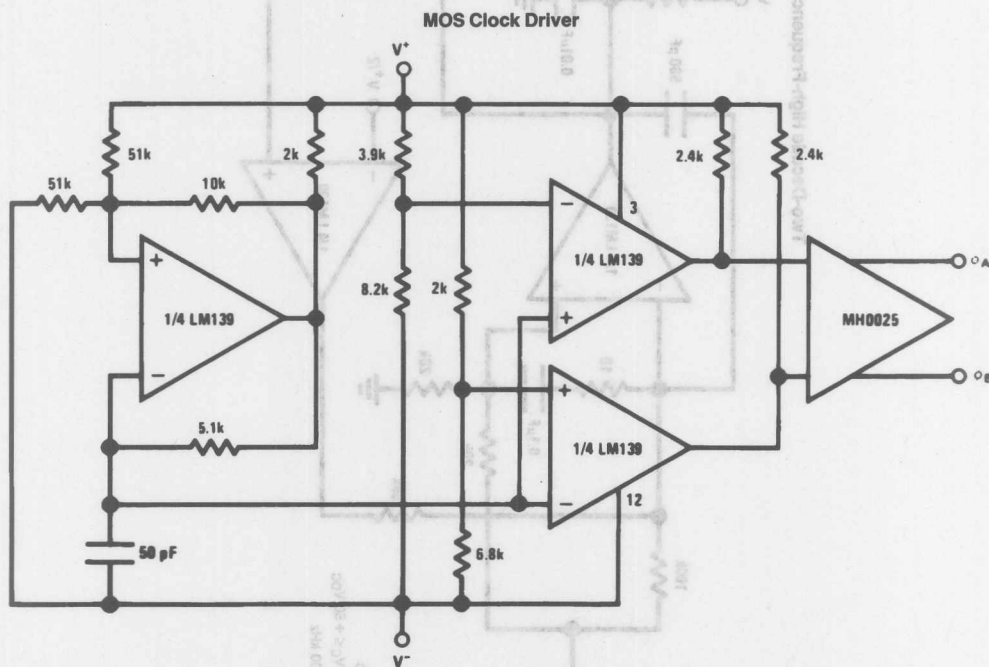


TL/H/5706-28



TL/H/5706-30

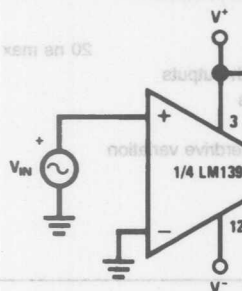
Split-Supply Applications ($V^+ = +15 V_{DC}$ and $V^- = -15 V_{DC}$)



TL/H/5706-31

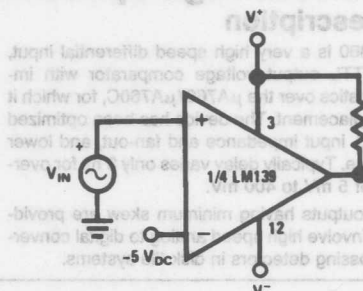
Split-Supply Applications ($V^+ = +15\text{ V}_{\text{DC}}$ and $V^- = -15\text{ V}_{\text{DC}}$) (Continued)

Zero Crossing Detector



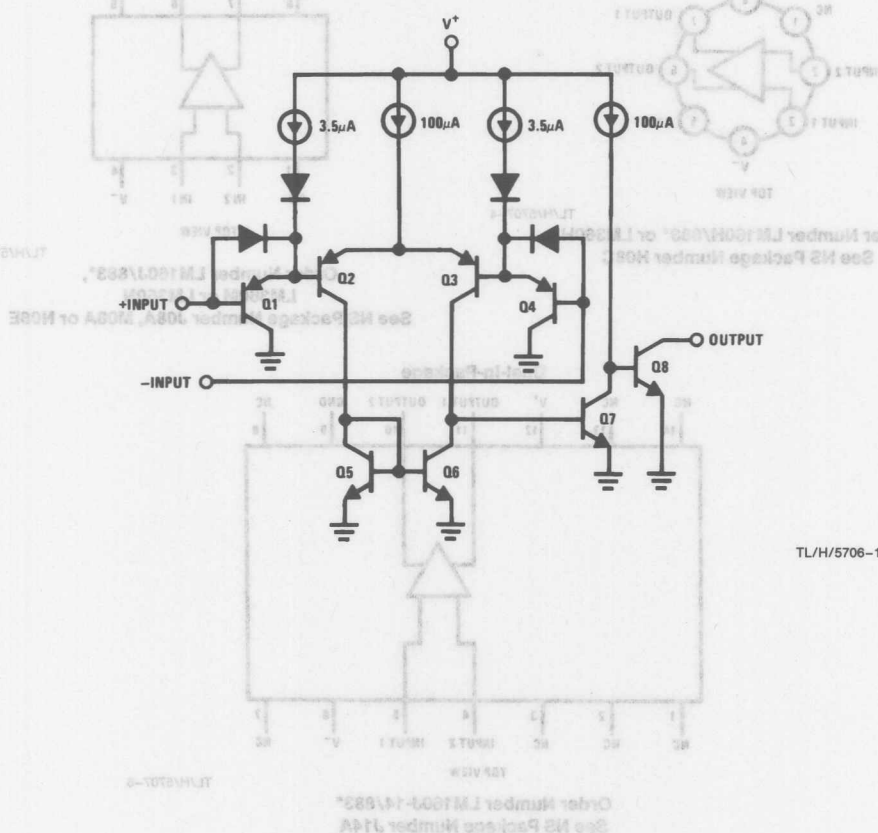
TL/H/5706-32

Comparator With a Negative Reference

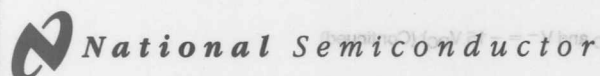


TL/H/5706-33

Schematic Diagram



TL/H/5706-1



LM160/LM360 High Speed Differential Comparator

General Description

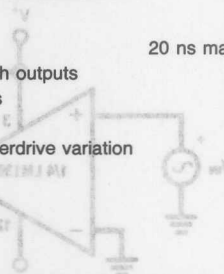
The LM160/LM360 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the $\mu\text{A}760/\mu\text{A}760\text{C}$, for which it is a pin-for-pin replacement. The device has been optimized for greater speed, input impedance and fan-out, and lower input offset voltage. Typically delay varies only 3 ns for overdrive variations of 5 mV to 400 mV.

Complementary outputs having minimum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

Features

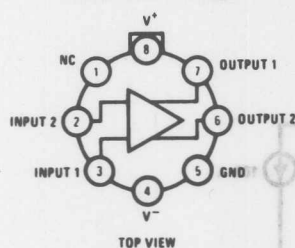
- Guaranteed high speed
- Tight delay matching on both outputs
- Complementary TTL outputs
- High input impedance
- Low speed variation with overdrive variation
- Fan-out of 4
- Low input offset voltage
- Series 74 TTL compatible

20 ns max



Connection Diagrams

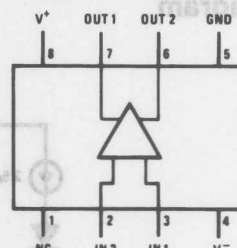
Metal Can Package



Order Number LM160H/883* or LM360H
See NS Package Number H08C

TL/H/5707-4

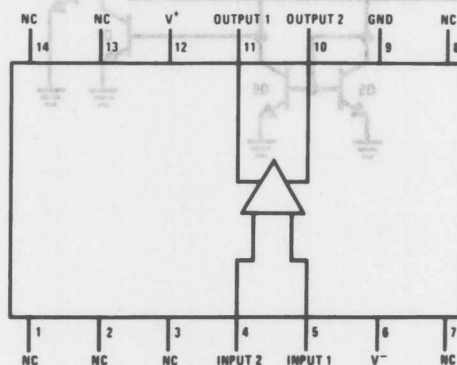
Dual-In-Line Package



Order Number LM160J/883*,
LM360M or LM360N
See NS Package Number J08A, M08A or N08E

TL/H/5707-5

Dual-In-Package



Order Number LM160J-14/883*
See NS Package Number J14A

TL/H/5707-6

*Also available in SMD # 5962-8767401

Absolute Maximum Ratings (Note 5)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 7)

| | |
|----------------------------|----------------------------|
| Positive Supply Voltage | +8V |
| Negative Supply Voltage | -8V |
| Peak Output Current | 20 mA |
| Differential Input Voltage | $\pm 5V$ |
| Input Voltage | $V^+ \geq V_{IN} \geq V^-$ |
| ESD Tolerance (Note 8) | 1600V |

Operating Temperature Range

| | |
|-------|-----------------|
| LM160 | -55°C to +125°C |
| LM360 | 0°C to +70°C |

Storage Temperature Range

-65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

260°C

Soldering Information

| | |
|--------------------------|-------|
| Dual-In-Line Package | 260°C |
| Soldering (10 seconds) | |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---------|-----------|------|------------------|
| Operating Conditions | | | | | |
| Supply Voltage V_{CC}^+ | | 4.5 | 5 | 6.5 | V |
| Supply Voltage V_{CC}^- | | -4.5 | -5 | -6.5 | V |
| Input Offset Voltage | $R_S \leq 200\Omega$ | | 2 | 5 | mV |
| Input Offset Current | | | 0.5 | 3 | μA |
| Input Bias Current | | | 5 | 20 | μA |
| Output Resistance (Either Output) | $V_{OUT} = V_{OH}$ | | 100 | | Ω |
| Response Time | $T_A = 25^\circ C, V_S = \pm 5V$ (Notes 1, 6) | | 13 | 25 | ns |
| | $T_A = 25^\circ C, V_S = \pm 5V$ (Notes 2, 6) | | 12 | 20 | ns |
| | $T_A = 25^\circ C, V_S = \pm 5V$ (Notes 3, 6) | | 14 | | ns |
| Response Time Difference between Outputs | | | | | |
| $(t_{pd} \text{ of } +V_{IN1}) - (t_{pd} \text{ of } -V_{IN2})$ | $T_A = 25^\circ C$ (Notes 1, 6) | | 2 | | ns |
| $(t_{pd} \text{ of } +V_{IN2}) - (t_{pd} \text{ of } -V_{IN1})$ | $T_A = 25^\circ C$ (Notes 1, 6) | | 2 | | ns |
| $(t_{pd} \text{ of } +V_{IN1}) - (t_{pd} \text{ of } +V_{IN2})$ | $T_A = 25^\circ C$ (Notes 1, 6) | | 2 | | ns |
| $(t_{pd} \text{ of } -V_{IN1}) - (t_{pd} \text{ of } -V_{IN2})$ | $T_A = 25^\circ C$ (Notes 1, 6) | | 2 | | ns |
| Input Resistance | $f = 1 \text{ MHz}$ | | 17 | | k Ω |
| Input Capacitance | $f = 1 \text{ MHz}$ | | 3 | | pF |
| Average Temperature Coefficient of Input Offset Voltage | $R_S = 50\Omega$ | | 8 | | $\mu V/^\circ C$ |
| Average Temperature Coefficient of Input Offset Current | | | 7 | | nA/°C |
| Common Mode Input Voltage Range | $V_S = \pm 6.5V$ | ± 4 | ± 4.5 | | V |
| Differential Input Voltage Range | | ± 5 | | | V |
| Output High Voltage (Either Output) | $I_{OUT} = -320 \mu A, V_S = \pm 4.5V$ | 2.4 | 3 | | V |
| Output Low Voltage (Either Output) | $I_{SINK} = 6.4 \text{ mA}$ | | 0.25 | 0.4 | V |
| Positive Supply Current | $V_S = \pm 6.5V$ | | 18 | 32 | mA |
| Negative Supply Current | $V_S = \pm 6.5V$ | | -9 | -16 | mA |

Note 1: Response time measured from the 50% point of a 30 mVp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 2: Response time measured from the 50% point of a 2 Vp-p 10 MHz sinusoidal input to the 50% point of the output.

Note 3: Response time measured from the start of a 100 mV input step with 5 mV overdrive to the time when the output crosses the logic threshold.

Note 4: Typical thermal impedances are as follows:

| | | | | | | |
|-----------------|---------------|---------|-------------|---------------|---------|-----------------------|
| Cavity DIP (J): | θ_{JA} | 135°C/W | Header (H): | θ_{JA} | 165°C/W | (Still Air) |
| Molded DIP (N): | θ_{JA} | 130°C/W | | θ_{JC} | 67°C/W | (400 LF/min Air Flow) |
| | | | | | 25°C/W | |

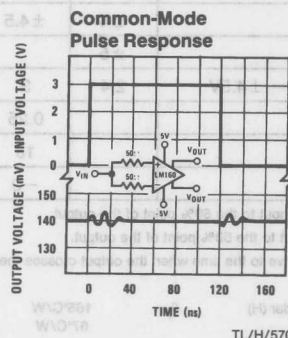
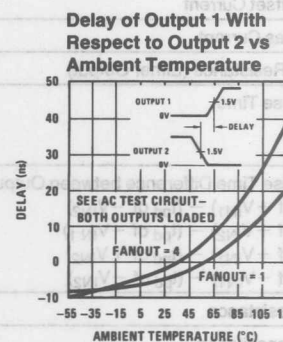
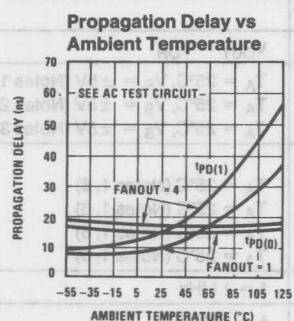
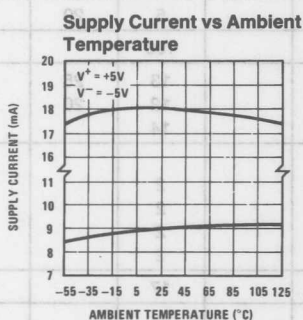
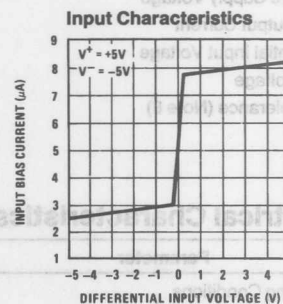
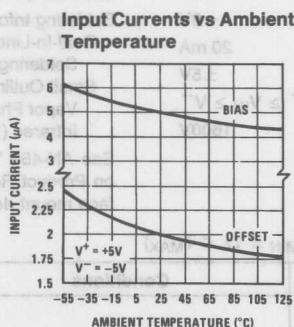
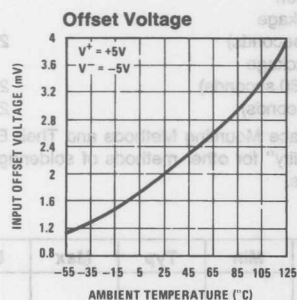
Note 5: The device may be damaged if used beyond the maximum ratings.

Note 6: Measurements are made in AC Test Circuit, Fanout = 1

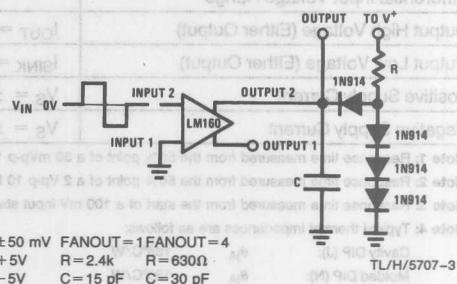
Note 7: Refer to RETS 160X for LM160H, LM160J-14 and LM160J military specifications.

Note 8: Human body model, 1.5 k Ω in series with 100 pF.

Typical Performance Characteristics



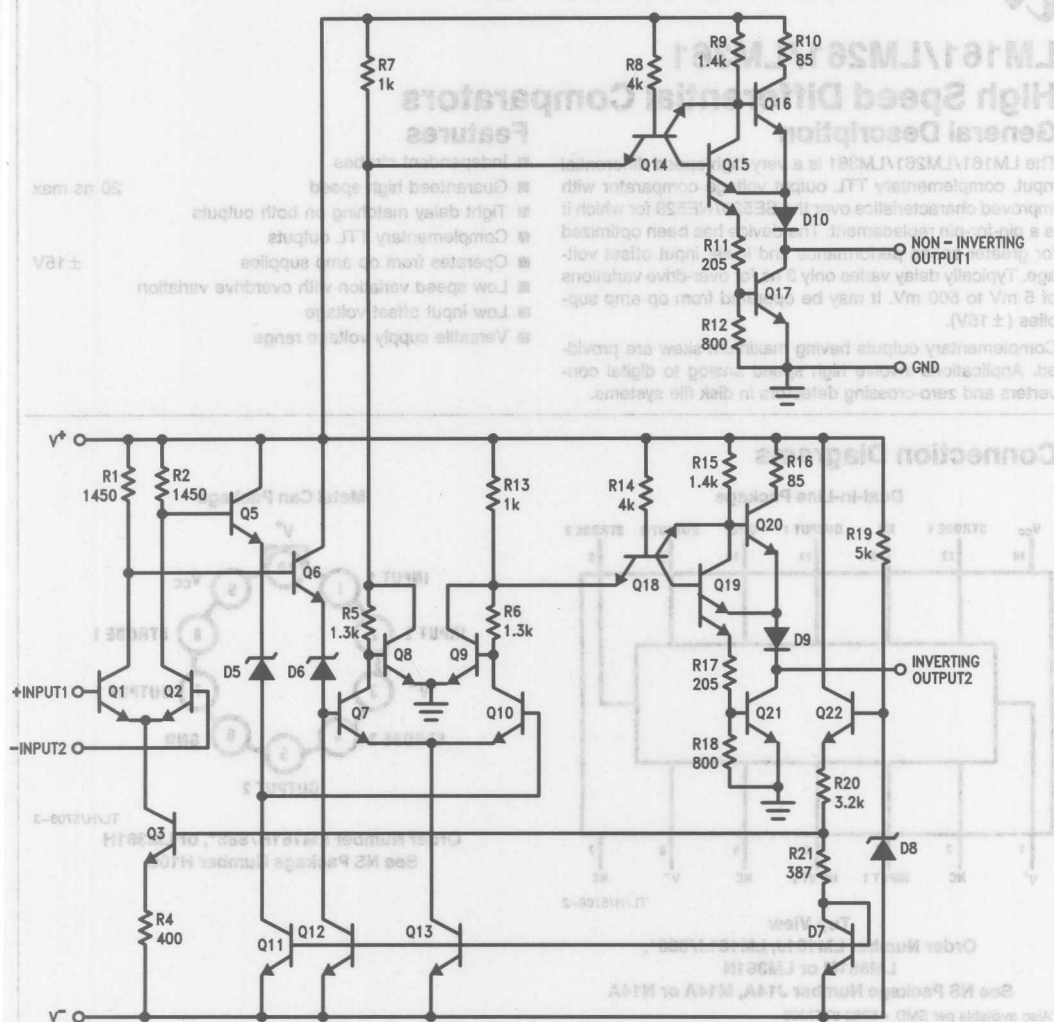
AC Test Circuit



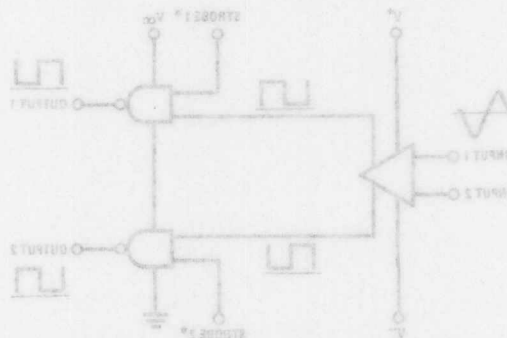
$V_{IN} = \pm 50 \text{ mV}$ FANOUT = 1 FANOUT = 4
 $V^+ = +5V$ $R = 2.4k$ $R = 630\Omega$
 $V^- = -5V$ $C = 15 \text{ pF}$ $C = 30 \text{ pF}$

TL/H/5707-2

Schematic Diagram



TL/H/5707-1



*Output is low when current is drawn from strobe pin.

LM160/LM360

LM161/LM261/LM361

High Speed Differential Comparators

General Description

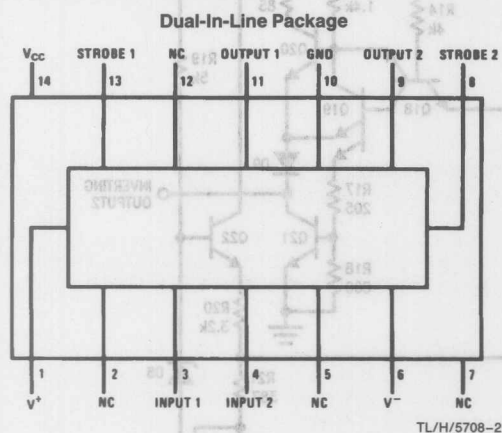
The LM161/LM261/LM361 is a very high speed differential input, complementary TTL output voltage comparator with improved characteristics over the SE529/NE529 for which it is a pin-for-pin replacement. The device has been optimized for greater speed performance and lower input offset voltage. Typically delay varies only 3 ns for over-drive variations of 5 mV to 500 mV. It may be operated from op amp supplies (± 15 V).

Complementary outputs having maximum skew are provided. Applications involve high speed analog to digital converters and zero-crossing detectors in disk file systems.

Features

- Independent strobes
- Guaranteed high speed 20 ns max
- Tight delay matching on both outputs
- Complementary TTL outputs
- Operates from op amp supplies ± 15 V
- Low speed variation with overdrive variation
- Low input offset voltage
- Versatile supply voltage range

Connection Diagrams

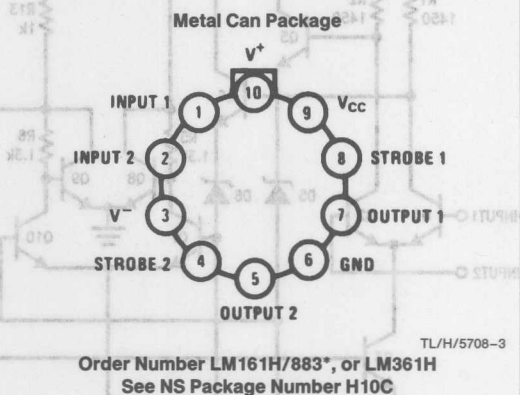


Top View

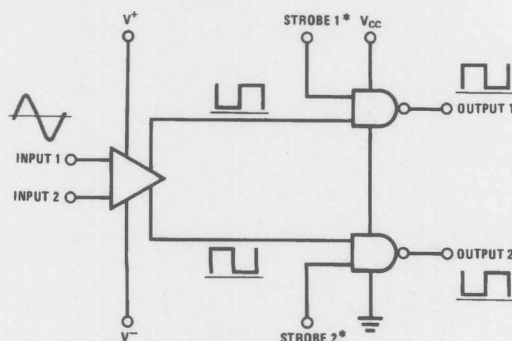
Order Number LM161J, LM161J/883*,
LM361M or LM361N

See NS Package Number J14A, M14A or N14A

*Also available per SMD #5962-8757203



Logic Diagram



please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

| | |
|------------------------------------|---------------------|
| Positive Supply Voltage, V^+ | +16V |
| Negative Supply Voltage, V^- | -16V |
| Gate Supply Voltage, V_{CC} | +7V |
| Output Voltage | +7V |
| Differential Input Voltage | $\pm 5V$ |
| Input Common Mode Voltage | $\pm 6V$ |
| Power Dissipation | 600 mW |
| Storage Temperature Range | -65°C to +150°C |
| Operating Temperature Range | T_{MIN} T_{MAX} |
| LM161 | -55°C to +125°C |
| LM261 | -25°C to +85°C |
| LM361 | 0°C to +70°C |
| Lead Temp. (Soldering, 10 seconds) | 260°C |
| For Any Device Lead Below V^- | 0.3V |

| | | |
|---|-------|-------|
| Supply Voltage V^+ | | |
| LM161/LM261 | 5V | 15V |
| LM361 | 5V | 15V |
| Supply Voltage V^- | | |
| LM161/LM261 | -6V | -15V |
| LM361 | -6V | -15V |
| Supply Voltage V_{CC} | | |
| LM161/LM261 | 4.5V | 5V |
| LM361 | 4.75V | 5V |
| ESD Tolerance (Note 5) | | 1600V |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | | 215°C |
| Infrared (15 seconds) | | 220°C |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | |

Electrical Characteristics ($V^+ = +10V$, $V_{CC} = +5V$, $V^- = -10V$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless noted)

| Parameter | Conditions | Limits | | | | | | Units |
|---|---|-------------|-----|------|-------|-----|------|-------|
| | | LM161/LM261 | | | LM361 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | | | 1 | 3 | | 1 | 5 | mV |
| Input Bias Current | T _A = 25°C | | 5 | 20 | | 10 | 30 | μA |
| Input Offset Current | T _A = 25°C | | 2 | 3 | | 2 | 5 | μA |
| Voltage Gain | T _A = 25°C | | 3 | | | 3 | | V/mV |
| Input Resistance | T _A = 25°C, f = 1 kHz | | 20 | | | 20 | | kΩ |
| Logical "1" Output Voltage | V _{CC} = 4.75V, I _{SOURCE} = −0.5 mA | 2.4 | 3.3 | | 2.4 | 3.3 | | V |
| Logical "0" Output Voltage | V _{CC} = 4.75V, I _{SINK} = 6.4 mA | | | 0.4 | | | 0.4 | V |
| Strobe Input "1" Current (Output Enabled) | V _{CC} = 5.25V, V _{STROBE} = 2.4V | | | 200 | | | 200 | μA |
| Strobe Input "0" Current (Output Disabled) | V _{CC} = 5.25V, V _{STROBE} = 0.4V | | | −1.6 | | | −1.6 | mA |
| Strobe Input "0" Voltage | V _{CC} = 4.75V | | | 0.8 | | | 0.8 | V |
| Strobe Input "1" Voltage | V _{CC} = 4.75V | 2 | | | 2 | | | V |
| Output Short Circuit Current | V _{CC} = 5.25V, V _{OUT} = 0V | −18 | | −55 | −18 | | −55 | mA |

Electrical Characteristics (Continued)(V⁺ = +10V, V_{CC} = +5V, V⁻ = -10V, T_{MIN} ≤ T_A ≤ T_{MAX}, unless noted)

| Parameter | Conditions | Limits | | | | | | Units |
|--|--|-------------|-----|-----|-------|-----|-----|-------|
| | | LM161/LM261 | | | LM361 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Supply Current I ⁺ | V ⁺ = 10V, V ⁻ = -10V, V _{CC} = 5.25V, -55°C ≤ T _A ≤ 125°C | | | 4.5 | | | | mA |
| Supply Current I ⁺ | V ⁺ = 10V, V ⁻ = -10V, V _{CC} = 5.25V, 0°C ≤ T _A ≤ 70°C | | | | | | 5 | mA |
| Supply Current I ⁻ | V ⁺ = 10V, V ⁻ = -10V, V _{CC} = 5.25V, -55°C ≤ T _A ≤ 125°C | | | 10 | | | | mA |
| Supply Current I ⁻ | V ⁺ = 10V, V ⁻ = -10V, V _{CC} = 5.25V, 0°C ≤ T _A ≤ 70°C | | | | | | 10 | mA |
| Supply Current I _{CC} | V ⁺ = 10V, V ⁻ = -10V, V _{CC} = 5.25V, -55°C ≤ T _A ≤ 125°C | | | 18 | | | | mA |
| Supply Current I _{CC} | V ⁺ = 10V, V ⁻ = -10V, V _{CC} = 5.25V, 0°C ≤ T _A ≤ 70°C | | | | | | 20 | mA |
| Transient Response | V _{IN} = 50 mV overdrive (Note 3) | | | | | | | |
| Propagation Delay Time (t _{pd(0)}) | T _A = 25°C | | 14 | 20 | | 14 | 20 | ns |
| Propagation Delay Time (t _{pd(1)}) | T _A = 25°C | | 14 | 20 | | 14 | 20 | ns |
| Delay Between Output A and B | T _A = 25°C | | 2 | 5 | | 2 | 5 | ns |
| Strobe Delay Time (t _{pd(0)}) | T _A = 25°C | | 8 | | | 8 | | ns |
| Strobe Delay Time (t _{pd(1)}) | T _A = 25°C | | 8 | | | 8 | | ns |

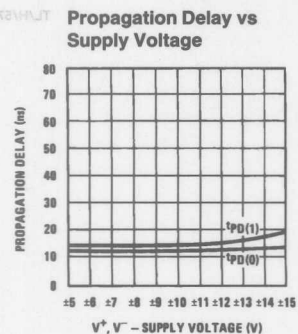
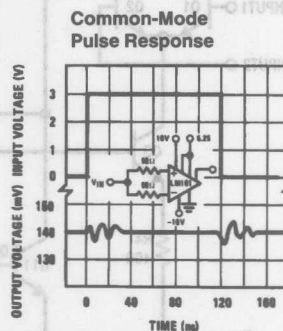
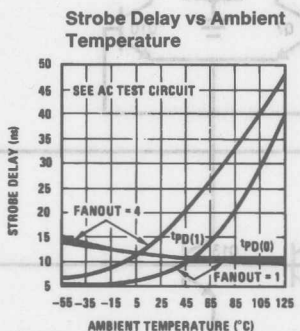
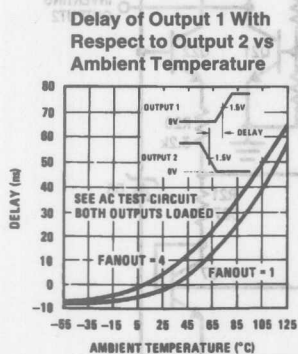
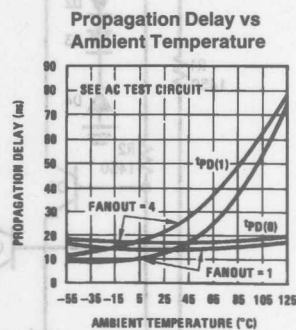
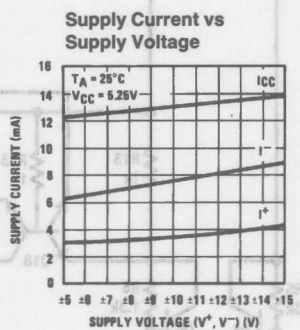
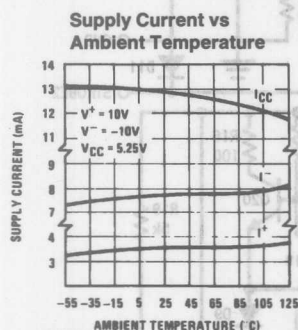
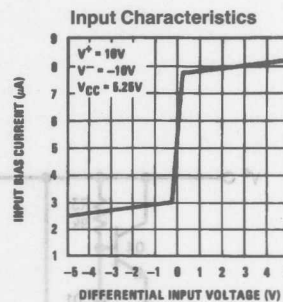
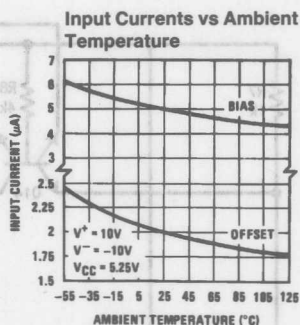
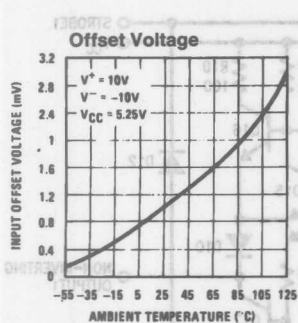
Note 1: The device may be damaged by use beyond the maximum ratings.**Note 2:** Typical thermal impedances are as follows:

| | H Package | J Package | N Package |
|-----------------|--|-----------|-----------|
| θ _{JA} | 165°C/W (Still Air) 67°C/W (400 LF/Min Air Flow) | 112°C/W | 105°C/W |
| θ _{JC} | 25°C/W | | |

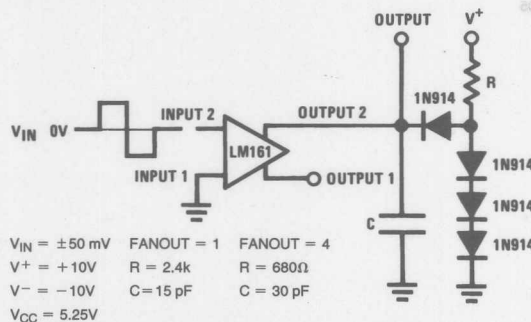
Note 3: Measurements using AC Test circuit, Fanout = 1. The devices are faster at low supply voltages.**Note 4:** Refer to RETS161X for LM161H and LM161J military specifications.**Note 5:** Human body model, 1.5 kΩ in series with 100 pF.

Typical Performance Characteristics

LM161/LM261/LM361



AC Test Circuit



TL/H/5708-5

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R

88.81R.01R



LM193/LM293/LM393/LM2903 Low Power Low Offset Voltage Dual Comparators

General Description

The LM193 series consists of two independent precision voltage comparators with an offset voltage specification as low as 2.0 mV max for two comparators which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM193 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, the LM193 series will directly interface with MOS logic where their low power drain is a distinct advantage over standard comparators.

Advantages

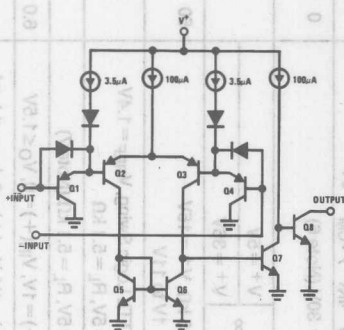
- High precision comparators
- Reduced V_{OS} drift over temperature

- Eliminates need for dual supplies
- Allows sensing near ground
- Compatible with all forms of logic
- Power drain suitable for battery operation

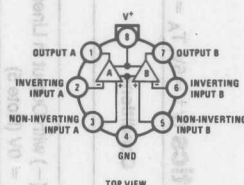
Features

- Wide supply
 - Voltage range 2.0V to 36V
 - single or dual supplies $\pm 1.0V$ to $\pm 18V$
- Very low supply current drain (0.4 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ± 5 nA
- and maximum offset voltage ± 3 mV
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage, 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams

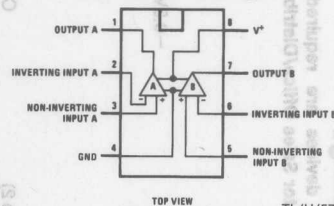


Metal Can Package



Order Number LM193H,
LM193H/883*,
LM193AH, LM193AH/883,
LM293H, LM293AH, LM393H
or LM393AH
See NS Package Number H08C

Dual-In-Line Package



Order Number LM193J/883*,
LM193AJ/883,
LM393J, LM393AJ,
LM393M, LM2903M, LM393N,
LM2903J or LM2903N
See NS Package Number J08A,
M08A or N08E

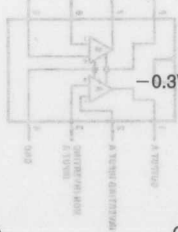
*Also available per JM38510/11202

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 10)

| | |
|---|---------------|
| Supply Voltage, V^+ | 36V |
| Differential Input Voltage (Note 8) | 36V |
| Input Voltage | -0.3V to +36V |
| Input Current ($V_{IN} < -0.3V$) (Note 3) | 50 mA |
| Power Dissipation (Note 1) | |
| Molded DIP | 780 mW |
| Metal Can | 660 mW |
| Small Outline Package | 510 mW |
| Output Short-Circuit to Ground (Note 2) | Continuous |



Operating Temperature Range

LM393/LM393A
LM293/LM293A
LM193/LM193A
LM2903

0°C to +70°C
-25°C to +85°C
-55°C to +125°C
-40°C to +85°C
-65°C to +150°C

Storage Temperature Range

Lead Temperature (Soldering, 10 seconds)

+260°C

Soldering Information

Dual-In-Line Package

Soldering (10 seconds)

260°C

Small Outline Package

Vapor Phase (60 seconds)

215°C

Infrared (15 seconds)

220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD rating (1.5 k Ω in series with 100 pF)

1300V

Electrical Characteristics ($V^+ = 5V$, $T_A = 25^\circ C$, unless otherwise stated)

| Parameter | Conditions | LM193A | | | LM293A, LM393A | | | LM193 | | | LM293, LM393 | | | LM2903 | | | Units |
|---------------------------------|---|--------|-----|-------------|----------------|-----|-------------|-------|-----|-------------|--------------|-----|-------------|--------|-----|-------------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 9) | 1.0 | | 2.0 | 1.0 | | 2.0 | 1.0 | | 5.0 | 1.0 | | 5.0 | 2.0 | | 7.0 | mV |
| Input Bias Current | $I_{IN}(+) \text{ or } I_{IN}(-)$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5) | 25 | | 100 | 25 | | 250 | 25 | | 100 | 25 | | 250 | 25 | | 250 | nA |
| Input Offset Current | $I_{IN}(+) - I_{IN}(-)$ $V_{CM} = 0V$ | 3.0 | | 25 | 5.0 | | 50 | 3.0 | | 25 | 5.0 | | 50 | 5.0 | | 50 | nA |
| Input Common Mode Voltage Range | $V^+ = 30V$ (Note 6) | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | 0 | | $V^+ - 1.5$ | V |
| Supply Current | $R_L = \infty$ $V^+ = 5V$ | 0.4 | | 1 | 0.4 | | 1 | 0.4 | | 1 | 0.4 | | 1 | 0.4 | | 1.0 | mA |
| | $V^+ = 36V$ | 1 | | 2.5 | 1 | | 2.5 | 1 | | 2.5 | 1 | | 2.5 | 1 | | 2.5 | mA |
| Voltage Gain | $R_L \geq 15 k\Omega$, $V^+ = 15V$ $V_O = 1V$ to $11V$ | 50 | | 200 | 50 | | 200 | 50 | | 200 | 50 | | 200 | 25 | | 100 | V/mV |
| Large Signal Response Time | $V_{IN} = TTL$ Logic Swing, $V_{REF} = 1.4V$ $V_{RL} = 5V$, $R_L = 5.1 k\Omega$ | 300 | | | 300 | | | 300 | | | 300 | | | 300 | | | ns |
| Response Time | $V_{RL} = 5V$, $R_L = 5.1 k\Omega$ (Note 7) | 1.3 | | | 1.3 | | | 1.3 | | | 1.3 | | | 1.5 | | | μs |
| Output Sink Current | $V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $V_O \leq 1.5V$ | 6.0 | | 16 | 6.0 | | 16 | 6.0 | | 16 | 6.0 | | 16 | 6.0 | | 16 | mA |
| Saturation Voltage | $V_{IN}(-) = 1V$, $V_{IN}(+) = 0$, $I_{SINK} \leq 4 mA$ | 250 | | 400 | 250 | | 400 | 250 | | 400 | 250 | | 400 | 250 | | 400 | mV |
| Output Leakage Current | $V_{IN}(-) = 0$, $V_{IN}(+) = 1V$, $V_O = 5V$ | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | | 0.1 | | | nA |

Electrical Characteristics ($V^+ = 5V$) (Note 4)

| Parameter | Conditions | LM193A | | LM293A, LM393A | | LM193 | | LM293, LM393 | | LM2903 | | Units | |
|---------------------------------|--|--------|-------------|----------------|-------------|-------|-------------|--------------|-------------|--------|-------------|-------|---------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | | Typ |
| Input Offset Voltage | (Note 9) | | | 4.0 | | | 4.0 | | 9 | | 9 | 15 | mV |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | | 100 | | | 150 | | 100 | | 150 | 200 | nA |
| Input Bias Current | $I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5) | | | 300 | | | 400 | | 300 | | 400 | 500 | nA |
| Input Common Mode Voltage Range | $V^+ = 30V$ (Note 6) | 0 | $V^+ - 2.0$ | 0 | $V^+ - 2.0$ | 0 | $V^+ - 2.0$ | 0 | $V^+ - 2.0$ | 0 | $V^+ - 2.0$ | | V |
| Saturation Voltage | $V_{IN(-)} = 1V$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4 \text{ mA}$ | | | 700 | | | 700 | | 700 | | 700 | | mV |
| Output Leakage Current | $V_{IN(-)} = 0$, $V_{IN(+)} = 1V$, $V_O = 30V$ | | | 1.0 | | | 1.0 | | 1.0 | | 1.0 | | μA |
| Differential Input Voltage | Keep All V_{IN} 's $\geq 0V$ (or V^- , if Used), (Note 8) | | | 36 | | | 36 | | 36 | | 36 | | V |

Note 1: For operating at high temperatures, the LM393/LM393A and LM2903 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 170°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM193/LM193A/LM293/LM293A must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100 \text{ mW}$), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+ .

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3V$.

Note 4: These specifications are limited to $-55^\circ C \leq T_A \leq +125^\circ C$, for the LM193/LM193A, With the LM293/LM293A all temperature specifications are limited to $-25^\circ C \leq T_A \leq +85^\circ C$ and the LM393/LM393A temperature specifications are limited to $0^\circ C \leq T_A \leq +70^\circ C$. The LM2903 is limited to $-40^\circ C \leq T_A \leq +85^\circ C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

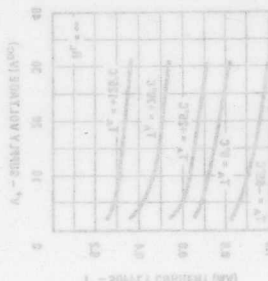
Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to 36V without damage, independent of the magnitude of V^+ .

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3V$ (or 0.3V below the magnitude of the negative power supply, if used).

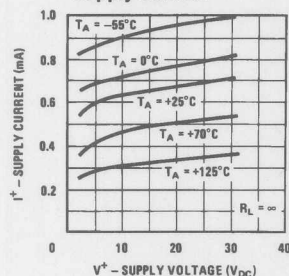
Note 9: At output switch point, $V_O \approx 1.4V$, $R_S = 0\Omega$ with V^+ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$), at 25°C.

Note 10: Refer to RETS193AX for LM193AH military specifications and to RETS193X for LM193H military specifications.

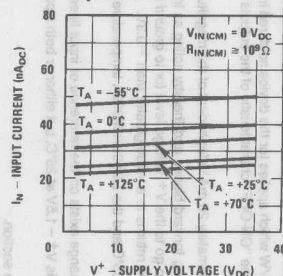


Typical Performance Characteristics LM193/LM293/LM393, LM193A/LM293A/LM393A

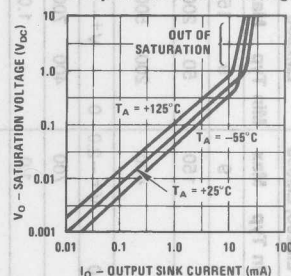
Supply Current



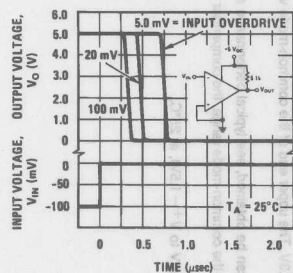
Input Current



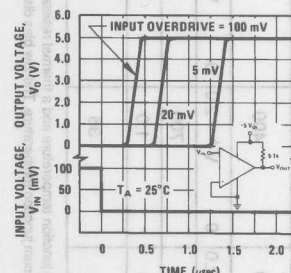
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



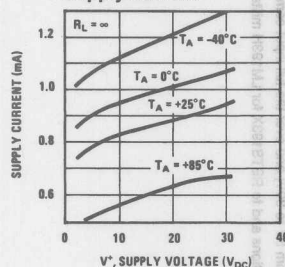
Response Time for Various Input Overdrives—Positive Transition



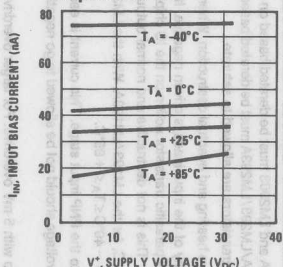
TL/H/5709-3

Typical Performance Characteristics LM2903

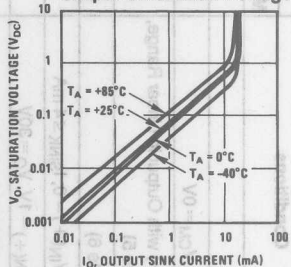
Supply Current



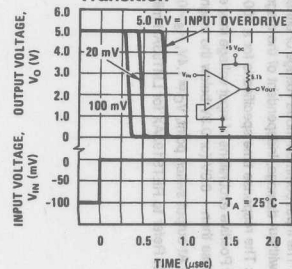
Input Current



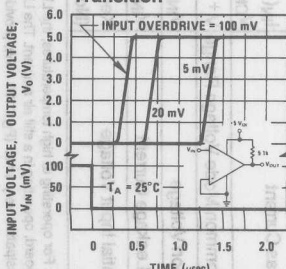
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



TL/H/5709-4

Application Hints

The LM193 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator change states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to $< 10 \text{ k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM193 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2.0 \text{ V}_{\text{DC}}$ to 30 V_{DC} .

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device (see Note 8). Protection should be provided to prevent the input voltages from going negative more than $-0.3 \text{ V}_{\text{DC}}$ (at 25°C). An input clamp diode can be used as shown in the applications section.

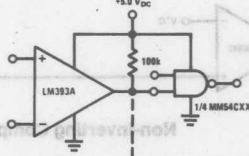
The output of the LM193 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM193 package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately $60\Omega \text{ } r_{\text{SAT}}$ of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V^+ = 5.0 \text{ V}_{\text{DC}}$)

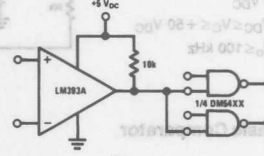
Basic Comparator



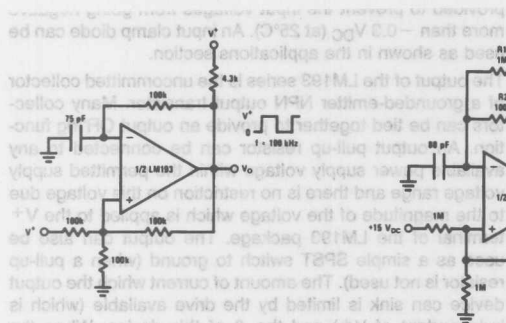
Driving CMOS



Driving TTL

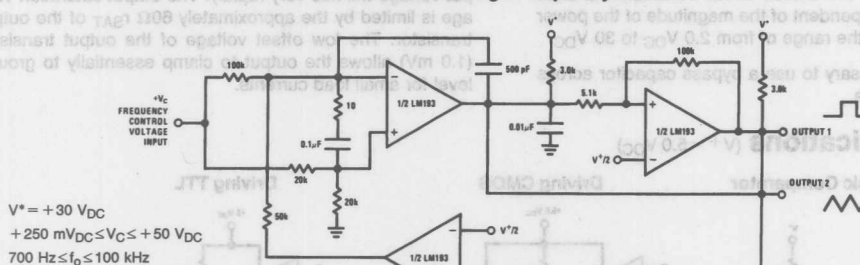


TL/H/5709-2



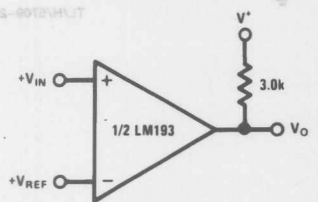
*For large ratios of $R1/R2$,
D1 can be omitted.

Two-Decade High-Frequency VCO



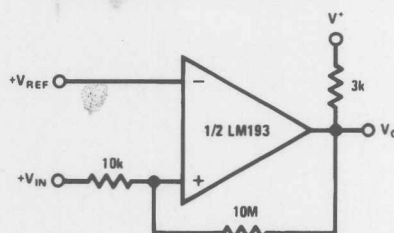
$V^+ = +30 V_{DC}$
 $+250 mV_{DC} \leq V_C \leq +50 V_{DC}$
 $700 Hz \leq f_o \leq 100 kHz$

Basic Comparator



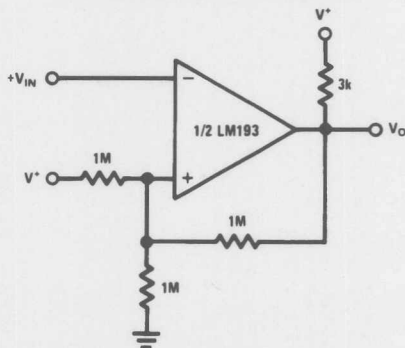
TL/H/5709-6

Non-Inverting Comparator with Hysteresis



TL/H/5709-9

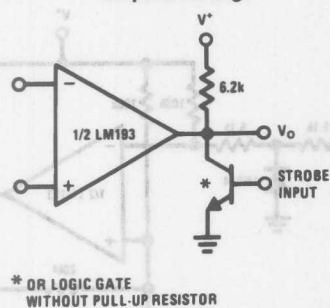
Inverting Comparator with Hysteresis



TL/H/5709-10

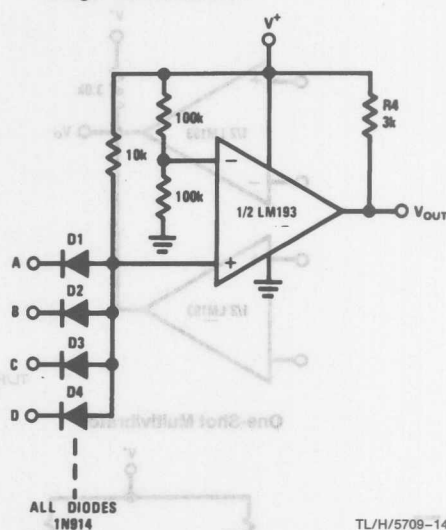
Typical Applications (Continued)

Output Strobing



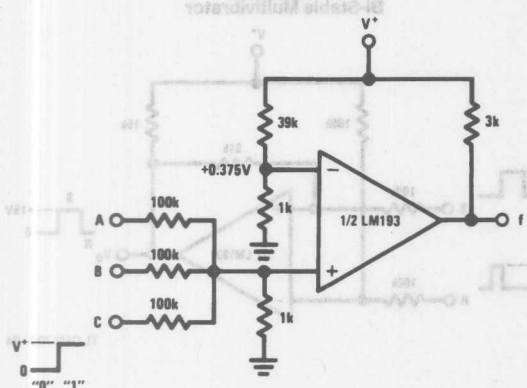
TL/H/5709-11

Large Fan-in AND Gate



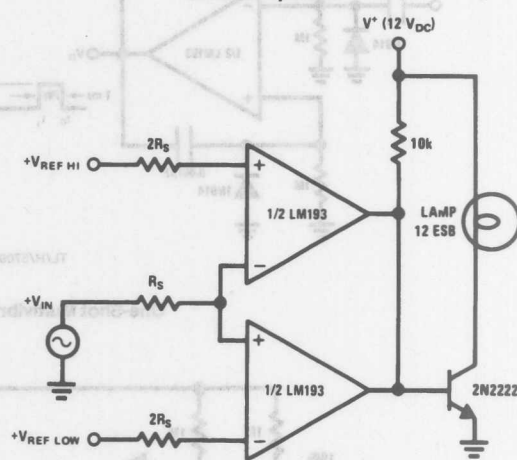
TL/H/5709-14

AND Gate



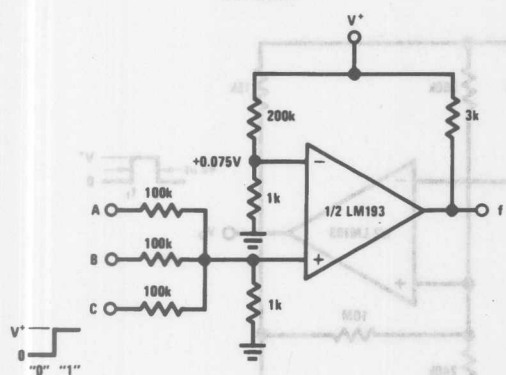
TL/H/5709-12

Limit Comparator



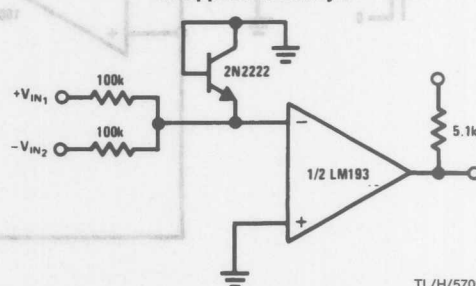
TL/H/5709-15

OR Gate



TL/H/5709-13

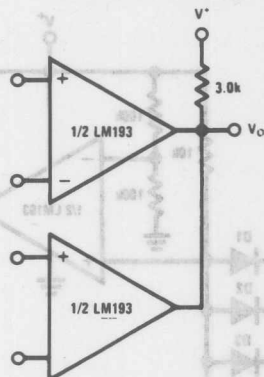
Comparing Input Voltages of Opposite Polarity



TL/H/5709-16

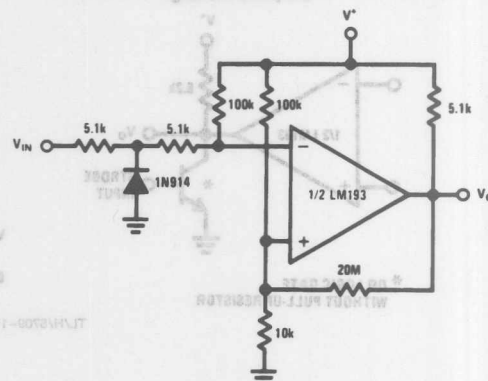
Typical Applications (Continued)

ORing the Outputs



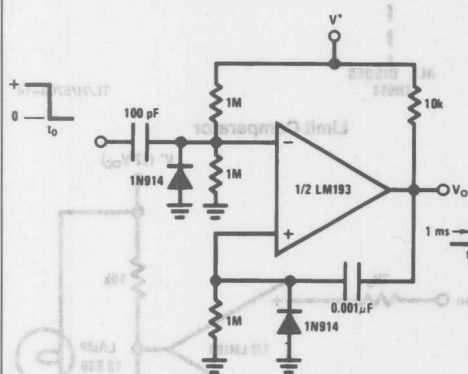
TL/H/5709-17

Zero Crossing Detector (Single Power Supply)



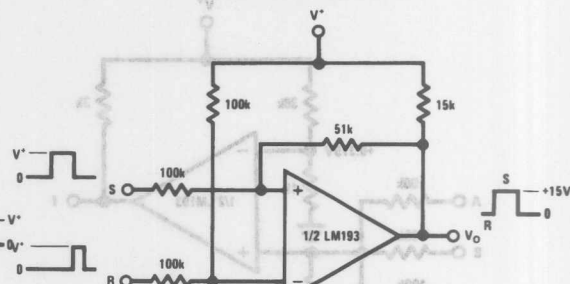
TL/H/5709-21

One-Shot Multivibrator



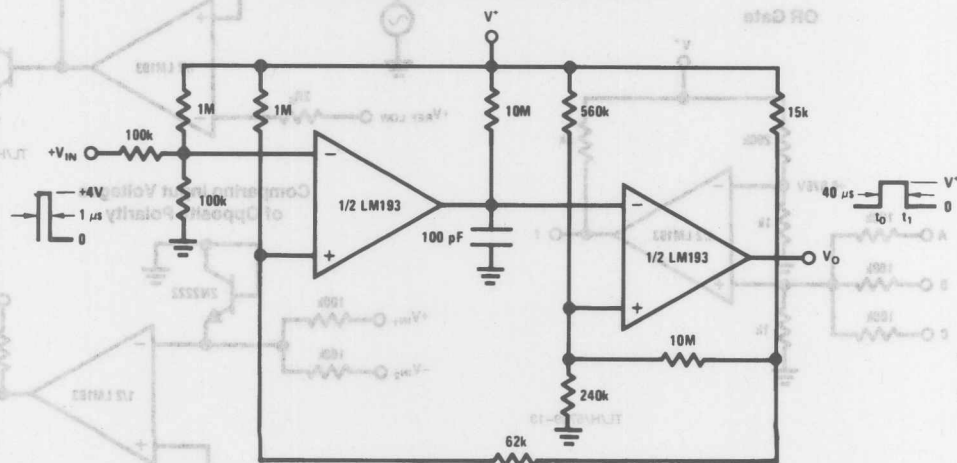
TL/H/5709-22

Bi-Stable Multivibrator



TL/H/5709-24

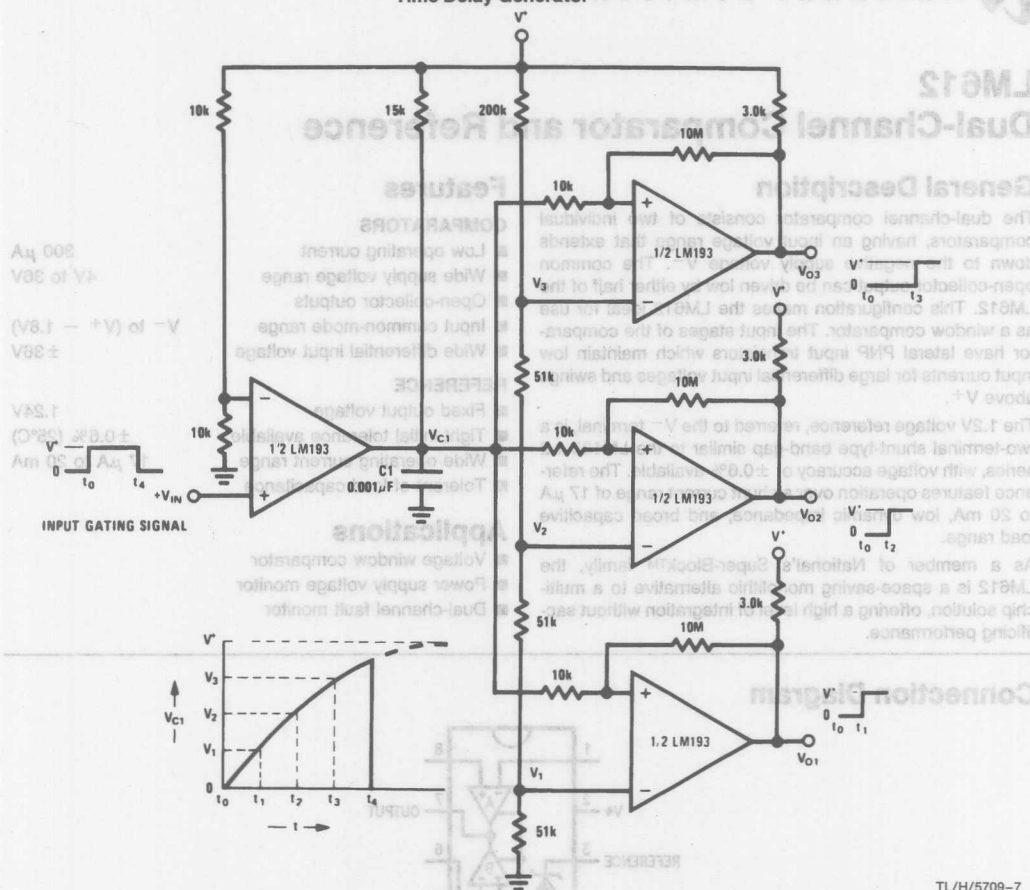
One-Shot Multivibrator with Input Lock Out



TL/H/5709-23

Typical Applications (Continued) ($V^+ = V_{DC}$)

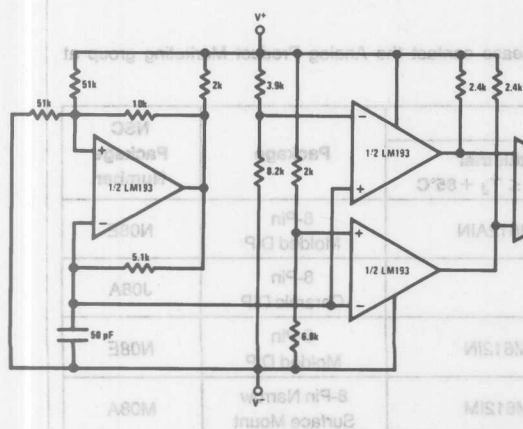
Time Delay Generator



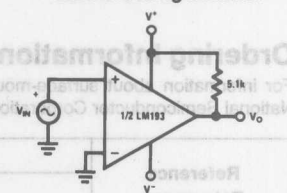
TL/H/5709-7

Split-Supply Applications ($V^+ = +15 V_{DC}$ and $V^- = -15 V_{DC}$)

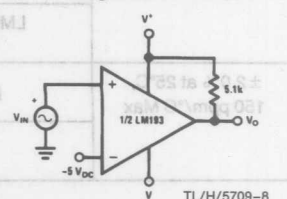
MOS Clock Driver



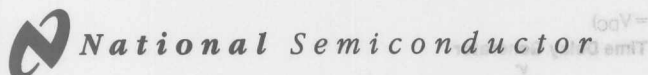
Zero Crossing Detector



Comparator With a Negative Reference



TL/H/5709-8



LM612 Dual-Channel Comparator and Reference

General Description

The dual-channel comparator consists of two individual comparators, having an input voltage range that extends down to the negative supply voltage V^- . The common open-collector output can be driven low by either half of the LM612. This configuration makes the LM612 ideal for use as a window comparator. The input stages of the comparator have lateral PNP input transistors which maintain low input currents for large differential input voltages and swings above V^+ .

The 1.2V voltage reference, referred to the V^- terminal, is a two-terminal shunt-type band-gap similar to the LM185-1.2 series, with voltage accuracy of $\pm 0.6\%$ available. The reference features operation over a shunt current range of $17 \mu\text{A}$ to 20 mA , low dynamic impedance, and broad capacitive load range.

As a member of National's Super-Block™ family, the LM612 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

- Low operating current 300 μA
- Wide supply voltage range 4V to 36V
- Open-collector outputs
- Input common-mode range V^- to $(V^+ - 1.8\text{V})$
- Wide differential input voltage $\pm 36\text{V}$

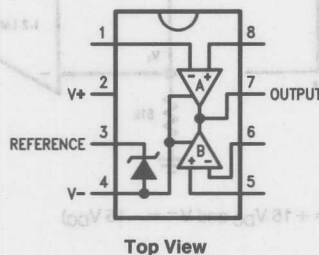
REFERENCE

- Fixed output voltage 1.24V
- Tight initial tolerance available $\pm 0.6\%$ (25°C)
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

- Voltage window comparator
- Power supply voltage monitor
- Dual-channel fault monitor

Connection Diagram



TL/H/11058-1

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corporation headquarters.

| Reference Tolerances | Temperature Range | | Package | NSC Package Number |
|--|--|---|-------------------------------|--------------------|
| | Military $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ | Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ | | |
| $\pm 0.6\%$ at 25°C, 80 ppm/°C Max | LM612AMN | LM612AIN | 8-Pin Molded DIP | N08E |
| | LM612AMJ/883 (Note 13) | | 8-Pin Ceramic DIP | J08A |
| $\pm 2.0\%$ at 25°C, 150 ppm/°C Max | LM612MN | LM612IN | 8-Pin Molded DIP | N08E |
| | | LM612IM | 8-Pin Narrow Surface Mount | M08A |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--|
| Voltage on Any Pin Except V_R (referred to V^- pin) | |
| (Note 2) | 36V (Max) |
| (Note 3) | -0.3V (Min) |
| Current through Any Input Pin and V_R Pin | ± 20 mA |
| Differential Input Voltage | ± 36 V |
| Output Short-Circuit Duration | (Note 4) |
| Storage Temperature Range | $-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ |
| Maximum Junction Temperature | 150°C |

Thermal Resistance, Junction-to-Ambient (Note 5)

N Package 100°C/W

Soldering Information

N Package

Soldering (10 seconds)

 260°C

ESD Tolerance (Note 6)

 ± 1 kV**Operating Temperature Range**

LM612AI, LM612I

 $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$

LM612AM, LM612M

 $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$

Electrical Characteristics These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = V^+ / 2$, $I_R = 100\ \mu\text{A}$, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM612AM LM612AI Limits (Note 8) | LM612M LM612I Limits (Note 8) | Units |
|---|--|---|---------------------|--|--|--|
| COMPARATORS | | | | | | |
| I_S | Total Supply Current | V^+ Current, $R_{\text{LOAD}} = \infty$, $3\text{V} \leq V^+ \leq 36\text{V}$ | 150 170 | 250 300 | 250 300 | μA Max μA Max |
| V_{OS} | Offset Voltage over V^+ Range | $4\text{V} \leq V^+ \leq 36\text{V}$, $R_L = 15\text{ k}\Omega$ | 1.0 2.0 | 3.0 6.0 | 5.0 7.0 | mV Max mV Max |
| V_{OS} | Offset Voltage over V_{CM} Range | $0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$, $V^+ = 30\text{V}$, $R_L = 15\text{ k}\Omega$ | 1.0 1.5 | 3.0 6.0 | 5.0 7.0 | mV Max mV Max |
| $\frac{\Delta V_{\text{OS}}}{\Delta T}$ | Average Offset Voltage Drift | | 15 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | 5 8 | 25 30 | 35 40 | nA Max nA Max |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA Max nA Max |
| A_V | Voltage Gain | $R_L = 10\text{ k}\Omega$ to 36V , $2\text{V} \leq V_{\text{OUT}} \leq 27\text{V}$ | 500 100 | 50 | 50 | V/mV Min V/mV |
| t_R | Large Signal Response Time | $V_{\text{IN}} = 1.4\text{V}$, $V_{\text{OUT}} = \text{TTL}$ Swing, $R_L = 5.1\text{ k}\Omega$ | 1.5 2.0 | | | μs μs |
| I_{SINK} | Output Sink Current | $V_{\text{IN}} = 0\text{V}$, $V_{\text{OUT}} = 1\text{V}$, $V_{\text{OUT}} = 1.5\text{V}$ | 20 13 | 10 8 | 10 8 | mA Min mA Min |
| | | $V_{\text{OUT}} = 0.4\text{V}$ | 2.8 2.4 | 1.0 0.5 | 0.8 0.5 | mA Min mA Min |
| I_L | Output Leakage Current | $V_{\text{IN}} = 1\text{V}$, $V_{\text{OUT}} = 0\text{V}$, $V_{\text{OUT}} = 36\text{V}$ | 0.1 0.2 | 10 | 10 | μA Max μA |

Operating Temperature Range. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 7) | LM612AM LM612AI Limits (Note 8) | LM612M LM612I Limits (Note 8) | Units |
|-----------------------------------|--------------------------------|---|---------------------|--|--|------------------------------|
| VOLTAGE REFERENCE (Note 9) | | | | | | |
| V_R | Reference Voltage | | 1.244 | 1.2365 1.2515 ($\pm 0.6\%$) | 1.2191 1.2689 ($\pm 2\%$) | V Min V Max |
| $\frac{\Delta V_R}{\Delta T}$ | Average Drift with Temperature | (Note 10) | 18 | 80 | 150 | ppm/°C Max |
| $\frac{\Delta V_R}{kH}$ | Average Drift with Time | $T_J = 40^\circ\text{C}$ $T_J = 150^\circ\text{C}$ | 400 1000 | | | ppm/kH ppm/kH |
| $\frac{\Delta V_R}{\Delta T_J}$ | Hysteresis | (Note 11) | 3.2 | | | $\mu\text{V}/^\circ\text{C}$ |
| $\frac{\Delta V_R}{\Delta I_R}$ | V_R Change with Current | $V_R[100\ \mu\text{A}] - V_R[17\ \mu\text{A}]$ | 0.05 0.1 | 1 1.1 | 1 1.1 | mV Max mV Max |
| | | $V_R[10\ \text{mA}] - V_R[100\ \mu\text{A}]$ (Note 12) | 1.5 2.0 | 5 5.5 | 5 5.5 | mV Max mV Max |
| R | Resistance | $\Delta V_R[10\ \text{mA to } 0.1\ \text{mA}]/9.9\ \text{mA}$ $\Delta V_R[100\ \mu\text{A to } 17\ \mu\text{A}]/83\ \mu\text{A}$ | 0.2 0.6 | 0.56 13 | 0.56 13 | Ω Max Ω Max |
| $\frac{\Delta V_R}{\Delta V^+}$ | V_R Change with V^+ Change | $V_R[V^+ = 5\text{V}] - V_R[V^+ = 36\text{V}]$ | 0.1 0.1 | 1.2 1.3 | 1.2 1.3 | mV Max mV Max |
| | | $V_R[V^+ = 5\text{V}] - V_R[V^+ = 3\text{V}]$ | 0.01 0.01 | 1 1.5 | 1 1.5 | mV Max mV Max |
| e_n | Voltage Noise | BW = 10 Hz to 10 kHz | 30 | | | μV_{RMS} |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is not allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting the Output to V^- will not cause power dissipation, so it may be continuous. However, shorting the Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If this total power causes the junction temperature to exceed 150°C , degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is $90^\circ\text{C}/\text{W}$ for the N package.

Note 6: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 7: Typical values in standard typeface are for $T_J = 25^\circ\text{C}$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for $T_J = 25^\circ\text{C}$ (standard type face) or over the full operating temperature range (**bold type face**).

Note 9: V_R is the reference output voltage, nominally 1.24V.

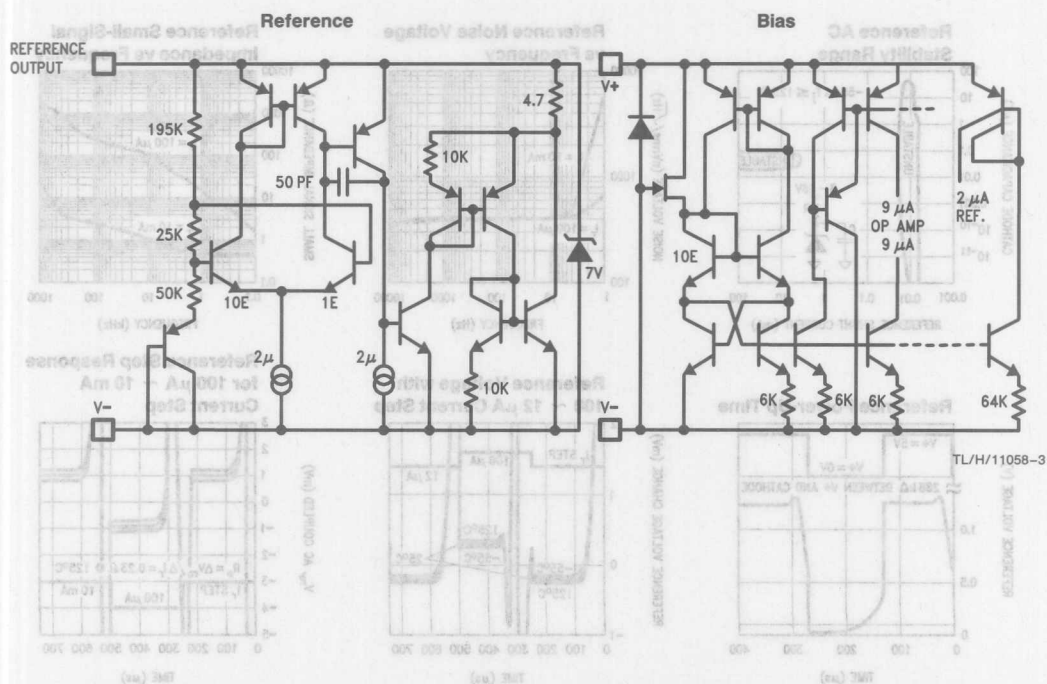
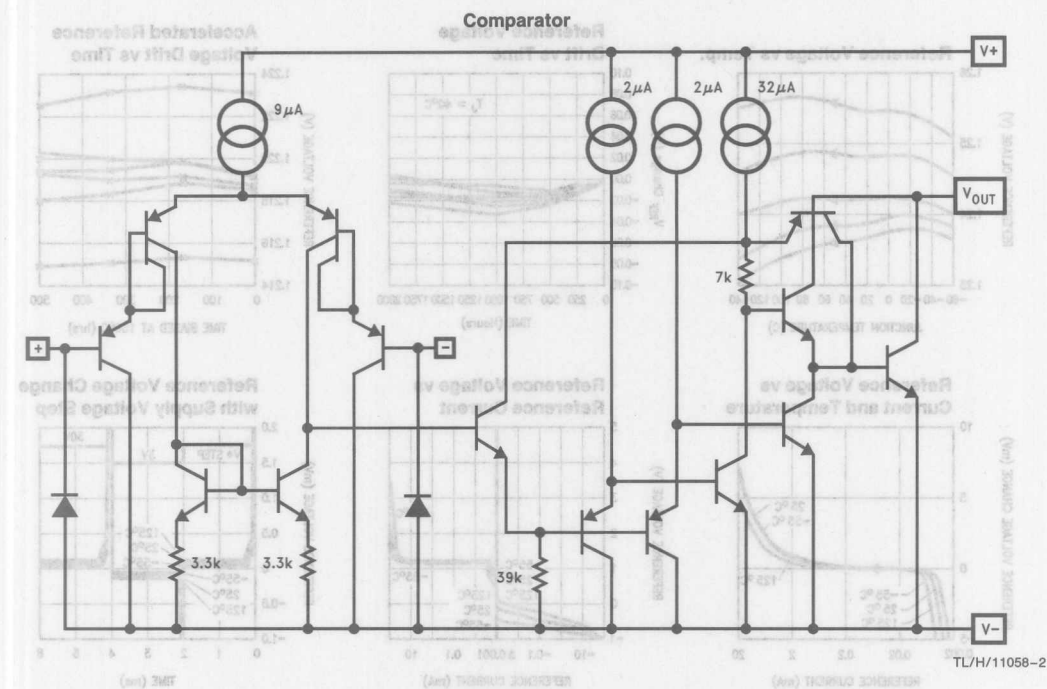
Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/°C, is $10^6 \cdot \Delta V_R / V_R[25^\circ\text{C}] \cdot \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_R[25^\circ\text{C}]$ is the value at 25°C , and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 11: Hysteresis is the change in V_R caused by a change in T_J , after the reference has been "dehysteresized". To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiralling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

Note 12: Low contact resistance is required for accurate measurement.

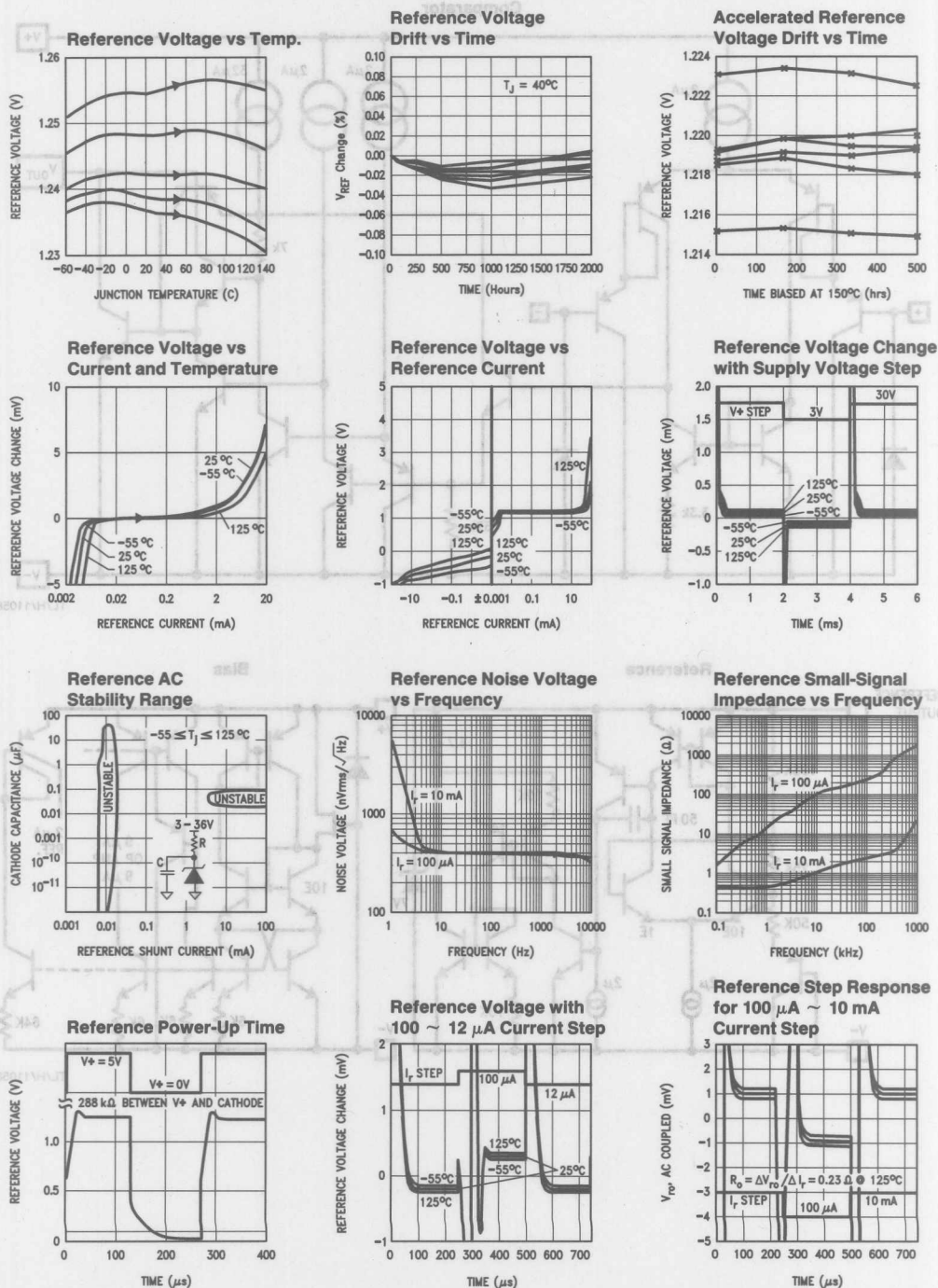
Note 13: A military RETS 612AMX electrical test specification is available on request. The military screened parts can also be procured as a Standard Military Drawing.

Simplified Schematic Diagrams



Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, $V^- = 0\text{V}$, unless otherwise noted

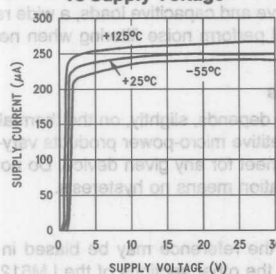


TL/H/11058-4

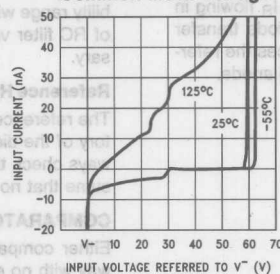
Typical Performance Characteristics (Comparators)

$T_J = 25^\circ\text{C}$, $V^+ = 5\text{V}$, $V^- = 0\text{V}$

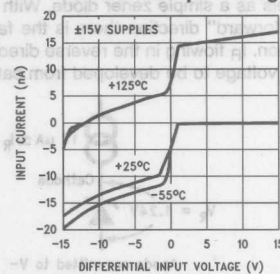
Supply Current vs Supply Voltage



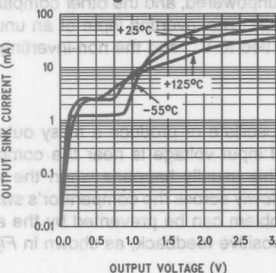
Input Bias Current vs Common-Mode Voltage



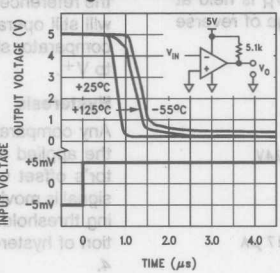
Input Current vs Differential Input Voltage



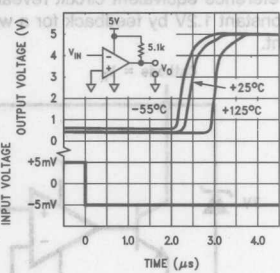
Output Saturation Voltage vs Sink Current



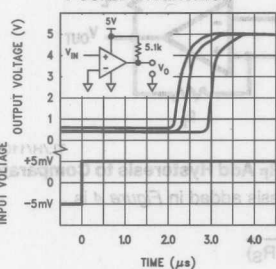
Small-Signal Response Times—Inverting Input, Negative Transition



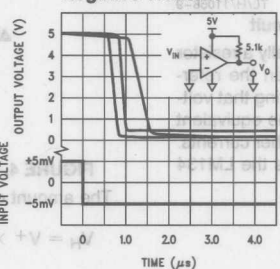
Small-Signal Response Times—Inverting Input, Positive Transition



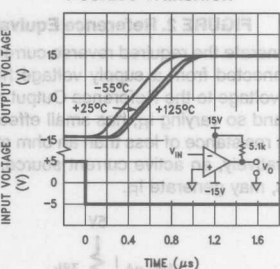
Small-Signal Response Times—Non-Inverting Input, Positive Transition



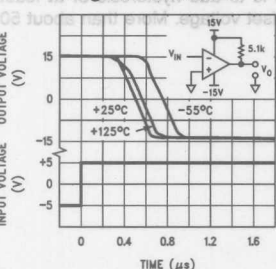
Small-Signal Response Times—Non-Inverting Input, Negative Transition



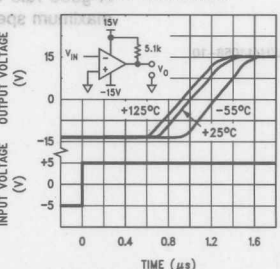
Large-Signal Response Times—Inverting Input, Positive Transition



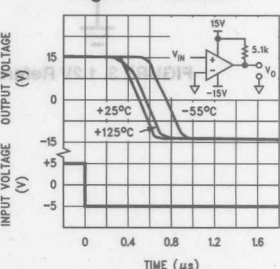
Large-Signal Response Times—Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



TL/H/11058-6

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_R flowing in the "forward" direction there is the familiar diode transfer function. I_R flowing in the reverse direction forces the reference voltage to be developed from cathode to anode.

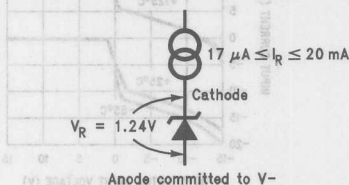


FIGURE 1. 1.24V Reference is Developed between Cathode and Anode; Current Source I_R is External

The reference equivalent circuit reveals how V_R is held at the constant 1.2V by feedback for a wide range of reverse current.

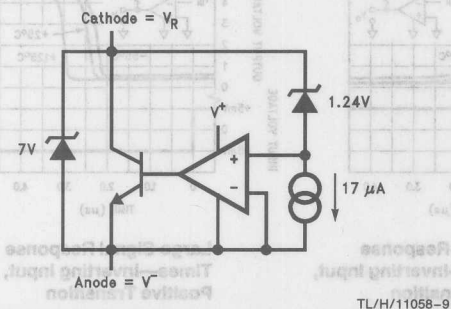


FIGURE 2. Reference Equivalent Circuit

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage to the Reference Output pin. Varying that voltage, and so varying I_R , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_R .

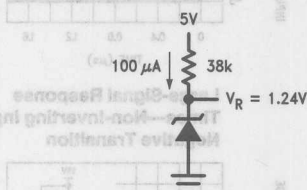


FIGURE 3. 1.2V Reference

the Reference AC Stability Range typical curve for capacitance values—from 20 μ A to 3 mA the reference is stable for any value of capacitance. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering when necessary.

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the datasheet for any given device. Do not assume that no specification means no hysteresis.

COMPARATORS

Either comparator or the reference may be biased in any way with no effect on the other sections of the LM612, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparator will still operate correctly. The inverting input of an unused comparator should be tied to V^- and the non-inverting tied to V^+ .

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in Figure 4.

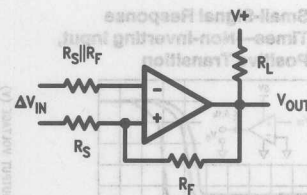


FIGURE 4. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in Figure 4 is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \quad \text{for } R_F \gg R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV

Application Information (Continued)

of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

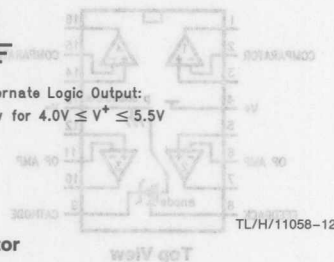
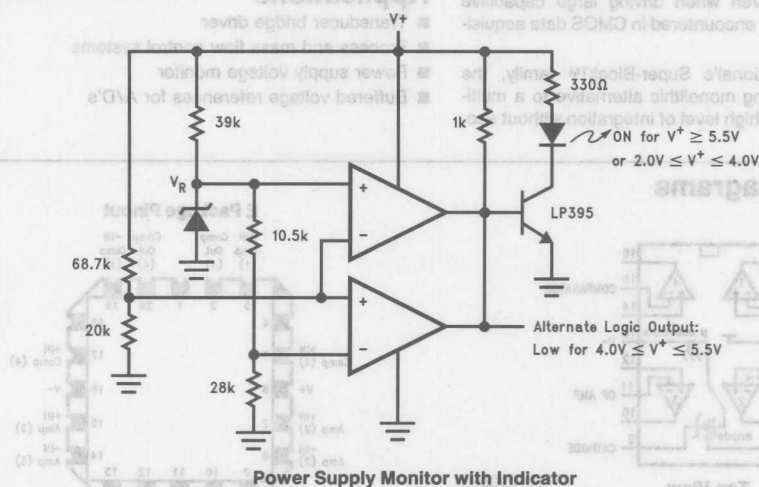
The guaranteed common-mode input voltage range for an LM612 is $V^- \leq V_{CM} \leq (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than $(V^- + 32V)$, even if this is greater than V^+ , the output will be at the correct state. If, however, either or both inputs are driven below V^- , and either input current exceeds $10 \mu A$, the output state is not guaranteed to be correct. If both inputs are above $(V^+ - 1.8V)$, the output state is also not guaranteed to be correct.

Output Stage

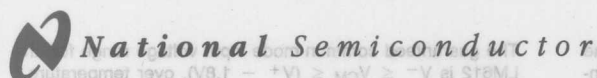
The comparators have a common open-collector output stage which requires a pull-up resistor to a positive supply voltage for the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.

Typical Applications



| Drawing | Package | Temperature Range | | | Reference Tolerance & Vos |
|---------|------------------------------|---|---|--|---|
| | | Commercial $-40^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | Industrial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ | Military $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | |
| N198 | 18-Pin Molded DIP | — | LM612AIN | LM612AMN | $\pm 0.8\%$ $80 \text{ ppm}/^{\circ}\text{C Max}$ $V_{OS} \leq 3.5 \text{ mV}$ |
| J18A | 18-Pin Ceramic DIP | — | — | LM612AMJ18B3 (Note 14) | |
| E20A | 20-Pin LCC | — | — | LM612AME18B3 (Note 14) | |
| N198 | 18-Pin Molded DIP | LM612CN | LM612IN | LM612MN | $\pm 2.0\%$ $150 \text{ ppm}/^{\circ}\text{C Max}$ $V_{OS} \leq 8.0 \text{ mV Max}$ |
| M183 | 18-Pin Wide Surface Mount | — | LM612WN | — | |



LM613 Dual Operational Amplifiers, Dual Comparators, and Adjustable Reference

General Description

The LM613 consists of dual op-amps, dual comparators, and a programmable voltage reference in a 16-pin package. The op-amps out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement, and data acquisition systems.

Combining a stable voltage reference with wide output swing op-amps makes the LM613 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode-signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM613 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

OP AMP

- Low operating current (Op Amp) 300 μ A
- Wide supply voltage range 4V to 36V
- Wide common-mode range V^- to $(V^+ - 1.8V)$
- Wide differential input voltage $\pm 36V$
- Available in plastic package rated for Military Temp. Range Operation

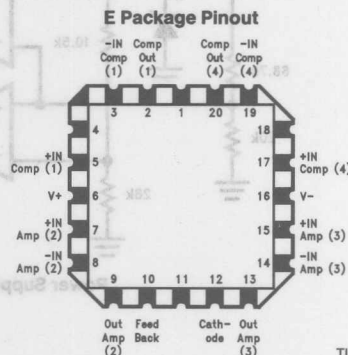
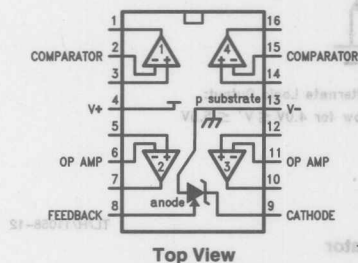
REFERENCE

- Adjustable output voltage 1.2V to 6.3V
- Tight initial tolerance available $\pm 0.6\%$
- Wide operating current range 17 μ A to 20 mA
- Tolerant of load capacitance

Applications

- Transducer bridge driver
- Process and mass flow control systems
- Power supply voltage monitor
- Buffered voltage references for A/D's

Connection Diagrams



Ordering Information

| Reference Tolerance & V _{OS} | Temperature Range | | | Package | NSC Drawing |
|--|--|---|---|---------------------------|-------------|
| | Military $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ | Industrial $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ | Commercial $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ | | |
| $\pm 0.6\%$ 80 ppm/ $^{\circ}\text{C}$ Max. $V_{OS} \leq 3.5$ mV | LM613AMN | LM613AIN | — | 16-Pin Molded DIP | N16E |
| | LM613AMJ/883 (Note 14) | — | — | 16-Pin Ceramic DIP | J16A |
| | LM613AME/883 (Note 14) | — | — | 20-Pin LCC | E20A |
| $\pm 2.0\%$ 150 ppm/ $^{\circ}\text{C}$ Max. $V_{OS} \leq 5.0$ mV Max. | LM613MN | LM613IN | LM613CN | 16-Pin Molded DIP | N16E |
| | — | LM613IWM | — | 16-Pin Wide Surface Mount | M16B |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage on Any Pin Except V_R (referred to V^- pin)
(Note 2) 36V (Max)
(Note 3) -0.3V (Min)

Current through Any Input Pin & V_R Pin ± 20 mA

Differential Input Voltage
Military and Industrial ± 36 V
Commercial ± 32 V

Storage Temperature Range $-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$

Maximum Junction Temperature (Note 4) 150°C

Thermal Resistance, Junction-to-Ambient (Note 5)

N Package 100°C/W

WM Package 150°C/W

Soldering Information (10 Seconds)

N Package 260°C

WM Package 220°C

ESD Tolerance (Note 6) ± 1 kV

Operating Temperature Range

LM613AI, LM613BI -40°C to $+85^\circ\text{C}$

LM613AM, LM613M -55°C to $+125^\circ\text{C}$

LM613C $0^\circ\text{C} \leq T_J \leq +70^\circ\text{C}$

Electrical Characteristics These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100 \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM613AM LM613AI Limits (Note 8) | LM613M LM613I Limits (Note 8) | Units |
|--------|----------------------|---|---------------------|--|--|--|
| I_S | Total Supply Current | $R_{\text{LOAD}} = \infty$, $4\text{V} \leq V^+ \leq 36\text{V}$ (32V for LM613C) | 450 550 | 940 1000 | 1000 1070 | μA (Max) μA (Max) |
| V_S | Supply Voltage Range | | 2.2 2.9 | 2.8 3 | 2.8 3 | V (Min) V (Min) |
| | | | 46 43 | 36 36 | 32 32 | V (Max) V (Max) |

OPERATIONAL AMPLIFIERS

| | | | | | | |
|-----------------------------------|--------------------------------------|---|-------------------|-------------------|-------------------|---------------------------------------|
| V_{OS1} | V_{OS} Over Supply | $4\text{V} \leq V^+ \leq 36\text{V}$ ($4\text{V} \leq V^+ \leq 32\text{V}$ for LM613C) | 1.5 2.0 | 3.5 6.0 | 5.0 7.0 | mV (Max) mV (Max) |
| V_{OS2} | V_{OS} Over V_{CM} | $V_{\text{CM}} = 0\text{V}$ through $V_{\text{CM}} =$ ($V^+ - 1.8\text{V}$), $V^+ = 30\text{V}$, $V^- = 0\text{V}$ | 1.0 1.5 | 3.5 6.0 | 5.0 7.0 | mV (Max) mV (Max) |
| $\frac{V_{\text{OS3}}}{\Delta T}$ | Average V_{OS} Drift | (Note 8) | 15 | | | $\mu\text{V}/^\circ\text{C}$ (Max) |
| I_B | Input Bias Current | | 10 11 | 25 30 | 35 40 | nA (Max) nA (Max) |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA (Max) nA (Max) |
| $\frac{I_{\text{OS1}}}{\Delta T}$ | Average Offset Current | | 4 | | | $\text{pA}/^\circ\text{C}$ |
| R_{IN} | Input Resistance | Differential | 1000 | | | M Ω |
| C_{IN} | Input Capacitance | Common-Mode | 6 | | | pF |
| e_n | Voltage Noise | $f = 100$ Hz, Input Referred | 74 | | | $\text{nV}/\sqrt{\text{Hz}}$ |
| I_n | Current Noise | $f = 100$ Hz, Input Referred | 58 | | | $\text{fA}/\sqrt{\text{Hz}}$ |
| CMRR | Common-Mode Rejection Ratio | $V^+ = 30\text{V}$, $0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$ $\text{CMRR} = 20 \log (\Delta V_{\text{CM}} / \Delta V_{\text{OS}})$ | 95 90 | 80 75 | 75 70 | dB (Min) dB (Min) |
| PSRR | Power Supply Rejection Ratio | $4\text{V} \leq V^+ \leq 30\text{V}$, $V_{\text{CM}} = V^+ / 2$, $\text{PSRR} = 20 \log (\Delta V^+ / V_{\text{OS}})$ | 110 100 | 80 75 | 75 70 | dB (Min) dB (Min) |
| A_v | Open Loop Voltage Gain | $R_L = 10 \text{ k}\Omega$ to GND, $V^+ = 30\text{V}$, $5\text{V} \leq V_{\text{OUT}} \leq 25\text{V}$ | 500 50 | 100 40 | 94 40 | V/mV (Min) |

Electrical Characteristics These specifications apply for $V_{-} = \text{GND} = 0\text{V}$, $V^{+} = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^{\circ}\text{C}$; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 7) | LM613AM LM613AI Limits (Note 8) | LM613M LM613I Limits (Note 8) | Units |
|---|-------------------------------------|---|--|--|---|--|
| OPERATIONAL AMPLIFIERS (Continued) | | | | | | |
| SR | Slew Rate | $V^{+} = 30\text{V}$ (Note 9) | 0.70 0.65 | 0.55 0.45 | 0.50 0.45 | $\text{V}/\mu\text{s}$ |
| GBW | Gain Bandwidth | $C_{\text{L}} = 50\text{ pF}$ | 0.8 0.5 | | | MHz |
| V_{O1} | Output Voltage Swing High | $R_{\text{L}} = 10\text{ k}\Omega$ to GND, $V^{+} = 36\text{V}$ (32V for LM613C) | $V^{+} + 1.4$ $V^{+} + 1.6$ | $V^{+} + 1.7$ $V^{+} + 1.9$ | $V^{+} + 1.8$ $V^{+} + 1.9$ | V (Min) V (Min) |
| V_{O2} | Output Voltage Swing Low | $R_{\text{L}} = 10\text{ k}\Omega$ to V^{+} , $V^{+} = 36\text{V}$ (32V for LM613C) | $V^{-} + 0.8$ $V^{-} + 0.9$ | $V^{-} + 0.9$ $V^{-} + 1.0$ | $V^{-} + 0.95$ $V^{-} + 1.0$ | V (Max) V (Max) |
| I_{OUT} | Output Source Current | $V_{\text{OUT}} = 2.5\text{V}$, $V^{+}_{\text{IN}} = 0\text{V}$, $V^{-}_{\text{IN}} = -0.3\text{V}$ | 25 15 | 20 13 | 16 13 | mA (Min) mA (Min) |
| I_{SINK} | Output Sink Current | $V_{\text{OUT}} = 1.6\text{V}$, $V^{+}_{\text{IN}} = 0\text{V}$, $V^{-}_{\text{IN}} = 0.3\text{V}$ | 17 9 | 14 8 | 13 8 | mA (Min) mA (Min) |
| I_{SHORT} | Short Circuit Current | $V_{\text{OUT}} = 0\text{V}$, $V^{+}_{\text{IN}} = 3\text{V}$, $V^{-}_{\text{IN}} = 2\text{V}$ | 30 40 | 50 60 | 50 60 | mA (Max) mA (Max) |
| | | $V_{\text{OUT}} = 5\text{V}$, $V^{+}_{\text{IN}} = 2\text{V}$, $V^{-}_{\text{IN}} = 3\text{V}$ | 30 32 | 60 80 | 70 90 | mA (Max) mA (Max) |
| COMPARATORS | | | | | | |
| V_{OS} | Offset Voltage | $4\text{V} \leq V^{+} \leq 36\text{V}$ (32V for LM613C), $R_{\text{L}} = 15\text{ k}\Omega$ | 1.0 2.0 | 3.0 6.0 | 5.0 7.0 | mV (Max) mV (Max) |
| V_{OS} V_{CM} | Offset Voltage over V_{CM} | $0\text{V} \leq V_{\text{CM}} \leq 36\text{V}$ $V^{+} = 36\text{V}$, (32V for LM613C) | 1.0 1.5 | 3.0 6.0 | 5.0 7.0 | mV (Max) mV (Max) |
| V_{OS} ΔT | Average Offset Voltage Drift | | 15 | | | $\mu\text{V}/^{\circ}\text{C}$ (Max) |
| I_{B} | Input Bias Current | | 5 8 | 25 30 | 35 40 | nA (Max) nA (Max) |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA (Max) nA (Max) |
| A_{V} | Voltage Gain | $R_{\text{L}} = 10\text{ k}\Omega$ to 36V (32V for LM613C) $2\text{V} \leq V_{\text{OUT}} \leq 27\text{V}$ | 500 100 | | | V/mV V/mV |
| t_{r} | Large Signal Response Time | $V^{+}_{\text{IN}} = 1.4\text{V}$, $V^{-}_{\text{IN}} = \text{TTL Swing}$, $R_{\text{L}} = 5.1\text{ k}\Omega$ | 1.5 2.0 | | | μs μs |
| I_{SINK} | Output Sink Current | $V^{+}_{\text{IN}} = 0\text{V}$, $V^{-}_{\text{IN}} = 1\text{V}$, $V_{\text{OUT}} = 1.5\text{V}$ | 20 13 | 10 8 | 10 8 | mA (Min) mA (Min) |
| | | $V_{\text{OUT}} = 0.4\text{V}$ | 2.8 2.4 | 1.0 0.5 | 0.8 0.5 | mA (Min) mA (Min) |
| I_{LEAK} | Output Leakage Current | $V^{+}_{\text{IN}} = 1\text{V}$, $V^{-}_{\text{IN}} = 0\text{V}$, $V_{\text{OUT}} = 36\text{V}$ (32V for LM613C) | 0.1 0.2 | 10 | 10 | μA (Max) μA (Max) |

Electrical Characteristics These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_R = 100\text{ }\mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over **Operating Temperature Range**. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 7) | LM613AM LM613AI Limits (Note 8) | LM613M LM613I Limits (Note 8) | Units |
|------------------------------------|--|--|---------------------|--|--|--------------------------------|
| VOLTAGE REFERENCE | | | | | | |
| V_R | Voltage Reference | (Note 10) | 1.244 | 1.2365 1.2515 ($\pm 0.6\%$) | 1.2191 1.2689 ($\pm 2\%$) | V (Min) V (Max) |
| $\frac{\Delta V_R}{\Delta T}$ | Average Temp. Drift | (Note 11) | 10 | 80 | 150 | ppm/ $^\circ\text{C}$ (Max) |
| $\frac{\Delta V_R}{\Delta T_J}$ | Hysteresis | (Note 12) | 3.2 | | | $\mu\text{V}/^\circ\text{C}$ |
| $\frac{\Delta V_R}{\Delta I_R}$ | V_R Change with Current | $V_R(100\text{ }\mu\text{A}) - V_R(17\text{ }\mu\text{A})$ | 0.05 0.1 | 1 1.1 | 1 1.1 | mV (Max) mV (Max) |
| | | $V_R(10\text{ mA}) - V_R(100\text{ }\mu\text{A})$ (Note 13) | 1.5 2.0 | 5 5.5 | 5 5.5 | mV (Max) mV (Max) |
| R | Resistance | $\Delta V_R(10 \rightarrow 0.1\text{ mA})/9.9\text{ mA}$ | 0.2 | 0.56 | 0.56 | Ω (Max) |
| | | $\Delta V_R(100 \rightarrow 17\text{ }\mu\text{A})/83\text{ }\mu\text{A}$ | 0.6 | 13 | 13 | Ω (Max) |
| $\frac{V_R}{\Delta V_{\text{RO}}}$ | V_R Change with High V_{RO} | $V_R(V_{\text{RO}} = V_R) - V_R(V_{\text{RO}} = 6.3\text{V})$ (5.06V between Anode and FEEDBACK) | 2.5 2.8 | 7 10 | 7 10 | mV (Max) mV (Max) |
| $\frac{V_R}{\Delta V^+}$ | V_R Change with V_{ANODE} Change | $V_R(V^+ = 5\text{V}) - V_R(V^+ = 36\text{V})$ ($V^+ = 32\text{V}$ for LM613C) | 0.1 0.1 | 1.2 1.3 | 1.2 1.3 | mV (Max) mV (Max) |
| | | $V_R(V^+ = 5\text{V}) - V_R(V^+ = 3\text{V})$ | 0.01 0.01 | 1 1.5 | 1 1.5 | mV (Max) mV (Max) |
| I_{FB} | FEEDBACK Bias Current | $V_{\text{ANODE}} \leq V_{\text{FB}} \leq 5.06\text{V}$ | 22 29 | 35 40 | 50 55 | nA (Max) nA (Max) |
| e_n | V_R Noise | 10 Hz to 10 kHz, $V_{\text{RO}} = V_R$ | 30 | | | μVRMS |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Simultaneous short-circuit of multiple comparators while using high supply voltages may force junction temperature above maximum, and thus should not be continuous.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is $90^\circ\text{C}/\text{W}$ for the N package, and $135^\circ\text{C}/\text{W}$ for the WM package.

Note 6: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 7: Typical values in standard typeface are for $T_J = 25^\circ\text{C}$; values in **bold face type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold type face**).

Note 9: Slew rate is measured with the op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and @ 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and the output voltage transition is sampled at 20V and 10V.

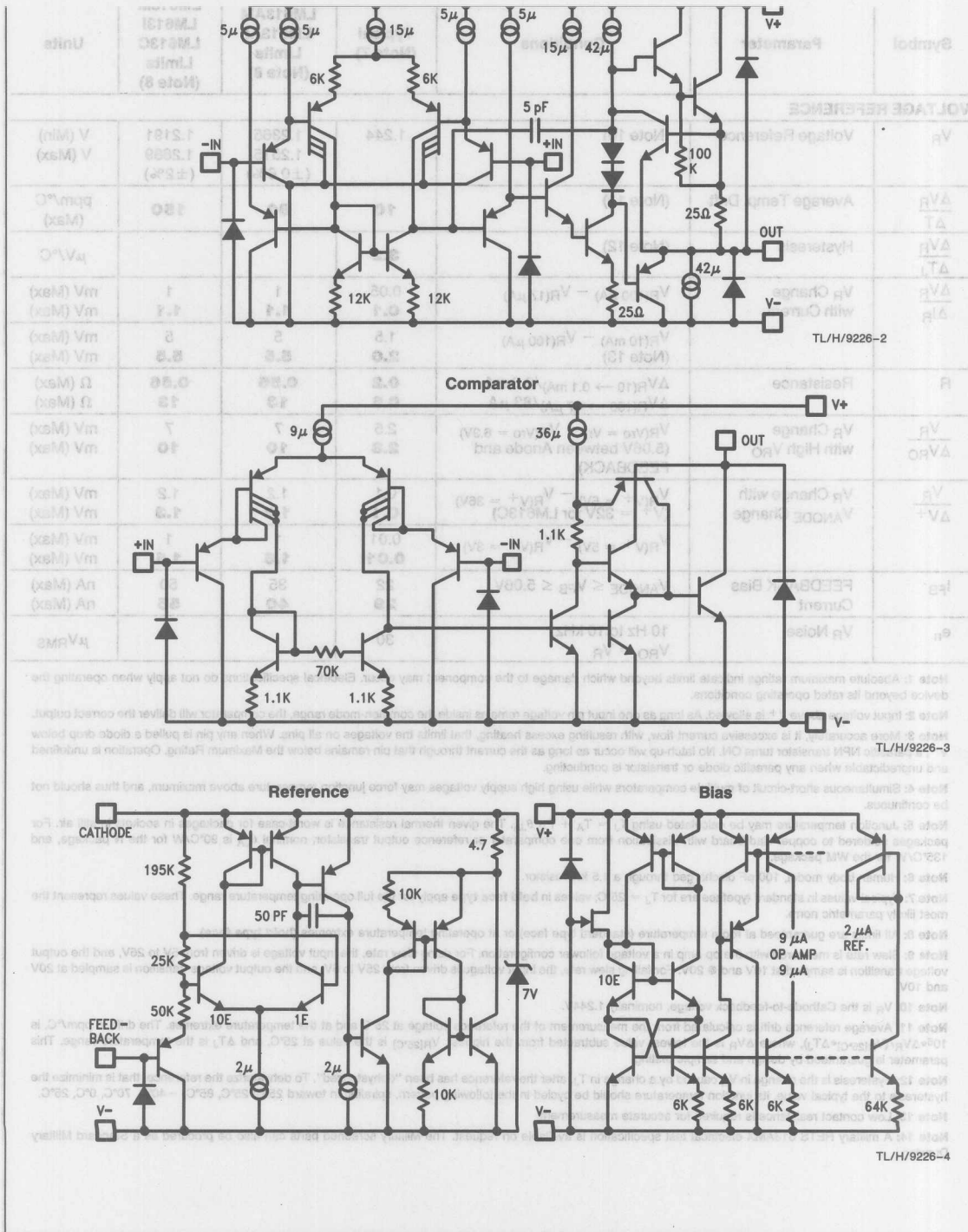
Note 10: V_R is the Cathode-to-feedback voltage, nominally 1.244V.

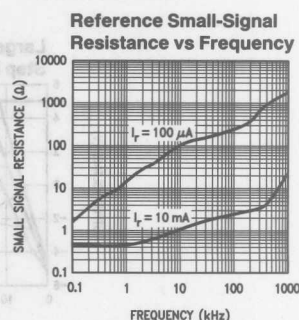
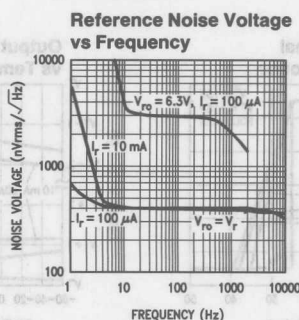
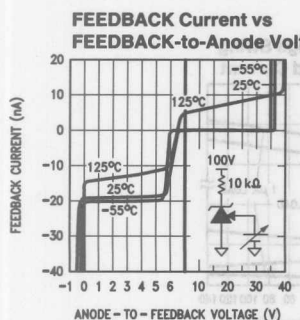
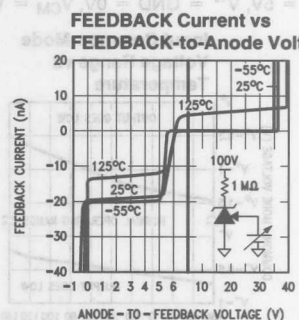
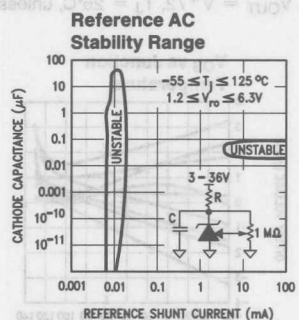
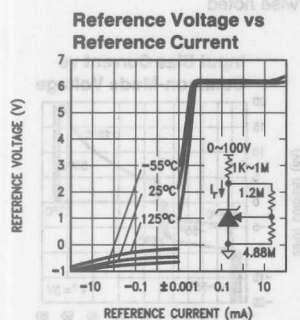
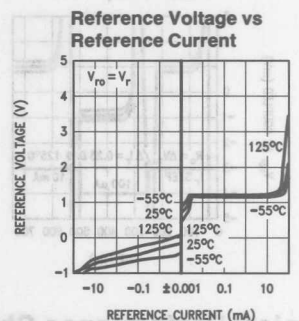
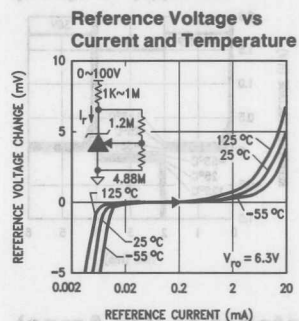
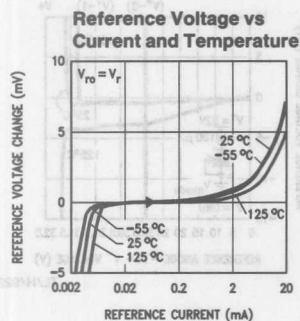
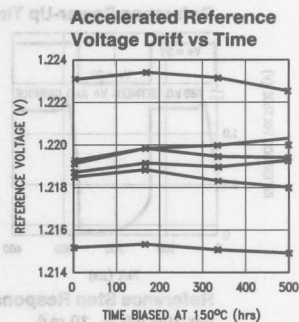
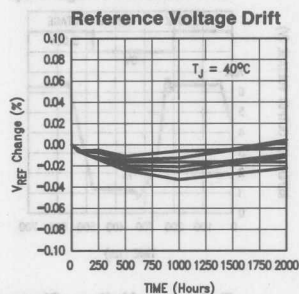
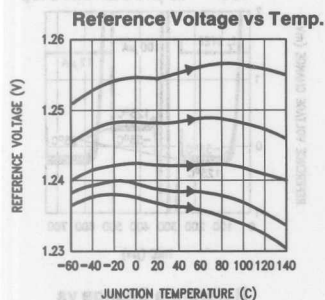
Note 11: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \Delta V_R / (V_R[25^\circ\text{C}] \Delta T_J)$, where ΔV_R is the lowest value subtracted from the highest, $V_R[25^\circ\text{C}]$ is the value at 25°C , and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 12: Hysteresis is the change in V_R caused by a change in T_J , after the reference has been "dehysteresized". To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

Note 13: Low contact resistance is required for accurate measurement.

Note 14: A military RETS 613AMX electrical test specification is available on request. The Military screened parts can also be procured as a Standard Military Drawing.

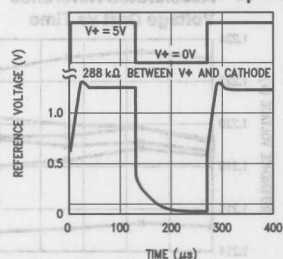




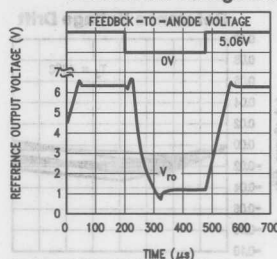
Typical Performance Characteristics (Reference) (Continued)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

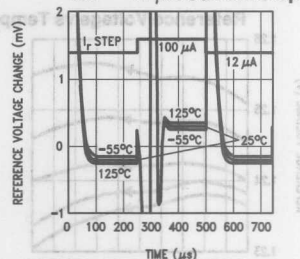
Reference Power-Up Time



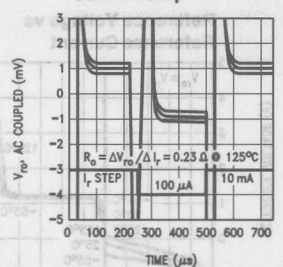
Reference Voltage with FEEDBACK Voltage Step



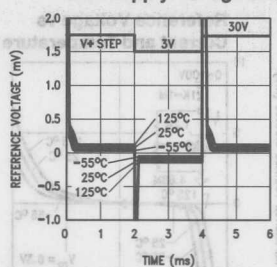
Reference Voltage with 100 ~ 12 μA Current Step



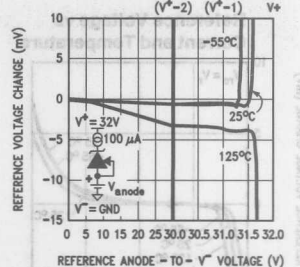
Reference Step Response for 100 μA ~ 10 mA Current Step



Reference Voltage Change with Supply Voltage Step



Reference Change vs Common-Mode Voltage ($V^+ - 2$) ($V^+ - 1$) V^+

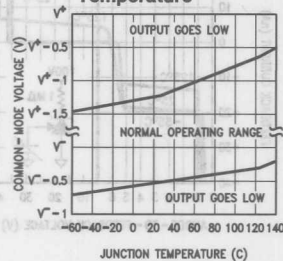


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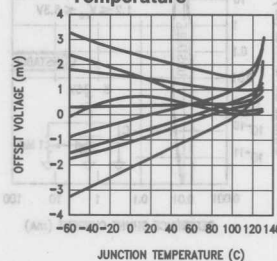
Typical Performance Characteristics (Op Amps)

$V^+ = 5\text{V}$, $V^- = \text{GND} = 0\text{V}$, $V_{\text{CM}} = V^+/2$, $V_{\text{OUT}} = V^+/2$, $T_J = 25^\circ\text{C}$, unless otherwise noted

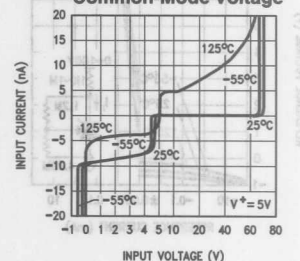
Input Common-Mode Voltage Range vs Temperature



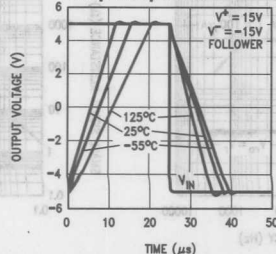
V_{OS} vs Junction Temperature



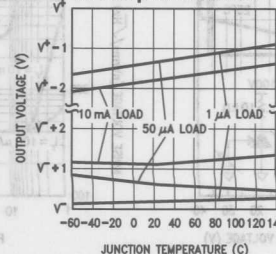
Input Bias Current vs Common-Mode Voltage



Large-Signal Step Response



Output Voltage Swing vs Temp. and Current

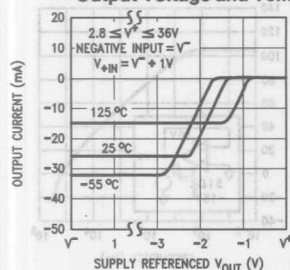


TL/H/9226-7

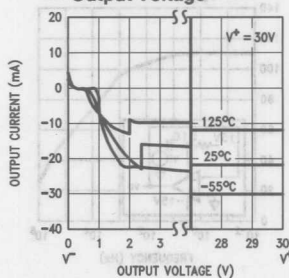
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

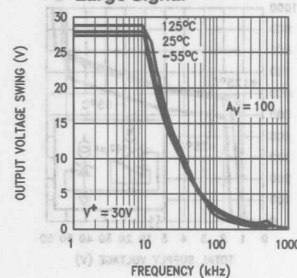
Output Source Current vs Output Voltage and Temp.



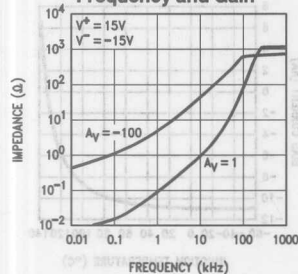
Output Sink Current vs Output Voltage



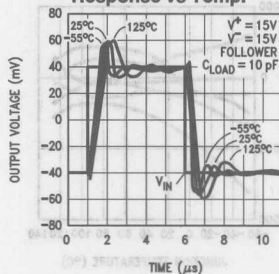
Output Swing, Large Signal



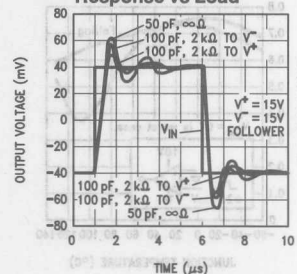
Output Impedance vs Frequency and Gain



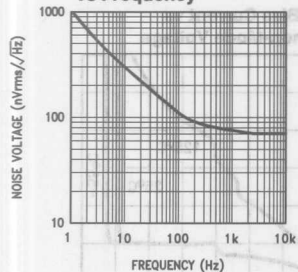
Small Signal Pulse Response vs Temp.



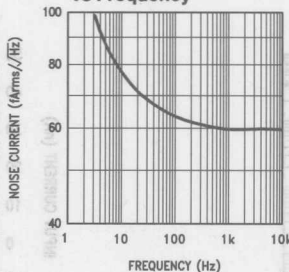
Small-Signal Pulse Response vs Load



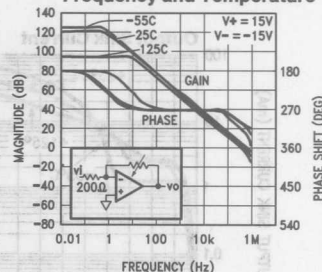
Op Amp Voltage Noise vs Frequency



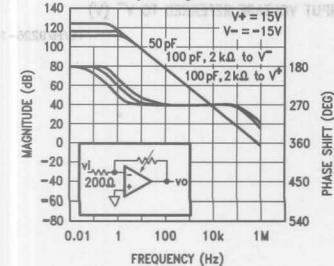
Op Amp Current Noise vs Frequency



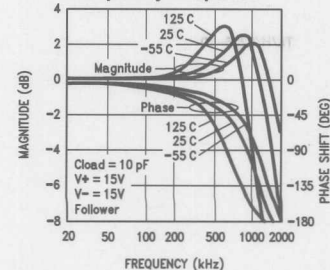
Small-Signal Voltage Gain vs Frequency and Temperature



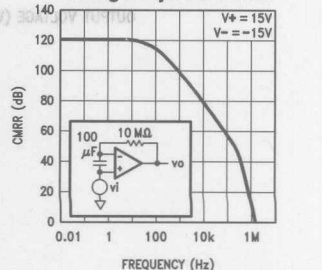
Small-Signal Voltage Gain vs Frequency and Load



Follower Small-Signal Frequency Response



Common-Mode Input Voltage Rejection Ratio

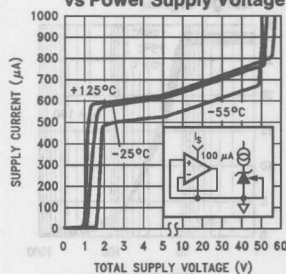


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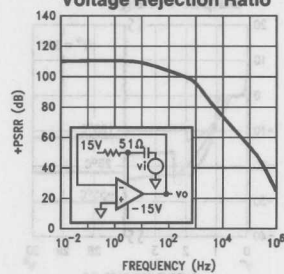
Typical Performance Characteristics (Op Amps) (Continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

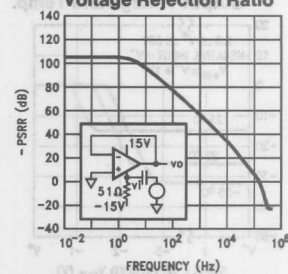
Power Supply Current vs Power Supply Voltage



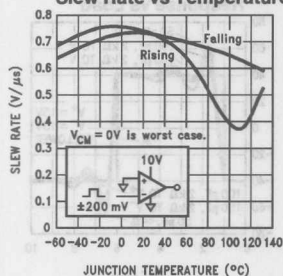
Positive Power Supply Voltage Rejection Ratio



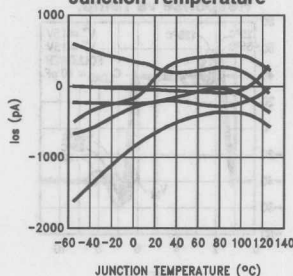
Negative Power Supply Voltage Rejection Ratio



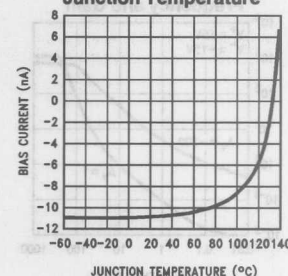
Slew Rate vs Temperature



Input Offset Current vs Junction Temperature



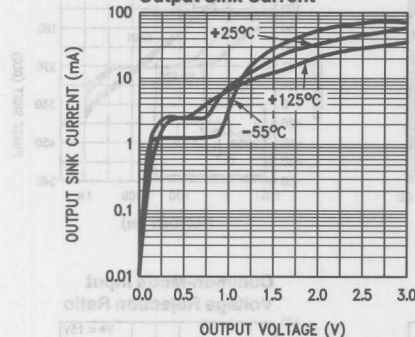
Input Bias Current vs Junction Temperature



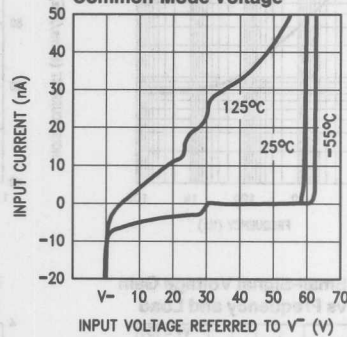
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Typical Performance Characteristics (Comparators)

Output Sink Current



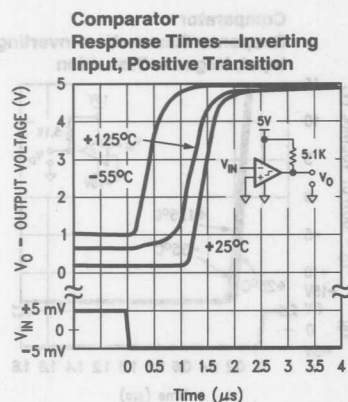
Input Bias Current vs Common-Mode Voltage



TL/H/9226-10

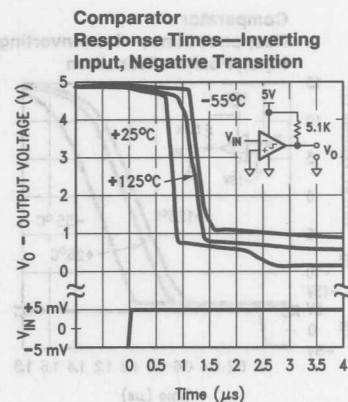
TL/H/9226-11

Typical Performance Characteristics (Comparators) (Continued)



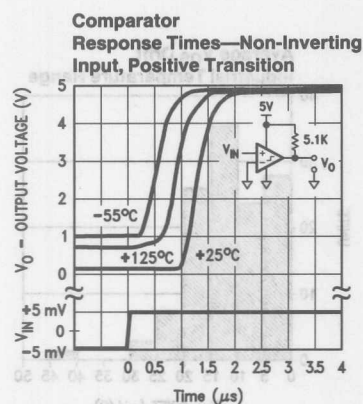
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TL/H/9226-12



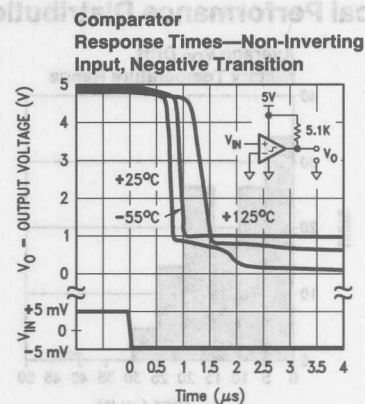
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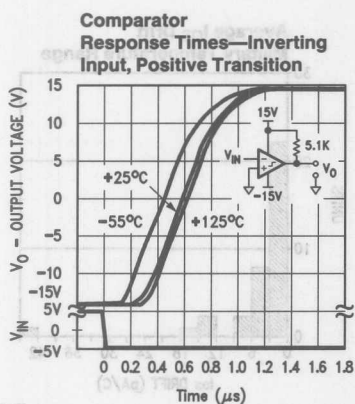
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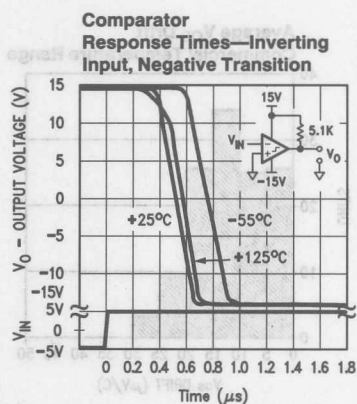
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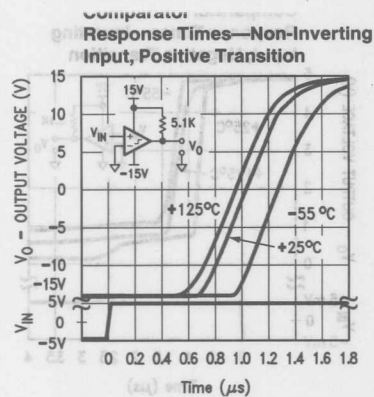
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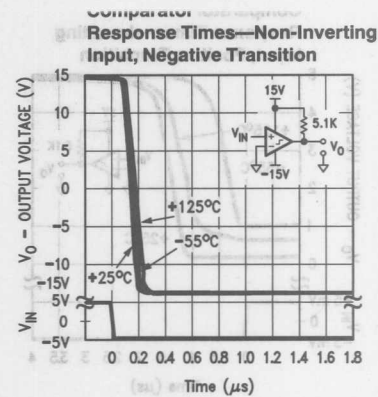


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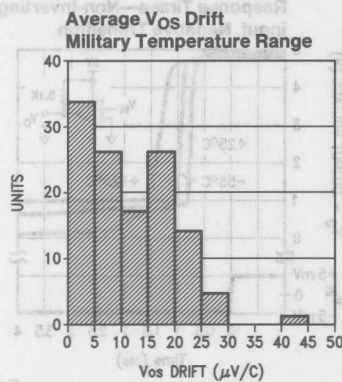


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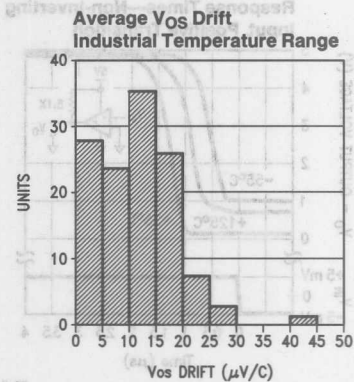


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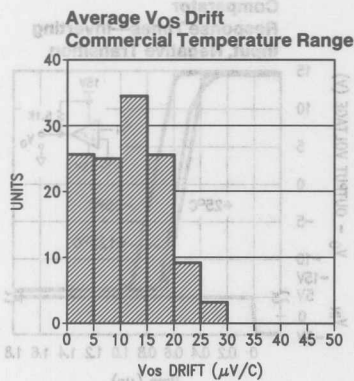
Typical Performance Distributions



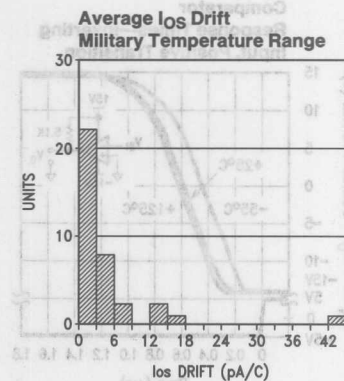
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TL/H/9226-21



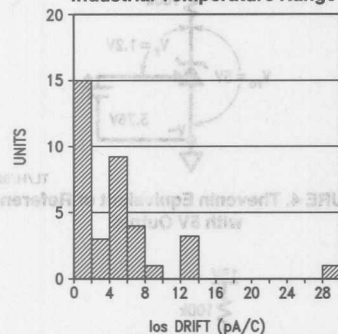
TL/H/9226-22



TL/H/9226-23

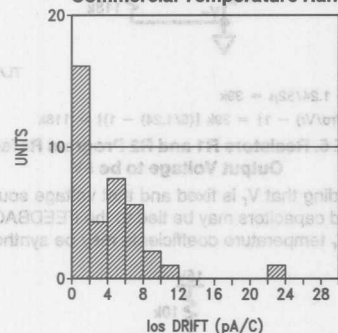
Typical Performance Distributions (Continued)

**Average I_{OS} Drift
Industrial Temperature Range**



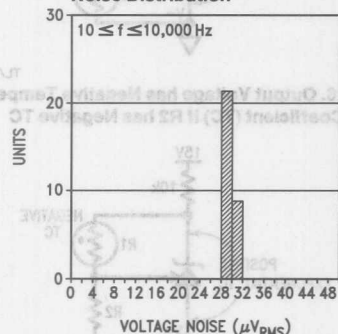
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**Average I_{OS} Drift
Commercial Temperature Range**



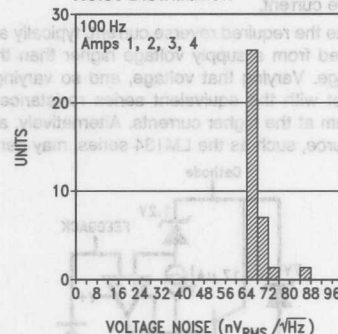
TL/H/9226-25

**Voltage Reference Broad-Band
Noise Distribution**



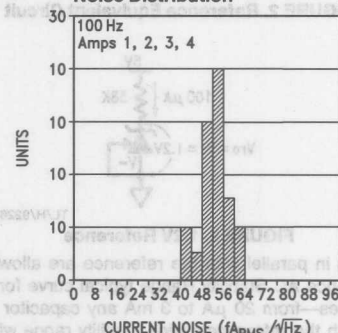
TL/H/9226-26

**Op Amp Voltage
Noise Distribution**



TL/H/9226-27

**Op Amp Current
Noise Distribution**



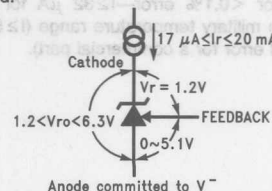
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Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V_r to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.



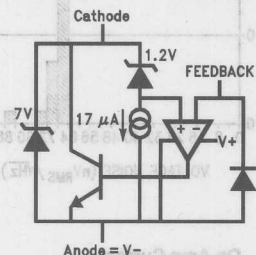
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**FIGURE 1. Voltage Associated with Reference
(current source I_r is external)**

Application Information (Continued)

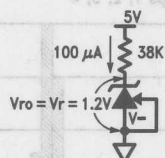
The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r .



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FIGURE 2. Reference Equivalent Circuit



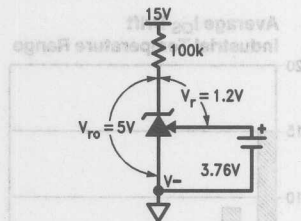
TL/H/9226-31

FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μ A to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

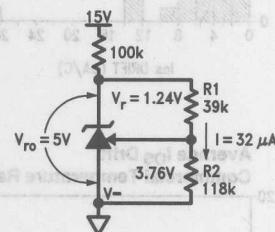
Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error— $I \geq 32 \mu$ A for the military grade over the military temperature range ($I \geq 5.5 \mu$ A for a 1% untrimmed error for a commercial part).



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FIGURE 4. Thevenin Equivalent of Reference with 5V Output



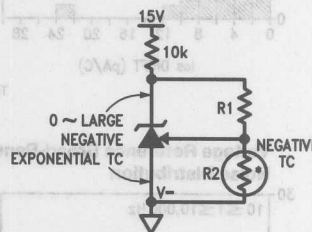
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$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1 \{ (Vro/Vr) - 1 \} = 39k \{ (5/1.24) - 1 \} = 118k$$

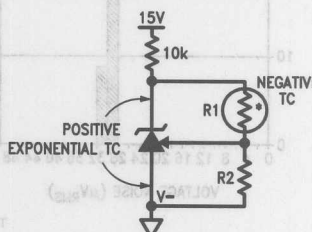
FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



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FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



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FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC

Application Information (Continued)

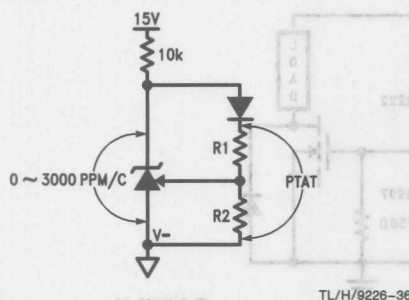
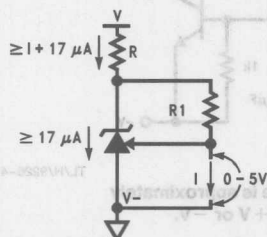


FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



$$I = V_r/R1 = 1.24/R1$$

FIGURE 9. Current Source is Programmed by R1

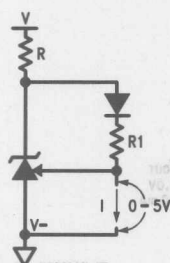


FIGURE 10. Proportional-to-Absolute-Temperature Current Source

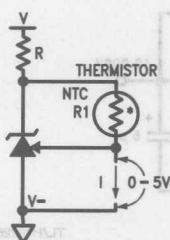


FIGURE 11. Negative-TC Current Source

Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIERS AND COMPARATORS

Any amp, comparator, or the reference may be biased in any way with no effect on the other sections of the LM613, except when a substrate diode conducts (see Electrical Characteristics Note 1). For example, one amp input may be outside the common-mode range, another amp may be operating as a comparator, and all other sections may have all terminals floating with no effect on the others. Tying inverting input to output and non-inverting input to V^- on unused amps is preferred. Unused comparators should have non-inverting input and output tied to V^+ , and inverting input tied to V^- . Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

These op amps, like the LM124 series, have flexible and relatively wide-swing output stages. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

- 1) **Output Swing:** Unloaded, the $42 \mu\text{A}$ pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than $42 \mu\text{A}$ is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ , at the cost of poorer sinking open-loop voltage gain.
- 2) **Cross-Over Distortion:** The LM613 has lower cross-over distortion (a $1 V_{BE}$ deadband versus $3 V_{BE}$ for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
- 3) **Capacitive Drive:** Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25Ω . 200 pF may then be driven without oscillation.

Comparator Output Stage

The comparators, like the LM139 series, have open-collector output stages. A pull-up resistor must be added from each output pin to a positive voltage for the output transistor to switch properly. When the output transistor is OFF, the output voltage will be this external positive voltage.

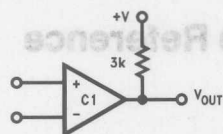
For the output voltage to be under the TTL-low voltage threshold when the output transistor is ON, the output current must be less than 8 mA (over temperature). This impacts the minimum value of pull-up resistor.

The offset voltage may increase when the output voltage is low and the output current is less than $30 \mu\text{A}$. Thus, for best accuracy, the pull-up resistor value should be low enough to allow the output transistor to sink more than $30 \mu\text{A}$.

Op Amp and Comparator Input Stage

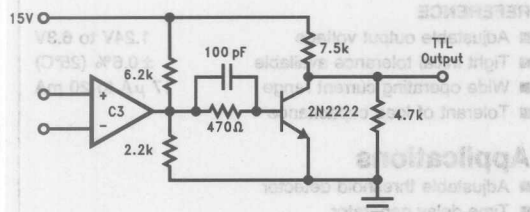
The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications (Continued)



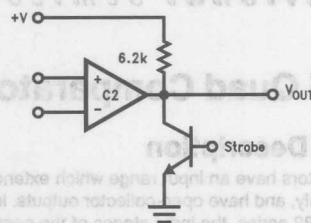
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FIGURE 16. Basic Comparator



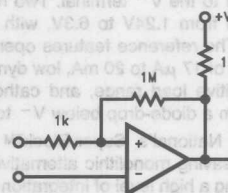
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FIGURE 18. Wide-Input Range Comparator with TTL Output

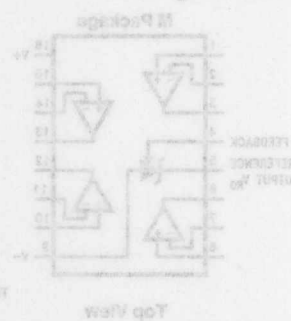
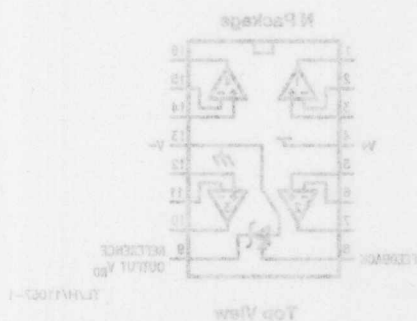


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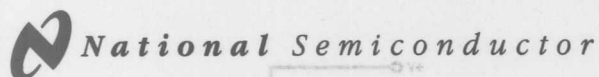
FIGURE 17. Basic Comparator with External Strobe



TL/H/9226-47

FIGURE 19. Comparator with Hysteresis ($\Delta V_H = +V(1k/1M)$)

| Package Number | Package | Temperature Range | | Hysteresis Tolerances |
|----------------|-----------------------------|-------------------|----------|--|
| | | Industrial | Military | |
| 1613A | 16-Pin Molded DIP | LM613A | LM613A | $\pm 0.5\%$ at 25°C 80 ppm/ $^\circ\text{C}$ max |
| 1613B | 16-Pin Ceramic DIP | LM613B | LM613B | |
| 1613C | 16-Pin Molded DIP | LM613C | LM613C | $\pm 0.5\%$ at 25°C 160 ppm/ $^\circ\text{C}$ max |
| 1613D | 16-Pin Pinout Surface Mount | LM613D | LM613D | |



LM615 Quad Comparator and Adjustable Reference

General Description

The comparators have an input range which extends to the negative supply, and have open-collector outputs. Improved over the LM139 series, the input stages of the comparators have lateral PNP input transistors which enable low input currents for large differential input voltages and swings above V^+ .

The voltage reference is a three-terminal shunt-type band-gap, and is referred to the V^- terminal. Two resistors program the reference from 1.24V to 6.3V, with accuracy of $\pm 0.6\%$ available. The reference features operation over a shunt current range of 17 μA to 20 mA, low dynamic impedance, broad capacitive load range, and cathode terminal voltage ranging from a diode-drop below V^- to above V^+ .

As a member of National's Super-Block™ family, the LM615 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

Features

COMPARATORS

- Low operating current 600 μA
- Wide supply voltage range 4V to 36V
- Open-collector outputs
- Input common-mode range V^- to $(V^+ - 1.8V)$
- Wide differential input voltage $\pm 36V$

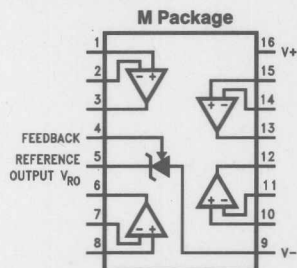
REFERENCE

- Adjustable output voltage 1.24V to 6.3V
- Tight initial tolerance available $\pm 0.6\%$ (25°C)
- Wide operating current range 17 μA to 20 mA
- Tolerant of load capacitance

Applications

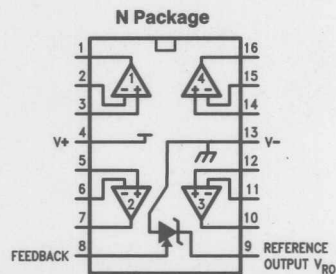
- Adjustable threshold detector
- Time-delay generator
- Voltage window comparator
- Power supply monitor
- RGB level detector

Connection Diagram



Top View

TL/H/11057-24



Top View

TL/H/11057-1

Ordering Information

For information about surface-mount packaging of this device, please contact the Analog Product Marketing group at National Semiconductor Corp. headquarters.

| Reference Tolerances | Temperature Range | | Package | NSC Package Number |
|--|--|---|-----------------------------|--------------------|
| | Military $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ | Industrial $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ | | |
| $\pm 0.6\%$ at 25°C, 80 ppm/°C max | LM615AMN | LM615AIN | 16-Pin Molded DIP | N16A |
| | LM615AMJ/883 (Note 13) | | 16-Pin Ceramic DIP | J16A |
| $\pm 2.0\%$ at 25°C, 150 ppm/°C max | LM615MN | LM615IN | 16-Pin Molded DIP | N16A |
| | | LM615IM | 16-Pin Narrow Surface Mount | M16A |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--|
| Voltage on Any Pin Except V_{RO} (referred to V^- pin) (Note 2) (Note 3) | 36V (Max) -0.3V (Min) |
| Current through Any Input Pin and V_{RO} Pin | ± 20 mA |
| Differential Input Voltage | ± 36 V |
| Output Short-Circuit Duration | (Note 4) |
| Storage Temperature Range | $-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$ |

| | |
|---|--------|
| Maximum Junction Temperature | 150°C |
| Thermal Resistance, Junction-to-Ambient (Note 5) N Package | 95°C/W |

| | |
|----------------------------------|------------|
| Soldering Information | |
| N Package Soldering (10 seconds) | 260°C |
| ESD Tolerance (Note 6) | ± 1 kV |

Operating Temperature Range

| | |
|-----------------|--|
| LM615AI, LM615I | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LM615A, LM615M | $-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$ |

Electrical Characteristics

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{CM} = V_{OUT} = V^+/2$, $I_R = 100 \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range.

| Symbol | Parameter | Conditions | Typical (Note 7) | LM615AM LM615AI Limits (Note 8) | LM615M LM615I Limits (Note 8) | Units |
|-------------------------------|---------------------------------------|---|--------------------------------------|--|--|--|
| COMPARATORS | | | | | | |
| I_S | Total Supply Current | V^+ Current, $R_{LOAD} = \infty$, $3\text{V} \leq V^+ \leq 36\text{V}$ | 250 350 | 550 600 | 600 650 | $\mu\text{A max}$ $\mu\text{A max}$ |
| V_{OS} | Offset Voltage over V^+ Range | $4\text{V} \leq V^+ \leq 36\text{V}$, $R_L = 15 \text{ k}\Omega$ | 1.0 2.0 | 3.0 6.0 | 5.0 7.0 | mV max mV max |
| V_{OS} | Offset Voltage over V_{CM} Range | $0\text{V} \leq V_{CM} \leq (V^+ - 1.8\text{V})$ $V^+ = 30\text{V}$, $R_L = 15 \text{ k}\Omega$ | 1.0 1.5 | 3.0 6.0 | 5.0 7.0 | mV max mV max |
| ΔV_{OS} ΔT | Average Offset Voltage Drift | | 15 | | | $\mu\text{V}/^\circ\text{C}$ |
| I_B | Input Bias Current | | -5 -8 | 25 30 | 35 40 | nA max nA max |
| I_{OS} | Input Offset Current | | 0.2 0.3 | 4 5 | 4 5 | nA max nA max |
| A_V | Voltage Gain | $R_L = 10 \text{ k}\Omega$ to 36V, $2\text{V} \leq V_{OUT} \leq 27\text{V}$ | 500 100 | 50 5 | 50 5 | V/mV min V/mV |
| t_R | Large Signal Response Time | $V_{+IN} = 1.4\text{V}$, $V_{-IN} = \text{TTL}$ Swing, $R_L = 5.1 \text{ k}\Omega$ | 1.5 2.0 | | | μs μs |
| I_{SINK} | Output Sink Current | $V_{+IN} = 0\text{V}$, $V_{-IN} = 1\text{V}$, $V_{OUT} = 1.5\text{V}$ $V_{OUT} = 0.4\text{V}$ | 20 13 2.8 2.4 | 10 8 1.0 0.5 | 10 8 0.8 0.5 | mA min mA min mA min mA min |
| I_L | Output Leakage Current | $V_{+IN} = 1\text{V}$, $V_{-IN} = 0\text{V}$, $V_{OUT} = 36\text{V}$ | 0.1 0.2 | 10 | 10 | $\mu\text{A max}$ μA |

unless otherwise specified. Limits in standard typeface are for $T_J = 25^\circ\text{C}$; limits in **boldface type** apply over the Operating Temperature Range. (Continued)

| Symbol | Parameter | Conditions | Typical (Note 7) | LM615AM LM615AI Limits (Note 8) | LM615M LM615I Limits (Note 8) | Units |
|------------------------------------|--------------------------------|---|--|--|--|--------------------------------------|
| VOLTAGE REFERENCE (Note 9) | | | | | | |
| V_R | Reference Voltage | | 1.244 | 1.2365 1.2515 ($\pm 0.6\%$) | 1.2191 1.2689 ($\pm 2\%$) | V min V max |
| $\frac{\Delta V_R}{\Delta T}$ | Average Drift with Temperature | (Note 10) | 18 | 80 | 150 | ppm/ $^\circ\text{C}$ max |
| $\frac{\Delta V_R}{\text{kHz}}$ | Average Drift with Time | $T_J = 40^\circ\text{C}$ $T_J = 150^\circ\text{C}$ | 400 1000 | | | ppm/kHz ppm/kHz |
| $\frac{\Delta V_R}{\Delta T_J}$ | Hysteresis | (Note 11) | 3.2 | | | $\mu\text{V}/^\circ\text{C}$ |
| $\frac{\Delta V_R}{\Delta I_R}$ | V_R Change with Current | $V_R[100\ \mu\text{A}] - V_R[17\ \mu\text{A}]$ | 0.05 0.1 | 1 1.1 | 1 1.1 | mV max mV max |
| | | $V_R[10\ \text{mA}] - V_R[100\ \mu\text{A}]$ (Note 12) | 1.5 2.0 | 5 5.5 | 5 5.5 | mV max mV max |
| R | Resistance | $\Delta V_R[10\ \text{mA to } 0.1\ \text{mA}]/9.9\ \text{mA}$ $\Delta V_R[100\ \mu\text{A to } 17\ \mu\text{A}]/83\ \mu\text{A}$ | 0.2 0.6 | 0.56 13 | 0.56 13 | Ω max Ω max |
| $\frac{\Delta V_R}{\Delta V_{RO}}$ | V_R Change with V_{RO} | $V_R[V_{RO} = V_R] - V_R[V_{RO} = 6.3\text{V}]$ | 2.5 2.8 | 5 10 | 5 10 | mV max mV max |
| $\frac{\Delta V_R}{\Delta V^+}$ | V_R Change with V^+ Change | $V_R[V^+ = 5\text{V}] - V_R[V^+ = 36\text{V}]$ $V_R[V^+ = 5\text{V}] - V_R[V^+ = 3\text{V}]$ | 0.1 0.1 0.01 0.01 | 1.2 1.3 1 1.5 | 1.2 1.3 1 1.5 | mV max mV max mV max mV max |
| I_{FB} | FEEDBACK Bias Current | $V^- \leq V_{FB} \leq 5.06\text{V}$ | 22 29 | 35 40 | 50 55 | nA max nA max |
| e_n | Voltage Noise | $\text{BW} = 10\ \text{Hz to } 10\ \text{kHz}$ | 30 | | | μV_{RMS} |

Note 1: Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.

Note 2: Input voltage above V^+ is allowed. As long as one input pin voltage remains inside the common-mode range, the comparator will deliver the correct output.

Note 3: More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.

Note 4: Shorting an Output to V^- will not cause power dissipation, so it may be continuous. However, shorting an Output to any more positive voltage (including V^+), will cause 80 mA (typ.) to be drawn through the output transistor. This current multiplied by the applied voltage is the power dissipation in the output transistor. If the total power from all shorted outputs causes the junction temperature to exceed 150°C , degraded reliability or destruction of the device may occur. To determine junction temperature, see Note 5.

Note 5: Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one comparator or reference output transistor, nominal θ_{JA} is $80^\circ\text{C}/\text{W}$ for the N package.

Note 6: Human body model, 100 pF discharge through a 1.5 k Ω resistor.

Note 7: Typical values in standard typeface are for $T_J = 25^\circ\text{C}$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

Note 8: All limits are guaranteed for $T_J = +25^\circ\text{C}$ (standard type face) or over the full operating temperature range (**bold type face**).

Note 9: V_{RO} is the reference output voltage, which may be set for 1.2V to 6.3V (see Application Information). V_R is the V_{RO} -to-FEEDBACK voltage (nominally 1.244V).

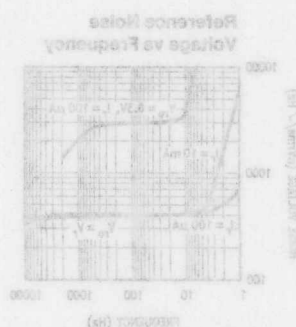
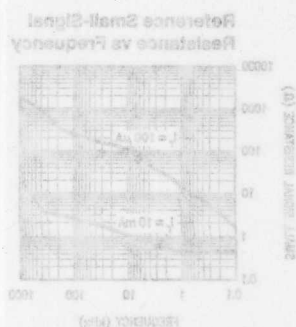
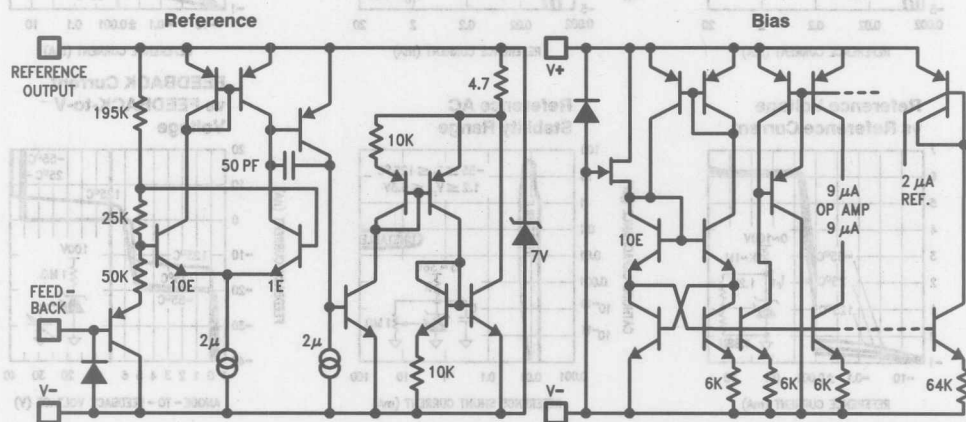
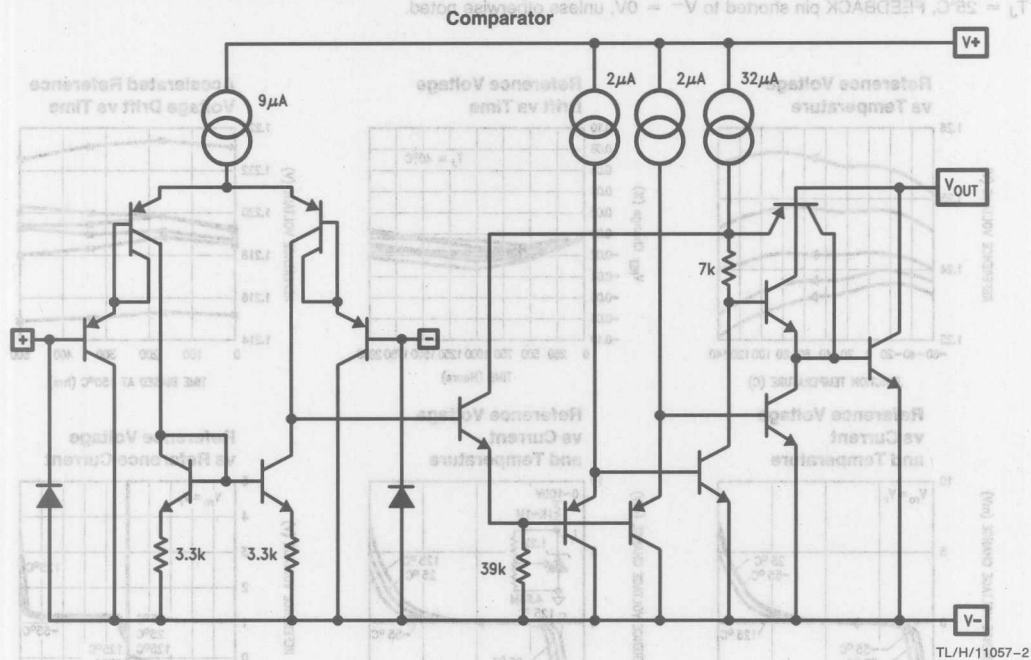
Note 10: Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \cdot \Delta V_R / V_R[25^\circ\text{C}] \cdot \Delta T_J$, where ΔV_R is the lowest value subtracted from the highest, $V_R[25^\circ\text{C}]$ is the value at 25°C , and ΔT_J is the temperature range. This parameter is guaranteed by design and sample testing.

Note 11: Hysteresis is the change in V_{RO} caused by a change in T_J , after the reference has been "dehysteresized." To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

Note 12: Low contact resistance is required for accurate measurement.

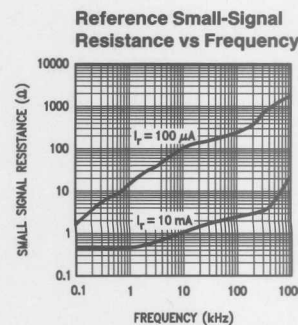
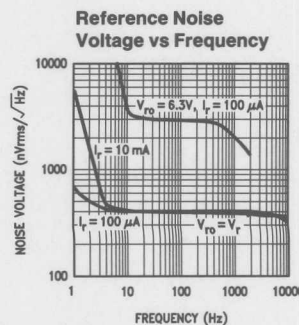
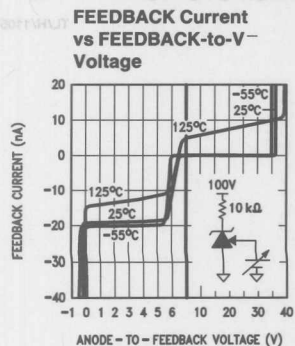
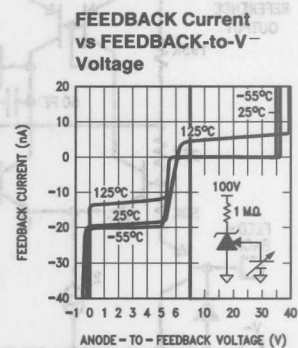
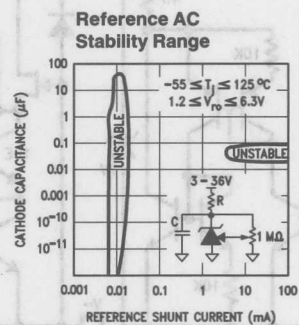
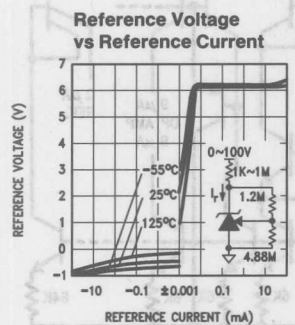
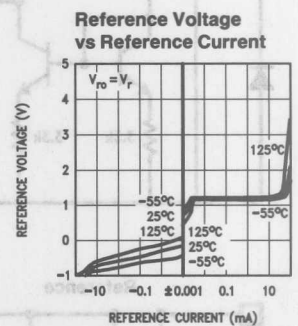
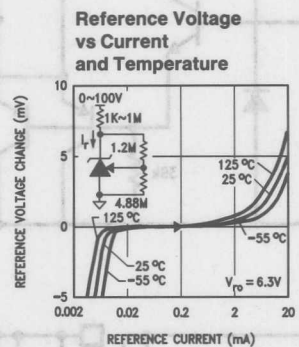
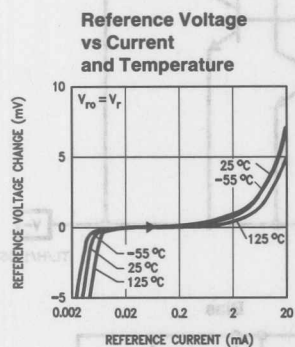
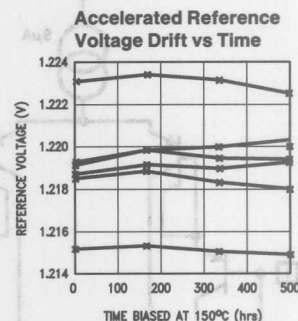
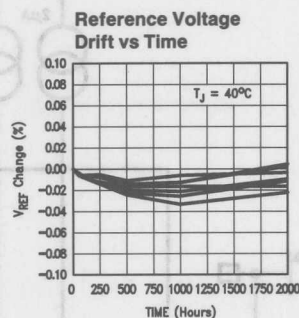
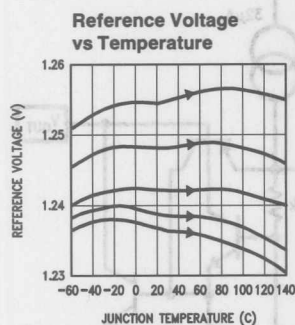
Note 13: A military RETS electrical test specification is available on request. The LM615AMJ/883 may also be procured as a Standard Military Drawing.

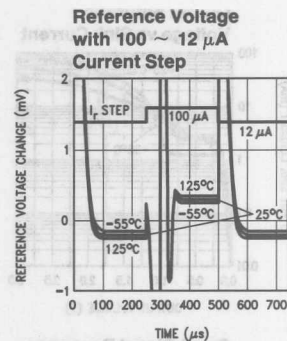
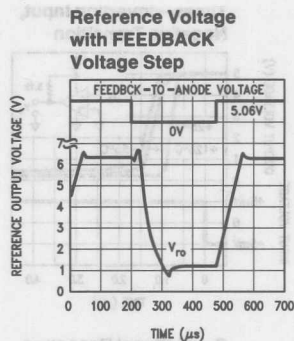
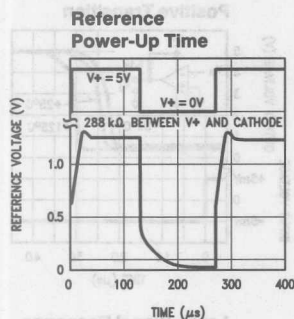
Simplified Schematic Diagrams



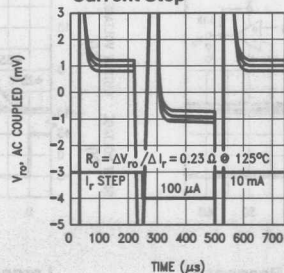
Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted.

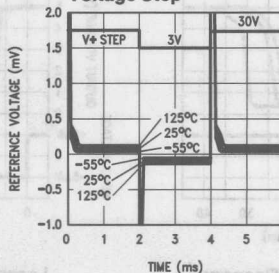




Reference Step Response for 100 μ ~ 10 mA Current Step



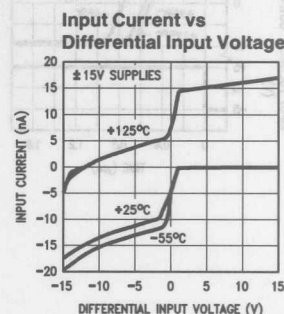
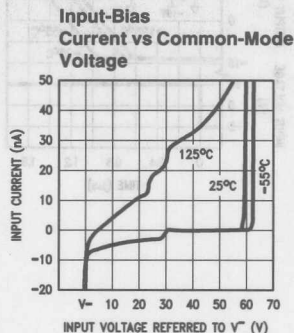
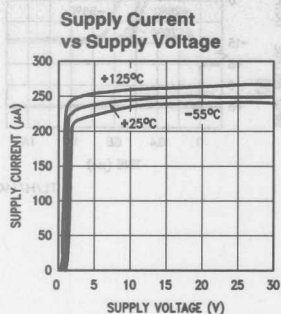
Reference Voltage Change with Supply Voltage Step



TL/H/11057-5

Typical Performance Characteristics (Comparators)

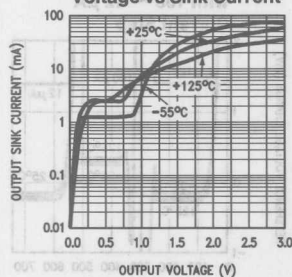
$T_J = 25^{\circ}\text{C}$, $V^+ = 5V$, $V^- = 0V$, unless otherwise noted



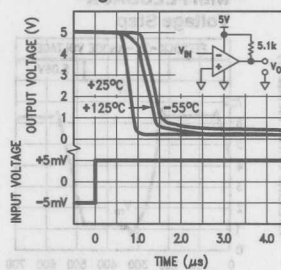
TL/H/11057-6

Typical Performance Characteristics (Comparators) (Continued)

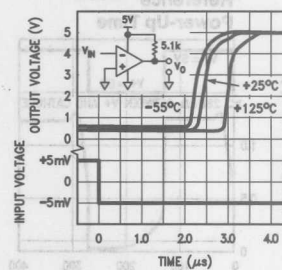
Output Saturation Voltage vs Sink Current



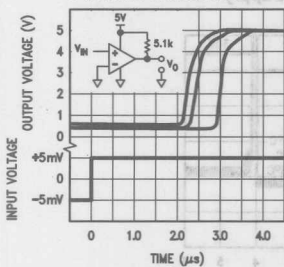
Small-Signal Response Times—Inverting Input, Negative Transition



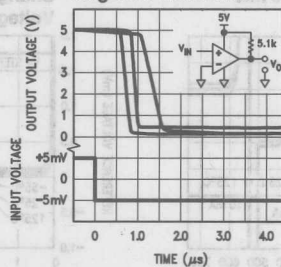
Small-Signal Response Times—Inverting Input, Positive Transition



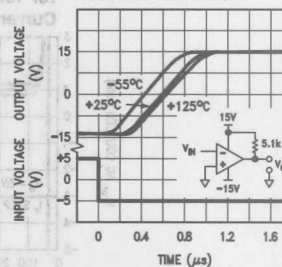
Small-Signal Response Times Non-Inverting Input, Positive Transition



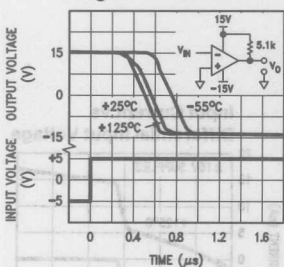
Small-Signal Response Times—Non-Inverting Input, Negative Transition



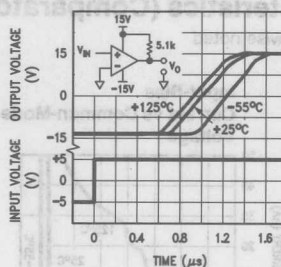
Large-Signal Response Times—Inverting Input, Positive Transition



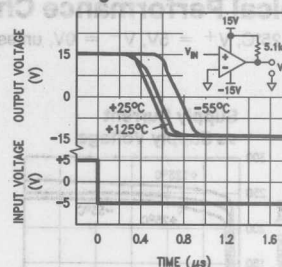
Large-Signal Response Times—Inverting Input, Negative Transition



Large-Signal Response Times—Non-Inverting Input, Positive Transition



Large-Signal Response Times—Non-Inverting Input, Negative Transition



TL/H/11057-8

Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the "forward" direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The cathode may swing from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.

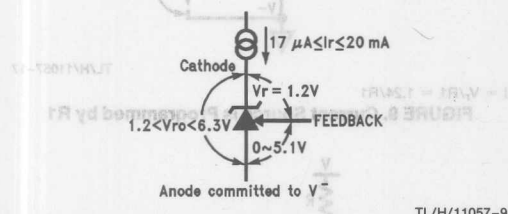


FIGURE 1. Voltage Associated with Reference (Current Source I_r is External)

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r .

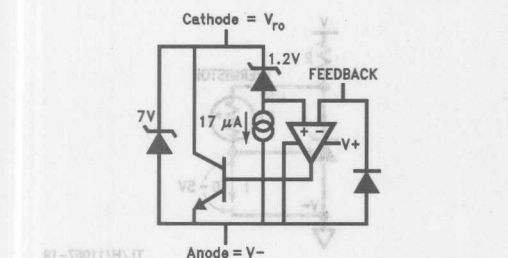


FIGURE 2. Reference Equivalent Circuit

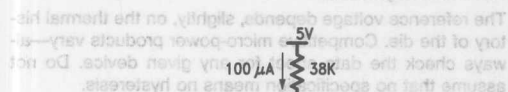


FIGURE 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range typical curve for capacitance values—from 20 μA to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I = R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2 = 3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error— $I \geq 32 \mu A$ for the military grade over the military temperature range ($I \geq 5.5 \mu A$ for a 1% untrimmed error for an industrial temperature range part).

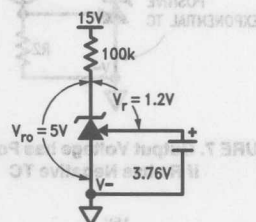
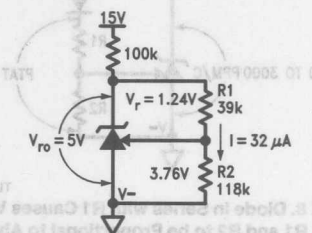


FIGURE 4. Thevenin Equivalent of Reference with 5V Output



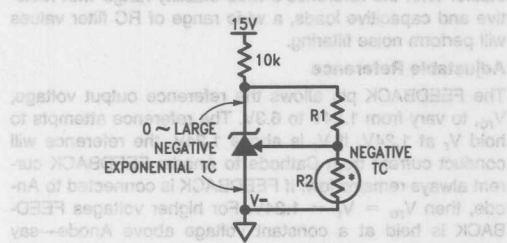
$$R1 = V_r / I = 1.24 / 32 \mu = 39k$$

$$R2 = R1 [(V_{ro}/V_r) - 1] = 39k [(5/1.24) - 1] = 118k$$

FIGURE 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

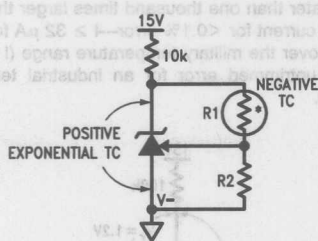
Application Information (Continued)

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.



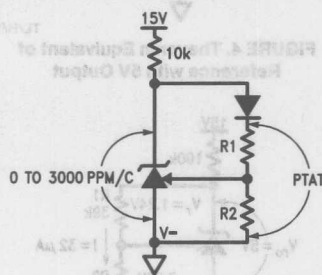
TL/H/11057-14

FIGURE 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC



TL/H/11057-15

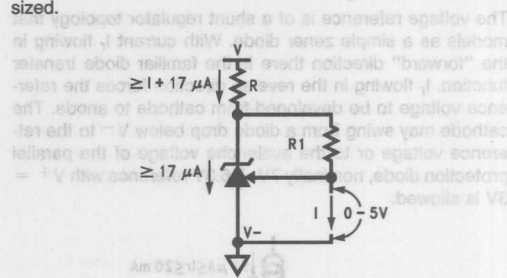
FIGURE 7. Output Voltage has Positive TC if R1 has Negative TC



TL/H/11057-16

FIGURE 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

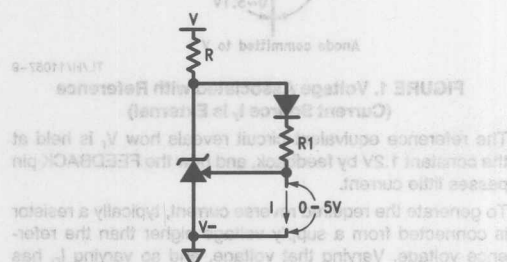
Connecting a resistor across V_{RO} -to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



TL/H/11057-17

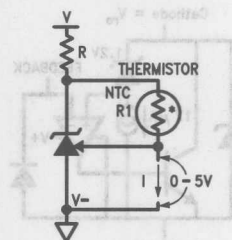
$$I = V_r/R1 = 1.24/R1$$

FIGURE 9. Current Source is Programmed by R1



TL/H/11057-18

FIGURE 10. Proportional-to-Absolute-Temperature Current Source



TL/H/11057-19

FIGURE 11. Negative-TC Current Source Reference Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

Application Information (Continued)

COMPARATORS

Any of the comparators or the reference may be biased in any way with no effect on the other sections of the LM615, except when a substrate diode conducts (see Electrical Characteristics Note 3). For example, one or both inputs of one comparator may be outside the input voltage range limits, the reference may be unpowered, and the other comparators will still operate correctly. Unused comparators should have inverting input and output tied to V^- , and non-inverting input tied to V^+ .

Hysteresis

Any comparator may oscillate or produce a noisy output if the applied differential input voltage is near the comparator's offset voltage. This usually happens when the input signal is moving very slowly across the comparator's switching threshold. This problem can be prevented by the addition of hysteresis, or positive feedback, as shown in Figure 12.

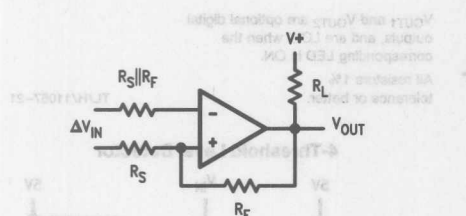


FIGURE 12. R_S and R_F Add Hysteresis to Comparator

The amount of hysteresis added in Figure 12 is

$$V_H = V^+ \times \frac{R_S}{(R_F + R_S)}$$

$$\approx V^+ \times \frac{R_S}{R_F} \quad \text{for } R_F \gg R_S$$

A good rule of thumb is to add hysteresis of at least the maximum specified offset voltage. More than about 50 mV of hysteresis can substantially reduce the accuracy of the comparator, since the offset voltage is effectively being increased by the hysteresis when the comparator output is high.

It is often a good idea to decrease the amount of hysteresis until oscillations are observed, then use three times that minimum hysteresis in the final circuit. Note that the amount of hysteresis needed is greatly affected by layout. The amount of hysteresis should be rechecked each time the layout is changed, such as changing from a breadboard to a P.C. board.

Input Stage

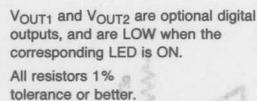
The input stage uses lateral PNP input transistors which, unlike those of many op amps, have breakdown voltage BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

The guaranteed common-mode input voltage range for an LM615 is $V^- \leq V_{CM} \leq (V^+ - 1.8V)$, over temperature. This is the voltage range in which the comparisons must be made. If both inputs are within this range, the output will be at the correct state. If one input is within this range, and the other input is less than $(V^- + 32V)$, even if this is greater than V^+ , the output will be at the correct state. If, however, either or both inputs are driven below V^- , and either input current exceeds $10 \mu A$, the output state is not guaranteed to be correct. If both inputs are above $(V^+ - 1.8V)$, the output state is also not guaranteed to be correct.

Output Stage

The comparators have open-collector output stages which require a pull-up resistor from each output pin to a positive supply voltage of the output to switch properly. When the internal output transistor is off, the output (HIGH) voltage will be pulled up to this external positive voltage.

To ensure that the LOW output voltage is under the TTL-low threshold, the output transistor's load current must be less than 0.8 mA (over temperature) when it turns on. This impacts the minimum value of the pull-up resistor.



TL/H/11057-22

3-106

LM710 Voltage Comparator

General Description

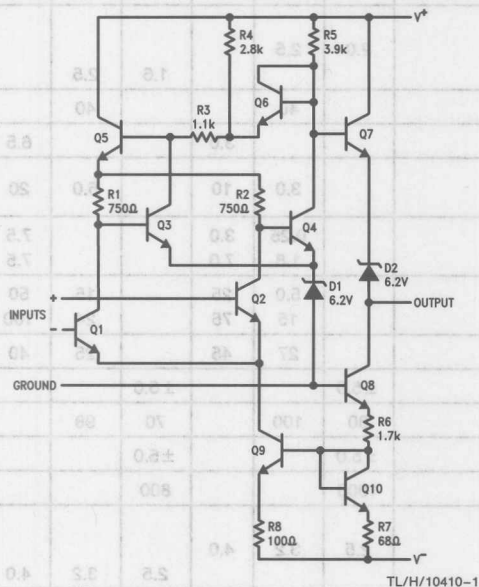
The LM710 series are high-speed voltage comparators intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime importance. The circuit has a differential input and a single-ended output, with saturated output levels compatible with practically all types of integrated logic.

The device is built on a single silicon chip which insures low offset and thermal drift. The use of a minimum number of stages along with minority-carrier lifetime control (gold doping) makes the circuit much faster than operational amplifiers in saturating comparator applications. In fact, the low

stray and wiring capacitances that can be realized with monolithic construction make the device difficult to duplicate with discrete components operating at equivalent power levels.

The LM710 series are useful as pulse height discriminators, voltage comparators in high-speed A/D converters or go, no-go detectors in automatic test equipment. They also have applications in digital systems as an adjustable-threshold line receiver or an interface between logic types. In addition, the low cost of the units suggests them for applications replacing relatively simple discrete component circuitry.

Schematic and Connection Diagrams



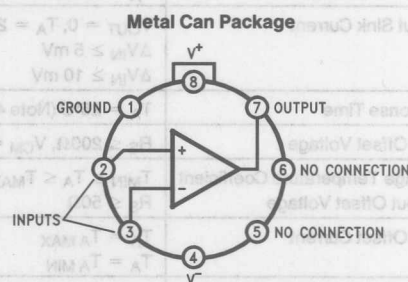
TL/H/10410-1

Ceramic Flatpak Package



Order Number LM710AMW/883*
See NS Package Number W10A

TL/H/10410-9



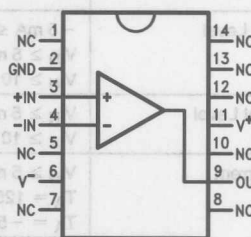
TL/H/10410-2

Top View

Note: Pin 4 is connected to case.

Order Number LM710AMH/883*, LM710H,
LM710H/883 or LM710CH
See NS Package Number H08C

Dual-In-Line Package



TL/H/10410-3

Top View

Order Number
LM710AMJ/883* or LM710CN
See NS Package Number N14A or J14A

*Also available per JM38510/10301

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-------------------------------|------------|
| Positive Supply Voltage | +14V |
| Negative Supply Voltage | -7V |
| Peak Output Current | 10 mA |
| Output Short Circuit Duration | 10 seconds |
| Differential Input Voltage | ±5V |
| Input Voltage | ±7V |

Power Dissipation

TO-99 (Note 1)

700 mW

Plastic Dual-In-Line Package (Note 2)

950 mW

Operating Temperature Range

LM710

-55°C to +125°C

LM710C

0°C to +70°C

Storage Temperature Range

-65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

260°C

Electrical Characteristics (Note 3)

| Parameter | Conditions | LM710 | | | LM710C | | | Units |
|---|---|------------|-------------|------------|--------|----------|------------|----------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | $R_S \leq 200\Omega$, $V_{CM} = 0V$, $T_A = 25^\circ C$ | | 0.6 | 2.0 | 1.6 | 5.0 | | mV |
| Input Offset Current | $V_{OUT} = 1.4V$, $T_A = 25^\circ C$ | | 0.75 | 3.0 | 1.8 | 5.0 | | μA |
| Input Bias Current | $T_A = 25^\circ C$ | | 13 | 20 | 16 | 25 | | μA |
| Voltage Gain | $T_A = 25^\circ C$ | 1250 | 1700 | | 1000 | 1500 | | |
| Output Resistance | $T_A = 25^\circ C$ | | 200 | | | 200 | | Ω |
| Output Sink Current | $V_{OUT} = 0$, $T_A = 25^\circ C$ $\Delta V_{IN} \geq 5 mV$ $\Delta V_{IN} \geq 10 mV$ | 2.0 | 2.5 | | 1.6 | 2.5 | | mA mA |
| Response Time | $T_A = 25^\circ C$ (Note 4) | | 40 | | | 40 | | ns |
| Input Offset Voltage | $R_S \leq 200\Omega$, $V_{CM} = 0V$ | | | 3.0 | | | 6.5 | mV |
| Average Temperature Coefficient of Input Offset Voltage | $T_{MIN} \leq T_A \leq T_{MAX}$ $R_S \leq 50\Omega$ | | 3.0 | 10 | | 5.0 | 20 | $\mu V/^\circ C$ |
| Input Offset Current | $T_A = T_{A MAX}$ $T_A = T_{A MIN}$ | | 0.25 1.8 | 3.0 7.0 | | | 7.5 7.5 | μA μA |
| Average Temperature Coefficient of Input Offset Current | $25^\circ C \leq T_A \leq T_{MAX}$ $T_{MIN} \leq T_A \leq 25^\circ C$ | | 5.0 15 | 25 75 | | 15 24 | 50 100 | nA/ $^\circ C$ nA/ $^\circ C$ |
| Input Bias Current | $T_A = T_{MIN}$ | | 27 | 45 | | 25 | 40 | μA |
| Input Voltage Range | $V^- = -7V$ | ±5.0 | | | ±5.0 | | | V |
| Common-Mode Rejection Ratio | $R_S \leq 200\Omega$ | 80 | 100 | | 70 | 98 | | dB |
| Differential Input Voltage Range | | ±5.0 | | | ±5.0 | | | V |
| Voltage Gain | | 1000 | | | 800 | | | V/V |
| Positive Output Level | $-5 mA \leq I_{OUT} \leq 0$ $V_{IN} \geq 5 mV$ $V_{IN} \geq 10 mV$ | 2.5 | 3.2 | 4.0 | 2.5 | 3.2 | 4.0 | V V |
| Negative Output Level | $V_{IN} \geq 5 mV$ $V_{IN} \geq 10 mV$ | -1.0 | -0.5 | 0 | -1.0 | -0.5 | 0 | V V |
| Output Sink Current | $V_{IN} \geq 5 mV$, $V_{OUT} = 0$ $T_A = 125^\circ C$ $T_A = -55^\circ C$ | 0.5 1.0 | 1.7 2.3 | | | | | mA mA |
| | $V_{IN} \geq 10 mV$, $V_{OUT} = 0$ $0^\circ C \leq T_A \leq +70^\circ C$ | | | | 0.5 | | | mA |

Electrical Characteristics (Note 3) (Continued)

| Parameter | Conditions | LM710 | | | LM710C | | | Units |
|-------------------------|-----------------------------|-------|-----|-----|--------|-----|-----|-------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Positive Supply Current | $V_{IN} \geq 5 \text{ mV}$ | | 5.2 | 9.0 | | 5.2 | 9.0 | mA |
| | $V_{IN} \geq 10 \text{ mV}$ | | | | | | | mA |
| Negative Supply Current | $V_{IN} \geq 5 \text{ mV}$ | | 4.6 | 7.0 | | 4.6 | 7.0 | mA |
| | $V_{IN} \geq 10 \text{ mV}$ | | | | | | | mA |
| Power Consumption | $I_{OUT} = 0$ | | | | | | | |
| | $V_{IN} \geq 5 \text{ mV}$ | | 90 | 150 | | | | mW |
| | $V_{IN} \geq 10 \text{ mV}$ | | | | | | 150 | mW |

Note 1: Rating applies for ambient temperatures of 25°C; derate linearly at 5.6 mW/°C for ambient temperatures above 25°C.

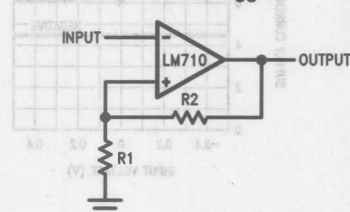
Note 2: Derate linearly at 9.5 mW/°C for ambient temperatures above 25°C.

Note 3: These specifications apply for $V^+ = 12\text{V}$, $V^- = -6\text{V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for LM710 and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for LM710C unless otherwise specified: The input offset voltage and input offset current (see definitions) are specified for a logic threshold voltage of 1.8V at -55°C , 1.4V at 25°C , and 1V at 125°C for LM710 and 1.5V at 0°C , 1.4V at 25°C , and 1.2V at 70°C for LM710C.

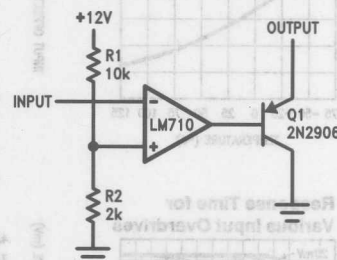
Note 4: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive (LM710) or a 10 mV overdrive (LM710C).

Typical Applications

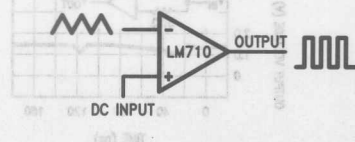
Schmitt Trigger



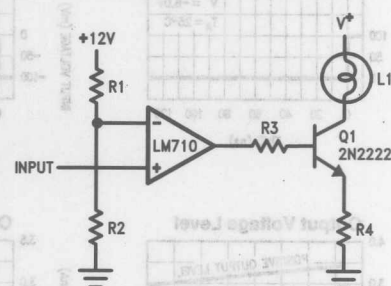
Line Receive with Increased Output Sink Current



Pulse Width Modulator

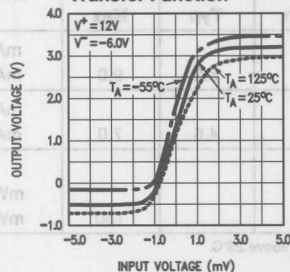


Level Detector with Lamp Driver

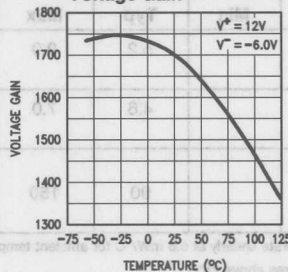


Typical Performance Characteristics

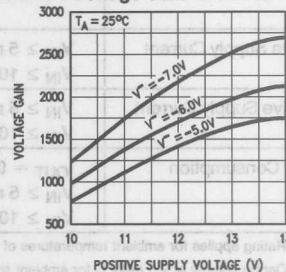
Transfer Function



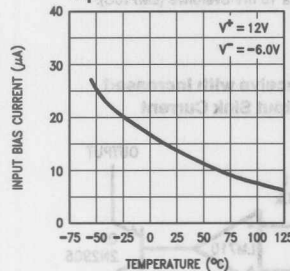
Voltage Gain



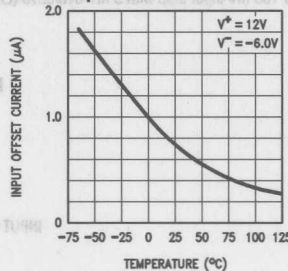
Voltage Gain



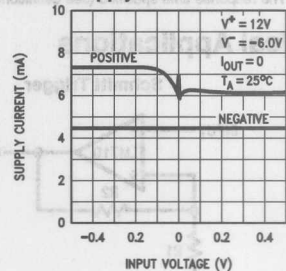
Input Bias Current



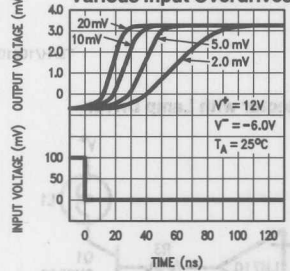
Input Offset Current



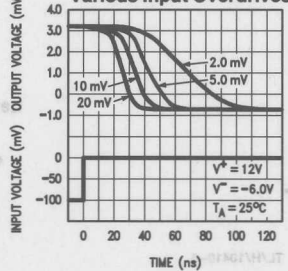
Supply Current



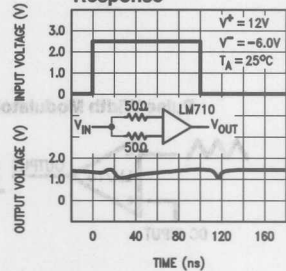
Response Time for Various Input Overdrives



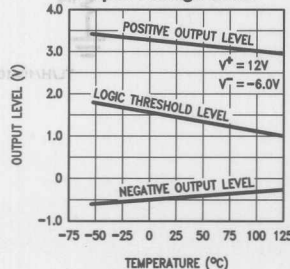
Response Time for Various Input Overdrives



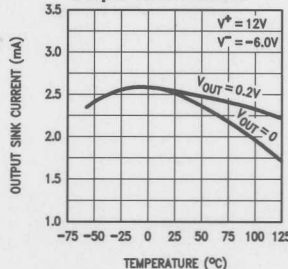
Common Mode Pulse Response



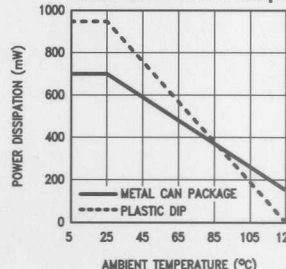
Output Voltage Level



Output Sink Current



Maximum Power Dissipation



TL/H/10410-8

LM760

High Speed Differential Comparator

General Description

The LM760 is a differential voltage comparator offering considerable speed improvement over the LM710 family and operates from symmetric supplies of $\pm 4.5\text{V}$ to $\pm 6.5\text{V}$. The LM760 can be used in high speed analog-to-digital conversion systems and as a zero crossing detector in disc file and tape amplifiers. The LM760 output features balanced rise and fall times for minimum skew and close matching between the complementary outputs. The outputs are TTL compatible with a minimum sink capability of two gate loads.

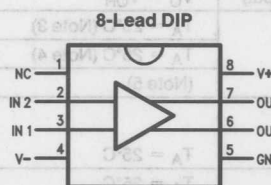
Features

- Guaranteed high speed—25 ns response time
- Guaranteed delay matching on both outputs
- Complementary TTL compatible outputs
- High sensitivity
- Standard supply voltages

Applications

- High speed A-to-D
- Peak or zero detector

Connection Diagram



Top View

Ordering Information

| Temperature Range Commercial 0°C to +70°C | Package Type | NSC Package Drawing |
|---|--------------------|---------------------------|
| LM760CN | 8-lead Plastic DIP | N08E |

| Symbol | Parameter | Conditions | Min | Typ | Max |
|----------|-------------------------------------|--|------|-----|-----|
| I_{+} | Positive Supply Current | $V_{CC} = \pm 5.5V$ | 18 | 32 | mA |
| I_{-} | Negative Supply Current | $V_{CC} = \pm 5.5V$ | 18 | 32 | mA |
| V_{OL} | Output Voltage LOW (Either Output) | $I_{OL} = 3.2mA$ | 0.28 | 0.4 | V |
| V_{OH} | Output Voltage HIGH (Either Output) | $I_{OH} = 80\mu A, V_{CC} = \pm 4.5V$ | 2.4 | 3.0 | V |
| V_{OH} | Output Voltage HIGH | $0mA \leq I_{OH} \leq 8.0mA$ $V_{CC} = +5.0V$ | 2.4 | 3.2 | V |
| V_{DR} | Differential Input Voltage Range | | | | V |
| V_{IP} | Input Voltage Range | | | | V |

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------|-----------------|
| Storage Temperature Range | |
| Metal Can and Ceramic DIP | -65°C to +175°C |
| Molded DIP | -65°C to +150°C |

| | |
|-----------------------------|-----------------|
| Operating Temperature Range | |
| Military (LM760) | -55°C to +125°C |
| Commercial (LM760C) | 0°C to +70°C |

| | |
|---------------------------------|-------|
| Lead Temperature | |
| Metal Can and Ceramic DIP | 300°C |
| (Soldering, 60 sec.) | 265°C |
| Molded DIP (Soldering, 10 sec.) | |

| | |
|----------------------------|-------------------------|
| Positive Supply Voltage | +8.0V |
| Negative Supply Voltage | -8.0V |
| Peak Output Current | 10 mA |
| Differential Input Voltage | ±5.0V |
| Input Voltage | $V^+ \geq V_i \geq V^-$ |
| ESD Susceptibility | TBD |

LM760

Electrical Characteristics

$V_{CC} = \pm 4.5V$ to $\pm 6.5V$, $T_A = -55^\circ C$ to $+125^\circ C$, $T_A = 25^\circ C$ for typical figures, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------|--|--|-----------|-----------|-----|------------------|
| V_{IO} | Input Offset Voltage | $R_S \leq 200\Omega$ | | 1.0 | 6.0 | mV |
| I_{IO} | Input Offset Current | | | 0.5 | 7.5 | μA |
| I_{IB} | Input Bias Current | | | 8.0 | 60 | μA |
| R_O | Output Resistance (Either Output) | $V_O = V_{OH}$ | | 100 | | Ω |
| t_{PD} | Response Time | $T_A = 25^\circ C$ (Note 3) | | 18 | 30 | ns |
| | | $T_A = 25^\circ C$ (Note 4) | | | 25 | |
| | | (Note 5) | | 16 | | |
| Δt_{PD} | Response Time Difference between Outputs (Note 1) (t_{PD} of $+V_{I1}$) - (t_{PD} of $-V_{I2}$) | $T_A = 25^\circ C$ | | | 5.0 | ns |
| | | $T_A = 25^\circ C$ | | | 5.0 | |
| | | $T_A = 25^\circ C$ | | | 7.5 | |
| | | $T_A = 25^\circ C$ | | | 7.5 | |
| | | $T_A = 25^\circ C$ | | | 7.5 | |
| R_i | Input Resistance | $f = 1.0$ MHz | | 12 | | k Ω |
| C_i | Input Capacitance | $f = 1.0$ MHz | | 8.0 | | pF |
| $\Delta V_{IO}/\Delta T$ | Average Temperature Coefficient of Input Offset Voltage | $R_S = 50\Omega$, $T_A = -55^\circ C$ to $+125^\circ C$ | | 3.0 | | $\mu V/^\circ C$ |
| $\Delta I_{IO}/\Delta T$ | Average Temperature Coefficient of Input Offset Current | $T_A = +25^\circ C$ to $+125^\circ C$ | | 2.0 | | nA/ $^\circ C$ |
| | | $T_A = +25^\circ C$ to $-55^\circ C$ | | 7.0 | | |
| V_{IR} | Input Voltage Range | $V_{CC} = \pm 6.5V$ | ± 4.0 | ± 4.5 | | V |
| V_{IDR} | Differential Input Voltage Range | | | ± 5.0 | | V |
| V_{OH} | Output Voltage HIGH (Either Output) | $0\text{ mA} \leq I_{OH} \leq 5.0\text{ mA}$ $V_{CC} = +5.0V$ | 2.4 | 3.2 | | V |
| | | $I_{OH} = 80\text{ }\mu A$, $V_{CC} = \pm 4.5V$ | 2.4 | 3.0 | | |
| V_{OL} | Output Voltage LOW (Either Output) | $I_{OL} = 3.2\text{ mA}$ | | 0.25 | 0.4 | V |
| I^+ | Positive Supply Current | $V_{CC} = \pm 6.5V$ | | 18 | 32 | mA |
| I^- | Negative Supply Current | $V_{CC} = \pm 6.5V$ | | 9.0 | 16 | mA |

LM760C

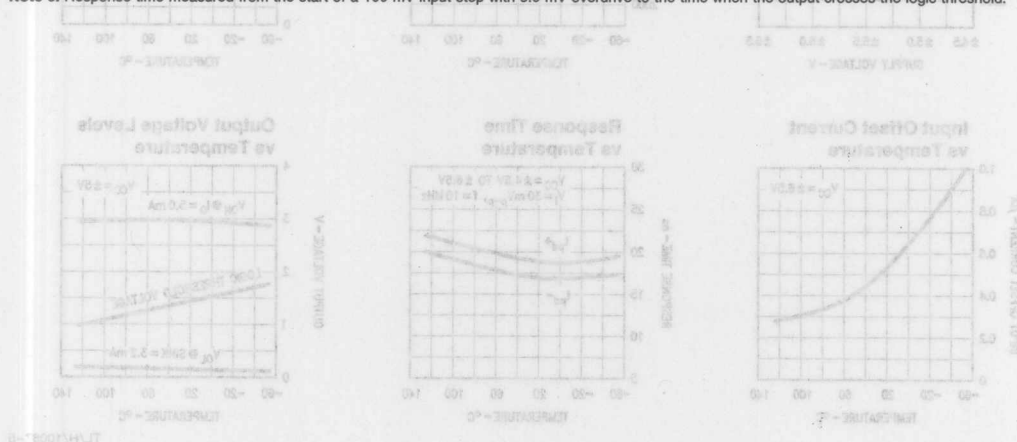
Electrical Characteristics

 $V_{CC} = \pm 4.5V$ to $\pm 6.5V$, $T_A = 0^\circ C$ to $+70^\circ C$, $T_A = 25^\circ C$ for typical figures, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------------------|--|--|-----------|-----------|-----|------------------|
| V_{IO} | Input Offset Voltage | $R_S \leq 200\Omega$ | | 1.0 | 6.0 | mV |
| I_{IO} | Input Offset Current | | | 0.5 | 7.5 | μA |
| I_{IB} | Input Bias Current | | | 8.0 | 60 | μA |
| R_O | Output Resistance (Either Output) | $V_O = V_{OH}$ | | 100 | | Ω |
| t_{PD} | Response Time | $T_A = 25^\circ C$ (Note 3) | | 18 | 30 | ns |
| | | $T_A = 25^\circ C$ (Note 4) | | | 25 | |
| | | (Note 5) | | 16 | | |
| | | | | | | |
| Δt_{PD} | Response Time Difference between Outputs (Note 1) (t_{PD} of $+V_{I1}$) - (t_{PD} of $-V_{I2}$) | $T_A = 25^\circ C$ | | | 5.0 | ns |
| | | $T_A = 25^\circ C$ | | | 5.0 | |
| | | $T_A = 25^\circ C$ | | | 10 | |
| | | $T_A = 25^\circ C$ | | | 10 | |
| R_I | Input Resistance | $f = 1.0$ MHz | | 12 | | k Ω |
| C_I | Input Capacitance | $f = 1.0$ MHz | | 8.0 | | pF |
| $\Delta V_{IO}/\Delta T$ | Average Temperature Coefficient of Input Offset Voltage | $R_S = 50\Omega$, $T_A = 0^\circ C$ to $+70^\circ C$ | | 3.0 | | $\mu V/^\circ C$ |
| $\Delta I_{IO}/\Delta T$ | Average Temperature Coefficient of Input Offset Current | $T_A = +25^\circ C$ to $+70^\circ C$ | | 5.0 | | nA/°C |
| | | $T_A = +25^\circ C$ to $0^\circ C$ | | 10 | | |
| V_{IR} | Input Voltage Range | $V_{CC} = \pm 6.5V$ | ± 4.0 | ± 4.5 | | V |
| V_{IDR} | Differential Input Voltage Range | | | ± 5.0 | | V |
| V_{OH} | Output Voltage HIGH (Either Output) | 0 mA $\leq I_{OH} \leq 5.0$ mA $V_{CC} = +5.0V$ | 2.4 | 3.2 | | V |
| | | $I_{OH} = 80$ μA , $V_{CC} = \pm 4.5V$ | 2.5 | 3.0 | | |
| V_{OL} | Output Voltage LOW (Either Output) | $I_{OL} = 3.2$ mA | | 0.25 | 0.4 | V |
| | | | | | | |
| I^+ | Positive Supply Current | $V_{CC} = \pm 6.5V$ | | 18 | 34 | mA |
| I^- | Negative Supply Current | $V_{CC} = \pm 6.5V$ | | 9.0 | 16 | mA |

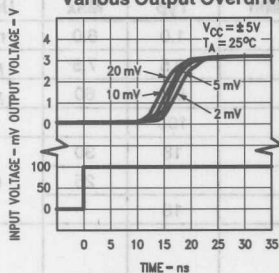
Note 1: T_J Max = $150^\circ C$.Note 2: Ratings apply to ambient temperature at $25^\circ C$.Note 3: Response time measured from the 50% point of a 30 mV_{p-p} 10 MHz sinusoidal input to the 50% point of the output.Note 4: Response time measured from the 50% point of a 2.0 V_{p-p} 10 MHz sinusoidal input to the 50% point of the output.

Note 5: Response time measured from the start of a 100 mV input step with 5.0 mV overdrive to the time when the output crosses the logic threshold.

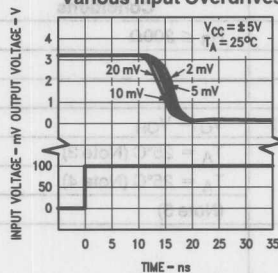


Typical Performance Characteristics

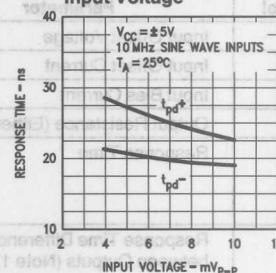
Response Time for Various Output Overdrives



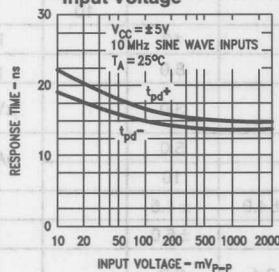
Response Time for Various Input Overdrives



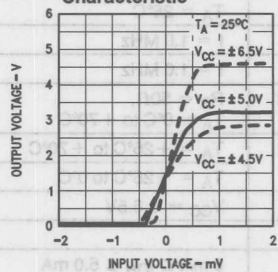
Response Time vs Input Voltage



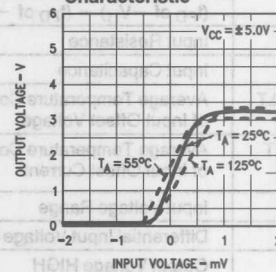
Response Time vs Input Voltage



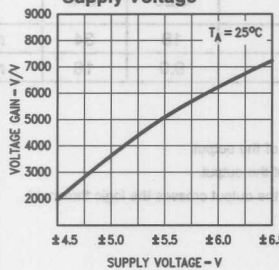
Voltage Transfer Characteristic



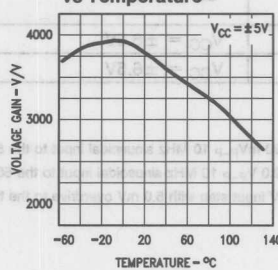
Voltage Transfer Characteristic



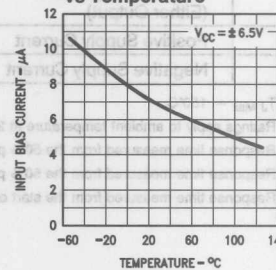
Voltage Gain vs Supply Voltage



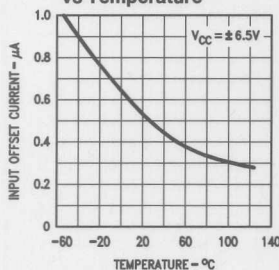
Voltage Gain vs Temperature



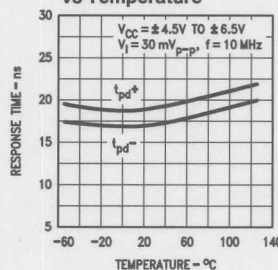
Input Bias Current vs Temperature



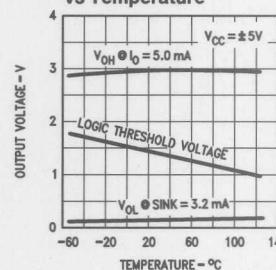
Input Offset Current vs Temperature



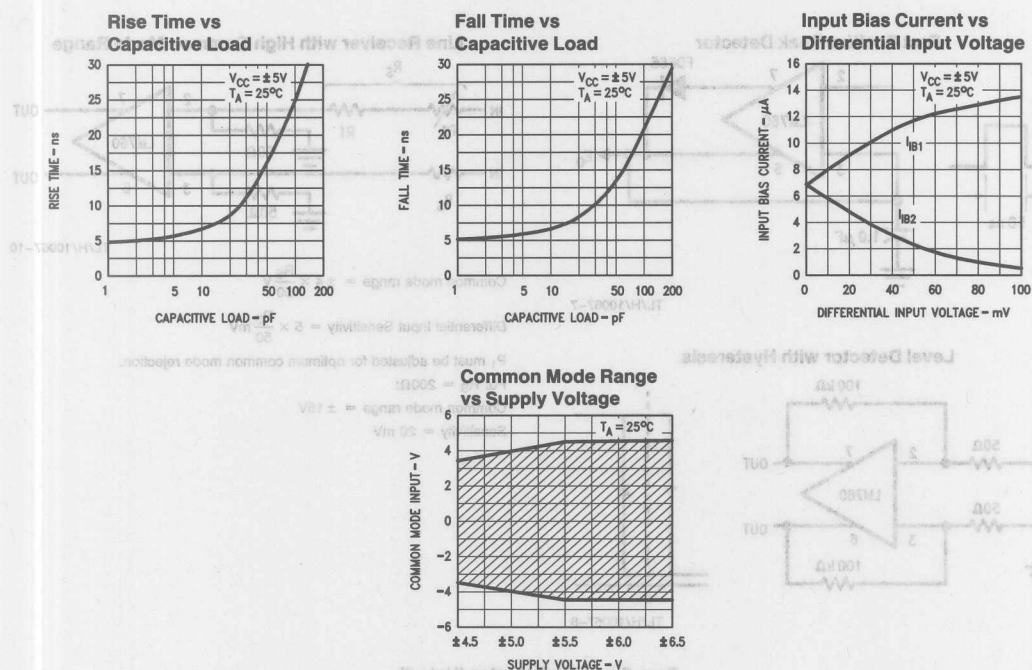
Response Time vs Temperature



Output Voltage Levels vs Temperature

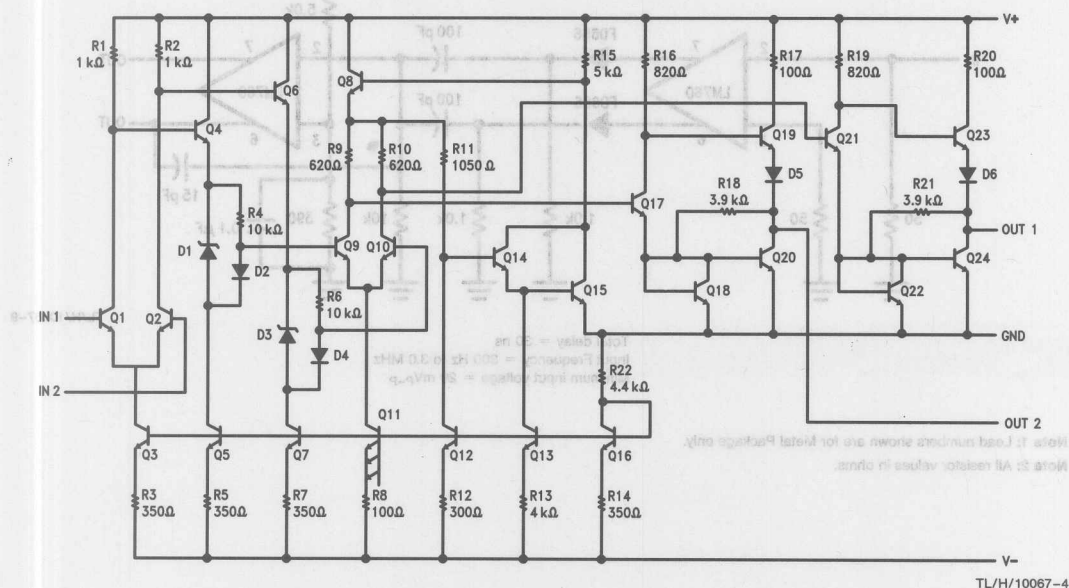


Typical Performance Characteristics (Continued)



TL/H/10067-6

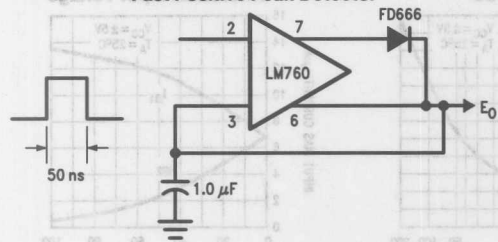
Equivalent Circuit



TL/H/10067-4

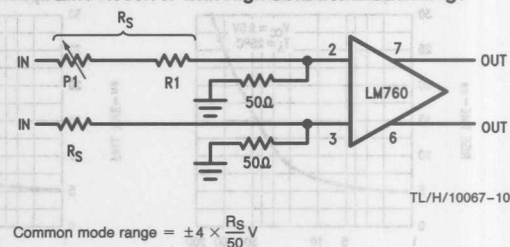
Typical Applications (Note 1)

Fast Positive Peak Detector



TL/H/10067-7

Line Receiver with High Common Mode Range



TL/H/10067-10

$$\text{Common mode range} = \pm 4 \times \frac{R_S}{50} V$$

$$\text{Differential Input Sensitivity} = 5 \times \frac{R_S}{50} mV$$

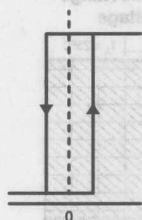
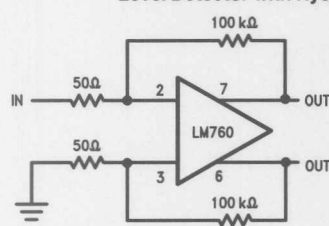
P1 must be adjusted for optimum common mode rejection.

For $R_S = 200\Omega$:

Common mode range = $\pm 16V$

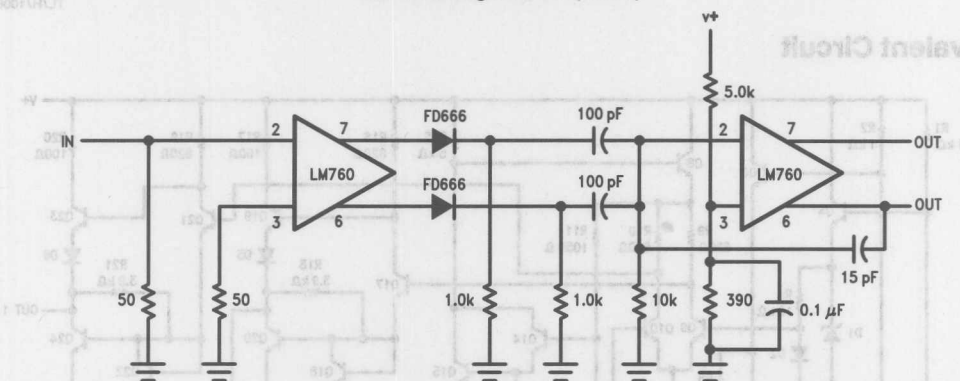
Sensitivity = 20 mV

Level Detector with Hysteresis



TL/H/10067-8

Zero Crossing Detector (Note 2)



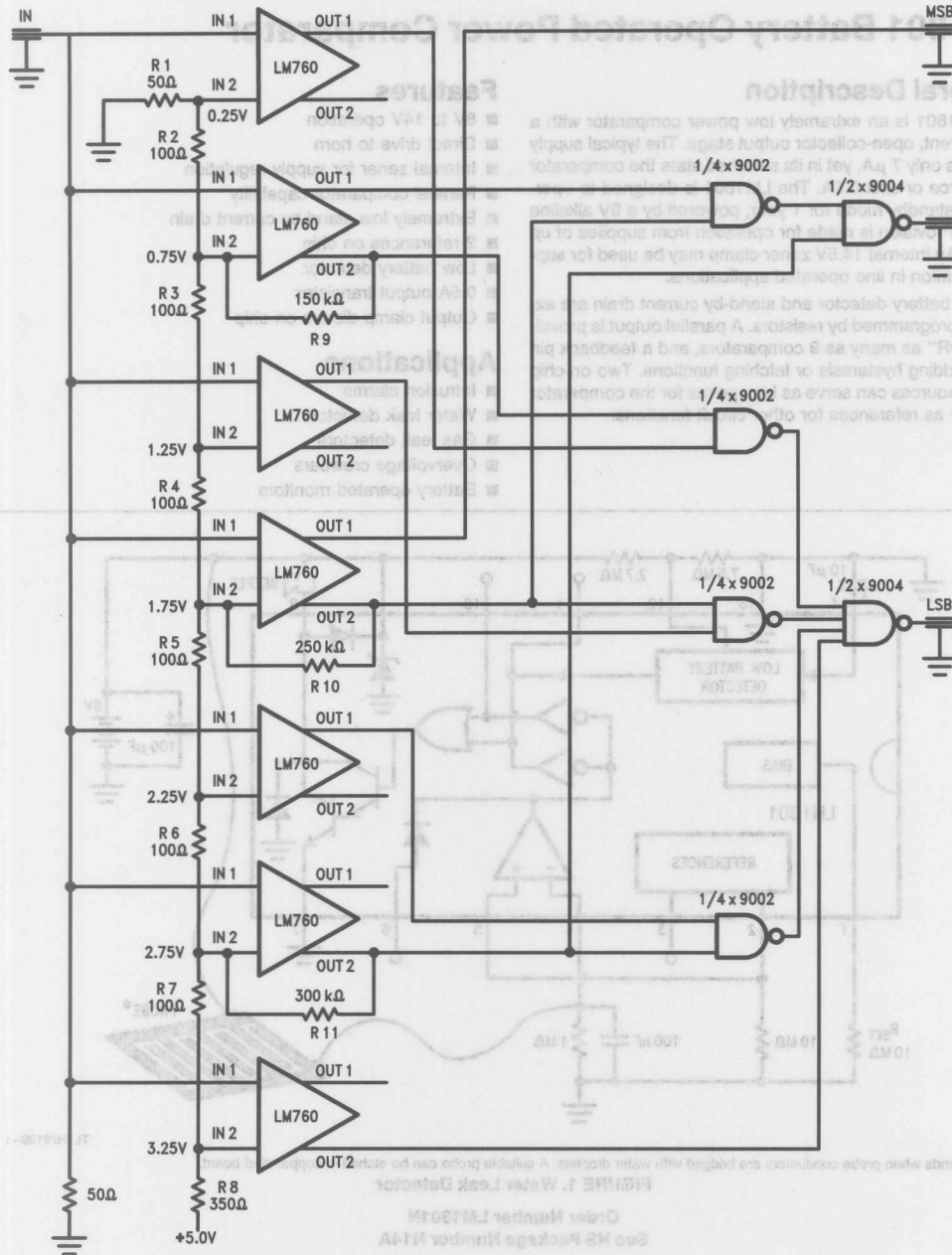
TL/H/10067-9

Total delay = 30 ns
Input Frequency = 300 Hz to 3.0 MHz
Minimum input voltage = 20 mV_{P-P}

Note 1: Lead numbers shown are for Metal Package only.

Note 2: All resistor values in ohms.

High Speed 3-Bit A/D Converter



Input voltage range = 3.5V
Typical conversion speed = 30 ns

TL/H/10067-11

LM1801 Battery Operated Power Comparator

General Description

The LM1801 is an extremely low power comparator with a high current, open-collector output stage. The typical supply current is only 7 μA , yet in its switched state the comparator can source or sink 0.5A. The LM1801 is designed to operate in a standby mode for 1 year, powered by a 9V alkaline battery. Provision is made for operation from supplies of up to 14V. An internal 14.5V zener clamp may be used for supply regulation in line operated applications.

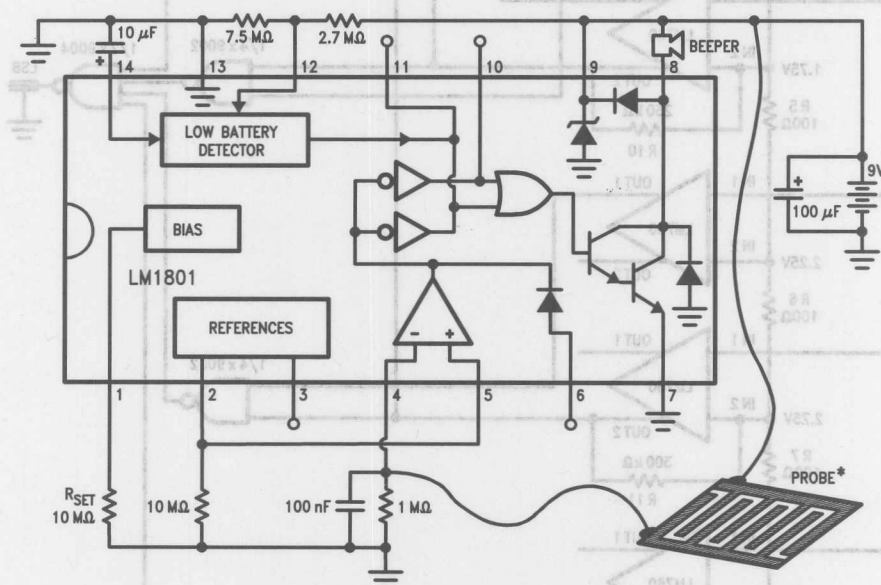
The low battery detector and stand-by current drain are externally programmed by resistors. A parallel output is provided to "OR" as many as 9 comparators, and a feedback pin allows adding hysteresis or latching functions. Two on-chip voltage sources can serve as bias points for the comparator inputs or as references for other circuit functions.

Features

- 8V to 14V operation
- Direct drive to horn
- Internal zener for supply regulation
- Parallel comparator capability
- Extremely low stand-by current drain
- 2 references on chip
- Low battery detector
- 0.5A output transistor
- Output clamp diodes on chip

Applications

- Intrusion alarms
- Water leak detectors
- Gas leak detectors
- Overvoltage crowbars
- Battery operated monitors



*Alarm sounds when probe conductors are bridged with water droplets. A suitable probe can be etched in copper clad board.

FIGURE 1. Water Leak Detector

Order Number LM1801N
See NS Package Number N14A

TL/H/9139-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|----------------------------|--------------|
| Supply Voltage | 14V |
| Input Voltage | -0.3V to 14V |
| Input Differential Voltage | ±14V |

Power Dissipation (Note 1)

1176 mW

Operating Temperature Range

0°C to +70°C

Storage Temperature Range

-65°C to +125°C

Lead Temperature (Soldering, 10 sec.)

260°C

ESD rating to be determined.

Electrical Characteristics (Note 2)

| Parameter | Conditions | Min | Typ | Max | Units |
|----------------------------|------------------------------------|-----|------|-----|---------|
| Comparator | | | | | |
| Input Offset Voltage | | | 5 | 15 | mV |
| Input Bias Current | | | 2 | 10 | nA |
| Input Offset Current | | | 0.5 | 8 | nA |
| Pin 6 Output Low | $I_{SINK} = 100 \mu A$ | | 1.5 | | V |
| Output Stage (Pin 8) | | | | | |
| Leakage Current | | | 5 | 100 | nA |
| Saturation Voltage | $I_B = 200 \text{ mA}$ | | 0.7 | 1.3 | V |
| Saturation Voltage | $I_B = 500 \text{ mA}$ | | 1.9 | | V |
| Common Alarm Line (Pin 10) | | | | | |
| Drive Capabilities | $V_4 > V_5$ | | | | |
| Output Voltage High | | | 6.8 | | V |
| Output Current | $V_{10} = 0.0V$ | | 6.5 | | mA |
| Driver Requirements | $V_5 > V_4$ | | | | |
| Input Voltage | | | 3.6 | | V |
| Input Current | $V_8 = 1.5V, I_B = 200 \text{ mA}$ | | 0.4 | | mA |
| Regulator | | | | | |
| Pin 2 Reference Voltage | | | 5.8 | | V |
| Temperature Coefficient | | | 5 | | mV/°C |
| Pin 3 Reference Voltage | | | 5.2 | | V |
| Temperature Coefficient | | | 7 | | mV/°C |
| Battery Check Oscillator | | | | | |
| Threshold Voltage (Pin 12) | | 5.5 | 6.0 | 6.5 | V |
| Period | $V^+ = 7.5V, C_1 = 10 \mu F$ | | 40 | 50 | s |
| Beep Pulse Width | $V^+ = 7.5V, C_1 = 10 \mu F$ | | 60 | | ms |
| Supply Current (Note 3) | | | 6 | 8 | μA |
| Zener Clamp Voltage, V9 | $I_B = 1 \text{ mA}$ | | 14.5 | | V |

Note 1: For operating at elevated temperatures, the device must be derated based on a 125°C maximum junction temperature and a thermal resistance of 85°C/W junction to ambient.

Note 2: $R_{SET} = 10 \text{ M}\Omega$, $V^+ = 9V$, $T_A = 25^\circ\text{C}$, (Figure 1).

Note 3: Output OFF.

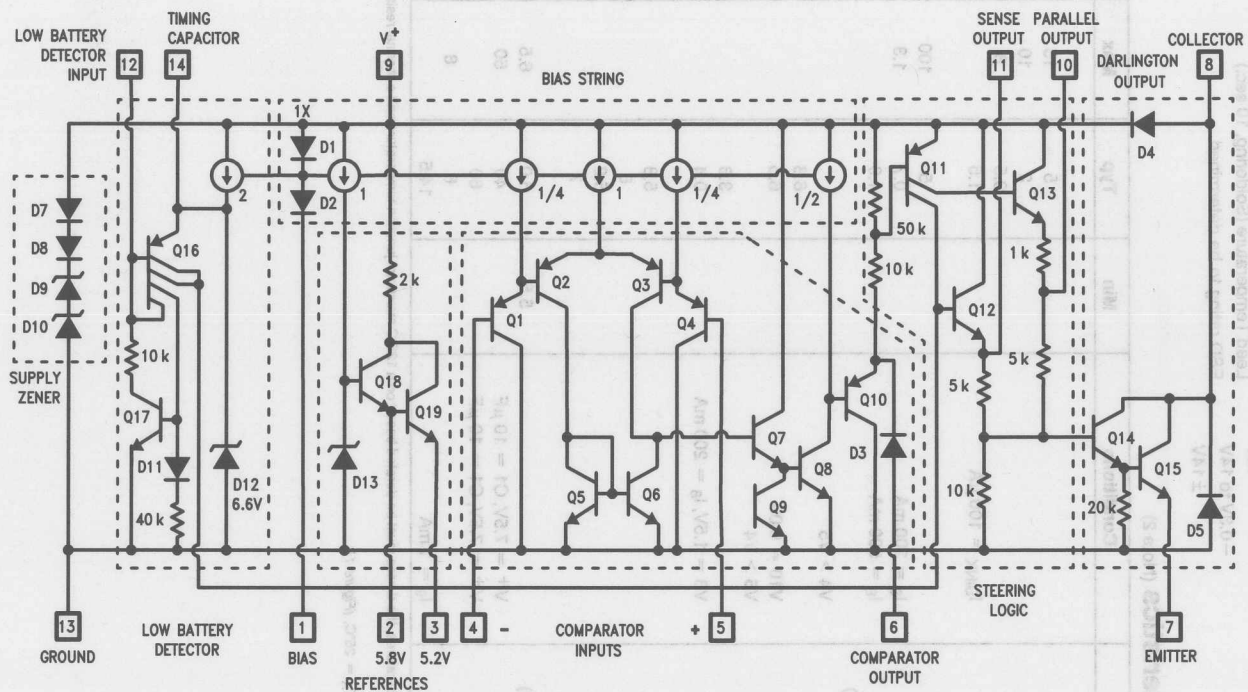


FIGURE 2. LM1801 Internal Schematic

Applications Hints

CIRCUIT OPERATION

The LM1801 includes a bias string, comparator, steering logic, output transistor, supply clamp, low voltage detector, and reference. An internal schematic is shown in *Figure 2*.

The chip is biased by a group of current sources that are controlled externally by a fixed resistor, R_{set} . In normal, or standby operation the supply current drain is nominally 6 times the set current at pin 1. The voltage at pin 1 is two forward diode potentials ($D1 + D2 = 1.2V$ typical) less than the positive supply voltage. Practical values of R_{set} range from 100 k Ω to 10 M Ω . Higher currents are useful where speed is important, while lower currents promote long battery life.

The total standby current drain of the LM1801 will include, in addition to the above, the current drawn by the external circuits connected at pins 2, 3, and 12. These are the resistive dividers used to set the low battery threshold and comparator threshold.

The voltage comparator consists of devices Q1 through Q10. The input features a common mode range from less than 300 mV to $V^+ - 1.2V$. If the non-inverting input is within this range, the output state remains valid for inverting inputs of 0V to V^+ . If the inverting input is within the common mode range, valid comparisons hold for non-inverting inputs of 300 mV to V^+ . The comparator may not switch low if the positive input is grounded.

With a set resistance of 10 M Ω , comparator input bias currents of 2 nA are typical. This allows the use of high-value resistors (10 M Ω) at the comparator inputs which help minimize total supply current. The comparator's output is available through a steering diode (D3) for latching or hysteresis functions.

The comparator output is also coupled internally to the steering logic (Q11–Q13). The comparator, low battery detector, and parallel output (pin 10) functions are OR'd in the logic circuit. In addition, the comparator output is steered to the parallel output. If the parallel outputs (pin 10) of two or more chips are wired together along with a common ground, the comparator on any one chip can cause all of the other output stages to switch, as well as its own output. Outputs are switched when the inverting comparator input is positive with respect to the non-inverting input. Low battery functions are coupled to the steering logic via Q12, and therefore do not affect the parallel output (Q13).

If the sense outputs (pin 11) of two or more chips are wired together, the comparator and low battery detector will cause all outputs to switch.

The output transistor is a 0.5A Darlington. Included in this structure are two clamp diodes. D4 clamps positive collector voltage excursions to the supply, and D5 clamps negative excursions to ground.

The output transistor is normally operated with the emitter grounded. Under these conditions the collector is guaranteed to saturate no higher than 1.3V at 200 mA. 1.9V saturation voltage is typical at 500 mA. The emitter may also be used as an output, and it can swing from ground potential up to 5V on a 9V supply. Emitter swing in the positive direction is limited in the parallel output mode.

A low battery detector with a 6V threshold is also included on chip. This circuit consists of Q16, Q17, D11, and D12. When pin 12, the battery sense input, is higher than 6V, D12 clamps the emitter of Q16 to 6.6V, and the output from the current source flows through the zener to ground. If pin 14 drops below 6V, Q16 is biased ON, and current is drawn away from the zener and into Q16. The SCR formed by Q16 and Q17 is triggered when Q16 is biased ON. The capacitor at pin 14 is discharged, part of its charge flows to the steering logic to pulse the output transistor, and the remainder holds the SCR in its ON state.

When the timing capacitor has discharged, conduction in Q16 and Q17 is commutated. Note that the output from the current source is less than the sustaining current required by the SCR. The current source slowly charges the capacitor until the voltage across it rises 0.6V above pin 12, where the cycle repeats itself. If pin 12 rises above 6V, the zener clamps the voltage at pin 14 and the low battery detector remains OFF.

Pin 12 is biased from an external resistive divider. The divider should be designed to detect at no lower than $V^+ = 7V$. The detector will continue to work at lower voltages providing pin 12 is at least 1V below the supply. For a 9V alkaline battery a threshold of 8.2V is common. A resistive divider of 2.7 M Ω and 7.5 M Ω provides the appropriate threshold.

In many applications the on-chip references can provide bias points. The references are driven from D13, and buffered by Q18 and Q19. If only one bias point is needed the first reference (pin 2) should be used, and the unused output (pin 3) may be left open. The tiny leakage currents in Q18 can cause Q19 (pin 3) to drift upward if a 10 M Ω load resistor is not included at pin 2. The combined output current from pins 2 and 3 should not exceed 1 mA. If neither reference output is used, pins 2 and 3 should be left open.

The last section of the LM1801 is the supply zener. It is built from a series combination of two diodes and two zeners. The breakdown voltage at 1 mA is 14.5V, and the series resistance is about 200 Ω . In line operated applications the zener may be used for supply regulation or transient protection. The zener is designed to carry up to 10 mA.

Applications Hints (Continued)

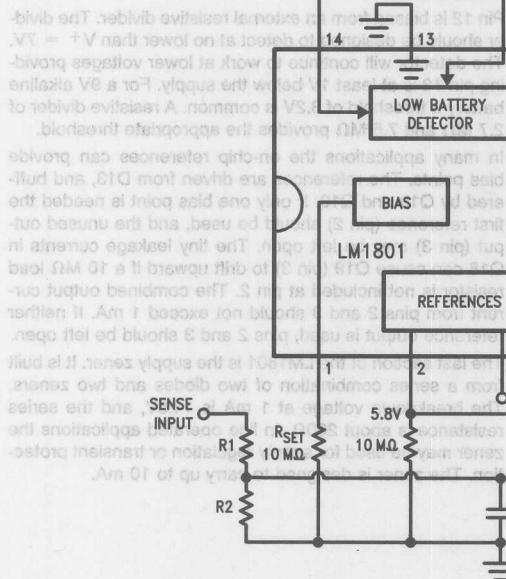
DESIGN HINTS

If the comparator inputs are subjected to electrostatic discharges (ESD), a series resistance is recommended to provide protection. Given the low input bias currents, 100 k Ω resistors can be added without affecting circuit performance, yet they greatly enhance static protection. The LM1801 is not designed to withstand reverse battery.

With a 10 M Ω R_{set} , the LM1801 responds to an input in approximately 2.5 μ s, and turns OFF in 200 μ s. Higher set currents decrease the response time. With $R_{set} = 1$ M Ω , the output switches low in 0.5 μ s, and high in 50 μ s, and with $R_{set} = 100$ k Ω , the response times are reduced to 0.2 μ s and 12 μ s.

When the circuit is in the standby state ($V_5 > V_4$), the current consumption in a typical application such as Figure 1 is less than approximately 7 μ A. However, when the comparator switches LOW ($V_4 > V_5$), the supply current increases to 3 mA owing to the Darlington base current. Therefore, to realize maximum battery life, any application should be devised so that $V_5 > V_4$ in the standby or resting state.

The current source slowly charges the capacitor by the SCR. The current source slowly charges the capacitor until the voltage across it has 0.8V above pin 12, where the cycle repeats itself. If pin 12 has above 0.8V, the cycle repeats the voltage at pin 12 and the low battery detector



$$R_1 + R_2 = 10 \text{ M}\Omega$$

$$V_{TRIP} = \left(\frac{R_1 + R_2}{R_2} \right) 5.8 \text{ V}$$

$$\text{Minimum trip voltage} = 5.8 \text{ V}$$

*Use series resistor for supplies > 14V. Select for $I_{ZENER} = 5$ mA.

**Reverse connections and add 1 M Ω resistor for overvoltage indication.

†Optional filter capacitor, 1 nF to 100 nF.

††Push to reset. Eliminate pin 6 connection for non-latching operation.

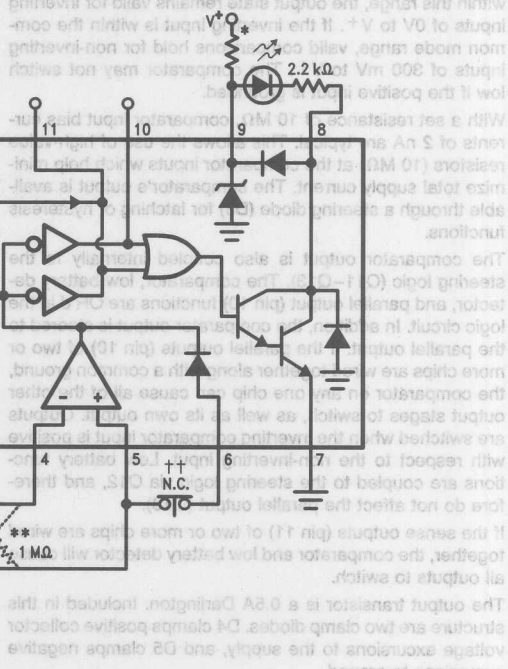
FIGURE 3. Under (Over) Voltage Indicator

The output stage can drive lamps, LEDs, buzzers, beepers, relays, motors, and solenoids. However, the low battery detector is not compatible with every load. Since the low battery detector generates only a short pulse (60 ms typical), it is intended for use with buzzers and beepers. Depending on the response time and resonant frequency, some buzzers may only produce a single click. Self-oscillating beepers usually start instantly and produce a recognizable "tweet" when a low battery condition is detected. Incandescent lamps, large relays and solenoids will do absolutely nothing when pulsed by the low battery detector.

Self-oscillating beepers are readily available, such as the Sonalert SNP428 and the Panasonic EAL-069A. These units are guaranteed to self-start when power is applied.

To defeat the low battery detector, short pins 12 and 14 together, and do not connect them to anything else.

Circuit board assembly procedures should include a thorough cleaning to remove flux and other residues. The input pins are often biased by very high impedance sources and even a 10 M Ω leakage path can upset circuit operation.



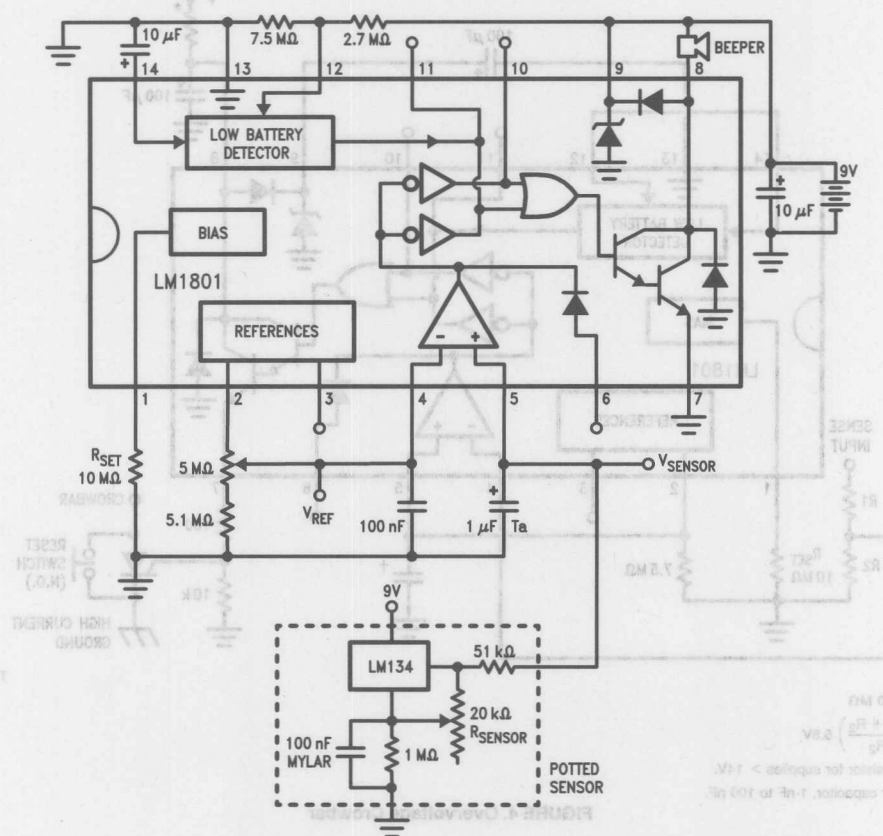
TL/H/9139-3



*Use series resistor for supplies > 14V.
†Optional filter capacitor, 1 nF to 100 nF.

FIGURE 4. Overvoltage Crowbar

Applications Hints (Continued)



TL/H/9139-5

To set trip point, trim V_{REF} to 4.5V. Trim R_{SENSOR} at room temperature (23°C) for:

$$V_{SENSOR} = 4.5 \left(\frac{273 + 23}{T_X + 273} \right)$$

where T_X is the desired trip point temperature in °C. As shown, the alarm is activated for over temperature conditions. Reverse the comparator connections for under temperature alarm. The 20 kΩ potentiometer allows an adjustment range of -55°C to +60°C. Add a 10k fixed resistance in series with the potentiometer for a +50°C to +125°C adjustment range. R_{SENSOR} can be replaced by a fixed resistor once the desired value is found. V_{REF} is used as a final adjustment.

FIGURE 5. Over (Under) Temperature Alarm

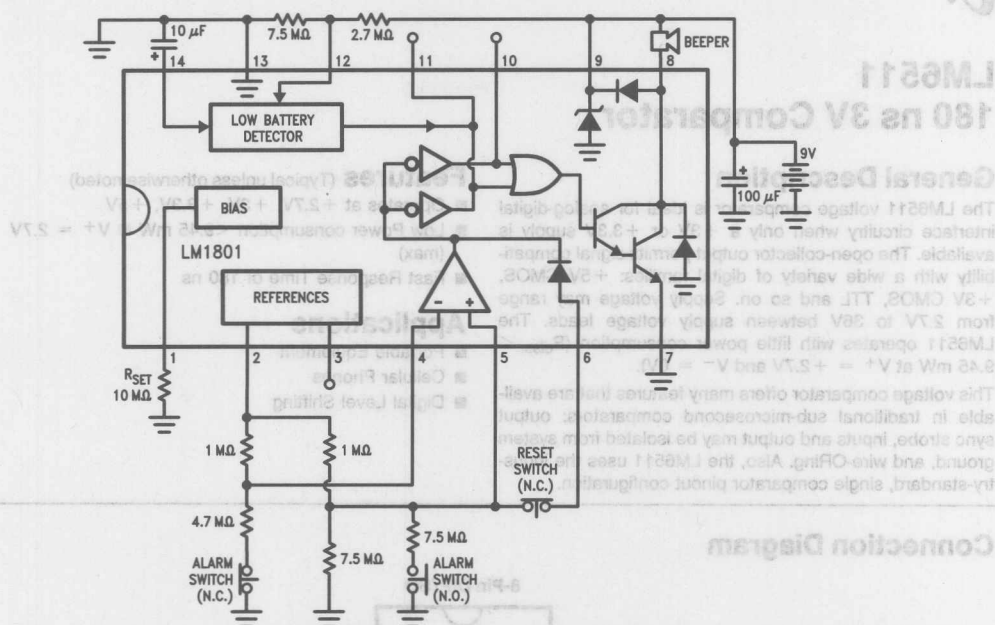


FIGURE 6. Simple Alarm Circuit

TL/H/9139-6

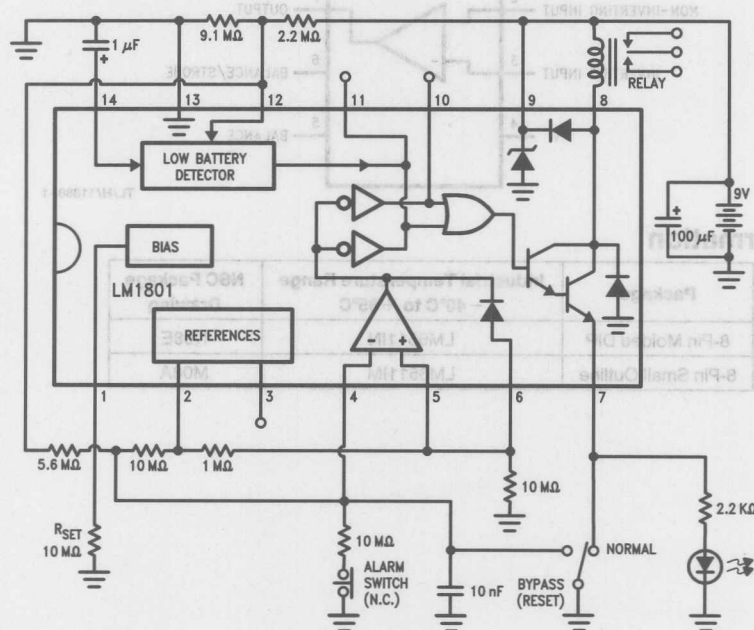


FIGURE 7. Full-Featured Intrusion Alarm

TL/H/9139-7

LM6511

180 ns 3V Comparator

General Description

The LM6511 voltage comparator is ideal for analog-digital interface circuitry when only a +3V or +3.3V supply is available. The open-collector output permits signal compatibility with a wide variety of digital families: +5V CMOS, +3V CMOS, TTL and so on. Supply voltage may range from 2.7V to 36V between supply voltage leads. The LM6511 operates with little power consumption ($P_{diss} < 9.45 \text{ mW}$ at $V^+ = +2.7\text{V}$ and $V^- = 0\text{V}$).

This voltage comparator offers many features that are available in traditional sub-microsecond comparators: output sync strobe, inputs and output may be isolated from system ground, and wire-ORing. Also, the LM6511 uses the industry-standard, single comparator pinout configuration.

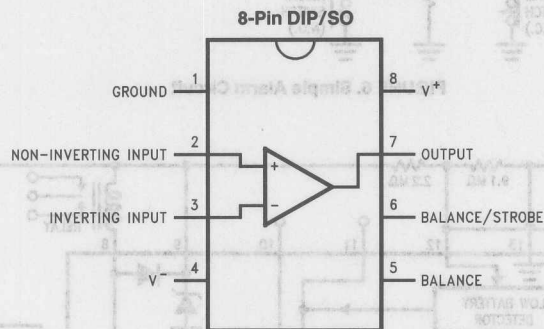
Features (Typical unless otherwise noted)

- Operates at +2.7V, +3V, +3.3V, +5V
- Low Power consumption $< 9.45 \text{ mW}$ @ $V^+ = 2.7\text{V}$ (max)
- Fast Response Time of 180 ns

Applications

- Portable Equipment
- Cellular Phones
- Digital Level Shifting

Connection Diagram



TL/H/11888-1

Ordering Information

| Package | Industrial Temperature Range -40°C to +85°C | NSC Package Drawing |
|---------------------|--|---------------------|
| 8-Pin Molded DIP | LM6511IN | N08E |
| 8-Pin Small Outline | LM6511IM | M08A |

Office/Distributors for availability and specifications.

| | |
|-----------------------------------|-----------------|
| Supply Voltage | -0.3 to +36V |
| Output to Negative Supply Voltage | 50V |
| Ground to Negative Supply Voltage | 30V |
| Differential Input Voltage | ±30V |
| Input Voltage | (Note 2) |
| Storage Temperature Range | -65°C to +150°C |

Soldering Information:

| | |
|------------------------------------|-------|
| DIP Package (Soldering in 10 sec) | 260°C |
| SO Package (Vapor Phase in 60 sec) | 215°C |
| SO Package (Infrared in 15 sec) | 220°C |

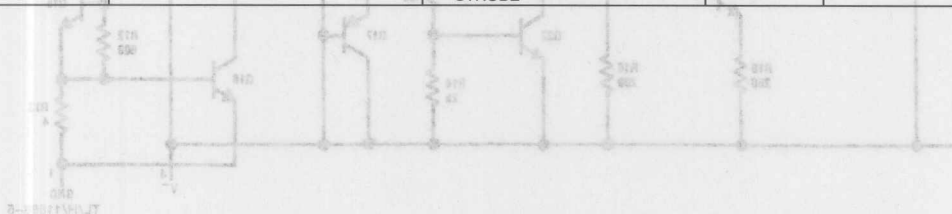
| | |
|--------------------------------------|-------|
| Junction Temperature | 150°C |
| ESD Rating (C = +100 pF, R = 1.5 kΩ) | 300V |

Operating Ratings (Note 1)

| | |
|---------------------------------------|--------------------------------|
| Supply Voltage | 2.5V to 30V |
| Temperature Range | -40°C ≤ T _J ≤ +85°C |
| Thermal Resistance (θ _{JA}) | |
| DIP Package | 110°C/W |
| SO Package | 170°C/W |

DC Electrical Characteristics Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 2.7V, V⁻ = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

| Symbol | Parameter | Conditions | Typical | LM6511I | Units (Limits) |
|---------------------|-----------------------------|--|---------|-----------------------|-------------------|
| | | | | Limit | |
| V _{OS} | Offset Voltage | R _S ≤ 50 kΩ (Note 3) | 1.5 | 5 8 | mV max |
| I _B | Input Bias Current | | 38 | 130 200 | nA max |
| I _{OS} | Input Offset Current | R _S ≤ 50 kΩ (Note 3) | 1.5 | 20 50 | nA max |
| I _S | Positive Supply Current | | 2.7 | 3.5 5 | mA max |
| | Negative Supply Current | | 1.5 | 2.0 2.5 | |
| V _{SAT} | Saturation Voltage | V _{IN} ≤ 10 mV I _{SINK} = 8 mA | 0.23 | 0.4 0.4 | V max |
| A _V | Large Signal Voltage Gain | ΔV _{OUT} = 2V | 40 | | V/mV |
| CMRR | Common Mode Rejection Ratio | | 72 | | dB |
| I _{STROBE} | Strobe ON Current | (Note 5) | 2.0 | 5.0 | mA max |
| V _{IN} | Input Voltage Range | | | 0.50 | V min |
| | | | | V ⁺ - 1.25 | V max |
| | Output Leakage Current | V _{IN} ≥ 10 mV, V _{OUT} = 35V, I _{STROBE} = 3 mA | 0.2 | | nA max |



AC Electrical Characteristics Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 2.7\text{V}$, $V^- = 0\text{V}$, $50\Omega \leq R_L \leq 50\text{ k}\Omega$, and $I_L = 1.0\text{ mA}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Typical | LM6511 | Units (Limits) |
|--------|---------------|------------|---------|--------|-------------------|
| | | | | Limit | |
| T_R | Response Time | (Note 4) | 180 | | ns |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

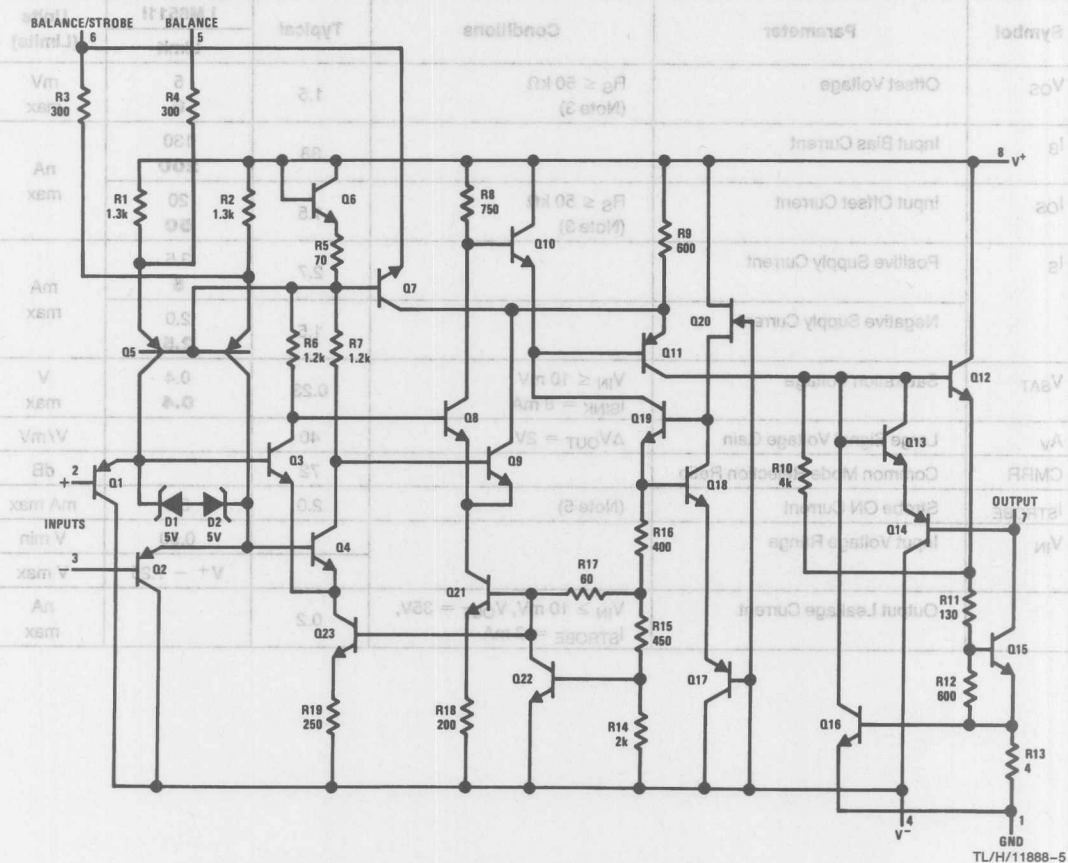
Note 2: The positive input voltage limit is 30V above the negative supply voltage. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply voltage, whichever is less.

Note 3: The offset voltage and offset current limits are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Therefore, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

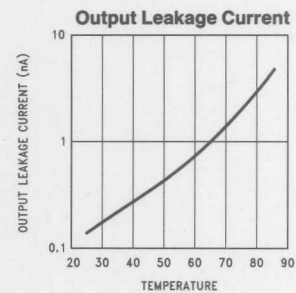
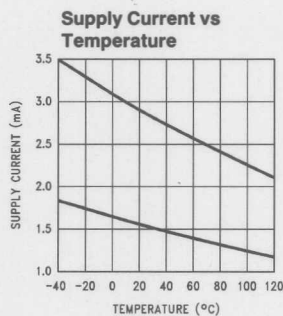
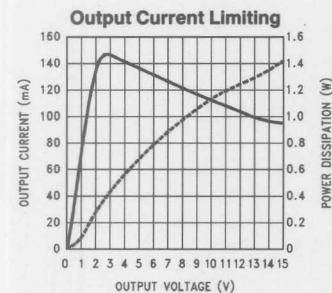
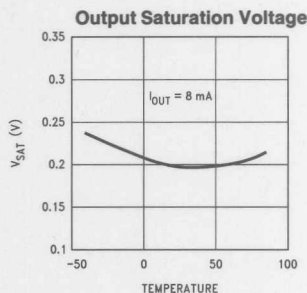
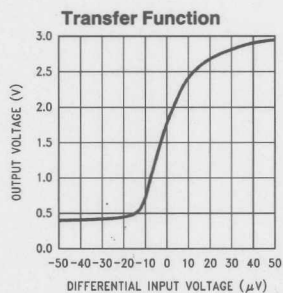
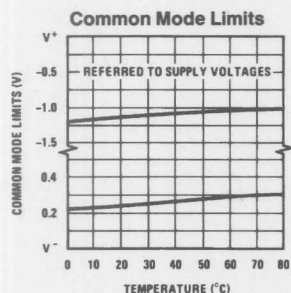
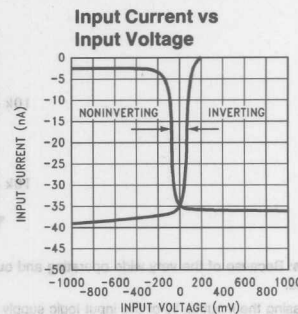
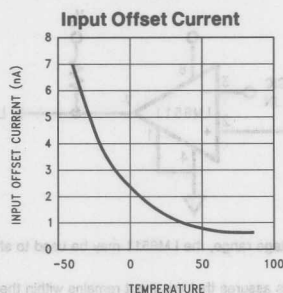
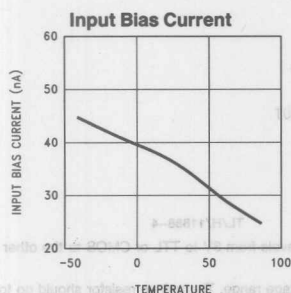
Note 4: This specification is for a 100 mV input step with a 25 mV overdrive.

Note 5: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 mA to 5 mA.

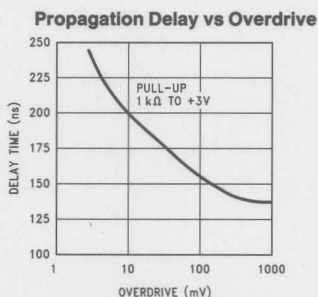
Schematic Diagram



LM6511 Typical Performance Characteristics $V_S = 3V$ unless otherwise noted



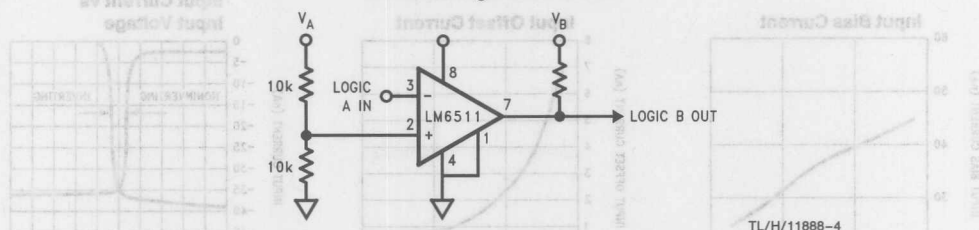
TL/H/11888-2



TL/H/11888-3

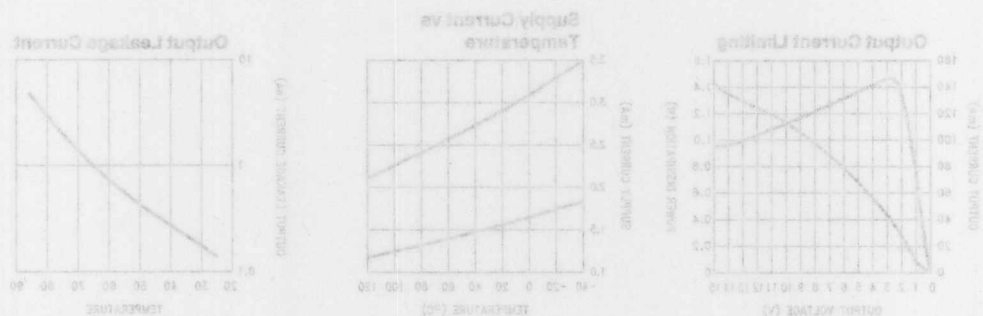
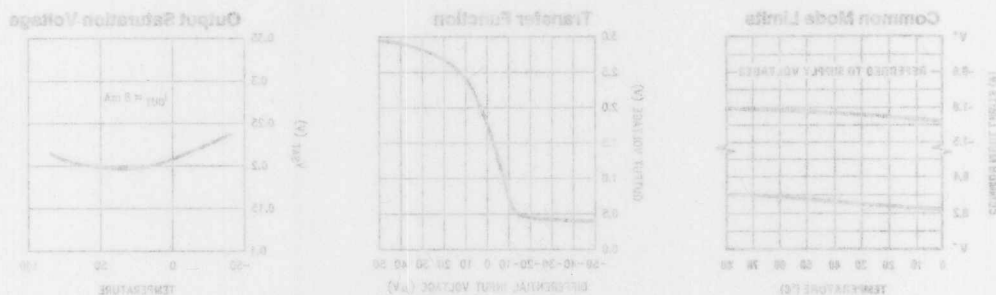
Typical Application

Universal Logic Level Shifter

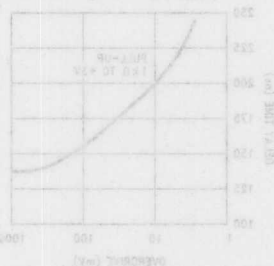


Notes: Because of the very wide operating and output voltage range, the LM6511 may be used to shift logic levels from 3V to TTL or CMOS to the other way around.

By biasing the input to $\frac{1}{2}$ of the input logic supply (V_A), this assures that this input remains within the input voltage range. The pull-up resistor should go to the output logic supply (V_B).



Propagation Delay vs. Overdrive



LMC6762 Dual/LMC6764 Quad MicroPower, Rail-To-Rail Input and Output CMOS Comparator

General Description

The LMC6762/4 is an ultra low power dual/quad comparator with a maximum supply current of 10 μA /comparator. It is designed to operate over a wide range of supply voltages, from 2.7V to 15V. The LMC6762/4 has guaranteed specs at 2.7V to meet the demands of 3V digital systems.

The LMC6762/4 has an input common-mode voltage range which exceeds both supplies. This is a significant advantage in low-voltage applications. The LMC6762/4 also features a push-pull output that allows direct connections to logic devices without a pull-up resistor.

A quiescent power consumption of 50 μW /amplifier (@ $V^+ = 5\text{V}$) makes the LMC6762/4 ideal for applications in portable phones and hand-held electronics. The ultra-low supply current is also independent of power supply voltage. Guaranteed operation at 2.7V and a rail-to-rail performance makes this device ideal for battery-powered applications.

Refer to the LMC6772/4 datasheet for an open-drain version of this device.

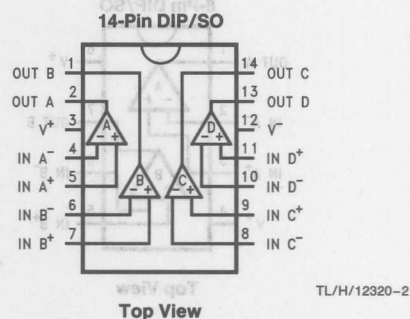
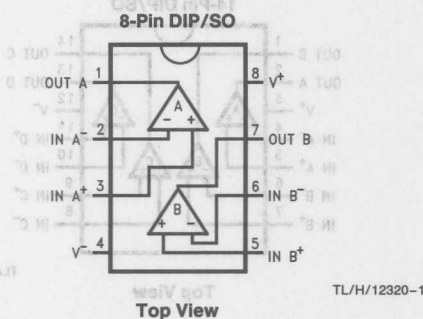
Features (Typical unless otherwise noted)

- Low power consumption (Guaranteed) $I_S = 10 \mu\text{A}/\text{comp}$
- Wide range of supply voltages 2.7V to 15V
- Rail-to-rail input common mode voltage range
- Rail-to-rail output swing (Within 100 mV of the supplies, @ $V^+ = 2.7\text{V}$, and $I_{\text{LOAD}} = 2.5 \text{ mA}$)
- Short circuit protection 40 mA
- Propagation delay (@ $V^+ = 5\text{V}$, 100 mV overdrive) 4 μs

Applications

- Laptop computers
- Mobile phones
- Metering systems
- Hand-held electronics
- RC timers
- Alarm and monitoring circuits
- Window comparators, multivibrators

Connection Diagrams



Ordering Information

| Package | Temperature Range -40°C to +85°C | NSC Drawing | Transport Media |
|----------------------|--|--------------|------------------------|
| 8-Pin Molded DIP | LMC6762AIN, LMC6762BIN | N08E | Rails |
| 8-Pin Small Outline | LMC6762AIM, LMC6762BIM LMC6762AIMX, LMC6762BIMX | M08A M08A | Rails Tape and Reel |
| 14-Pin Molded DIP | LMC6764AIN, LMC6764BIN | N08E | Rails |
| 14-Pin Small Outline | LMC6764AIM, LMC6764BIM LMC6764AIMX, LMC6764BIMX | M14A M14A | Rails Tape and Reel |

LMC6772 Dual, LMC6774 Quad, Micro-Power Rail-To-Rail Input and Open Drain Output CMOS Comparator

General Description

The LMC6772/4 is an ultra low power dual/quad comparator with a maximum 10 μA /comparator power supply current. It is designed to operate over a wide range of supply voltages, from 2.7V to 15V. The LMC6772/4 has guaranteed specs at 2.7V to meet the demands of 3V digital systems.

The LMC6772/4 has an input common-mode voltage range which exceeds both rails. This is a significant advantage in low-voltage applications. The LMC6772/4 also features an open-drain output. This architecture is ideal for mixed supply voltage systems as an external resistor can be used to pull the output up to +15V, regardless of the supply voltage.

A quiescent power consumption of 50 μW /Amplifier (@ $V_{\text{S}} = 5\text{V}$) makes the LMC6772/4 ideal for applications in portable phones and hand-held electronics. The ultra-low supply current is also independent of the power supply voltage. Guaranteed operation at 2.7V and rail-to-rail performance make the device ideal for battery-powered applications.

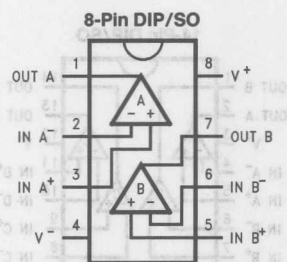
Features (Typical unless otherwise noted)

- Low power consumption $I_{\text{S}} = 10 \mu\text{A}/\text{comp}$
- Wide range of supply voltages 2.7V to 15V
- Rail-to-Rail Input Common Mode Voltage Range
- Open-drain output stage
- Short circuit protection 40 mA
- Propagation delay (@ $V_{\text{S}} = 5\text{V}$, 100 mV overdrive) 5 μs
- Refer to the LMC6762/4 datasheet for a device with similar specs and a push-pull output stage

Applications

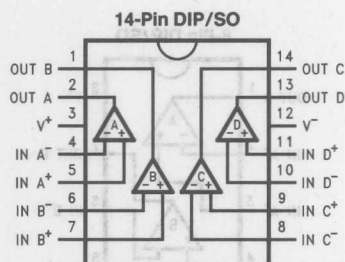
- Laptop computers
- Mobile Phones
- Metering systems
- Hand-held electronics
- RC timers, Window Comparators, Multivibrators
- Alarm and monitoring circuits

Connection Diagrams



Top View

TL/H/12347-1



Top View

TL/H/12347-2

| Package | Temperature Range Industrial, -40°C to $+85^{\circ}\text{C}$ | NSC Drawing | Transport Media |
|----------------------|---|----------------|--------------------|
| 8-Pin Molded DIP | LMC6772AIN, LMC6772BIN | N08E | Rails |
| 8-Pin Small Outline | LMC6772AIM, LMC6772BIM | M08A | Rails |
| | LMC6772AIMX, LMC6772BIMX | | Tape and Reel |
| 14-Pin Molded DIP | LMC6774AIN, LMC6774BIN | N14A | Rails |
| 14-Pin Small Outline | LMC6774AIM, LMC6774BIM | M14A | Rails |
| | LMC6774AIMX, LMC6774BIMX | | Tape and Reel |

LMC7211

Tiny CMOS Comparator with Rail-to-Rail Input

General Description

The LMC7211 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes the comparator ideal for space and weight critical designs. The LMC7211 is available in SO-8 surface mount packages and in conventional 8-pin DIP packages. The LMC7211 is supplied in two offset voltage grades, 5 mV and 15 mV.

The main benefits of the Tiny package are most apparent in small portable electronic devices, such as mobile phones, pagers, notebook computers, personal digital assistants, and PCMCIA cards. The rail-to-rail input voltage makes the LMC7211 a good choice for sensor interfacing, such as light detector circuits, optical and magnetic sensors, and alarm and status circuits.

The Tiny Comparator's outside dimensions (length x width x height) of 3.05mm x 3.00mm x 1.43mm allow it to fit into tight spaces on PC boards.

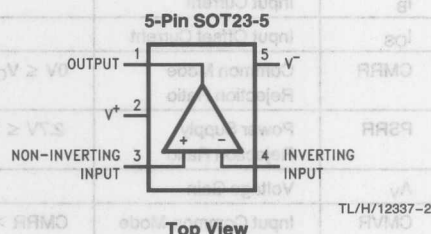
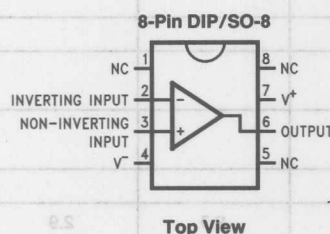
Features

- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 7 μ A at 5V
- Response time of 8 μ s at 5V
- LMC7211—push-pull output
- Input common-mode range beyond V^- and V^+
- Low input current

Applications

- Battery Powered Products
- Notebooks and PDAs
- PCMCIA cards
- Mobile Communications
- Alarm and Security circuits
- Direct Sensor Interface
- Replaces amplifiers used as comparators with better performance and lower current

Connection Diagrams



| Package | Ordering Information | NSC Drawing Number | Package Marking | Transport Media |
|----------------|----------------------|--------------------|-----------------|--------------------------|
| 8-Pin DIP | LMC7211AIN | N08E | LMC7211AIN | rails |
| 8-Pin DIP | LMC7211BIN | N08E | LMC7211BIN | rails |
| 8-Pin SO-8 | LMC7211AIM | M08A | LM7211AIM | rails |
| 8-Pin SO-8 | LMC7211BIM | M08A | LM7211BIM | rails |
| 8-Pin SO-8 | LMC7211AIMX | M08A | LM7211AIM | 2.5k units tape and reel |
| 8-Pin SO-8 | LMC7211BIMX | M08A | LM7211BIM | 2.5k units tape and reel |
| 5-Pin SOT 23-5 | LMC7211AIM5 | MA05A | C00A | 250 units tape and reel |
| 5-Pin SOT 23-5 | LMC7211BIM5 | MA05A | C00B | 250 units tape and reel |
| 5-Pin SOT 23-5 | LMC7211AIM5X | MA05A | C00A | 3k units tape and reel |
| 5-Pin SOT 23-5 | LMC7211BIM5X | MA05A | C00B | 3k units tape and reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------------|---|
| ESD Tolerance (Note 2) | 2 kV |
| Differential Input Voltage | $(V_{CC}) + 0.3V$ to $(-V_{CC}) - 0.3V$ |
| Voltage at Input/Output Pin | $(V_{CC}) + 0.3V$ to $(-V_{CC}) - 0.3V$ |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Current at Input Pin | ± 5 mA |
| Current at Output Pin (Note 3) | ± 20 mA |
| Current at Power Supply Pin | 40 mA |
| Lead Temperature (soldering, 10 sec) | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Junction Temperature (Note 4) | 150°C |

2.7V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 2.7V$, $V^- = 0V$, $V_{CM} = V_O = V^+ / 2$. **Boldface** limits apply at the temperature extremes.

Operating Ratings (Note 1)

| | |
|--------------------------------------|---|
| Supply Voltage | $2.7 \leq V_{CC} \leq 15V$ |
| Junction Temperature Range | $-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ |
| LMC7211AI, LMC7211BI | |
| Thermal Resistance (θ_{JA}) | |
| N Package, 8-pin Molded DIP | 115°C/W |
| SO-8 Package, 8-Pin Surface Mount | 165°C/W |
| M05A Package, 5-Pin Surface Mount | 325°C/W |

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7211AI Limit (Note 6) | LMC7211BI Limit (Note 6) | Units |
|------------|---|----------------------------|-----------------|--------------------------------|--------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 3 | 5 8 | 15 18 | mV max |
| TCV_{OS} | Input Offset Voltage Temperature Drift | | 1.0 | | | $\mu\text{V}/^\circ\text{C}$ |
| | Input Offset Voltage Average Drift | | 3.3 | | | $\mu\text{V}/\text{Month}$ |
| I_B | Input Current | | 0.04 | | | pA |
| I_{OS} | Input Offset Current | | 0.02 | | | pA |
| CMRR | Common Mode Rejection Ratio | $0V \leq V_{CM} \leq 2.7V$ | 75 | | | dB |
| PSRR | Power Supply Rejection Ratio | $2.7V \leq V^+ \leq 5V$ | 80 | | | dB |
| A_V | Voltage Gain | | 100 | | | dB |
| CMVR | Input Common-Mode Voltage Range | CMRR > 55 dB | 3.0 | 2.9 2.7 | 2.9 2.7 | V min |
| | | CMRR > 55 dB | -0.3 | -0.2 0.0 | -0.2 0.0 | V max |
| V_{OH} | Output Voltage High | $I_{load} = 2.5$ mA | 2.5 | 2.4 2.3 | 2.4 2.3 | V max |
| V_{OL} | Output Voltage Low | $I_{load} = 2.5$ mA | 0.2 | 0.3 0.4 | 0.3 0.4 | V max |
| I_S | Supply Current | $V_{OUT} = \text{low}$ | 7 | 12 14 | 12 14 | μA max |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

5.0V and 15.0V Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V^+ = 5.0\text{V}$ and 15V , $V^- = 0\text{V}$, $V_{CM} = V_O = V^+/2$.
Boldface limits apply at the temperature extremes.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC7211AI Limit (Note 6) | LMC7211BI Limit (Note 6) | Units |
|------------|---|--------------------------------------|-----------------|--------------------------------|--------------------------------|------------------------------|
| V_{OS} | Input Offset Voltage | | 3 | 5 8 | 15 18 | mV max |
| TCV_{OS} | Input Offset Voltage Temperature Drift | $V^+ = 5\text{V}$ | 1.0 | | | $\mu\text{V}/^\circ\text{C}$ |
| | | $V^+ = 15\text{V}$ | 4.0 | | | |
| | Input Offset Voltage Average Drift | $V^+ = 5\text{V}$ | 3.3 | | | $\mu\text{V}/\text{Month}$ |
| | | $V^+ = 15\text{V}$ | 4.0 | | | |
| I_B | Input Current | | 0.04 | | | pA |
| I_{OS} | Input Offset Current | | 0.02 | | | pA |
| CMRR | Common Mode Rejection Ratio | $V^+ = 5.0\text{V}$ | 75 | | | dB |
| | | $V^+ = 15.0\text{V}$ | 82 | | | dB |
| PSRR | Power Supply Rejection Ratio | $5\text{V} \leq V^+ \leq 10\text{V}$ | 80 | | | dB |
| A_V | Voltage Gain | | 100 | | | dB |
| CMVR | Input Common-Mode Voltage Range | $V^+ = 5.0\text{V}$ | 5.3 | 5.2 | 5.2 | V |
| | | CMRR > 55 dB | | 5.0 | 5.0 | min |
| | | $V^+ = 5.0\text{V}$ | -0.3 | -0.2 | -0.2 | V |
| | | CMRR > 55 dB | | 0.0 | 0.0 | max |
| | | $V^+ = 15.0\text{V}$ | 15.3 | 15.2 | 15.2 | V |
| V_{OH} | Output Voltage High | CMRR > 55 dB | | 15.0 | 15.0 | max |
| | | $V^+ = 15.0\text{V}$ | -0.3 | -0.2 | -0.2 | V |
| | | CMRR > 55 dB | | 0.0 | 0.0 | max |
| | | $V^+ = 5\text{V}$ | 4.8 | 4.6 | 4.6 | mV |
| | | $I_{load} = 5\text{ mA}$ | | 4.45 | 4.45 | max |
| V_{OL} | Output Voltage Low | $V^+ = 15\text{V}$ | 14.8 | 14.6 | 14.6 | mV |
| | | $I_{load} = 5\text{ mA}$ | | 14.45 | 14.45 | max |
| | | $V^+ = 5\text{V}$ | 0.2 | 0.40 | 0.40 | mV |
| | | $I_{load} = 5\text{ mA}$ | | 0.55 | 0.55 | min |
| | | $V^+ = 15\text{V}$ | 0.2 | 0.40 | 0.40 | mV |
| | | $I_{load} = 5\text{ mA}$ | | 0.55 | 0.55 | min |
| I_S | Supply Current | $V_{OUT} = \text{low}$ | 7 | 14 18 | 14 18 | μA max |
| I_{SC} | Short Circuit Current | Sourcing | 30 | | | mA min |
| | | Sinking | 45 | | | mA min |

| Symbol | Parameter | Conditions | Typ (Note 5) | Limit (Note 6) | Limit (Note 6) | Units |
|------------|------------------------------------|--|-----------------|-------------------|-------------------|---------------|
| t_{rise} | Rise Time | $f = 10 \text{ kHz}$, $C_I = 50 \text{ pF}$, Overdrive = 10 mV | 0.3 | | | μs |
| t_{fall} | Fall Time | $f = 10 \text{ kHz}$, $C_I = 50 \text{ pF}$, Overdrive = 10 mV | 0.3 | | | μs |
| t_{PHL} | Propagation Delay (High to Low) | $f = 10 \text{ kHz}$, $C_I = 50 \text{ pF}$ | 10 mV | 10 | | μs |
| | | | 100 mV | 4 | | |
| | | $V^+ = 2.7\text{V}$, $f = 10 \text{ kHz}$, $C_I = 50 \text{ pF}$ | 10 mV | 10 | | μs |
| | | | 100 mV | 4 | | |
| t_{PLH} | Propagation Delay (Low to High) | $f = 10 \text{ kHz}$, $C_I = 50\text{p}$ | 10 mV | 6 | | μs |
| | | | 100 mV | 4 | | |
| | | $V^+ = 2.7\text{V}$, $f = 10 \text{ kHz}$, $C_I = 50 \text{ pF}$ | 10 mV | 7 | | μs |
| | | | 100 mV | 4 | | |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF.

Note 3: Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C.

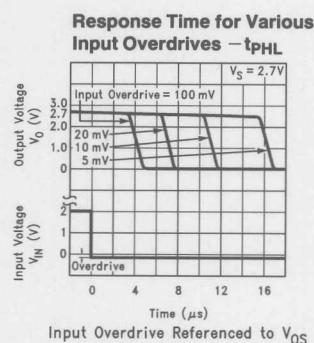
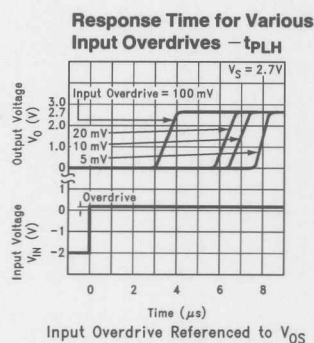
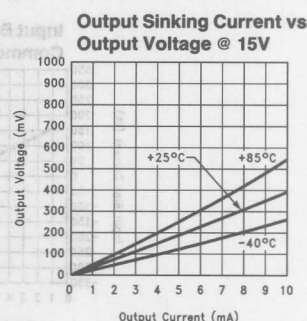
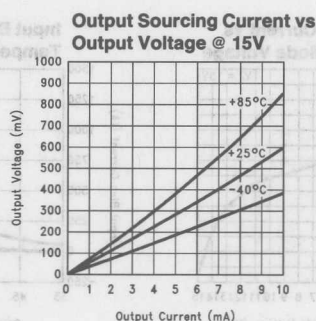
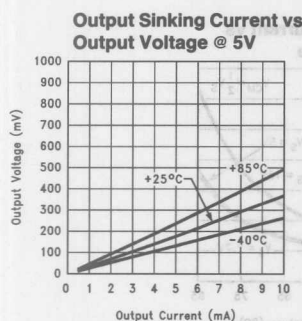
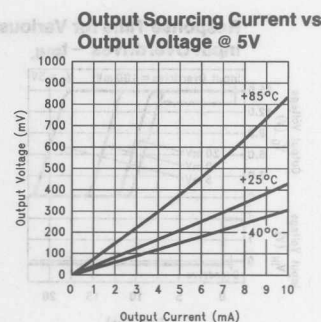
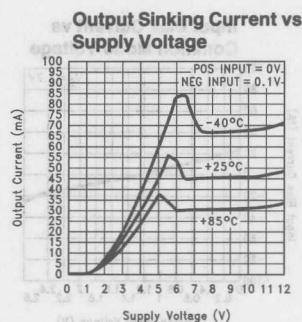
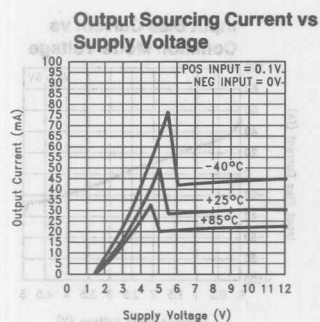
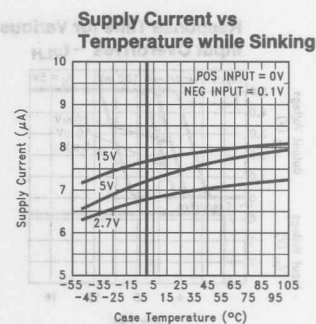
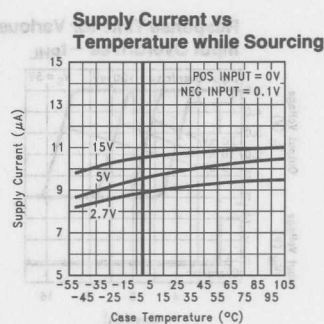
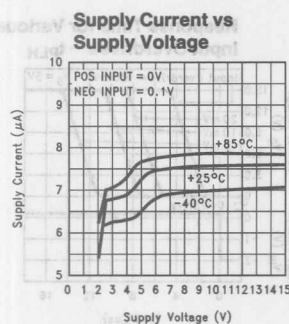
Note 4: The maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)} - T_A)/\theta_{JA}$. All numbers apply for packages soldered directly into a PC board.

Note 5: Typical values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

| | | | | | | |
|---------|------|------|------|-------------------------|-----------------------|----------|
| V_m | 3.4 | 3.4 | 3.4 | $V_O = +V$ | Output Voltage High | V_O |
| x_{m} | 2.4 | 2.4 | 2.4 | $I_{O1} = 5 \text{ mA}$ | | |
| V_m | 3.4 | 3.4 | 3.4 | $V_O = -V$ | Output Voltage Low | V_O |
| x_{m} | 2.4 | 2.4 | 2.4 | $I_{O1} = 5 \text{ mA}$ | | |
| V_m | 0.40 | 0.40 | 0.40 | $V_O = 0\text{V}$ | | |
| n_m | 0.05 | 0.05 | 0.05 | $I_{O1} = 5 \text{ mA}$ | | |
| V_m | 0.40 | 0.40 | 0.40 | $V_O = 0\text{V}$ | | |
| n_m | 0.05 | 0.05 | 0.05 | $I_{O1} = 5 \text{ mA}$ | | |
| A_v | 14 | 14 | 14 | $V_{O1} = 0\text{V}$ | Supply Current | I_S |
| x_{m} | 2.4 | 2.4 | 2.4 | | | |
| n_m | 0.05 | 0.05 | 0.05 | | Short Circuit Current | I_{SC} |
| n_m | 0.05 | 0.05 | 0.05 | | | |

Typical Performance Characteristics

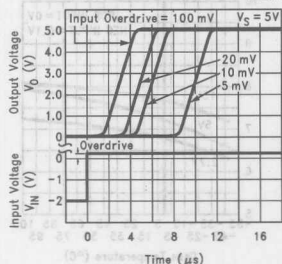
Single Supply $T_A = 25^\circ\text{C}$ unless specified

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Typical Performance Characteristics

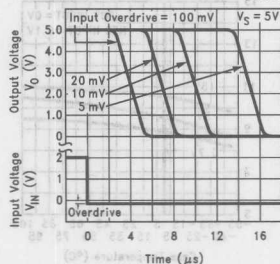
Single Supply, $T_A = 25^\circ\text{C}$ unless specified (Continued)

Response Time for Various Input Overdrives – t_{PLH}



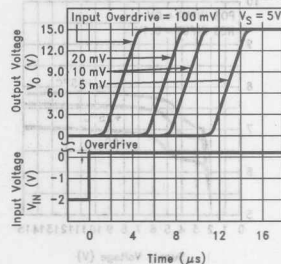
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives – t_{PLH}



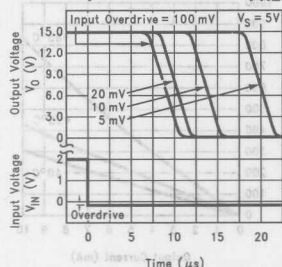
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives – t_{PLH}



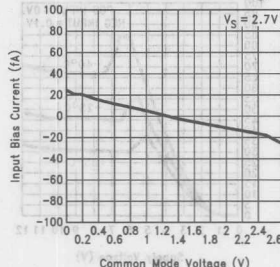
Input Overdrive Referenced to V_{OS}

Response Time for Various Input Overdrives – t_{PLH}

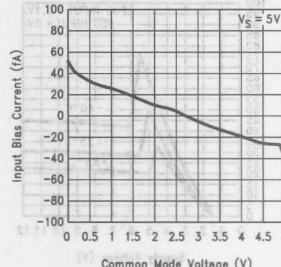


Input Overdrive Referenced to V_{OS}

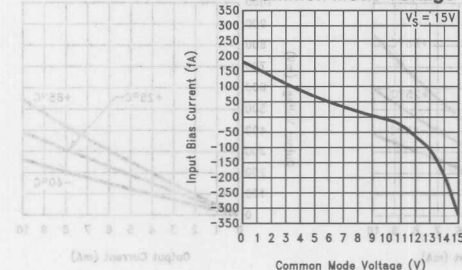
Input Bias Current vs Common Mode Voltage



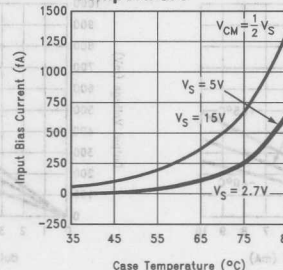
Input Bias Current vs Common Mode Voltage



Input Bias Current vs Common Mode Voltage



Input Bias Current vs Temperature



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Application Information

1.0 Benefits of the LMC7211 Tiny Comparator

Size. The small footprint of the SOT 23-5 packaged Tiny Comparator, (0.120 x 0.118 inches, 3.05 x 3.00 mm) saves space on printed circuit boards, and enable the design of smaller electronic products. Because they are easier to carry, many customers prefer smaller and lighter products.

Height. The height (0.056 inches, 1.43 mm) of the Tiny Comparator makes it possible to use it in PCMCIA type III cards.

Simplified Board Layout. The Tiny Comparator can simplify board layout in several ways. First, by placing a comparator where comparators are needed, instead of routing signals to a dual or quad device, long pc traces may be avoided.

By using multiple Tiny Comparators instead of duals or quads, complex signal routing and possibly crosstalk can be reduced.

DIPs available for prototyping. LMC7211 comparators packaged in conventional 8-pin dip packages can be used for prototyping and evaluation without the need to use surface mounting in early project stages.

Low Supply Current. The typical 7 μ A supply current of the LMC7211 extends battery life in portable applications, and may allow the reduction of the size of batteries in some applications.

Wide Voltage Range. The LMC7211 is characterized at 15V, 5V and 2.7V. Performance data is provided at these popular voltages. This wide voltage range makes the LMC7211 a good choice for devices where the voltage may vary over the life of the batteries.

Digital Outputs Representing Signal Level. Comparators provide a high or low digital output depending on the voltage levels of the (+) and (-) inputs. This makes comparators useful for interfacing analog signals to microprocessors and other digital circuits. The LMC7211 can be thought of as a one-bit a/d converter.

Push-Pull Output. The push-pull output of the LMC7211 is capable of both sourcing and sinking milliamp level currents even at a 2.7 volt supply. This can allow the LMC7211 to drive multiple logic gates.

Driving LEDs (Light Emitting Diodes). With a 5 volt power supply, the LMC7211's output sinking current can drive small, high efficiency LEDs for indicator and test point circuits. The small size of the Tiny package makes it easy to find space to add this feature to even compact designs.

Input range to Beyond Rail to Rail. The input common mode range of the LMC7211 is slightly larger than the actual power supply range. This wide input range means that the comparator can be used to sense signals close to the power supply rails. This wide input range can make design easier by eliminating voltage dividers, amplifiers, and other front end circuits previously used to match signals to the limited input range of earlier comparators. This is useful to power supply monitoring circuits which need to sense their own power supply, and compare it to a reference voltage which

is close to the power supply voltage. The wide input range can also be useful for sensing the voltage drop across a current sense resistor for battery chargers.

Zero Crossing Detector. Since the LMC7211's common mode input range extends below ground even when powered by a single positive supply, it can be used with large input resistors as a zero crossing detector.

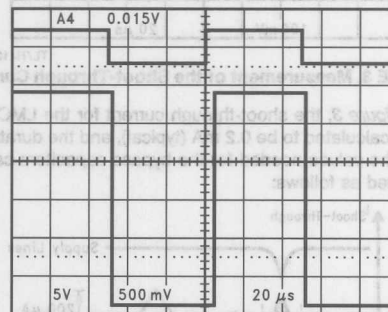
Low Input Currents and High Input Impedance. These characteristics allow the LMC7211 to be used to sense high impedance signals from sensors. They also make it possible to use the LMC7211 in timing circuits built with large value resistors. This can reduce the power dissipation of timing circuits. For very long timing circuits, using high value resistors can reduce the size and cost of large value capacitors for the same R-C time constant.

Direct Sensor Interfacing. The wide input voltage range and high impedance of the LMC7211 may make it possible to directly interface to a sensor without the use of amplifiers or bias circuits. In circuits with sensors which can produce outputs in the tens to hundreds of millivolts, the LMC7211 can compare the sensor signal with an appropriately small reference voltage. This may be done close to ground or the positive supply rail. Direct sensor interfacing may eliminate the need for an amplifier for the sensor signal. Eliminating the amplifier can save cost, space, and design time.

2.0 Low Voltage Operation

Comparators are the common devices by which analog signals interface with digital circuits. The LMC7211 has been designed to operate at supply voltages of 2.7V without sacrificing performance to meet the demands of 3V digital systems.

At supply voltages of 2.7V, the common-mode voltage range extends 200 mV (guaranteed) below the negative supply. This feature, in addition to the comparator being able to sense signals near the positive rail, is extremely useful in low voltage applications.



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FIGURE 1. Even at Low-Supply Voltage of 2.7V, an Input Signal which Exceeds the Supply Voltages Produces No Phase Inversion at the Output

At $V^+ = 2.7V$ propagation delays are $t_{PLH} = 4 \mu s$ and $t_{PHL} = 4 \mu s$ with overdrives of 100 mV.

Please refer to the performance curves for more extensive characterization.

Application Information (Continued)

3.0 Shoot-Through Current

The shoot-through current is defined as the current surge, above the quiescent supply current, between the positive and negative supplies of a device. The current surge occurs when the output of the device switches states. The shoot-through current results in glitches in the supply voltages. Usually, glitches in the supply lines are prevented by bypass capacitors. When the glitches are minimal, the value of the bypass capacitors can be reduced.

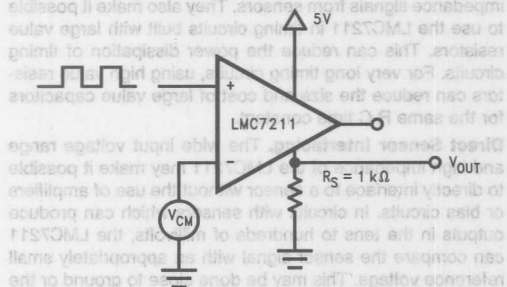


FIGURE 2. Circuit for Measurement of the Shoot-Through Current

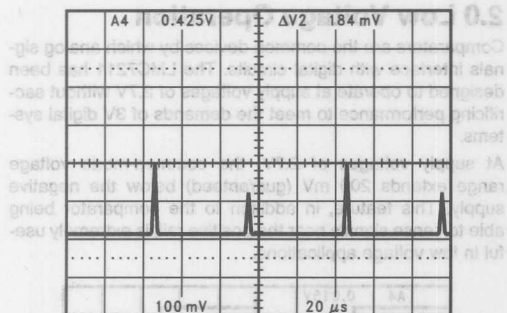
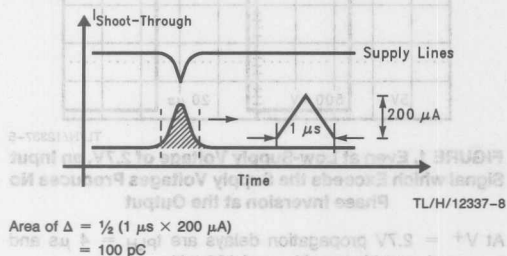


FIGURE 3. Measurement of the Shoot-Through Current

From Figure 3, the shoot-through current for the LMC7211 can be calculated to be 0.2 mA (typical), and the duration is 1 μs. The values needed for the bypass capacitors can be calculated as follows:



The capacitor needs to supply 100 picocoulomb. To avoid large shifts in the comparator threshold due to changes in the voltage level, the voltage drop at the bypass capacitor should be limited to 100 mV or less.

The charge needed (100 picocoulomb) and the allowable voltage drop (100 mV) will give us the minimum capacitor value required.

$$\Delta Q = C (\Delta V)$$

$$C = \Delta Q / \Delta V = 100 \text{ picocoulomb} / 100 \text{ mV}$$

$$C = 10^{-10} / 10^{-1} = 10^{-9} = 1 \text{ nF} = 0.001 \mu\text{F}$$

$$10^{-9} = 1 \text{ nF} = 0.001 \mu\text{F}$$

The voltage drop of ~100 mV will cause a threshold shift in the comparator. This threshold shift will be reduced by the power supply rejection ratio, (PSRR). The PSRR which is applicable here is not the DC value of PSRR (~80 dB), but a transient PSRR which will be usually about 20 dB–40 dB, depending on the circuit and the speed of the transient. This will result in an effective threshold shift of about 1 mV to 10 mV.

For precision and level sensing circuits, it is generally a good goal to reduce the voltage delta on the power supply to a value equal to or less than the hysteresis of the comparator circuit. If the above circuit was to be used with 50 mV of hysteresis, it would be reasonable to increase the bypass capacitor to 0.01 μF to reduce the voltage delta to 10 mV. Larger values may be useful for obtaining more accurate and consistent switching.

Note that the switching current of the comparator can spread to other parts of the board as noise. The bypass capacitor reduces this noise. For low noise systems this may be reason to make the capacitor larger.

For non-precision circuits, such as using a comparator to determine if a push-button switch is on or off, it is often cheaper and easier to use a larger value of hysteresis and a small value or bypass capacitance. The low shoot-through current of the LMC7211 can allow the use of smaller and less expensive bypass capacitors in non-critical circuits.

4.0 Output Short Circuit Current

The LMC7211 has short circuit protection of 40 mA. However, it is not designed to withstand continuous short circuits, transient voltage or current spikes, or shorts to any voltage beyond the supplies. A resistor in series with the output should reduce the effect of shorts. For outputs which send signals off PC boards additional protection devices, such as diodes to the supply rails, and varistors may be used.

5.0 Hysteresis

If the input signal is very slow or very noisy, the comparator output might trip several times as the input signal passes through the threshold. Using positive feedback to add hysteresis to the switching can reduce or eliminate this problem. The positive feedback can be added by a high value resistor (R_F). This will result in two switching thresholds, one for increasing signals and one for decreasing signals. A capacitor can be added across R_F to increase the switching speed and provide more short term hysteresis. This can result in greater noise immunity for the circuit.

See Figures 4, 5 and 6.

Application Information (Continued)

Note that very heavy loading of the comparator output, such as LED drive or bipolar logic gates, will change the output voltage and shift the voltage thresholds.

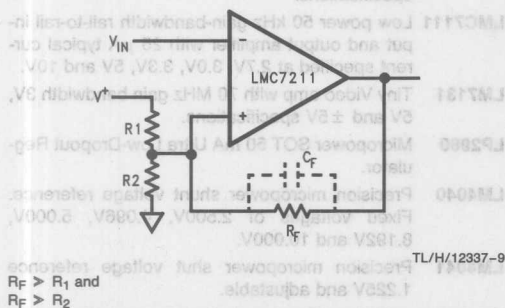


FIGURE 4. Positive Feedback for Hysteresis

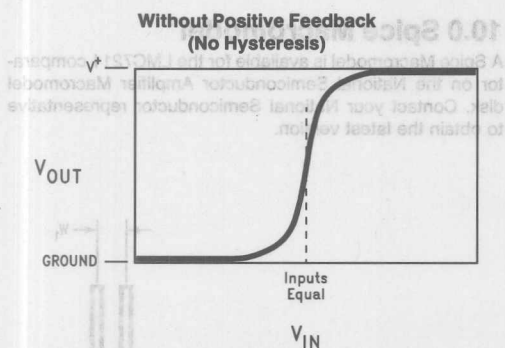


FIGURE 5

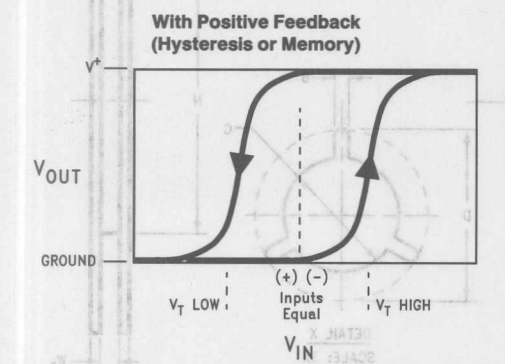


FIGURE 6

6.0 Input Protection

If input signals are like to exceed the common mode range of the LMC7211, or it is likely that signals may be present when power is off, damage to the LMC7211 may occur. Large value (100 kΩ to MΩ) input resistors may reduce the likelihood of damage by limiting the input currents. Since the LMC7211 has very low input leakage currents, the effect on accuracy will be small. Additional protection may require the use of diodes, as shown in Figure 7. Note that diode leakage current may affect accuracy during normal operation. The R-C time constant of R_{IN} and the diode capacitance may also slow response time.

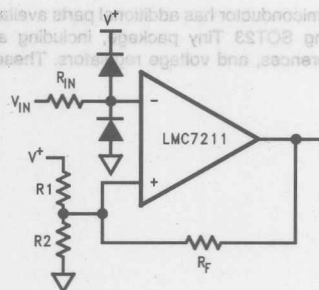


FIGURE 7

7.0 Layout Considerations

The LMC7211 is not an especially fast comparator, so high speed design practices are not required. The LMC7211 is capable of operating with very high impedance inputs, so precautions should be taken to reduce noise pickup with high impedance (~ 100 kΩ and greater) designs and in electrically noisy environments.

Keeping high value resistors close to the LMC7211 and minimizing the size of the input nodes is a good practice. With multilayer designs, try to avoid long loops which could act as inductors (coils). Sensors which are not close to the comparator may need twisted pair or shielded connections to reduce noise.

8.0 Open Drain Output, Dual and Quad Versions

The LMC7221 is a comparator similar to the LMC7211, but with an open drain output which allows the output voltage to be different (higher or lower) than the supply voltage. The open drain output is like the open collector output of a logic gate. This makes the LMC7221 very useful for mixed voltage systems. Many systems will have different voltages for the analog and microprocessor sections. Please see the LMC7221 datasheet for details.

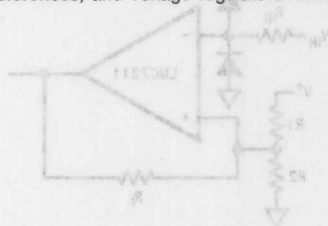
The performance of the LMC7211 is available in dual devices. Please see the LMC6762 datasheet for details on a dual push-pull output device. For a dual device with open drain outputs, please see the LMC6772 datasheet.

| Type | Size | A | B | C | D | N | W1 | W2 | W3 |
|------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| mm | 25.00 | 1.50 | 20.00 | 10.00 | 10.00 | 10.00 | 10.00 | 10.00 | 10.00 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |
| | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 | 0.000 |

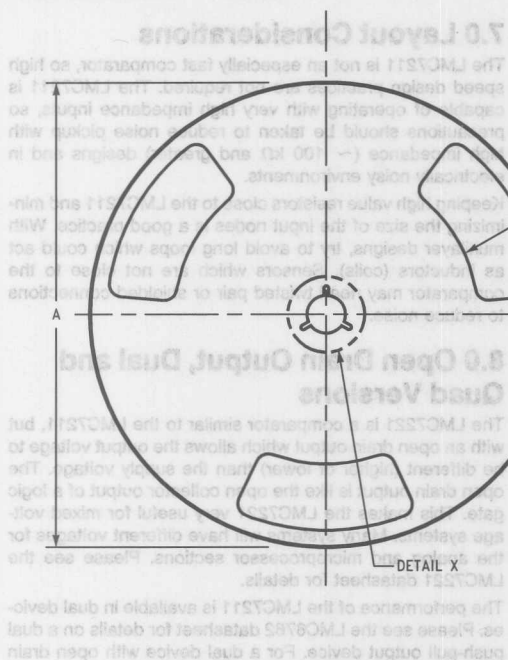
| Push-Pull Output | | | |
|-------------------|--------------------|--------|--|
| LMC7211 | Tiny, SOT23-5, DIP | Single | |
| LMC6762 | SO-8, DIP | Dual | |
| Open Drain Output | | | |
| LMC7221 | Tiny, SOT23-5, DIP | Single | |
| LMC6772 | SO-8, DIP | Dual | |

9.0 Additional SOT23-5 Tiny Devices

National Semiconductor has additional parts available in the space saving SOT23 Tiny package, including amplifiers, voltage references, and voltage regulators. These devices include—



REEL DIMENSIONS

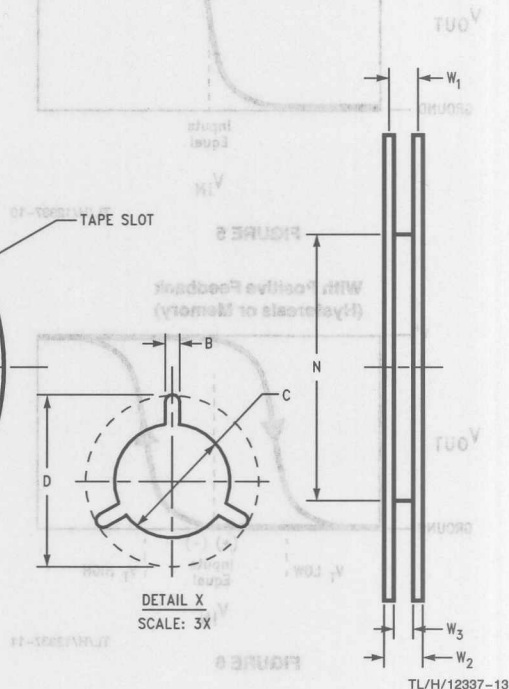


- put amplifier—high input impedance and high gain 700 μ A typical current 2.7V, 3V, 5V and 15V specifications.
- LMC7111** Low power 50 kHz gain-bandwidth rail-to-rail input and output amplifier with 25 μ A typical current specified at 2.7V, 3.0V, 3.3V, 5V and 10V.
- LM7131** Tiny Video amp with 70 MHz gain bandwidth 3V, 5V and \pm 5V specifications.
- LP2980** Micropower SOT 50 mA Ultra Low-Dropout Regulator.
- LM4040** Precision micropower shunt voltage reference. Fixed voltages of 2.500V, 4.096V, 5.000V, 8.192V and 10.000V.
- LM4041** Precision micropower shut voltage reference 1.225V and adjustable.

Contact your National Semiconductor representative for the latest information.

10.0 Spice Macromodel

A Spice Macromodel is available for the LMC7211 comparator on the National Semiconductor Amplifier Macromodel disk. Contact your National Semiconductor representative to obtain the latest version.



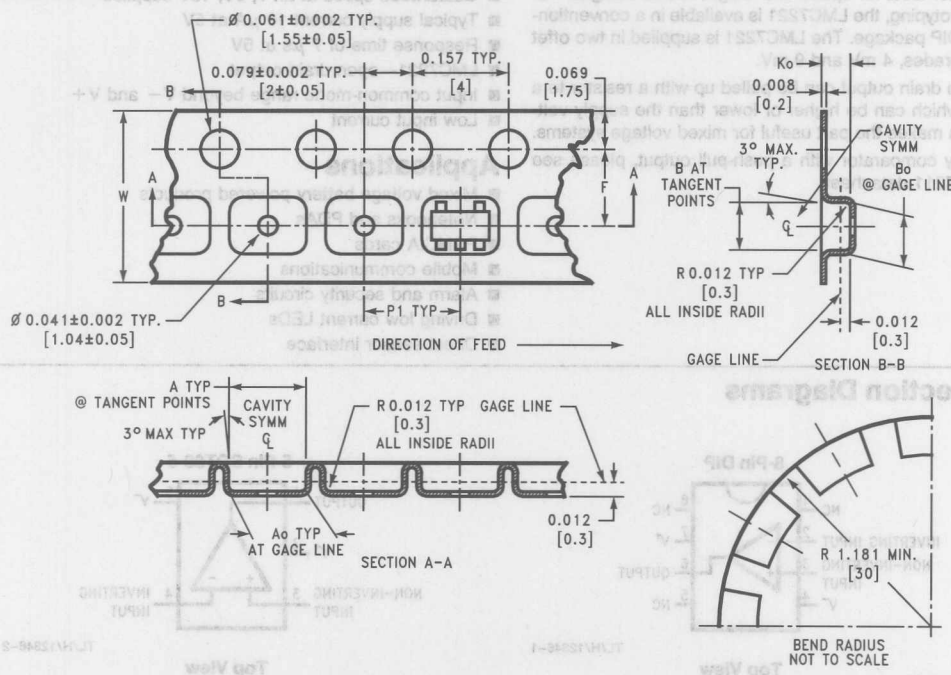
| 8 mm | 7.00 | 0.059 | 0.512 | 0.795 | 2.165 | 0.331 + 0.059/-0.000 | 0.567 | W1 + 0.078/-0.039 |
|-----------|--------|-------|-------|-------|-------|----------------------|-------|-------------------|
| | 330.00 | 1.50 | 13.00 | 20.20 | 55.00 | 8.40 + 1.50/-0.00 | 14.40 | W1 + 2.00/-1.00 |
| Tape Size | A | B | C | D | N | W1 | W2 | W3 |

SOT-23-5 Tape and Reel Specification

TAPE FORMAT

| Tape Section | # Cavities | Cavity Status | Cover Tape Status |
|-----------------------|------------|---------------|-------------------|
| Leader (Start End) | 0 (min) | Empty | Sealed |
| | 75 (min) | Empty | Sealed |
| Carrier | 3000 | Filled | Sealed |
| | 250 | Filled | Sealed |
| Trailer (Hub End) | 125 (min) | Empty | Sealed |
| | 0 (min) | Empty | Sealed |

TAPE DIMENSIONS



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| 8 mm | 0.130 (3.3) | 0.124 (3.15) | 0.130 (3.3) | 0.126 (3.2) | 0.138 ± 0.002 (3.5 ± 0.05) | 0.055 ± 0.004 (1.4 ± 0.11) | 0.157 (4) | 0.315 ± 0.012 (8 ± 0.3) |
|-----------|----------------|--------------------|----------------|--------------------|-------------------------------|-------------------------------|--------------|----------------------------|
| Tape Size | DIM A | DIM A ₀ | DIM B | DIM B ₀ | DIM F | DIM K ₀ | DIM P1 | DIM W |

| | | | | | | | | |
|---------------|-------|------|-------|------|-------|------|-------|------|
| 8 mm SOT-23-5 | MA08A | CO1A | MA08A | CO1A | MA08A | CO1A | MA08A | CO1A |
| 8 mm SOT-23-5 | MA08A | CO1B | MA08A | CO1B | MA08A | CO1B | MA08A | CO1B |
| 8 mm SOT-23-5 | MA08A | CO1C | MA08A | CO1C | MA08A | CO1C | MA08A | CO1C |
| 8 mm SOT-23-5 | MA08A | CO1D | MA08A | CO1D | MA08A | CO1D | MA08A | CO1D |
| 8 mm SOT-23-5 | MA08A | CO1E | MA08A | CO1E | MA08A | CO1E | MA08A | CO1E |
| 8 mm SOT-23-5 | MA08A | CO1F | MA08A | CO1F | MA08A | CO1F | MA08A | CO1F |
| 8 mm SOT-23-5 | MA08A | CO1G | MA08A | CO1G | MA08A | CO1G | MA08A | CO1G |
| 8 mm SOT-23-5 | MA08A | CO1H | MA08A | CO1H | MA08A | CO1H | MA08A | CO1H |

LMC7221

Tiny CMOS Comparator with Rail-To-Rail Input and Open Drain Output

General Description

The LMC7221 is a micropower CMOS comparator available in the space saving SOT23-5 package. This makes this comparator ideal for space and weight critical designs. For easy prototyping, the LMC7221 is available in a conventional 8-pin DIP package. The LMC7221 is supplied in two offset voltage grades, 4 mV and 9 mV.

The open drain output can be pulled up with a resistor to a voltage which can be higher or lower than the supply voltage—this makes the part useful for mixed voltage systems.

For a tiny comparator with a push-pull output, please see the LMC7211 datasheet.

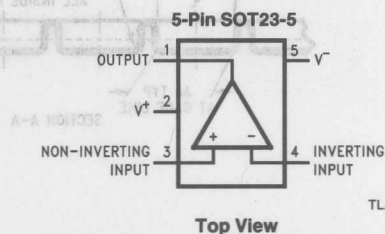
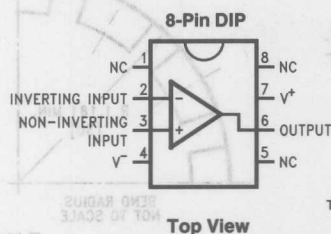
Features

- Tiny SOT 23-5 package saves space
- Package is less than 1.43 mm thick
- Guaranteed specs at 2.7V, 5V, 15V supplies
- Typical supply current 10 μ A at 5V
- Response time of 7 μ s at 5V
- LMC7221—open drain output
- Input common-mode range beyond V^- and V^+
- Low input current

Applications

- Mixed voltage battery powered products
- Notebooks and PDAs
- PCMCIA cards
- Mobile communications
- Alarm and security circuits
- Driving low current LEDs
- Direct sensor interface

Connection Diagrams



Ordering Information

| Package | Ordering Information | NSC Drawing Number | Package Marking | Transport Media |
|----------------|----------------------|--------------------|-----------------|----------------------------|
| 8-Pin DIP | LMC7221AIN | N08E | LMC7221AIN | Rails |
| 8-Pin DIP | LMC7221BIN | N08E | LMC7221BIN | Rails |
| 5-Pin SOT 23-5 | LMC7221AIM5 | MA05A | C01A | 250 Units on Tape and Reel |
| 5-Pin SOT 23-5 | LMC7221BIM5 | MA05A | C01B | 250 Units on Tape and Reel |
| 5-Pin SOT 23-5 | LMC7221AIM5X | MA05A | C01A | 3k Units Tape and Reel |
| 5-Pin SOT 23-5 | LMC7221BIM5X | MA05A | C01B | 3k Units Tape and Reel |

LP311 Voltage Comparator

General Description

The LP311 is a low power version of the industry-standard LM311. It takes advantage of stable high-value ion-implanted resistors to perform the same function as an LM311, with a 30:1 reduction in power drain, but only a 6:1 slowdown of response time. Thus the LP311 is well suited for battery-powered applications, and all other applications where fast response is not needed. It operates over a wide range of supply voltages from 36V down to a single 3V supply, with less than 200 μ A drain, but it is still capable of driving a 25 mA load. The LP311 is quite easy to apply without any oscillation, if ordinary precautions are taken to minimize stray coupling from the output to either input or to the balance pins (as described in the LM311 datasheet Application Hints).

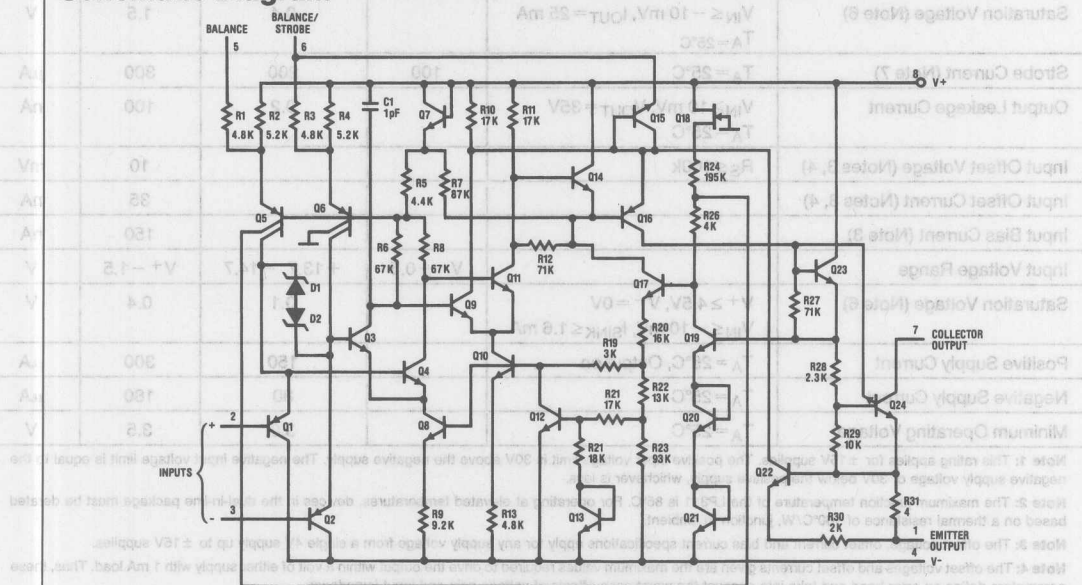
Features

- Low power drain, 900 μ W on 5V supply
- Operates from ± 15 V or a single supply as low as 3V
- Output can drive 25 mA
- Emitter output can swing below negative supply
- Response time: 1.2 μ s
- Same pin-out as LM311
- Low input currents: 2 nA of offset, 15 nA of bias
- Large common-mode input range: -14.6 V to 13.6 V with ± 15 V supply

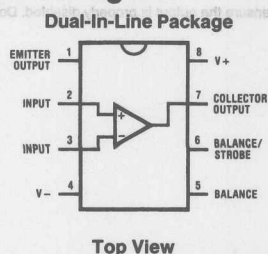
Applications

- Level-detector for battery-powered instruments
- Low-power lamp or relay driver
- Low-power zero-crossing detector

Schematic Diagram



Connection Diagram



Order Number LP311M or LP311N
See NS Package Numbers M08A or N08E

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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|-----------|
| Total Supply Voltage (V_{8-4}) | 36V |
| Collector Output to Negative Supply Voltage (V_{7-4}) | 40V |
| Collector Output to Emitter Output | 40V |
| Emitter Output to Negative Supply Voltage (V_{1-4}) | $\pm 30V$ |
| Differential Input Voltage | $\pm 30V$ |
| Input Voltage (Note 1) | $\pm 15V$ |

| | |
|--|----------------|
| Power Dissipation (Note 2) | 500 mW |
| Output Short Circuit Duration | 10 sec |
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | -65°C to 150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C |

Electrical Characteristics

These specifications apply for $V_S = \pm 15V$ and $0^\circ C \leq T_A \leq 70^\circ C$, unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------------|---|-------------|----------------|-------------|---------|
| Input Offset Voltage (Notes 3, 4) | $T_A = 25^\circ C, R_S \leq 100k$ | | 2.0 | 7.5 | mV |
| Input Offset Current (Notes 3, 4) | $T_A = 25^\circ C$ | | 2.0 | 25 | nA |
| Input Bias Current (Note 3) | $T_A = 25^\circ C$ | | 15 | 100 | nA |
| Voltage Gain | $T_A = 25^\circ C, R_L = 5k$ | 40 | 200 | | V/mV |
| Response Time (Note 5) | $T_A = 25^\circ C$ | | 1.2 | | μs |
| Saturation Voltage (Note 6) | $V_{IN} \leq -10 mV, I_{OUT} = 25 mA$ $T_A = 25^\circ C$ | | 0.4 | 1.5 | V |
| Strobe Current (Note 7) | $T_A = 25^\circ C$ | 100 | 200 | 300 | μA |
| Output Leakage Current | $V_{IN} \geq 10 mV, V_{OUT} = 35V$ $T_A = 25^\circ C$ | | 0.2 | 100 | nA |
| Input Offset Voltage (Notes 3, 4) | $R_S \leq 100k$ | | | 10 | mV |
| Input Offset Current (Notes 3, 4) | | | | 35 | nA |
| Input Bias Current (Note 3) | | | | 150 | nA |
| Input Voltage Range | | $V^- + 0.5$ | $+13.7, -14.7$ | $V^+ - 1.5$ | V |
| Saturation Voltage (Note 6) | $V^+ \geq 4.5V, V^- = 0V$ $V_{IN} \leq -10 mV, I_{SINK} \leq 1.6 mA$ | | 0.1 | 0.4 | V |
| Positive Supply Current | $T_A = 25^\circ C$, Output on | | 150 | 300 | μA |
| Negative Supply Current | $T_A = 25^\circ C$ | | 80 | 180 | μA |
| Minimum Operating Voltage | $T_A = 25^\circ C$ | | 3.0 | 3.5 | V |

Note 1: This rating applies for $\pm 15V$ supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 2: The maximum junction temperature of the LP311 is 85°C. For operating at elevated temperatures, devices in the dual-in-line package must be derated based on a thermal resistance of 160°C/W, junction to ambient.

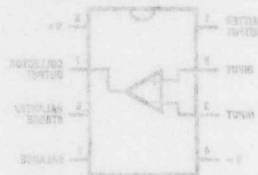
Note 3: The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 4V supply up to $\pm 15V$ supplies.

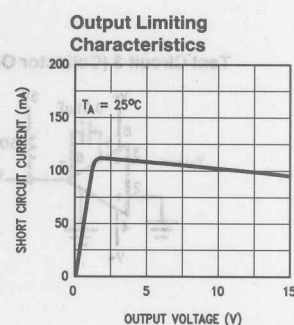
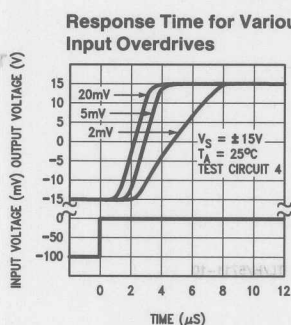
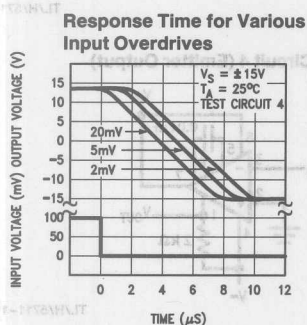
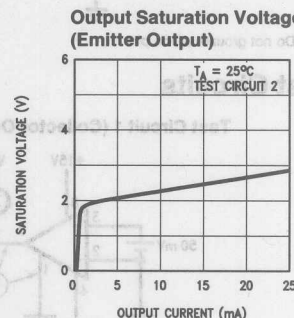
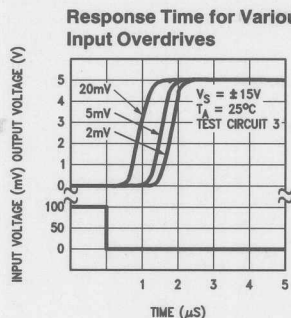
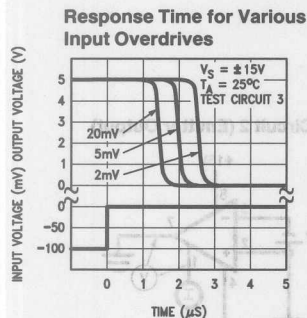
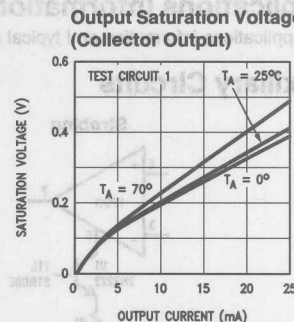
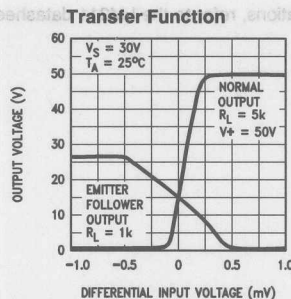
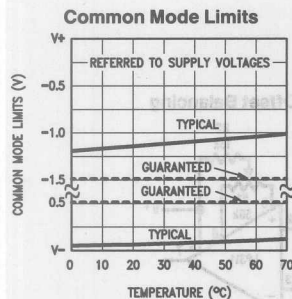
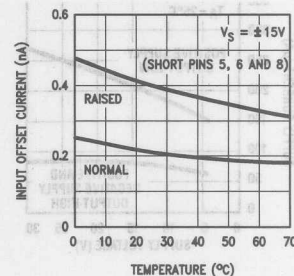
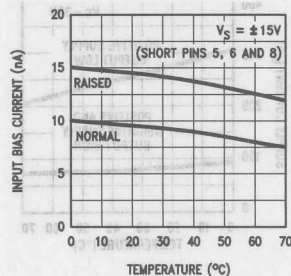
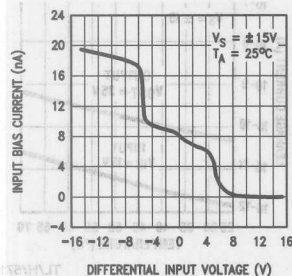
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with 1 mA load. Thus, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.

Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

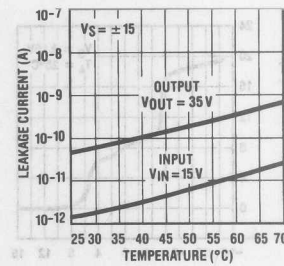
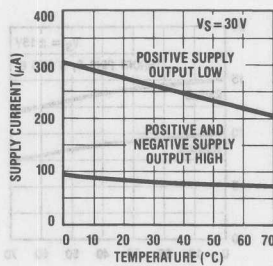
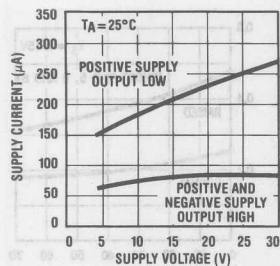
Note 6: Saturation voltage specification applies to collector-emitter voltage (V_{7-1}) for $V_{COLLECTOR} \leq (V^+ - 3V)$.

Note 7: This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground. It should be current driven, 100 μA to 300 μA .





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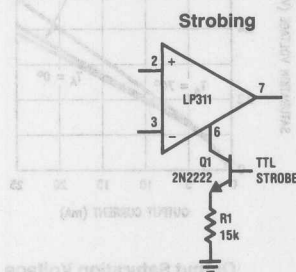


TL/H/5711-6

Applications Information

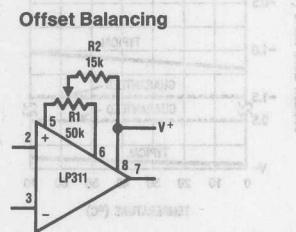
For applications information and typical applications, refer to the LM311 datasheet.

Auxiliary Circuits



TL/H/5711-1

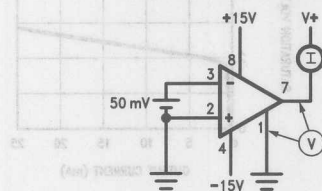
Note: Do not ground strobe pin.



TL/H/5711-2

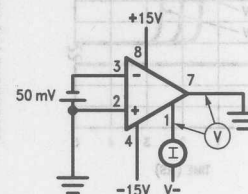
Test Circuits

Test Circuit 1 (Collector Output)



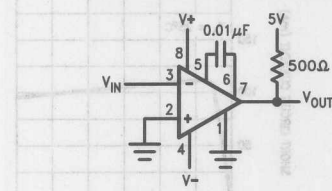
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Test Circuit 2 (Emitter Output)



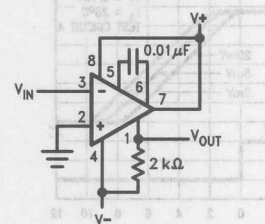
TL/H/5711-9

Test Circuit 3 (Collector Output)



TL/H/5711-10

Test Circuit 4 (Emitter Output)



TL/H/5711-11

LP339 Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 μA of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

Advantages

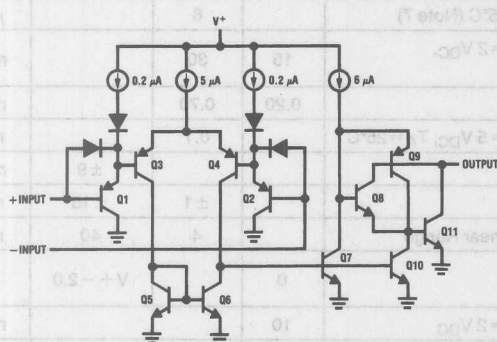
- Ultra-low power supply drain suitable for battery applications

- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

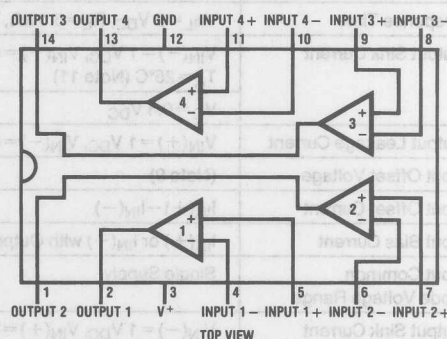
Features

- Ultra-low power supply current drain (60 μA)—independent of the supply voltage (75 $\mu\text{W/comparator}$ at +5 V_{DC})
- Low input biasing current 3 nA
- Low input offset current ± 0.5 nA
- Low input offset voltage ± 2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at $V_O = 2 V_{\text{DC}}$)
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



TL/H/5226-1



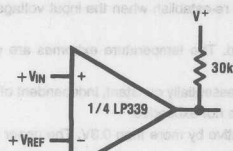
TL/H/5226-2

Order Number LP339M for S.O. Package
See NS Package Number M14A

Order Number LP339N for Dual-In-Line Package
See NS Package Number N14A

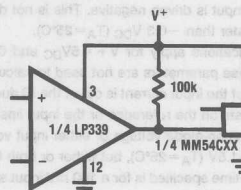
Typical Applications ($V^+ = 5.0 V_{\text{DC}}$)

Basic Comparator



TL/H/5226-3

Driving CMOS



TL/H/5226-4

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---------------------------------------|--|
| Supply Voltage | 36 V _{DC} or ± 18 V _{DC} |
| Differential Input Voltage | ± 36 V _{DC} |
| Input Voltage | -0.3 V _{DC} to 36 V _{DC} |
| Power Dissipation (Note 1) Molded DIP | 570 mW |
| Output Short Circuit to GND (Note 2) | Continuous |

| | |
|---|----------------|
| Input Current V _{IN} < -0.3 V _{DC} (Note 3) | 50 mA |
| Operating Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65° to +150°C |
| Soldering Information: | |
| Dual-In-Line Package (10 sec.) | +260°C |
| S.O. Package: | |
| Vapor Phase (60 sec.) | +215°C |
| Infrared (15 sec.) | +220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (V₊ = 5 V_{DC}, Note 4)

| Parameter | Conditions | Min | Typ | Max | Units |
|---------------------------------|---|------|-----------|----------------------|------------------|
| Input Offset Voltage | T _A = 25°C (Note 9) | | ± 2 | ± 5 | mV _{DC} |
| Input Bias Current | I _{IN} (+) or I _{IN} (-) with the Output in the Linear Range, T _A = 25°C (Note 5) | | 2.5 | 25 | nA _{DC} |
| Input Offset Current | I _{IN} (+) - I _{IN} (-), T _A = 25°C | | ± 0.5 | ± 5 | nA _{DC} |
| Input Common Mode Voltage Range | T _A = 25°C (Note 6) | 0 | | V ₊ - 1.5 | V _{DC} |
| Supply Current | R _L = Infinite on all Comparators, T _A = 25°C | | 60 | 100 | μA _{DC} |
| Voltage Gain | V _O = 1 V _{DC} to 11 V _{DC} , R _L = 15 kΩ, V ₊ = 15 V _{DC} , T _A = 25°C | | 500 | | V/mV |
| Large Signal Response Time | V _{IN} = TTL Logic Swing, V _{REF} = 1.4 V _{DC} , V _{RL} = 5 V _{DC} , R _L = 5.1 kΩ, T _A = 25°C | | 1.3 | | μSec |
| Response Time | V _{RL} = 5 V _{DC} , R _L = 5.1 kΩ, T _A = 25°C (Note 7) | | 8 | | μSec |
| Output Sink Current | V _{IN} (-) = 1 V _{DC} , V _{IN} (+) = 0, V _O = 2 V _{DC} , T _A = 25°C (Note 11) | 15 | 30 | | mA _{DC} |
| | V _O = 0.4 V _{DC} | 0.20 | 0.70 | | mA _{DC} |
| Output Leakage Current | V _{IN} (+) = 1 V _{DC} , V _{IN} (-) = 0, V _O = 5 V _{DC} , T _A = 25°C | | 0.1 | | nA _{DC} |
| Input Offset Voltage | (Note 9) | | | ± 9 | mV _{DC} |
| Input Offset Current | I _{IN} (+) - I _{IN} (-) | | ± 1 | ± 15 | nA _{DC} |
| Input Bias Current | I _{IN} (+) or I _{IN} (-) with Output in Linear Range | | 4 | 40 | nA _{DC} |
| Input Common Mode Voltage Range | Single Supply | 0 | | V ₊ - 2.0 | V _{DC} |
| Output Sink Current | V _{IN} (-) = 1 V _{DC} , V _{IN} (+) = 0, V _O = 2 V _{DC} | 10 | | | mA _{DC} |
| Output Leakage Current | V _{IN} (+) = 1 V _{DC} , V _{IN} (-) = 0, V _O = 30 V _{DC} | | | 1.0 | μA _{DC} |
| Differential Input Voltage | All V _{IN} 's ≥ 0 V _{DC} (or V ₋ on split supplies) (Note 8) | | | 36 | V _{DC} |

Note 1: For elevated temperature operation, T_J max is 125°C for the LP339. θ_{JA} (junction to ambient) is 175°C/W for the LP339N and 120°C/W for the LP339M when either device is soldered in a printed circuit board in a still air environment. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small (P_D ≤ 100 mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V₊ can cause excessive heating and eventual destruction. The maximum output current is approximately 50 mA.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input clamp diodes. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the V₊ voltage level (or to ground for a large input overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than -0.3 V_{DC} (T_A = 25°C).

Note 4: These specifications apply for V₊ = 5 V_{DC} and 0°C ≤ T_A ≤ 70°C, unless otherwise stated. The temperature extremes are guaranteed but not 100% production tested. These parameters are not used to calculate outgoing AQL.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or the input lines as long as the common-mode range is not exceeded.

Note 6: The input common-mode voltage or either input voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V₊ - 1.5V (T_A = 25°C), but either or both inputs can go to 30 V_{DC} without damage.

Note 7: The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 1.3 μs can be obtained. See Typical Performance Characteristics section.

Electrical Characteristics ($V^+ = 5\text{ V}_{\text{DC}}$, Note 4) (Continued)

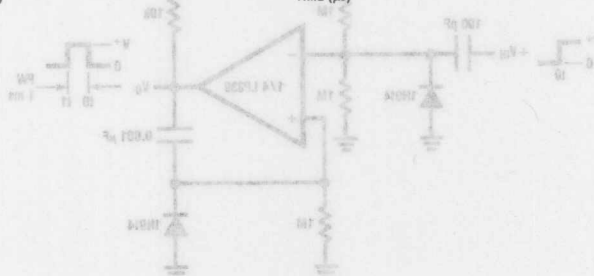
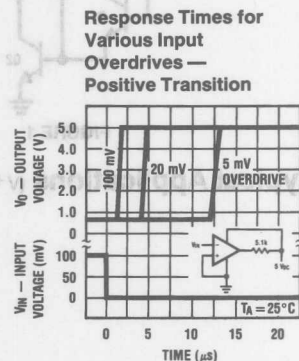
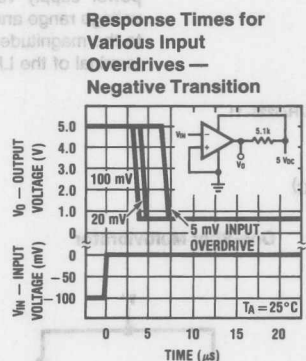
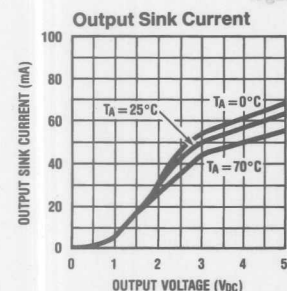
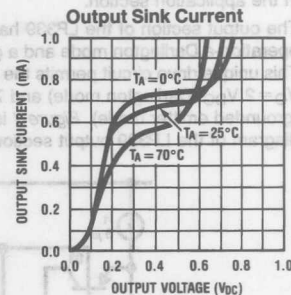
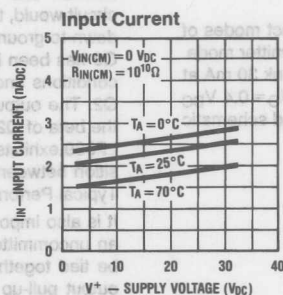
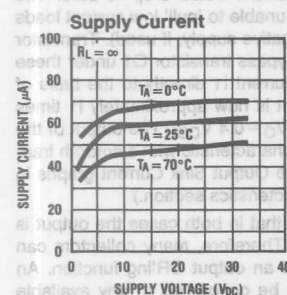
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\text{ V}_{\text{DC}}$ (or 0.3 V_{DC} below the magnitude of the negative power supply, if used) at $T_A = 25^\circ\text{C}$.

Note 9: At output switch point, $V_O = 1.4\text{ V}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC} ; and over the full input common-mode range (0 V_{DC} to $V^+ - 1.5\text{ V}_{\text{DC}}$).

Note 10: For input signals that exceed V^+ , only the overdriven comparator is affected. With a 5 V supply, V_{IN} should be limited to 25 V maximum, and a limiting resistor should be used on all inputs that might exceed the positive supply.

Note 11: The output sink current is a function of the output voltage. The LP339 has a bi-modal output section which allows it to sink large currents via a Darlington connection at output voltages greater than approximately 1.5 V_{DC} and sink lower currents below this point. (See typical characteristics section and applications section).

Typical Performance Characteristics



TL/H/5226-10

Application Hints

All pins of any unused comparators should be grounded.

The bias network of the LP339 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from $2 V_{DC}$ to $30 V_{DC}$.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than $-0.3 V_{DC}$ (at 25°C). An input clamp diode can be used as shown in the application section.

The output section of the LP339 has two distinct modes of operation—a Darlington mode and a grounded emitter mode. This unique drive circuit permits the LP339 to sink 30 mA at $V_O = 2 V_{DC}$ (Darlington mode) and $700 \mu\text{A}$ at $V_O = 0.4 V_{DC}$ (grounded emitter mode). Figure 7 is a simplified schematic diagram of the LP339 output section.

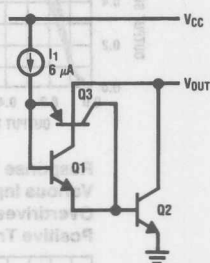
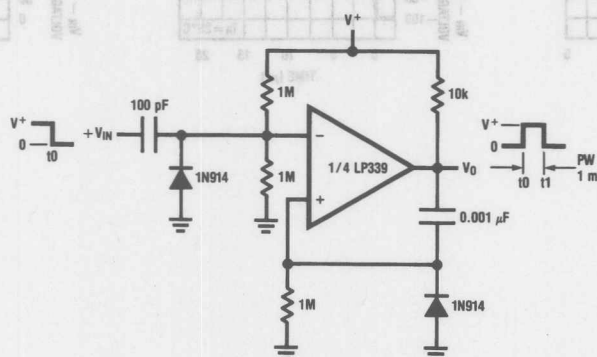


FIGURE 1

Typical Applications ($V^+ = 15 V_{DC}$)

One-Shot Multivibrator



TL/H/5226-13

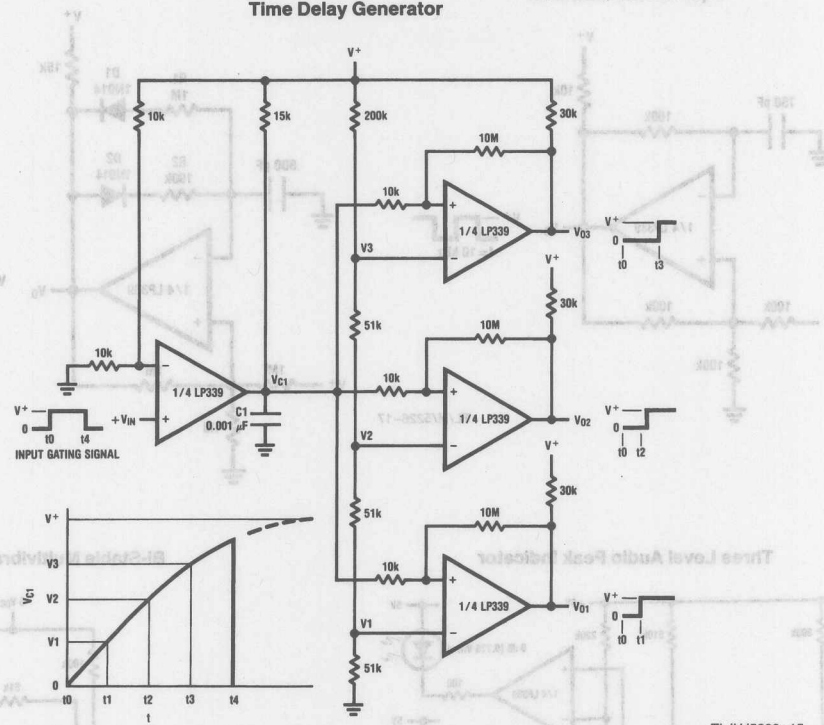
Notice that the output section is configured in a Darlington connection (ignoring Q3). Therefore, if the output voltage is held high enough ($V_O \geq 1 V_{DC}$), Q1 is not saturated and the output current is limited only by the product of the betas of Q1, Q2 and I1 (and the $60 \Omega R_{SAT}$ of Q2). The LP339 is thus capable of driving LED's, relays, etc. in this mode while maintaining an ultra-low power supply current of typically $60 \mu\text{A}$.

If transistor Q3 were omitted, and the output voltage allowed to drop below about $0.8 V_{DC}$, transistor Q1 would saturate and the output current would drop to zero. The circuit would, therefore, be unable to 'pull' low current loads down to ground (or the negative supply, if used). Transistor Q3 has been included to bypass transistor Q1 under these conditions and apply the current I1 directly to the base of Q2. The output sink current is now approximately I1 times the beta of Q2 ($700 \mu\text{A}$ at $V_O = 0.4 V_{DC}$). The output of the LP339 exhibits a bi-modal characteristic with a smooth transition between modes. (See Output Sink Current graphs in Typical Performance Characteristics section.)

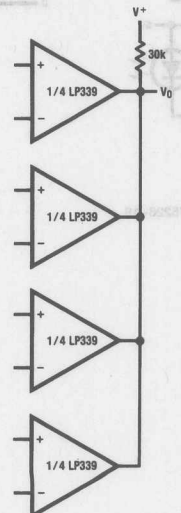
It is also important to note that in both cases the output is an uncommitted collector. Therefore, many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted power supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LP339 package.

Typical Applications ($V^+ = 15 V_{DC}$)

Time Delay Generator



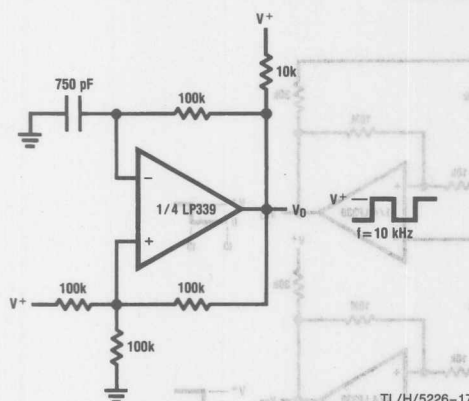
Oring the Outputs



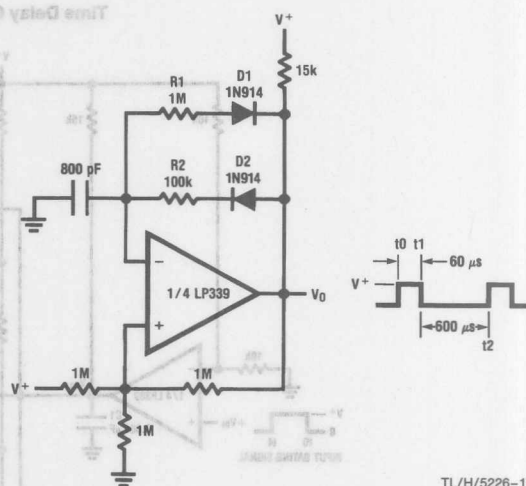
Typical Applications (Continued) ($V^+ = 15\text{ V}_{\text{DC}}$)

Typical Applications ($V^+ = +15\text{ V}_{\text{DC}}$)

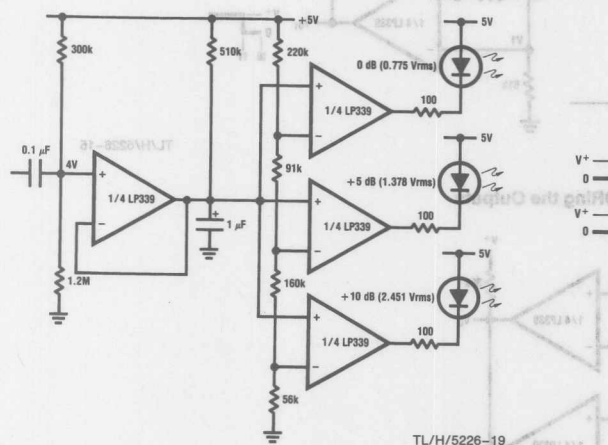
Squarewave Oscillator



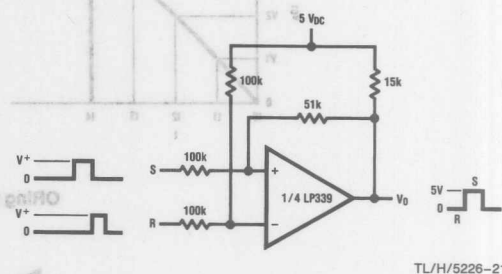
Pulse Generator



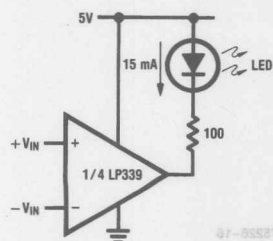
Three Level Audio Peak Indicator



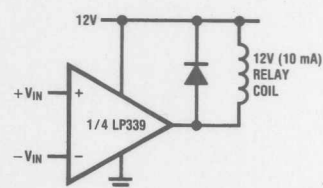
Bi-Stable Multivibrator



LED Driver

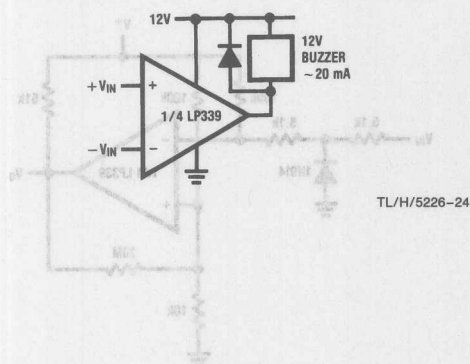


Relay Driver

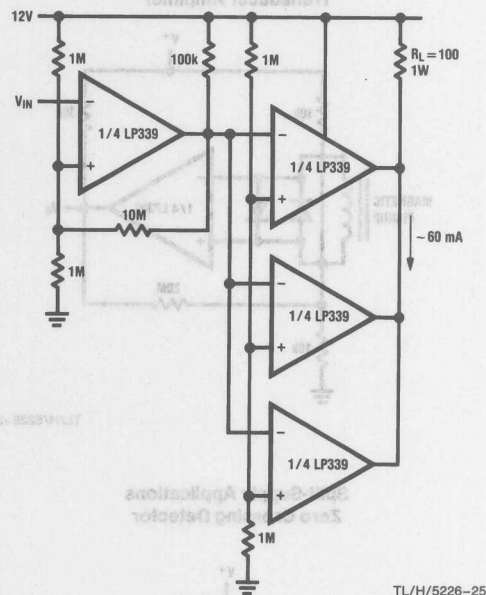


Typical Applications (Continued) (Single Supply)

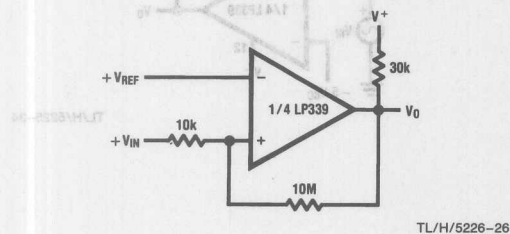
Buzzer Driver



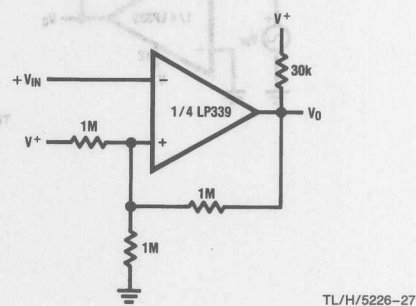
Comparator With 60 mA Sink Capability



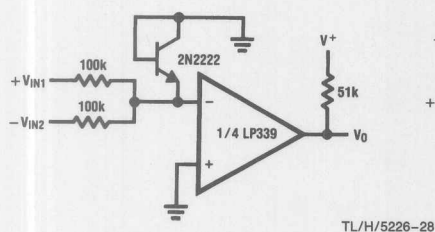
Non-Inverting Comparator with Hysteresis



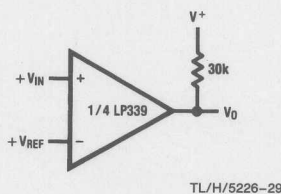
Inverting Comparator with Hysteresis



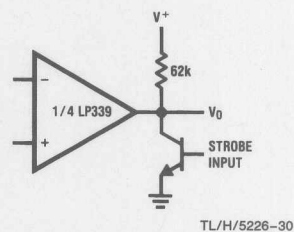
Comparing Input Voltages of Opposite Polarity



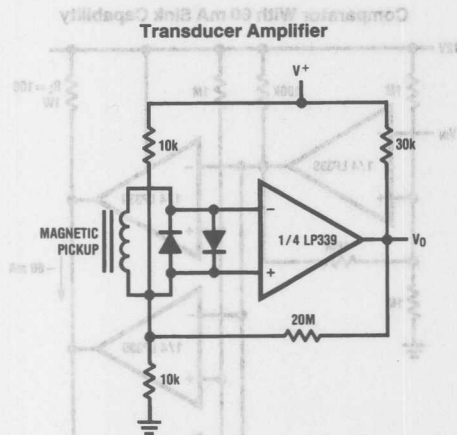
Basic Comparator



Output Strobing

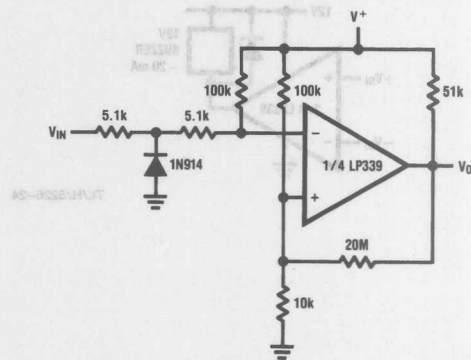


Typical Applications (Continued) (Single Supply)



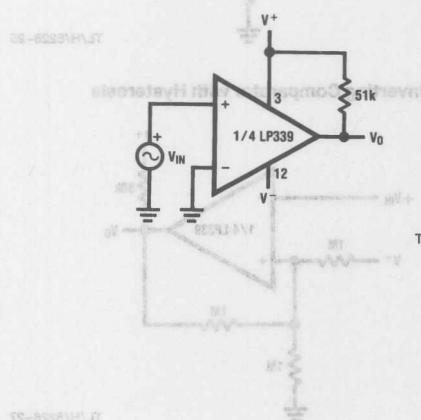
TL/H/5226-31

Zero Crossing Detector (Single Power Supply)



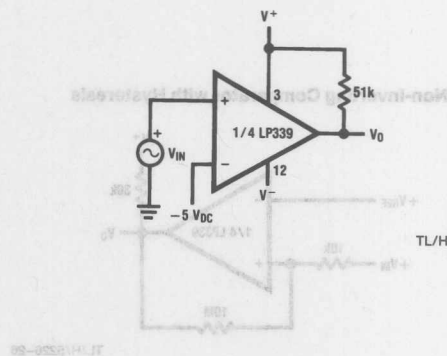
TL/H/5226-32

Split-Supply Applications Zero Crossing Detector



TL/H/5226-33

Comparator With a Negative Reference



TL/H/5226-34



Section 4 Contents

| | |
|-----|---|
| 4-8 | LM8104 Quad Gray Scale Current Feedback Amplifier |
| 4-1 | LM8305 STN LCD Display Bias Voltage Source |
| 4-8 | LMC8008 8 Channel Buffer |

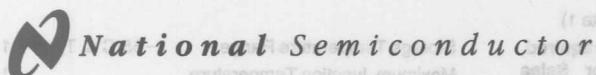
Section 4 Active Matrix/LCD Display Drivers



Section 4 Contents

| | |
|---|-----|
| LM6104 Quad Gray Scale Current Feedback Amplifier | 4-3 |
| LM8305 STN LCD Display Bias Voltage Source | 4-7 |
| LMC6008 8 Channel Buffer | 4-8 |

Section 4
Active Matrix/LCD
Display Drivers



LM6104 Quad Gray Scale Current Feedback Amplifier

General Description

The LM6104 quad amplifier meets the requirements of battery operated liquid crystal displays by providing high speed while maintaining low power consumption.

Combining this high speed with high integration, the LM6104 conserves valuable board space in portable systems with a cost effective, surface mount quad package.

Built on National's advanced high speed VIPTM (Vertically Integrated PNP) process, the LM6104 current feedback architecture is easily compensated for speed and loading conditions. These features make the LM6104 ideal for buffering grey levels in liquid crystal displays.

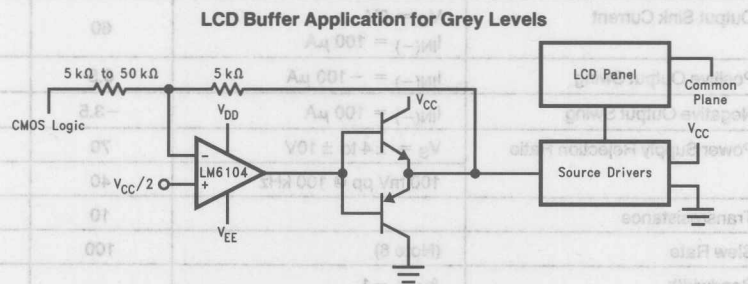
Features (Typical unless otherwise noted)

- Low power $I_S = 875 \mu A/\text{amplifier}$
- Slew rate $100V/\mu s$
- 3dB bandwidth ($R_F = 1 k\Omega$) 30 MHz
- High output drive $\pm 5V$ into 100Ω
- Wide operating range $V_S = 5V$ to $\pm 12V$
- High integration Quad surface mount

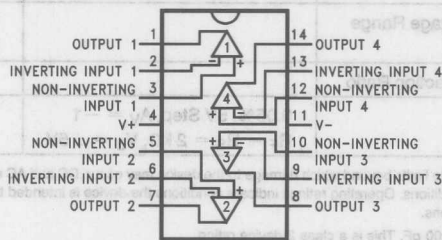
Applications

- Grey level buffer for liquid crystal displays
- Column buffer for portable LCDs
- Video distribution amplifiers, video line drivers
- Hand-held, high speed signal conditioning

Typical Application



Connection Diagram



Order Number LM6104M
See NS Package Number M14A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|----------------------------|------------------|
| Supply Voltage | 24V |
| Differential Input Voltage | ±6V |
| Input Voltage | ± Supply Voltage |
| Inverting Input Current | 15 mA |
| Soldering Information | |
| Vapor Phase (60s) | 215°C |
| Infrared (15s) | 220°C |

Storage Temperature Range $-65^{\circ}\text{C} \leq T_J \leq +150^{\circ}\text{C}$

Maximum Junction Temperature 150°C

ESD Rating (Note 2) 2000V

Operating Ratings

Supply Voltage Range 4.75V to 24V

Junction Temperature Range (Note 3)
LM6104M $-20^{\circ}\text{C} \leq T_J \leq +80^{\circ}\text{C}$

Electrical Characteristics

The following specifications apply for $V_+ = 8\text{V}$, $V_- = -5\text{V}$, $R_L = R_F = 2\text{ k}\Omega$ and $0^{\circ} \leq T_J \leq 60^{\circ}\text{C}$ unless otherwise noted.

| Symbol | Parameter | Conditions | LM6104M | | Units |
|----------|----------------------------------|--|--|--------------------|----------------------|
| | | | Typical (Note 4) | Limits (Note 5) | |
| V_{OS} | Input Offset Voltage | | 10 | 30 | mV max |
| I_B | Inverting Input Bias Current | | 5.0 | 20 | μA max |
| | Non-Inverting Input Bias Current | | 0.5 | 2 | μA max |
| I_S | Supply Current | $V_O = 0\text{V}$ | 3.5 | 4.0 | mA max |
| I_{SC} | Output Source Current | $V_O = 0\text{V}$ $I_{IN(-)} = -100\text{ }\mu\text{A}$ | 60 | 45 | mA min |
| | Output Sink Current | $V_O = 0\text{V}$ $I_{IN(-)} = 100\text{ }\mu\text{A}$ | 60 | 45 | mA min |
| V_O | Positive Output Swing | $I_{IN(-)} = -100\text{ }\mu\text{A}$ | 6.5 | 6.1 | V min |
| | Negative Output Swing | $I_{IN(-)} = 100\text{ }\mu\text{A}$ | -3.5 | -3.1 | V max |
| PSRR | Power Supply Rejection Ratio | $V_S = \pm 4$ to $\pm 10\text{V}$ | 70 | 60 | dB min |
| | | 100 mV pp @ 100 kHz | 40 | 30 | dB min |
| R_T | Transresistance | | 10 | 5 | M Ω min |
| SR | Slew Rate | (Note 6) | 100 | 55 | V/ μs min |
| BW | Bandwidth | $A_V = -1$ $R_{IN} = R_F = 2\text{ k}\Omega$ | 7.5 | 5.0 | MHz |
| | Amp-to-Amp Isolation | $R_L = 2\text{ k}\Omega$ $F = 1\text{ MHz}$ | 60 | | dB |
| CMVR | Common Mode Voltage Range | | $V_+ - 1.4\text{V}$ $V_- + 1.4\text{V}$ | | V |
| CMRR | Common Mode Rejection Ratio | | 60 | | dB |
| t_S | Settling Time | 0.05%, 5V Step, $A_V = -1$ $R_F = R_S = 2\text{ k}\Omega$, $V_S = \pm 5\text{V}$ | 240 | | ns |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. Operating ratings indicate conditions the device is intended to be functional, but device parameter specifications may not be guaranteed under the conditions.

Note 2: Human body model 1.5 k Ω and 100 pF. This is a class 2 device rating.

Note 3: Thermal resistance of the SO package is 98°C/W. When operating at $T_A = 80^{\circ}\text{C}$, maximum power dissipation is 700 mW.

Note 4: Typical values represent the most likely parametric norm.

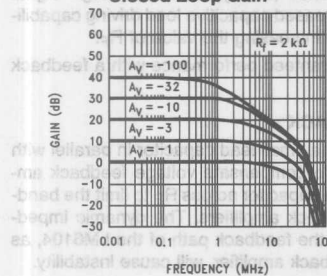
Note 5: All limits guaranteed at operating temperature extremes.

Note 6: $A_V = -1$ with $R_{IN} = R_F = 2\text{ k}\Omega$. Slew rate is calculated from the 25% to the 75% point on both rising and falling edges. Output swing is -0.6V to $+5.6\text{V}$ and 5.6V to 0.6V .

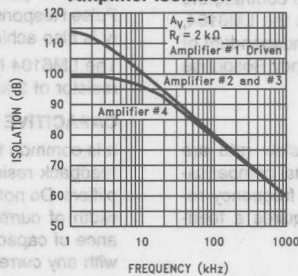
Typical Performance Characteristics

Bandwidth and slew rate are inversely proportional to the value of R_F (see typical curve Frequency Response vs R_F). The small-signal bandwidth of conventional voltage feedback amplifiers is relatively independent of the closed-loop gain. The LM6104 has a constant bandwidth of 10 MHz for all closed-loop gains.

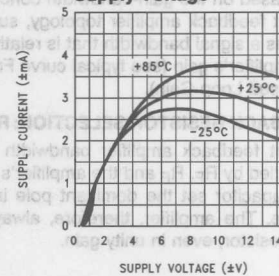
Frequency Response vs Closed Loop Gain



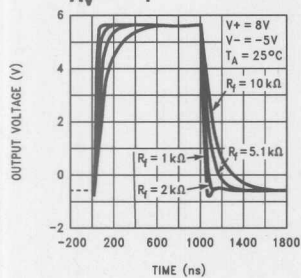
Amplifier to Amplifier Isolation



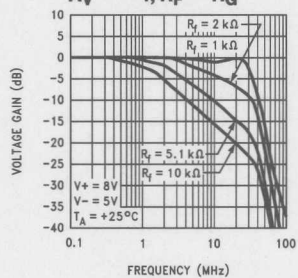
Supply Current vs Supply Voltage



Large Signal Pulse Response

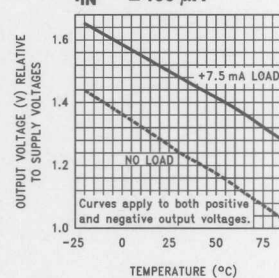


Frequency Response vs R_F

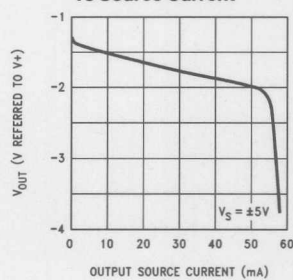


V_{OUT} Referred to Supplies

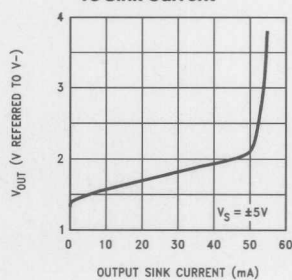
$V_S = \pm 5V$
 $I_{IN} = \pm 100 \mu A$



LM6104 Output Voltage vs Source Current



LM6104 Output Voltage vs Sink Current



TL/H/11979-3

Applications Information

CURRENT FEEDBACK TOPOLOGY

The small-signal bandwidth of conventional voltage feedback amplifiers is inversely proportional to the closed-loop gain based on the gain-bandwidth concept. In contrast, the current feedback amplifier topology, such as the LM6104, enables a signal bandwidth that is relatively independent of the amplifier's gain (see typical curve Frequency Response vs Closed Loop Gain).

FEEDBACK RESISTOR SELECTION: R_F

Current feedback amplifier bandwidth and slew rate are controlled by R_F . R_F and the amplifier's internal compensation capacitor set the dominant pole in the frequency response. The amplifier, therefore, always requires a feedback resistor, even in unity gain.

Typical Performance Characteristics

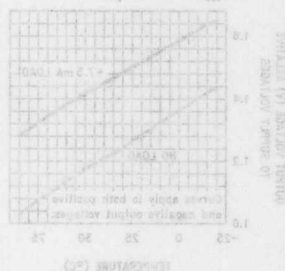
Bandwidth and slew rate are inversely proportional to the value of R_F (see typical curve Frequency Response vs R_F). This makes the amplifier especially easy to compensate for a desired pulse response (see typical curve Large Signal Pulse Response). Increased capacitive load driving capability is also achieved by increasing the value of R_F .

The LM6104 has guaranteed performance with a feedback resistor of 2 k Ω .

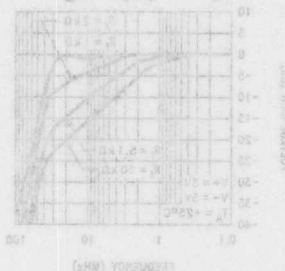
CAPACITIVE FEEDBACK

It is common to place a small lead capacitor in parallel with feedback resistance to compensate voltage feedback amplifiers. Do not place a capacitor across R_F to limit the bandwidth of current feedback amplifiers. The dynamic impedance of capacitors in the feedback path of the LM6104, as with any current feedback amplifier, will cause instability.

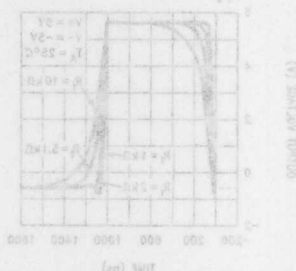
Output Voltage vs. Input Voltage
 $V_S = \pm 5V$
 $I_{IN} = \pm 100 \mu A$



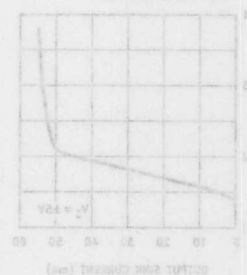
Frequency Response vs. R_F
 $A_V = -1$
 $R_F = 2k\Omega$
 $R_F = 10k\Omega$
 $R_F = 20k\Omega$
 $R_F = 50k\Omega$
 $R_F = 100k\Omega$
 $R_F = 200k\Omega$
 $R_F = 500k\Omega$
 $R_F = 1M\Omega$
 $V_S = 5V$
 $T_A = 25^\circ C$



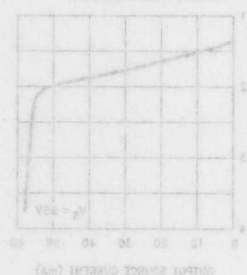
Large Signal Pulse Response
 $A_V = -1$
 $V_S = 5V$
 $T_A = 25^\circ C$
 $R_F = 10k\Omega$
 $R_F = 20k\Omega$
 $R_F = 50k\Omega$
 $R_F = 100k\Omega$
 $R_F = 200k\Omega$
 $R_F = 500k\Omega$
 $R_F = 1M\Omega$



LM6104 Output Voltage
 vs Sink Current
 $V_S = 5V$



LM6104 Output Voltage
 vs Source Current
 $V_S = 5V$



Source 8 Channel Buffer LM6008

General Description

The LM8305M contains five buffered voltage sources to provide the voltage ratios required to drive a standard STN LCD display panel using a time-multiplexed voltage waveform to activate, or deactivate, a pixel once every picture frame. The internal resistor array features a binary weighted array to allow the user to select the proper ratio for the display being driven. The user can use an external resistor to set the ratio, if desired.

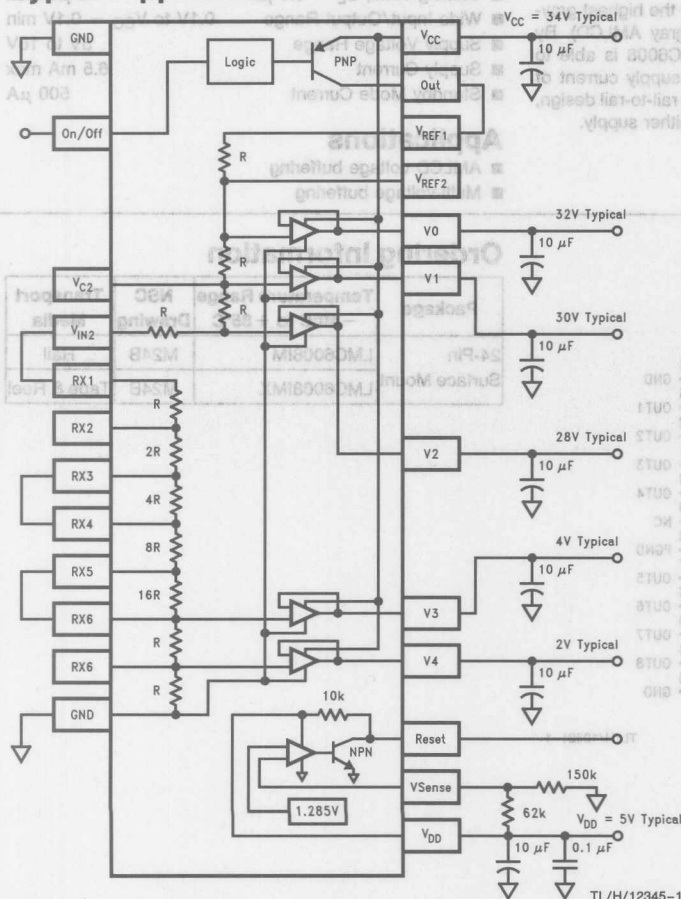
The LM8305 has a maximum operating supply voltage of 50V to support higher multiplexing rates.

The LM8305 also features an internal high side PNP switch, and an independent voltage comparator with an internal bandgap reference.

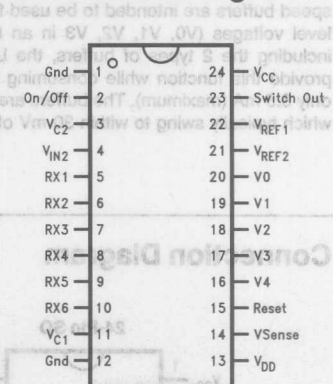
Features

- High operating voltages, 50V maximum
- Internal resistor array with binary weighting
- Ratios from 1/6 to 1/37
- Optional external resistors
- High-side PNP switch from V_{CC}
- Separate voltage comparator circuit with band-gap voltage reference
- Surface mount 24-pin package

Typical Application

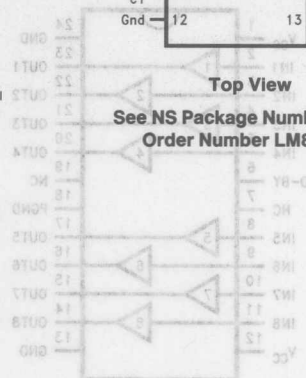


Connection Diagram



TL/H/12345-2

Top View
See NS Package Number M24B
Order Number LM8305M



LMC6008

8 Channel Buffer

General Description

The LMC6008 octal buffer is designed for use in an active matrix liquid-crystal display (AMLCD), specifically to buffer the gray-level voltages going to the inputs of the column driver integrated circuits. In an 8-gray-level (512 color) or 16-gray-level (4096 color) AMLCD, the function of the column drivers is to switch the gray-level voltage inputs to the AMLCD columns. Thus, the voltage buffers must be able to drive the column capacitance of the entire display panel. The LMC6008 AC characteristics, including settling time, are specified for a capacitive load of 0.1 μF for this reason.

The LMC6008 contains 4 high-speed buffers and 4 low-power buffers. The high-speed buffers can provide an output current of at least 250 mA (minimum), and the low-power buffers can provide at least 150 mA (minimum). The high-speed buffers are intended to be used for the highest gray-level voltages (V0, V1, V2, V3 in an 8-gray AMLCD). By including the 2 types of buffers, the LMC6008 is able to provide this function while consuming a supply current of only 6.5 mA (maximum). The buffers are a rail-to-rail design, which typically swing to within 30 mV of either supply.

The LMC6008 also contains a standby function which puts the buffer into a high-impedance mode. The supply current in the standby mode is a low 500 μA max. Also, a thermal limit circuit is included to protect the device from overload conditions.

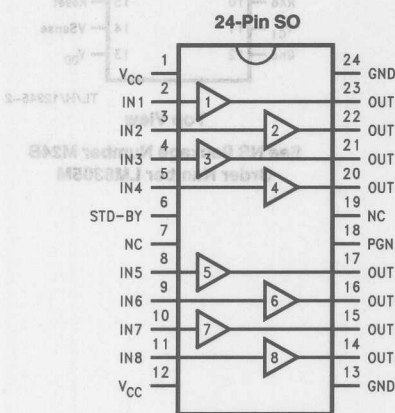
Features

- High Output Current:
 - High Speed Buffers 250 mA min
 - Low Power Buffers 150 mA min
- Slew Rate:
 - High Speed Buffers 1.7 V/ μs
 - Low Power Buffers 0.85V/ μs
- Settling Time, $C_L = 0.1 \mu\text{F}$ 16 μs max
- Wide Input/Output Range 0.1V to $V_{CC} - 0.1\text{V}$ min
- Supply Voltage Range 5V to 16V
- Supply Current 6.5 mA max
- Standby Mode Current 500 μA

Applications

- AMLCD voltage buffering
- Multi-voltage buffering

Connection Diagram



Top View

Note: Buffers 1, 3, 5 and 7 are High Speed and Buffers 2, 4, 6 and 8 are Low Speed.

Ordering Information

| Package | Temperature Range -40°C to +85°C | NSC Drawing | Transport Media |
|----------------------|-------------------------------------|-------------|-----------------|
| 24-Pin Surface Mount | LMC6008IM | M24B | Rail |
| | LMC6008IMX | M24B | Tape & Reel |

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-----------------------------|
| ESD Tolerance (Note 2) | 2000V |
| Voltage at Input Pin | $V^+ + 0.4V$, $V^- - 0.4V$ |
| Voltage at Output Pin | $V^+ + 0.4V$, $V^- - 0.4V$ |
| Supply Voltage ($V^+ - V^-$) | 16V |
| Lead Temperature (soldering, 10 sec.) | 260°C |
| Storage Temperature Range | -55°C to +150°C |
| Junction Temperature (Note 4) | 150°C |
| Power Dissipation (Note 4) | Internally Limited |

Operating Ratings (Note 1)

| | |
|--------------------------------------|--------------------------|
| Supply Voltage | $4.5V \leq V^+ \leq 16V$ |
| Temperature Range | -20°C to +100°C |
| Thermal Resistance (θ_{JA}) | |
| M Package, 24-Pin Surface Mount | 50°C/W |

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V_{CC} = 14.5V$ and $R_L = 0$.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6008 Limit (Note 6) | Units |
|----------------|---------------------------------------|--|-----------------|------------------------------|-------------------|
| V_{OS} | Input Offset Voltage | $R_S = 10\text{ k}\Omega$ | | 25 | mV max |
| A_V | $V_O = 10\text{ V}_{PP}$ | | | 0.985 | V/V |
| I_B | Input Bias Current | | | 300 | nA max |
| I_{LP} | Peak Load Current | Hi Speed Buffers $V_O = 13\text{ V}_{PP}$ | | -250 +250 | mA max mA min |
| I_{LP} | Peak Load Current | Lo Speed Buffers $V_O = 13\text{ V}_{PP}$ | | -150 +150 | mA max mA min |
| V_{ERR} | Output Voltage Difference (Note 9) | | 35 | | mV max |
| V_{IH} | Standby Logic High Voltage | | | 3.30 | V min |
| V_{IL} | $I_{STANDBY}$ Logic Low Voltage | | | 1.80 | V max |
| I_{IH} | Standby High Input Current | | | 1.0 | μA max |
| I_{IL} | Standby Low Input Current | | | 1.0 | μA max |
| I_O (STD-BY) | Output Leakage Current | $V_{STD-BY} = \text{High}$ | | 5 | μA max |
| I_{CC} | Supply Current | $V_{IL} = \text{Low}$, $V_{IN} = 7.25V$ | | 6.5 | mA max |
| I_{STD-BY} | Standby Current | $V_{STD-BY} = \text{High}$ | | 500 | μA max |
| PSRR | Power Supply Rejection Ratio | $5V < V_{CC} < 14.5V$ | | 55 | dB min |
| V_O | Voltage Output Swing | | | 0.1 $V_{CC} - 0.1$ | V min V max |

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$, $V_{CC} = 14.5\text{V}$ and $R_L = 0\Omega$.

| Symbol | Parameter | Conditions | Typ (Note 5) | LMC6008 Limit (Note 6) | Units |
|-----------|---------------------------|---|-----------------|------------------------------|----------------------|
| SR | Slew Rate | Buffers 1, 3, 5, 7 (Note 3) | | 1.70 | V/ μs min |
| | | Buffers 2, 4, 6, 8 (Note 3) | | 0.85 | V/ μs min |
| t_S | Settling Time | (Notes 3, 7) | | 16 | μs max |
| t_{ON} | Standby Response Time ON | | | 10 | μs max |
| t_{OFF} | Standby Response Time OFF | | | 10 | μs max |
| PBW | Power Bandwidth | $V_O = 10 V_{PP}$ for Hi-Speed $V_O = 5 V_{PP}$ for Lo-Speed (Note 3) | | 45 | KHz min |
| C_L | Load Capacitance | | | 0.1 | μF max |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and the test conditions, see the Electrical Characteristics.

Note 2: Human body model, 1.5 k Ω in series with 100 pF.

Note 3: The Load is a series connection of a 0.1 μF capacitor and a 1 Ω resistor.

Note 4: The maximum power dissipation is a function of $T_{J(\text{max})}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(\text{max})} - T_A)/\theta_{JA}$, where the junction-to-ambient thermal resistance $\theta_{JA} = 50^\circ\text{C/W}$. If the maximum allowable power dissipation is exceeded, the thermal limit circuit will limit the die temperature to approximately 160°C . All numbers apply for packages soldered directly into a PC board.

Note 5: Typical Values represent the most likely parametric norm.

Note 6: All limits are guaranteed by testing or statistical analysis.

Note 7: The settling time is measured from the input transition to a point 50 mV of the final value, for both rising and falling transitions. The input swing is 0.5V to 13.5V for buffers 1, 3, 5, 7 and 3.75V to 10.25V for buffers 2, 4, 6, 8. Input rise time should be less than 1 μs .

Note 8: High-Speed Buffers are 1, 3, 5, 7 and Low-Speed Buffers are 2, 4, 6, 8.

Note 9: Output Voltage Difference is the difference between the highest and lowest buffer output voltage when all buffer inputs are at identical voltages.

| | | | | | |
|---------------|-------------------|------|---|--|------------------------------------|
| V_{CC} | V max | 14.5 | | | Voltage Output Swing |
| V_{CC} | V min | 0.1 | | | Voltage Output Swing |
| PSRR | dB min | 55 | $V_{CC} > 14.5\text{V}$ | | Power Supply Rejection Ratio |
| I_{SD} | μA max | 500 | $V_{CC} = \text{Low}$, $V_{IN} = 7.25\text{V}$ | | Standby Current |
| I_{SC} | μA max | 5 | $V_{CC} = \text{Low}$, $V_{IN} = 7.25\text{V}$ | | Supply Current |
| I_{OL} | μA max | 5 | $V_{CC} = \text{High}$ | | Output Leakage Current |
| I_{IH} | μA max | 1.0 | | | Standby Low Input Current |
| I_{IL} | μA max | 1.0 | | | Standby High Input Current |
| V_{IL} | V max | 7.50 | | | Low Voltage Standby Logic |
| V_{IH} | V min | 3.30 | | | High Voltage Standby Logic |
| V_{ERR} | mV max | 35 | | | Output Voltage Difference (Note 9) |
| I_{IN} | nA max | 150 | | | |



Section 5 Contents

| | | |
|------|-------|--|
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| 5-7 | | DH0034 High Speed Dual Level Transistor |
| 5-11 | | DH0035\DH0035C Pin Diode Driver |
| 5-14 | | LH0094 Multifunction Converter |
| 5-23 | | LM134\LM394 Superswitch Pair |
| 5-31 | | LM135\LM395 Ultra Reliable Power Transistors |
| 5-42 | | LM3045\LM3048\LM3086 Transistor Arrays |
| 5-47 | | LM3148 High Voltage Transistor Array |
| 5-52 | | LP395 Ultra Reliable Power Transistor |

Section 5 Special Functions



Section 5 Contents

| | |
|--|------|
| DH0006/DH0006C Current Drivers | 5-3 |
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| DH0035/DH0035C Pin Diode Driver | 5-11 |
| LH0094 Multifunction Converter | 5-14 |
| LM194/LM394 Supermatch Pair | 5-23 |
| LM195/LM395 Ultra Reliable Power Transistors | 5-31 |
| LM3045/LM3046/LM3086 Transistor Arrays | 5-42 |
| LM3146 High Voltage Transistor Array | 5-47 |
| LP395 Ultra Reliable Power Transistor | 5-52 |

DH0006/DH0006C* Current Drivers

General Description

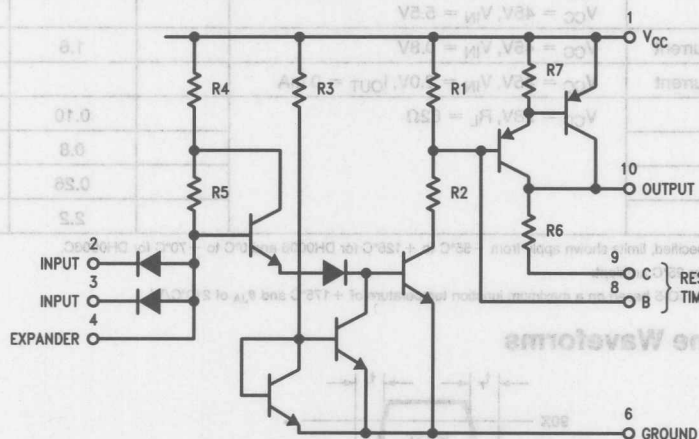
The DH0006/DH0006C is an integrated high voltage, high current driver designed to accept standard DTL or TTL logic levels and drive a load of up to 400 mA at 28V. AND inputs are provided along with an Expander connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are driven.

Since one side of the load is normally grounded, there is less likelihood of false turn-on due to an inadvertent short in the drive line.

Features

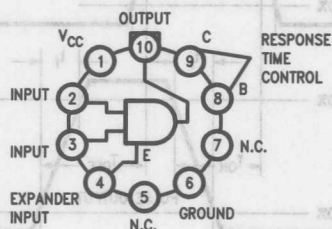
- Operation from a Single +10V to +45V Power Supply
- Low Standby Power Dissipation of only 35 mW for 28V Power Supply
- 1.5A, 50 ms, Pulse Current Capability

Schematic and Connection Diagrams



TL/K/10120-1

Metal Can Package



Top View

Order Number DH0006H or DH0006CH
See NS Package Number H10F

TL/K/10120-2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|------|
| Peak Power Supply Voltage (for 0.1 sec) | 60V |
| Continuous Supply Voltage | 45V |
| Input Voltage | 5.5V |

| | |
|--|--|
| Input Extender Current | 5.0 mA |
| Peak Output Current (50 ms On/1 sec Off) | 1.5A |
| Operating Temperature | DH0006 -55°C to +125°C DH0006C 0°C to +70°C |
| Storage Temperature | -65°C to +150°C |

Electrical Characteristics (Note 1)

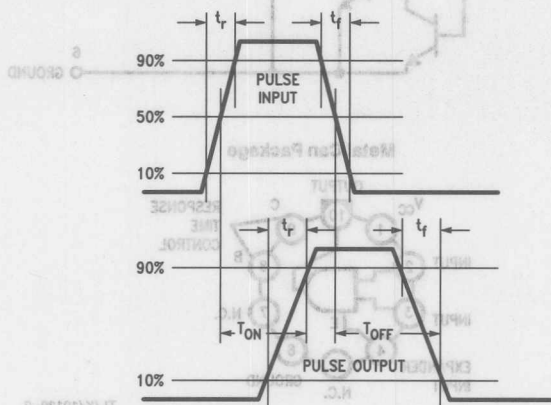
| Parameter | Conditions | Min | Typ (Note 2) | Max | Units |
|----------------------------|--|------|-----------------|------------|-------|
| Logical "1" Input Voltage | $V_{CC} = 45V$ to $10V$ | 2.0 | | | V |
| Logical "0" Input Voltage | $V_{CC} = 45V$ to $10V$ | | | 0.8 | |
| Logical "1" Output Voltage | $V_{CC} = 28V$, $V_{IN} = 2.0V$, $I_{OUT} = 400$ mA | 26.5 | 27.0 | | |
| Logical "0" Output Voltage | $V_{CC} = 45V$, $V_{IN} = 0.8V$, $R_L = 1k$ | | 0.001 | 0.01 | |
| Logical "1" Output Voltage | $V_{CC} = 10V$, $V_{IN} = 2.0V$, $I_{OUT} = 150$ mA | 8.8 | 9.2 | | mA |
| Logical "0" Input Current | $V_{CC} = 45V$, $V_{IN} = 0.4V$ | | -0.8 | -1.0 | |
| Logical "1" Input Current | $V_{CC} = 45V$, $V_{IN} = 2.4V$ $V_{CC} = 45V$, $V_{IN} = 5.5V$ | | 0.5 | 5.0 100 | |
| "Off" Power Supply Current | $V_{CC} = 45V$, $V_{IN} = 0.8V$ | | 1.6 | 2.0 | |
| "On" Power Supply Current | $V_{CC} = 45V$, $V_{IN} = 2.0V$, $I_{OUT} = 0$ mA | | | 8 | μs |
| Rise Time | $V_{CC} = 28V$, $R_L = 82\Omega$ | | 0.10 | | |
| Fall Time | | | 0.8 | | |
| T_{on} | | | 0.26 | | |
| T_{off} | | | 2.2 | | |

Note 1: Unless otherwise specified, limits shown apply from -55°C to +125°C for DH0006 and 0°C to +70°C for DH0006C.

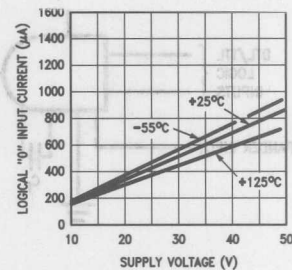
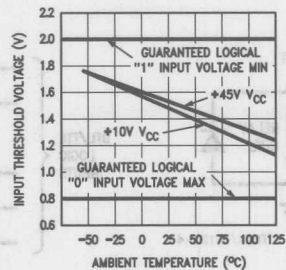
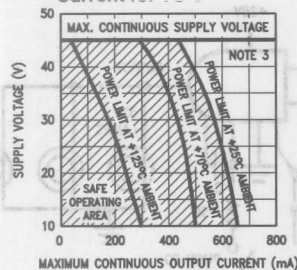
Note 2: Typical values are for 25°C ambient.

Note 3: Power ratings for the TO-5 based on a maximum junction temperature of +175°C and θ_{JA} of 210°C/W.

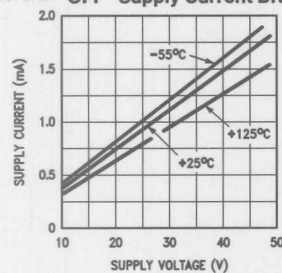
Switching Time Waveforms



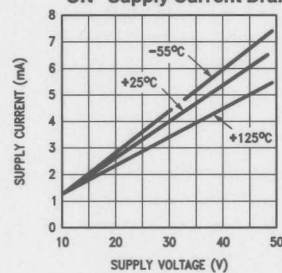
TL/K/10120-6



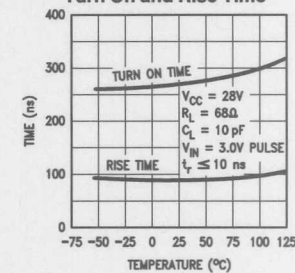
"OFF" Supply Current Drain



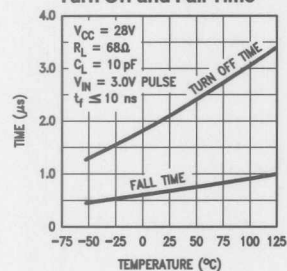
"ON" Supply Current Drain



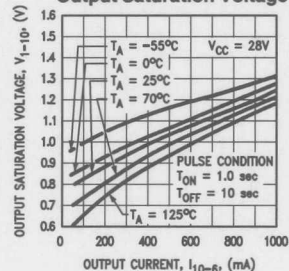
Turn On and Rise Time



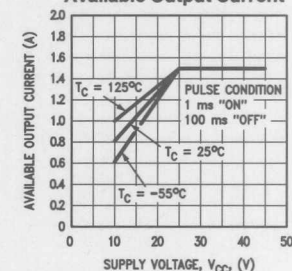
Turn Off and Fall Time



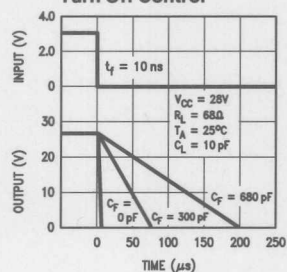
Output Saturation Voltage



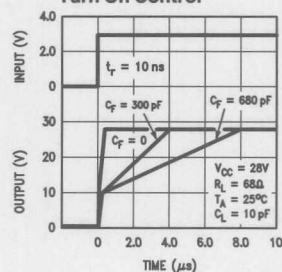
Available Output Current



Turn Off Control

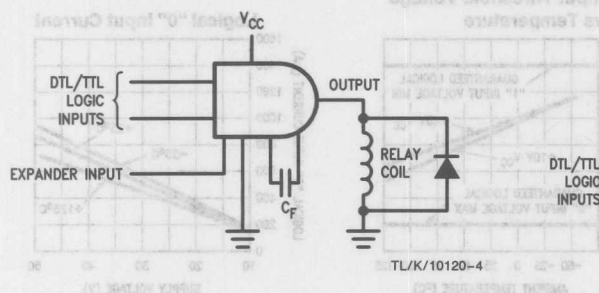


Turn On Control

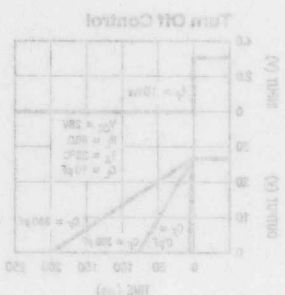
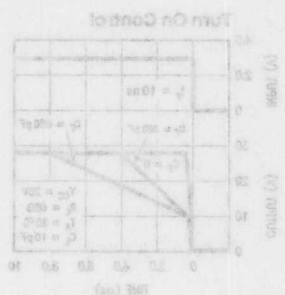
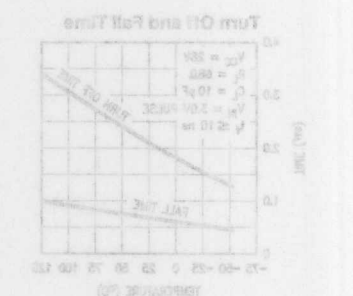
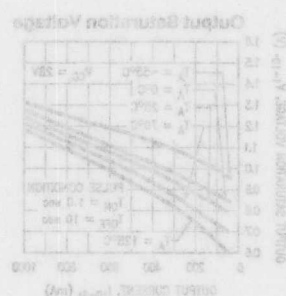
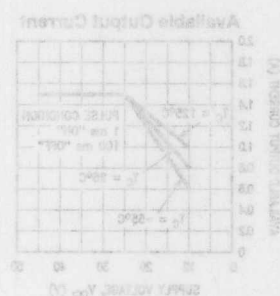
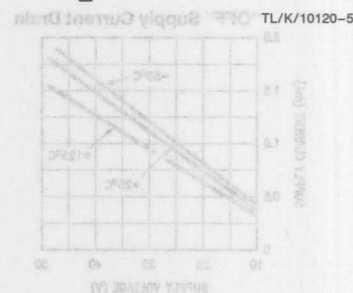
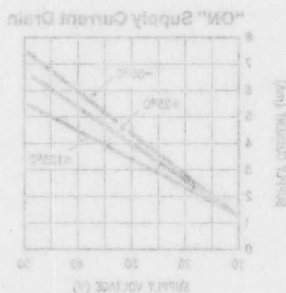
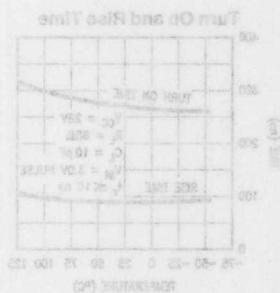
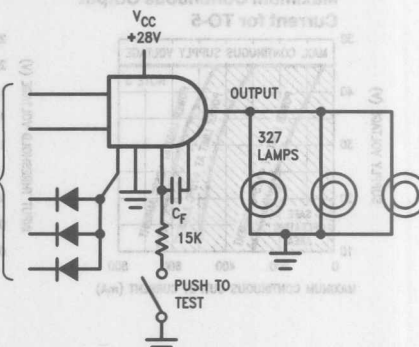


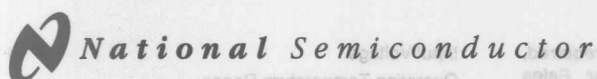
Typical Applications

Relay Driver



Lamp Driver with Expanded Inputs





DH0034

High Speed Dual Level Translator

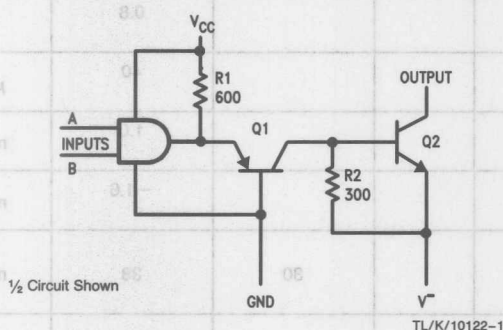
General Description

The DH0034 is a high speed level translator suitable for interfacing to MOS or junction FET analog switches. It may also be used as a universal logic level shifter capable of accepting TTL/DTL input levels and shifting to CML, MOS, or SLT levels.

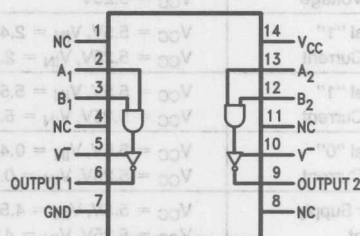
Features

- Fast switching, t_{pd0} : typically 15 ns; t_{pd1} : typically 35 ns
- Large output voltage range: 25V
- Input is TTL/DTL compatible
- Low output leakage: typically 0.1 μ A

Schematic and Connection Diagrams



Dual-In-Line Package



Top View

Order Number DH0034D-MIL
or DH0034CD
See NS Package Number D14D

DH0034

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--------------------------------|----------|
| V _{CC} Supply Voltage | 7.0V |
| Negative Supply Voltage | -30V |
| Positive Supply Voltage | +25V |
| Differential Supply Voltage | 25V |
| Maximum Output Current | 100 mA |
| Power Dissipation | (Note 4) |

| | |
|---------------------------------------|-----------------|
| Input Voltage | +5.5V |
| Operating Temperature Range | -55°C to +125°C |
| DH0034D-MIL | 0°C to +85°C |
| DH0034CD | -65°C to 150°C |
| Storage Temperature Range | 300°C |
| Lead Temperature (Soldering, 10 sec.) | |

Electrical Characteristics (See Notes 1 and 2)

| Parameter | Conditions | DH0034 | | | Units |
|--------------------------------------|---|--------|---|-----------------------|-------|
| | | Min | Typ | Max | |
| Logical "1" Input Voltage | V _{CC} = 4.5V V _{CC} = 4.75V | 2.0 | | | V |
| Logical "0" Input Voltage | V _{CC} = 5.5V V _{CC} = 5.25V | | | 0.8 | V |
| Logical "1" Input Current | V _{CC} = 5.5V, V _{IN} = 2.4V V _{CC} = 5.25V, V _{IN} = 2.4V | | | 40 | μA |
| Logical "1" Input Current | V _{CC} = 5.5V, V _{IN} = 5.5V V _{CC} = 5.25V, V _{IN} = 5.5V | | | 1.0 | mA |
| Logical "0" Input Current | V _{CC} = 5.5V, V _{IN} = 0.4V V _{CC} = 5.25V, V _{IN} = 0.4V | | | -1.6 | mA |
| Power Supply Current Logic "0" | V _{CC} = 5.5V, V _{IN} = 4.5V V _{CC} = 5.25V, V _{IN} = 4.5V (Note 3) | | 30 | 38 | mA |
| Power Supply Current Logic "1" | V _{CC} = 5.5V, V _{IN} = 0V V _{CC} = 5.25V, V _{IN} = 0V (Note 3) | | 37 | 48 | mA |
| Logical "0" Output Voltage | V _{CC} = 4.5V, I _{OUT} = 100 mA V _{CC} = 4.5V, I _{OUT} = 50 mA | | V ⁻ + 0.50 V ⁻ + 0.3 | V ⁻ + 0.50 | V |
| Output Leakage Current | V _{CC} = 5.5V, V _{IN} = 0.8V V ⁺ - V ⁻ = 25V | | 0.1 | 5.0 | μA |
| Transition Time to Logical "0" | V _{CC} = 5.0V, V ₃ = 0V, T _A = 25°C V ⁻ = 25V, R _L = 510Ω | | 15 | 25 | ns |
| Transition Time to Logical "1" | V _{CC} = 5.0V, T _A = 25°C V ⁻ = -25V, R _L = 510Ω | | 35 | 75 | ns |

Note 1: The specifications apply over the temperature range -55°C to +125°C for the DH0034D-MIL and over the temperature range -25°C to +85°C for DH0034CD with a 510Ω resistor connected between output and ground, and V⁻ connected to -25V, unless otherwise specified.

Note 2: All typical values are for T_A = 25°C.

Note 3: Current measured is total drawn from V_{CC} supply.

Note 4: Power rating for the Cavity DIP based on a maximum junction temperature of 175°C and θ_{JA} = 180°C/W.

Theory of Operation

When both inputs of the DH0034 are raised to logic "1", the input AND gate is turned "on" allowing Q1's emitter to become forward biased. Q1 provides a level shift and constant output current. The collector current is essentially the same as the emitter which is given by

$$\frac{V_{CC} - V_{BE}}{R1}$$

Approximately 7.0 mA flows out of Q1's collector.

About 2 mA of Q1's collector current is drawn off by pull down resistor, R2. The balance, 5 mA, is available as base drive to Q2 and to charge its associated Miller capacitance. The output is pulled to within a V_{SAT} of V^- . When either (or both) input to the DH0034 is lowered to logic "0", the AND gate output drops to 0.2V turning Q1 off. Deprived of base drive Q2 rapidly turns off causing the output to rise to the V_3 supply voltage. Since Q2's emitter operates between 0.6V and 0.2V, the speed of the DH0034 is greatly enhanced.

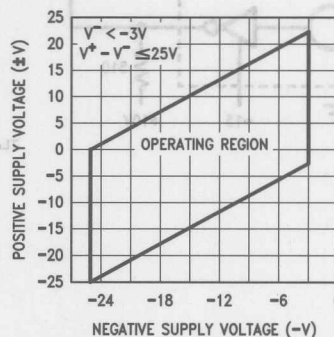
Applications Information

1. Paralleling the Outputs

The outputs of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wire OR". In order to prevent current hogging by one output transistor or the other, resistors of $2\Omega/100$ mA value should be inserted between the emitters of the output transistors and the minus supply.

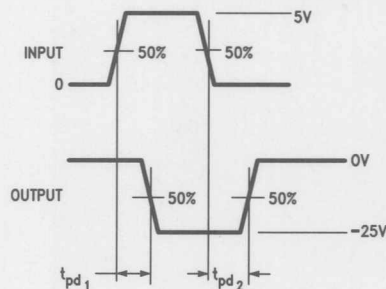
2. Recommended Output Voltage Swing

The graph shows boundary conditions which govern proper operation of the DH0034. **The range of operation for the negative supply is shown on the X axis and must be between -3V and -25V.** The allowable range for the positive supply is governed by the value chosen for V^- . V^+ may be selected by drawing a vertical line through the selected value for V^- and terminated by the boundaries of the operating region. For example, a value of V^- equal to -6V would dictate values of V^+ between -5V and +19V. In general, it is desirable to maintain at least 5V difference between the supplies.



TL/K/10122-6

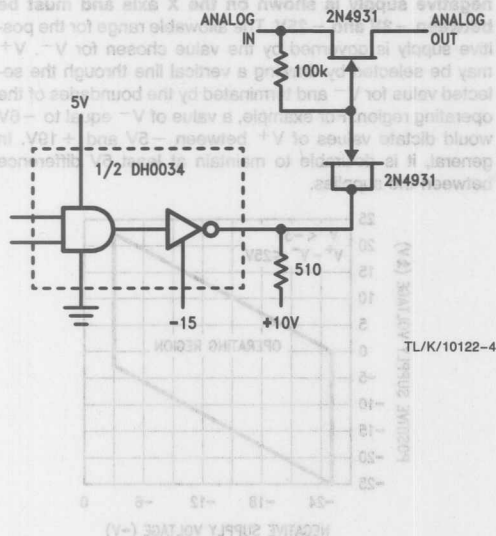
Switching Time Waveforms



TL/K/10122-7

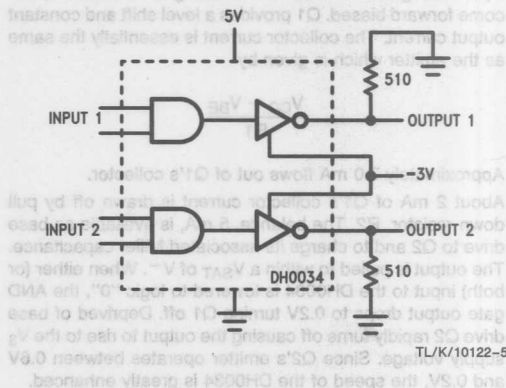
Typical Applications

5 MHz Analog Switch



TL/K/10122-4

TTL to IBM (SLT) Logic Levels

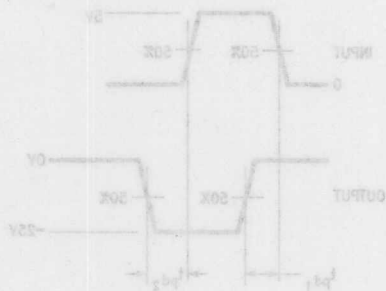


TL/K/10122-5

Applications Information

1. Paralleling the Outputs
The output of the DH0034 may be paralleled to increase output drive capability or to accomplish the "wired OR" in order to prevent current hogging by one output transistor. The other, resistor of 50k/100mA value should be inched between the emitters of the output transistors and the minus supply.

Switching Time Waveforms



T-5/10122-7

DH0035/DH0035C PIN Diode Driver

General Description

The DH0035/DH0035C is a high speed digital driver designed to drive PIN diodes in RF modulators and switches. The device is used in conjunction with an input buffer such as the DM7830/DM8830 or DM5440/DM7440.

Features

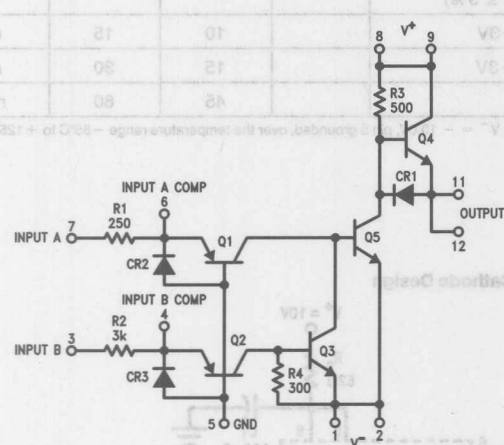
- Large output voltage swing—30V
- Peak output current in excess of 1A
- Inputs TTL/DTL compatible

- Short propagation delay—10 ns
- High repetition rate—5 MHz

The DH0035/DH0035C is capable of driving a variety of PIN diode types including parallel, serial, anode grounded and cathode grounded. For additional information, see *AN-49 PIN Diode Drivers*.

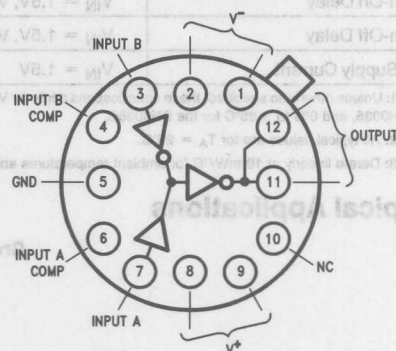
The DH0035 is guaranteed over the temperature range -55°C to +125°C whereas the DH0035C is guaranteed from 0°C to +85°C.

Schematic and Connection Diagrams



TL/K/10124-1

Metal Can Package



TL/K/10124-2

Top View

Order Number DH0035G-MIL or DH0035CG
See NS Package Number G12B

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|-------------|
| V^- Supply Voltage Differential (Pin 5 to Pin 1 or 2) | 40V |
| V^+ Supply Voltage Differential (Pin 1 or 2 to Pin 8 or 9) | 30V |
| Input Current (Pin 3 or 7) | ± 75 mA |
| Peak Output Current | ± 1.0 A |

| | |
|---------------------------------------|---|
| Power Dissipation (Note 3) | 1.5W |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Operating Temperature Range | |
| DH0035 | -55°C to $+125^\circ\text{C}$ |
| DH0035C | 0°C to $+85^\circ\text{C}$ |
| Lead Temperature (Soldering, 10 sec.) | 300°C |

Electrical Characteristics (Notes 1 and 2)

| Parameter | Conditions | Limits | | | Units |
|--------------------------------|--|--------|------|------|-------|
| | | Min | Typ | Max | |
| Input Logic "1" Threshold | $V_{\text{OUT}} = -8\text{V}$, $R_L = 100\Omega$ | | 1.0 | 2.0 | V |
| Input Logic "0" Threshold | $V_{\text{OUT}} = +8\text{V}$, $R_L = 100\Omega$ | 0.4 | 0.6 | | V |
| Positive Output Swing | $I_{\text{OUT}} = 100$ mA | 7.0 | +8.0 | | V |
| Negative Output Swing | $I_{\text{OUT}} = 100$ mA | | -8.0 | -7.0 | V |
| Positive Short Circuit Current | $V_{\text{IN}} = 0\text{V}$, $R_L = 0\Omega$ (Pulse Test, Duty Cycle $\leq 3\%$) | 400 | 800 | | mA |
| Negative Short Circuit Current | $V_{\text{IN}} = 1.5\text{V}$, $I_{\text{IN}} = 50$ mA, $R_L = 0\Omega$ (Pulse Test, Duty Cycle $\leq 3\%$) | 800 | 1000 | | mA |
| Turn-On Delay | $V_{\text{IN}} = 1.5\text{V}$, $V_{\text{OUT}} = -3\text{V}$ | | 10 | 15 | ns |
| Turn-Off Delay | $V_{\text{IN}} = 1.5\text{V}$, $V_{\text{OUT}} = +3\text{V}$ | | 15 | 30 | ns |
| On Supply Current | $V_{\text{IN}} = 1.5\text{V}$ | | 45 | 60 | mA |

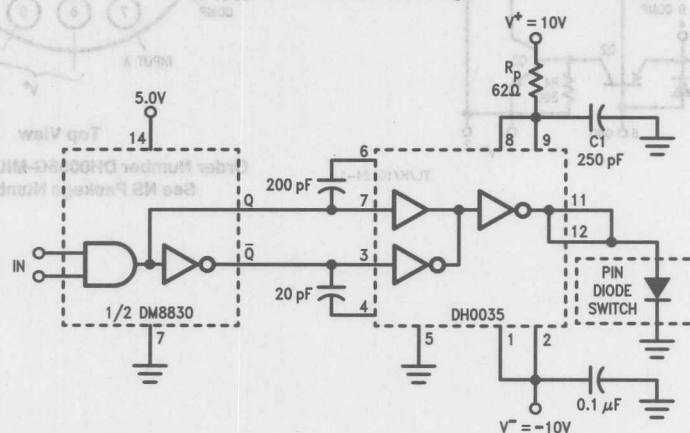
Note 1: Unless otherwise specified, these specifications apply for $V^+ = 10.0\text{V}$, $V^- = -10.0\text{V}$, pin 5 grounded, over the temperature range -55°C to $+125^\circ\text{C}$ for the DH0035, and 0°C to $+85^\circ\text{C}$ for the DH0035C.

Note 2: All typical values are for $T_A = 25^\circ\text{C}$.

Note 3: Derate linearly at 10 mW/ $^\circ\text{C}$ for ambient temperatures above 25°C .

Typical Applications

Grounded Cathode Design



Note: Cathode grounded PIN diode: $R_p = 62\Omega$ limits diode forward current to 100 mA. Typical switching for HP33604A, RF turn-on 25 ns, turn-off 5 ns. $C_2 = 250$ pF, $R_p = 0\Omega$, $C_1 = 0.1\text{F}$.

TL/K/10124-3

LH0094 Multifunction Converter

General Description

The LH0094 multifunction converter generates an output voltage per the transfer function:

$$E_O = V_Y \left(\frac{V_Z}{V_X} \right)^m, 0.1 \leq m \leq 10, m \text{ continuously adjustable}$$

m is set by 2 resistors.

Features

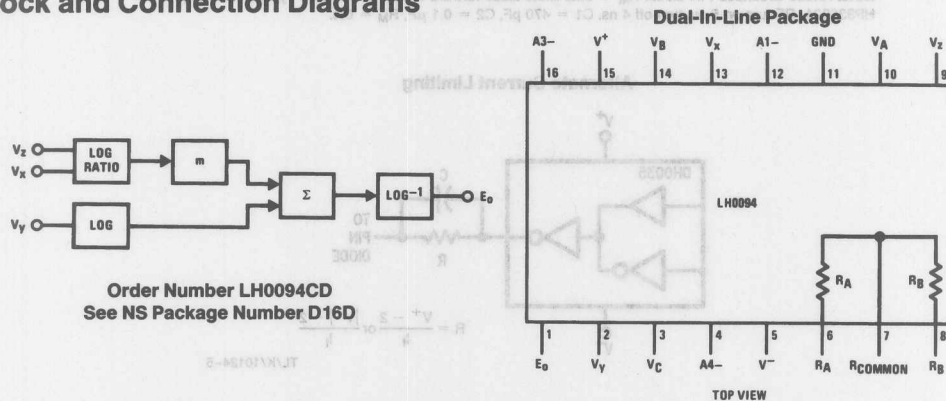
- Low cost
- Versatile
- High accuracy—0.05%
- Wide supply range— $\pm 5V$ to $\pm 22V$

- Minimum component count
- Internal matched resistor pair for setting $m=2$ and $m=0.5$

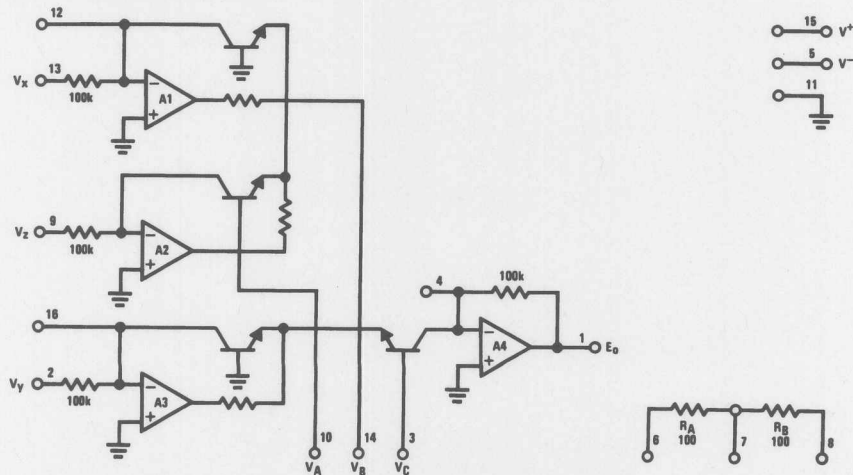
Applications

- Precision divider, multiplier
- Square root
- Square
- Trigonometric function generator
- Companding
- Linearization
- Control systems
- Log amp

Block and Connection Diagrams



Simplified Schematic



please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage $\pm 22V$
Input Voltage $\pm 22V$
Output Short-Circuit Duration Continuous

LH0094CD $-25^{\circ}C$ to $+85^{\circ}C$
Storage Temperature Range $-55^{\circ}C$ to $+125^{\circ}C$
LH0094CD
Lead Temperature (Soldering, 10 seconds) $260^{\circ}C$

Electrical Characteristics

$V_S = \pm 15V$, $T_A = 25^{\circ}C$ unless otherwise specified. Transfer function: $E_O = V_Y \frac{V_Z^m}{V_X}$; $0.1 \leq m \leq 10$; $OV \leq V_X, V_Y, V_Z \leq 10V$

| Parameter | Conditions | LH0094C | | | Units |
|------------------------|---|------------|-----------|--------|-------------|
| | | Min | Typ | Max | |
| ACCURACY | | | | | |
| Multiply | $E_O = V_Z V_Y$ ($0.03 \leq V_Y \leq 10V$; $0.01 \leq V_Z \leq 10V$) | | | | % F.S. |
| Untrimmed | (Figure 2) | | 0.45 | 0.9 | (10V) |
| External Trim | (Figure 3) | | 0.1 | | % F.S. |
| | vs. Temperature | | 0.2 | | mV/°C |
| Divide | $E_O = 10V_Z/V_X$ | | | | |
| Untrimmed | (Figure 4), $0.5 \leq V_X \leq 10$; $0.01 \leq V_Z \leq 10$ | | 0.45 | 0.9 | % F.S. |
| External Trim | (Figure 5), $(0.1 \leq V_X \leq 10$; $0.01 \leq V_Z \leq 10$) | | 0.1 | | % F.S. |
| | vs. Temperature | | 0.2 | | mV/°C |
| Square Root | $E_O = 10\sqrt{V_Z/10}$ | | | | |
| Untrimmed | (Figure 8), $(0.03 \leq V_Z \leq 10$) | | 0.45 | 0.9 | % F.S. |
| External Trim | (Figure 9), $(0.01 \leq V_Z \leq 10$) | | 0.15 | | % F.S. |
| Square | $E_O = 10(V_Z/10)^2$ ($0.1 \leq V_Z \leq 10$) | | | | |
| Untrimmed | (Figure 6) | 1.0 | 2.0 | % F.S. | |
| External Trim | (Figure 7) | 0.15 | | % F.S. | |
| Low Level | $E_O = \sqrt{10V_Z}$; $5.0mV \leq V_Z \leq 10V$, (Figure 10) | | 0.05 | | % F.S. |
| Square Root | | | | | |
| Exponential | $m = 0.2$, $E_O = 10(V_Z/10)^2$ (Figure 11), $(0.1 \leq V_Z \leq 10)$ | | 0.08 | | % F.S. |
| Circuits | $m = 5.0$, $E_O = 10(V_Z/10)^5$ (Figure 11), $(1.0 \leq V_Z \leq 10)$ | | 0.08 | | % F.S. |
| OUTPUT OFFSET | | | | | |
| | $V_X = 10V$, $V_Y = V_Z = 0$ | | 5.0 | 10 | mV |
| AC CHARACTERISTICS | | | | | |
| 3 dB Bandwidth | $m = 1.0$, $V_X = 10V$, $V_Y = 0.1 V_{rms}$ | | 10 | | kHz |
| Noise | 10 Hz to 1.0 kHz, $m = 1.0$, $V_Y = V_Z = OV$ | | | | |
| | $V_X = 10V$ | | 100 | | $\mu V/rms$ |
| | $V_X = 0.1V$ | | 300 | | $\mu V/rms$ |
| EXPONENT | | | | | |
| m | | 0.2 to 5.0 | 0.1 to 10 | | |
| INPUT CHARACTERISTICS | | | | | |
| Input Voltage | (For Rated Performance) | 0 | | 10 | V |
| Input Impedance | (All Inputs) | 98 | 100 | | k Ω |
| OUTPUT CHARACTERISTICS | | | | | |
| Output Swing | ($R_L \leq 10k$) | 10 | 12 | | V |
| Output Impedance | | | 1.0 | | Ω |
| Supply Current | ($V_S = \pm 15V$) (Note 1) | | 3.0 | 5.0 | mA |

Note 1: Refer to RETS0094D drawing for specifications of the military LH00940 version.

Applications Information

GENERAL INFORMATION

Power supply bypass capacitors (0.1 μ F) are recommended for all applications.

The LH0094 series is designed for positive input signals only. However, negative input up to the supply voltage will not damage the device.

A clamp diode (Figure 1) is recommended for those applications in which the inputs may be subjected to open circuit or negative input signals.

For basic applications (multiply, divide, square, square root) it is possible to use the device without any external adjustments or components. Two matched resistors are provided internally to set m for square or square root.

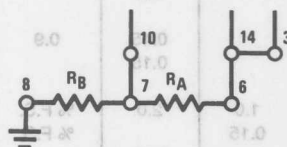
When using external resistors to set m , such resistors should be as close to the device as possible.

SELECTION OF RESISTORS TO SET m

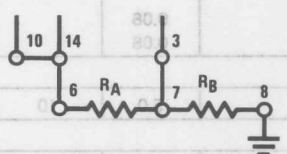
Internal Matched Resistors

R_A and R_B are matched internal resistors. They are $100\Omega \pm 10\%$, but matched to 0.1%.

(a) $m = 2^*$



(b) $m = 0.5^*$

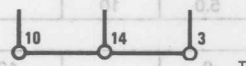


*No external resistors required, strap as indicated

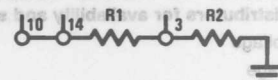
External Resistors

The exponent is set by 2 external resistors or it may be continuously varied by a single trim pot. ($R_1 + R_2 \leq 500\Omega$).

(a) $m = 1$

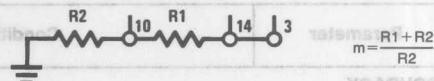


(b) $m < 1$



$$m = \frac{R_2}{R_1 + R_2} \quad R_1 + R_2 \approx 200\Omega$$

(c) $m > 1$



ACCURACY (ERROR)

The accuracy of the LH0094 is specified for both externally adjusted and unadjusted cases.

Although it is customary to specify the errors in percent of full-scale (10V), it is seen from the typical performance curves that the actual errors are in percent of reading. Thus, the specified errors are overly conservative for small input voltages. An example of this is the LH0094 used in the multiplication mode. The specified typical error is 0.25% of full-scale (25 mV). As seen from the curve, the unadjusted error is ≈ 25 mV at 10V input, but the error is less than 10 mV for inputs up to 1V. Note also that if either the multiplier or the multiplier is at less than 10V, (5V for example) the unadjusted error is less. Thus, the errors specified are at full-scale—the worst case.

The LH0094 is designed such that the user is able to externally adjust the gain and offset of the device—thus trim out all of the errors of conversion. In most applications, the gain adjustment is the only external trim needed for super accuracy—except in division mode, where a denominator offset adjust is needed for small denominator voltages.

EXPONENTS

The LH0094 is capable of performing roots to 0.1 and powers up to 10. However, care should be taken when applying these exponent—otherwise, results may be misinterpreted. For example, consider the $1/10$ th power of a number: i.e., 0.001 raised to 0.1 power is 0.5011; 0.1 raised to the 0.1 power is 0.7943; and 10 raised to the 0.1 power is 1.2589. Thus, it is seen that while the input has changed 4 decades, the output has only changed a little more than a factor of 2. It is also seen that with as little as 1 mV of offset, the output will also be greater than zero with zero input.

Applications Information (Continued)

1. CLAMP DIODE CONNECTION

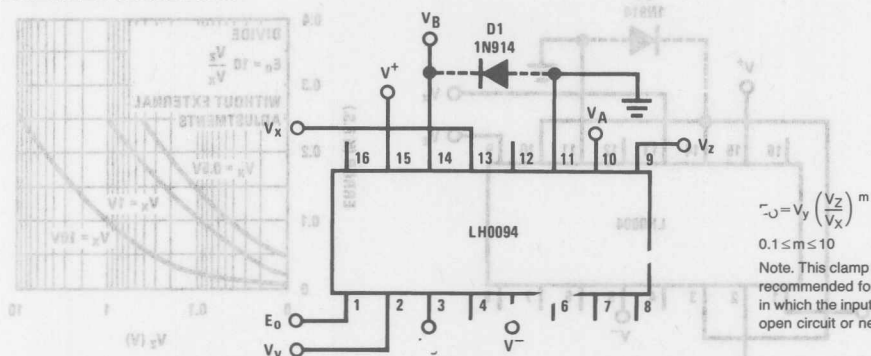


FIGURE 1. Clamp Diode Connection

2. MULTIPLY

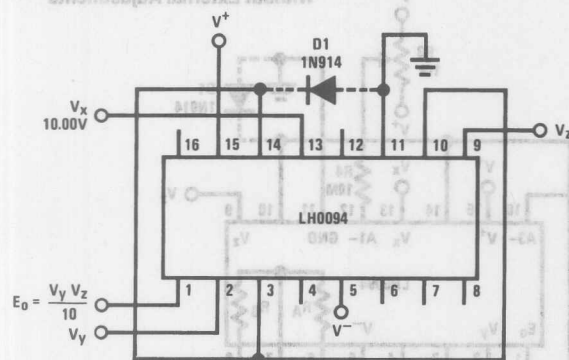


FIGURE 2a. LH0094 Used to Multiply (No External Adjustment)

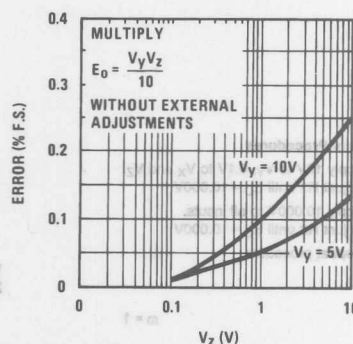


FIGURE 2b. Typical Performance of LH0094 in Multiply Mode Without External Adjustment

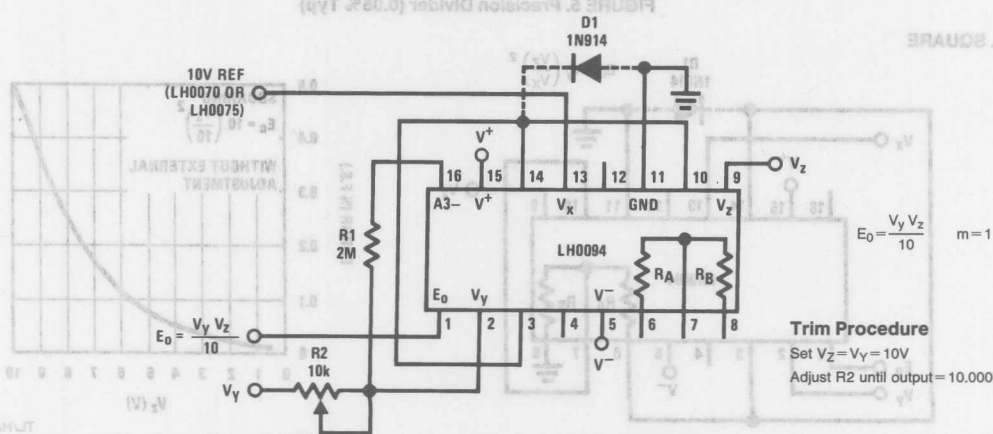


FIGURE 3. Precision Multiplier (0.02% Typ) with 1 External Adjustment

Applications Information (Continued)

3. DIVIDE

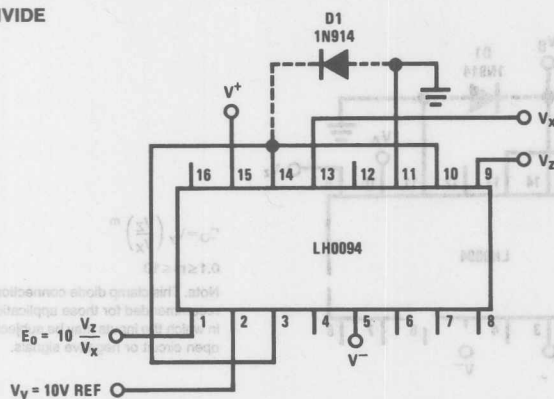


FIGURE 4a. LH0094 Used to Divide (No External Adjustment)

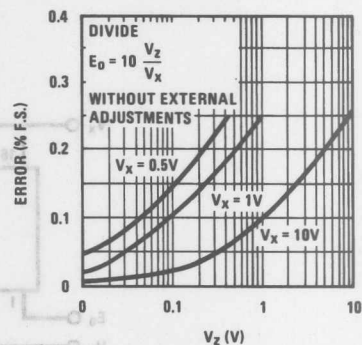


FIGURE 4b. Typical Performance, Divide Mode, Without External Adjustments

Trim Procedures

Apply 10V to V_y , 0.1V to V_x and V_z .
Adjust R3 until $E_0 = 10.000V$.

Apply 10.000V to all inputs.
Adjust R2 until $E_0 = 10.000V$.
Repeat procedure.

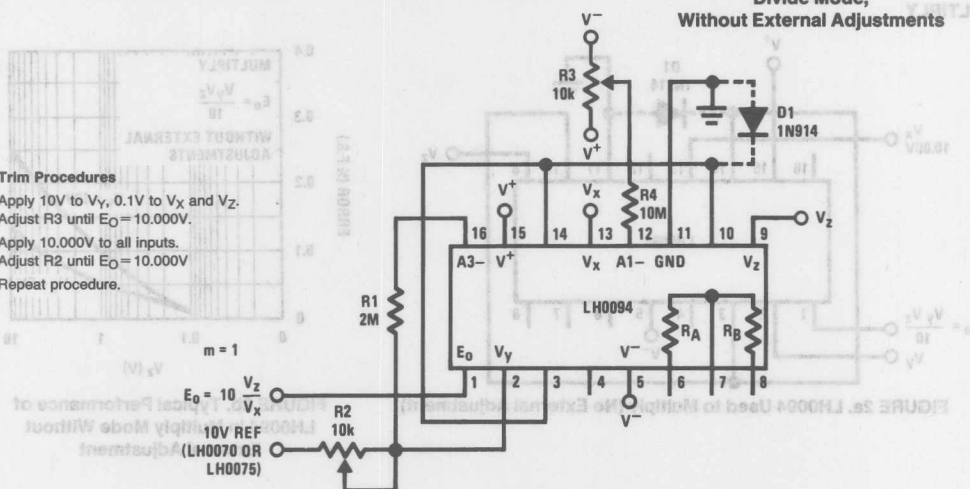


FIGURE 5. Precision Divider (0.05% Typ)

4. SQUARE

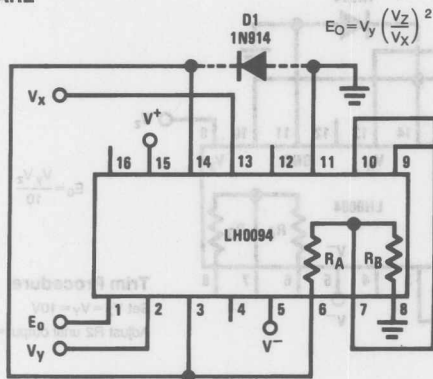
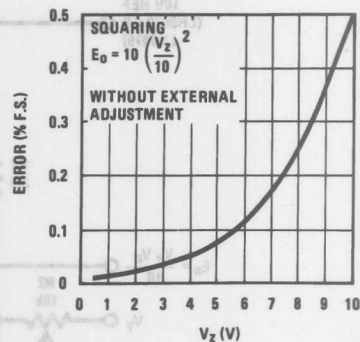
FIGURE 6a. Basic Connection of LH0094 ($m = 2$) without External Adjustment Using Internal Resistors to Set m 

FIGURE 6b. Squaring Mode without External Adjustment

TL/H/5695-6

Applications Information (Continued)

4. SQUARE (Continued)

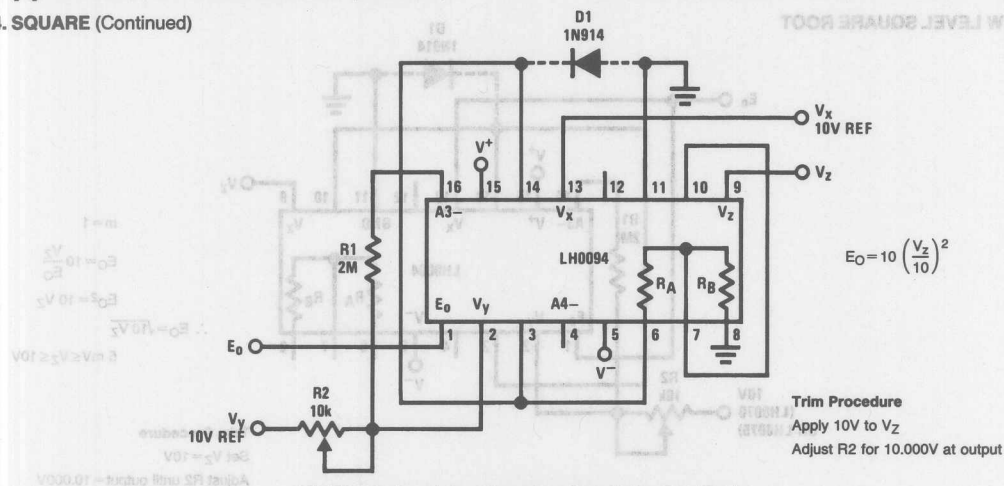


FIGURE 7. Precision Squaring Circuit (0.15% Typ)

5. SQUARE ROOT

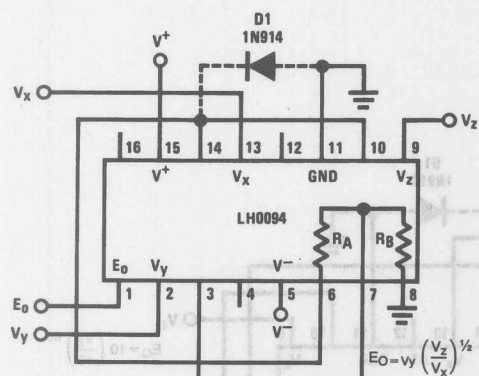
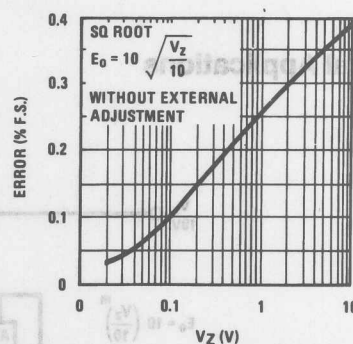
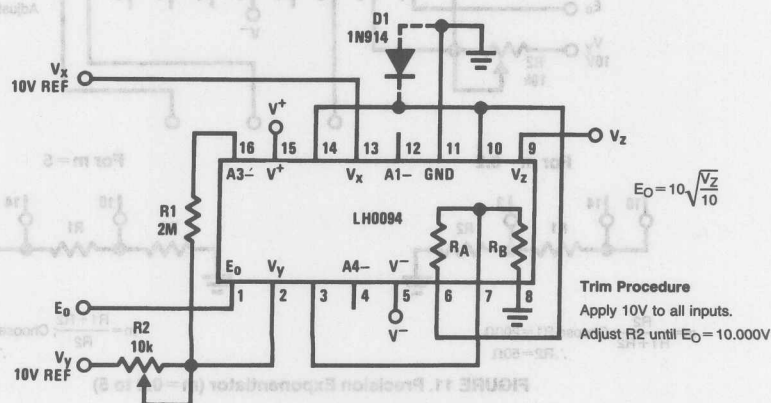
FIGURE 8a. Basic Connection of LH0094 ($m=0.5$)
without External Adjustment Using Internal Resistors
to Set m FIGURE 8b. Typical Performance Curve Square Root,
No External Adjustment

FIGURE 9. Precision Square Rooter (0.15% Typ)

TL/H/5695-7

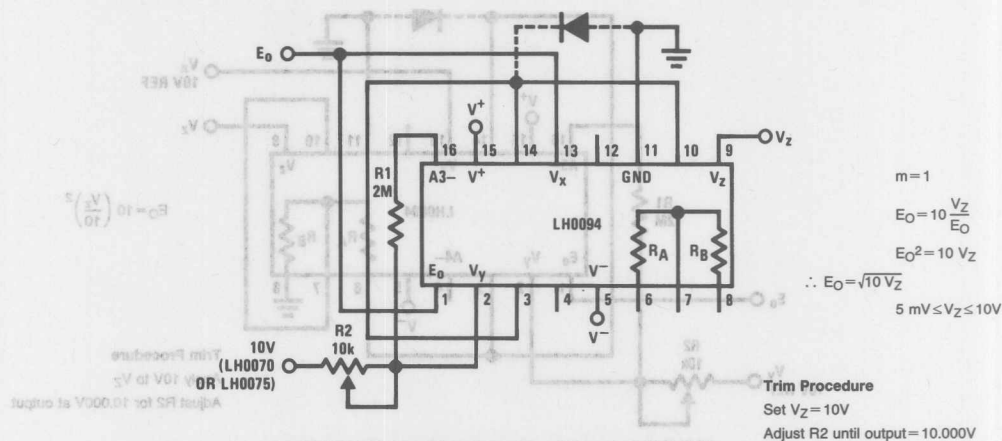


FIGURE 10. 3-Decade Precision Square Root Circuit Using the LH0094 with $m = 1$

Typical Applications

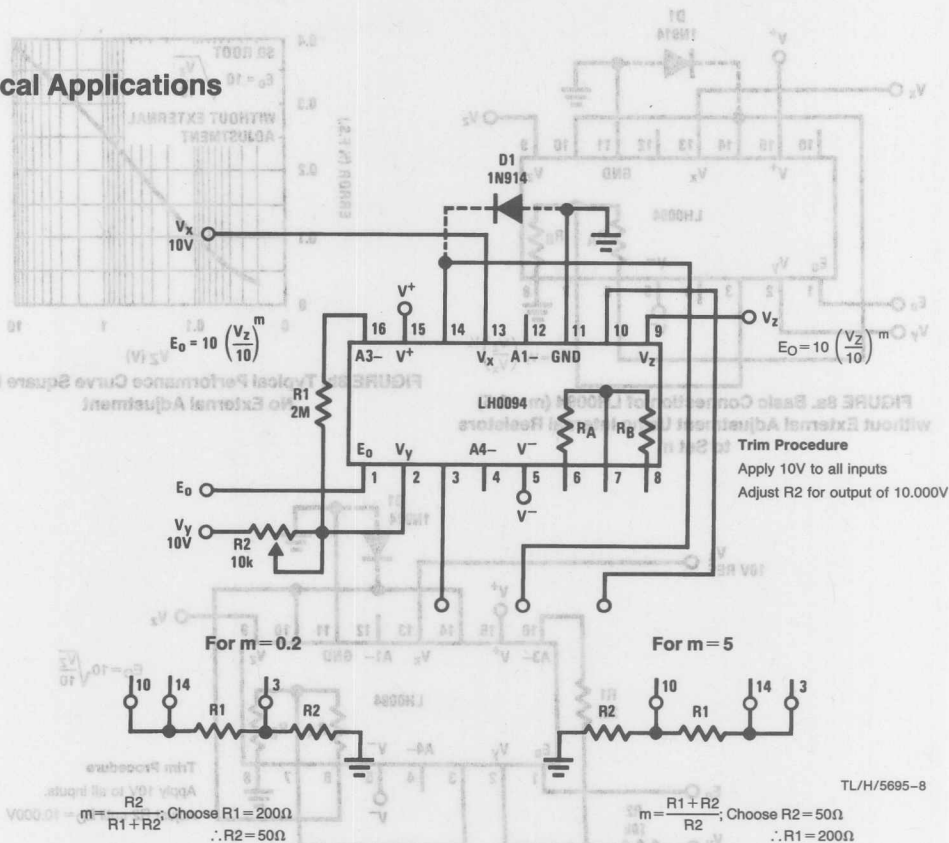
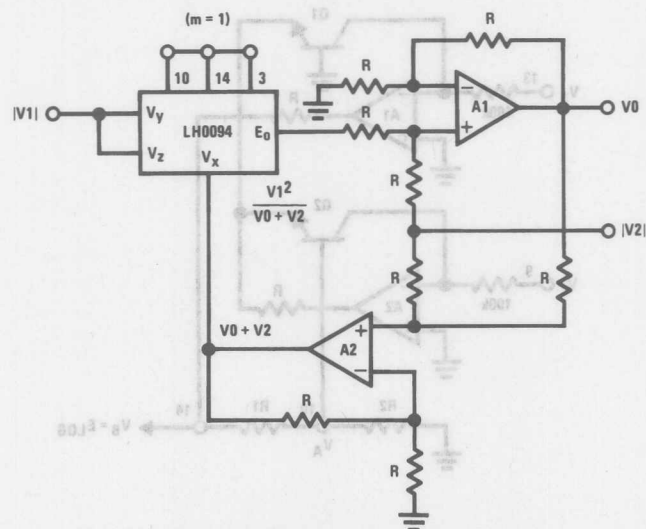


FIGURE 11. Precision Exponentiator ($m = 0.2$ to 5)

Typical Applications (Continued)



Note. The LH0094 may be used to generate a voltage equivalent to:

$$V_0 = \sqrt{V_1^2 + V_2^2}$$

$$V_0 = V_2 + \frac{V_1^2}{V_0 + V_2}$$

$$V_0^2 + V_0 V_2 = V_2 V_0 + V_2^2 + V_1^2$$

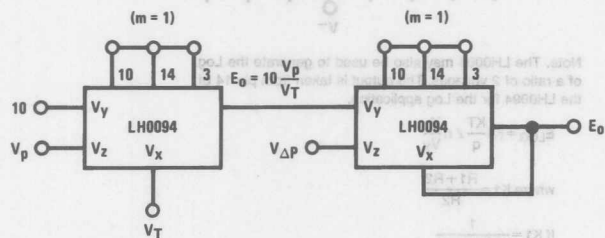
$$V_0^2 = V_1^2 + V_2^2$$

$$\therefore V_0 = \sqrt{V_1^2 + V_2^2} \quad V_1, V_2 \rightarrow 0 \rightarrow 10V$$

$$R \approx 10k$$

National Semiconductor resistor array RA08—10k is recommended

FIGURE 12. Vector Magnitude Function



Note. The LH0094 may be used in direct measurement of gas flow.

$$\text{Flow} = k \sqrt{\frac{P \Delta P}{T}}$$

$$E_0 = 10 \frac{V_P}{V_T} \times \frac{V_{\Delta P}}{E_0}$$

$$E_0^2 = 10 \frac{V_P V_{\Delta P}}{V_T}$$

$$E_0 = \sqrt{10 \frac{V_P V_{\Delta P}}{V_T}}$$

P = Absolute pressure

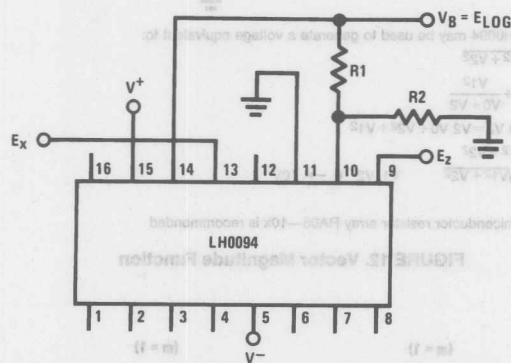
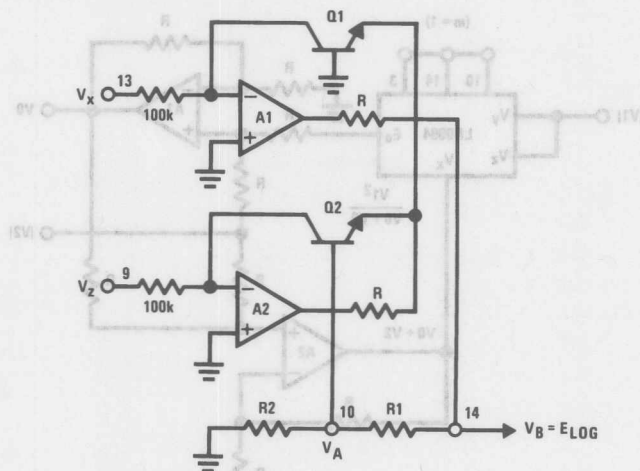
T = Absolute temperature

ΔP = Pressure drop

FIGURE 13. Mass Gas Flow Circuit

TL/H/5695-9

Typical Applications (Continued)



Note. The LH0094 may also be used to generate the Log of a ratio of 2 voltages. The output is taken from pin 14 of the LH0094 for the Log application.

$$E_{\text{LOG}} = K1 \frac{KT}{q} \ln \frac{V_Z}{V_X}$$

$$\text{where } K1 = \frac{R1 + R2}{R2}$$

$$\text{If } K1 = \frac{1}{KT/q \ln 10}$$

$$\text{then } E_{\text{LOG}} = \log_{10} \frac{V_Z}{V_X}$$

$$R1 = 15.9 R2$$

$$R2 \approx 400 \Omega$$

R2 must be a thermistor with a tempco of $\approx 0.33\%/^{\circ}\text{C}$ to be compensated over temperature.

FIGURE 14. Log Amp Application

LM194/LM394 Supermatch Pair

General Description

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This was accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1 μA to 1 mA and 0V up to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current—the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely

matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

The LM194 and LM394/LM394B/LM394C are available in an isolated header 6-lead TO-5 metal can package. The LM394/LM394B/LM394C are available in an 8-pin plastic dual-in-line package. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

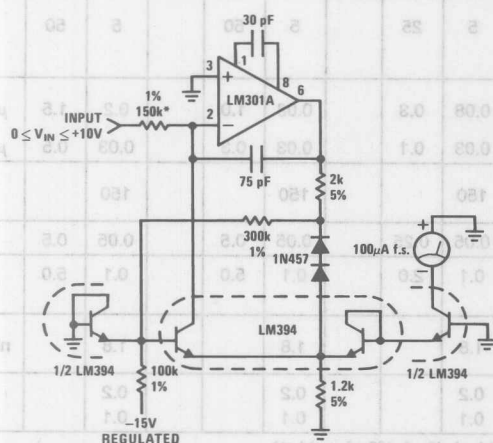
Features

- Emitter-base voltage matched to 50 μV
- Offset voltage drift less than 0.1 $\mu\text{V}/^\circ\text{C}$
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120 dB
- Parameters guaranteed over 1 μA to 1 mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

Typical Applications

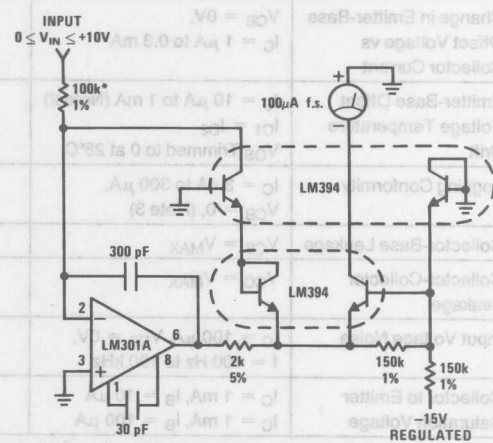
Low Cost Accurate Square Root Circuit

$$I_{OUT} = 10^{-5} \sqrt{10 V_{IN}}$$



Low Cost Accurate Squaring Circuit

$$I_{OUT} = 10^{-6} (V_{IN})^2$$



TL/H/9241-1
*Trim for full scale accuracy

TL/H/9241-2

please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 4)

| | |
|------------------------------------|-----------|
| Collector Current | 20 mA |
| Collector-Emitter Voltage | V_{MAX} |
| Collector-Emitter Voltage LM394C | 35V |
| Collector-Base Voltage LM394C | 20V |
| Collector-Substrate Voltage LM394C | 35V |
| Collector-Collector Voltage LM394C | 20V |

Power Dissipation 500 mW

Junction Temperature

LM194 -55°C to $+125^{\circ}\text{C}$

LM394/LM394B/LM394C -25°C to $+85^{\circ}\text{C}$

Storage Temperature Range -65°C to $+150^{\circ}\text{C}$

Soldering Information

Metal Can Package (10 sec.) 260°C

Dual-In-Line Package (10 sec.) 260°C

Small Outline Package

Vapor Phase (60 sec.) 215°C

Infrared (15 sec.) 220°C

See AN-450 "Surface Mounting and their Effects on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics ($T_J = 25^{\circ}\text{C}$)

| Parameter | Conditions | LM194 | | | LM394 | | | LM394B/394C | | | Units |
|---|--|-------|------|------|-------|------|-----|-------------|------|-----|--------------------------------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Current Gain (h_{FE}) | $V_{CB} = 0\text{V}$ to V_{MAX} (Note 1) | | | | | | | | | | |
| | $I_C = 1\text{ mA}$ | 350 | 700 | | 300 | 700 | | 225 | 500 | | |
| | $I_C = 100\text{ }\mu\text{A}$ | 350 | 550 | | 250 | 550 | | 200 | 400 | | |
| | $I_C = 10\text{ }\mu\text{A}$ | 300 | 450 | | 200 | 450 | | 150 | 300 | | |
| | $I_C = 1\text{ }\mu\text{A}$ | 200 | 300 | | 150 | 300 | | 100 | 200 | | |
| Current Gain Match, (h_{FE} Match) $= \frac{100 [\Delta I_B] [h_{FE(MIN)}]}{I_C}$ | $V_{CB} = 0\text{V}$ to V_{MAX} | | | | | | | | | | |
| | $I_C = 10\text{ }\mu\text{A}$ to 1 mA | | 0.5 | 2 | | 0.5 | 4 | | 1.0 | 5 | % |
| | $I_C = 1\text{ }\mu\text{A}$ | | 1.0 | | | 1.0 | | | 2.0 | | % |
| Emitter-Base Offset Voltage | $V_{CB} = 0$ $I_C = 1\text{ }\mu\text{A}$ to 1 mA | | 25 | 100 | | 25 | 150 | | 50 | 200 | μV |
| Change in Emitter-Base Offset Voltage vs Collector-Base Voltage (CMRR) | (Note 1) $I_C = 1\text{ }\mu\text{A}$ to 1 mA , $V_{CB} = 0\text{V}$ to V_{MAX} | | 10 | 25 | | 10 | 50 | | 10 | 100 | μV |
| Change in Emitter-Base Offset Voltage vs Collector Current | $V_{CB} = 0\text{V}$, $I_C = 1\text{ }\mu\text{A}$ to 0.3 mA | | 5 | 25 | | 5 | 50 | | 5 | 50 | μV |
| Emitter-Base Offset Voltage Temperature Drift | $I_C = 10\text{ }\mu\text{A}$ to 1 mA (Note 2) $I_{C1} = I_{C2}$ | | 0.08 | 0.3 | | 0.08 | 1.0 | | 0.2 | 1.5 | $\mu\text{V}/^{\circ}\text{C}$ |
| | V_{OS} Trimmed to 0 at 25°C | | 0.03 | 0.1 | | 0.03 | 0.3 | | 0.03 | 0.5 | $\mu\text{V}/^{\circ}\text{C}$ |
| Logging Conformity | $I_C = 3\text{ nA}$ to $300\text{ }\mu\text{A}$, $V_{CB} = 0$, (Note 3) | | 150 | | | 150 | | | 150 | | μV |
| Collector-Base Leakage | $V_{CB} = V_{MAX}$ | | 0.05 | 0.25 | | 0.05 | 0.5 | | 0.05 | 0.5 | nA |
| Collector-Collector Leakage | $V_{CC} = V_{MAX}$ | | 0.1 | 2.0 | | 0.1 | 5.0 | | 0.1 | 5.0 | nA |
| Input Voltage Noise | $I_C = 100\text{ }\mu\text{A}$, $V_{CB} = 0\text{V}$, $f = 100\text{ Hz}$ to 100 kHz | | 1.8 | | | 1.8 | | | 1.8 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| Collector to Emitter Saturation Voltage | $I_C = 1\text{ mA}$, $I_B = 10\text{ }\mu\text{A}$ | | 0.2 | | | 0.2 | | | 0.2 | | V |
| | $I_C = 1\text{ mA}$, $I_B = 100\text{ }\mu\text{A}$ | | 0.1 | | | 0.1 | | | 0.1 | | V |

Note 1: Collector-base voltage is swept from 0 to V_{MAX} at a collector current of $1\text{ }\mu\text{A}$, $10\text{ }\mu\text{A}$, $100\text{ }\mu\text{A}$, and 1 mA .

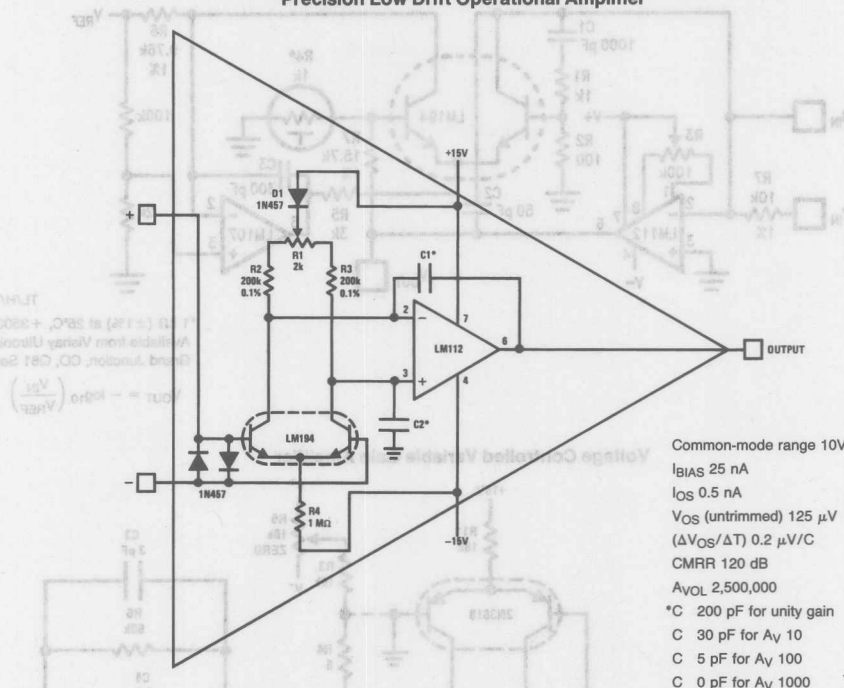
Note 2: Offset voltage drift with $V_{OS} = 0$ at $T_A = 25^{\circ}\text{C}$ is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at $+25^{\circ}\text{C}$ and temperature extremes.

Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

Note 4: Refer to RETS194X drawing of military LM194H version for specifications.

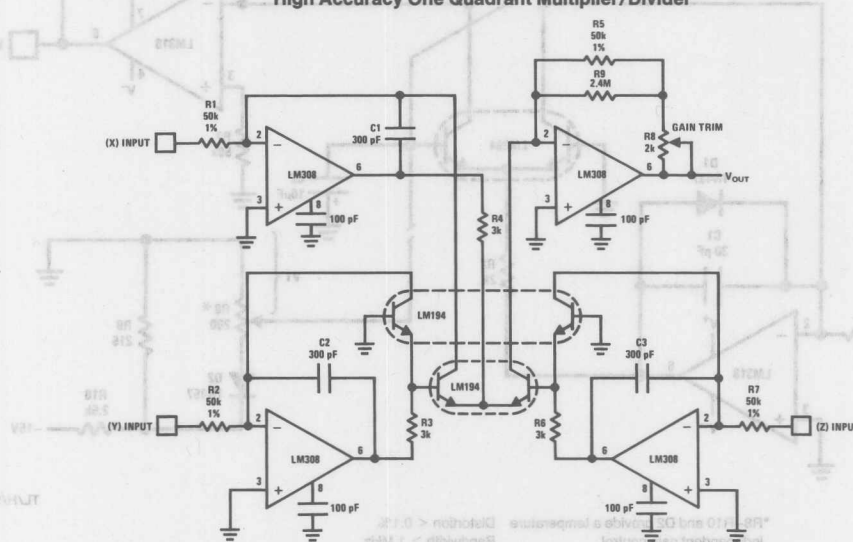
Typical Applications (Continued)

Precision Low Drift Operational Amplifier



TL/H/9241-5

High Accuracy One Quadrant Multiplier/Divider



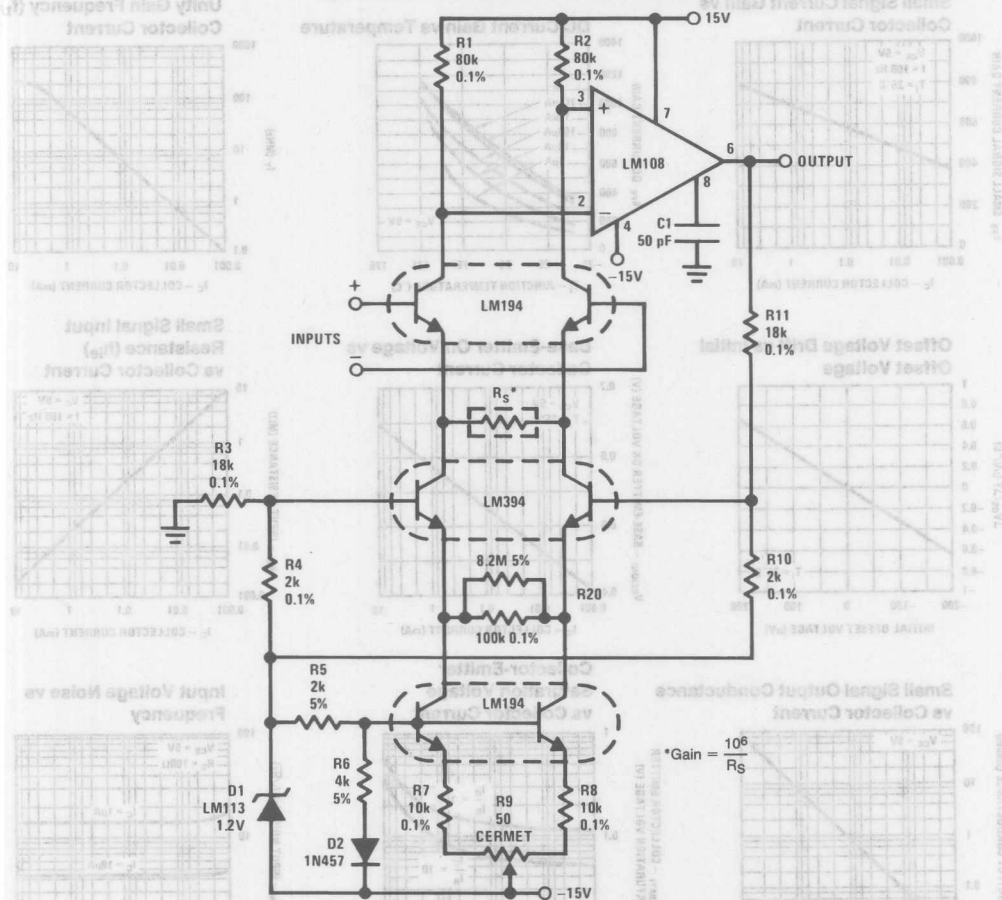
$$V_{OUT} = \frac{(X)(Y)}{(Z)}; \text{positive inputs only.}$$

*Typical linearity 0.1%

TL/H/9241-6

Typical Applications (Continued)

High Performance Instrumentation Amplifier

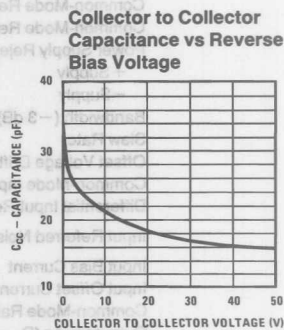
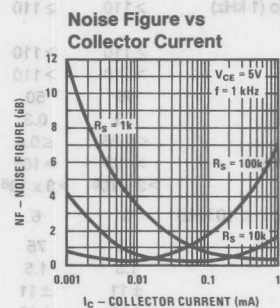
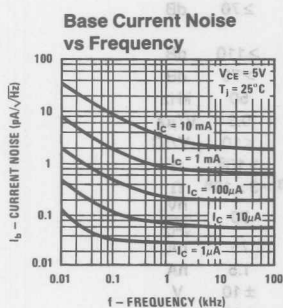
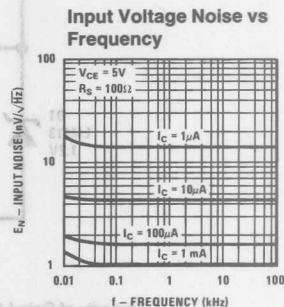
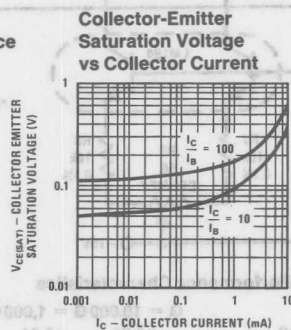
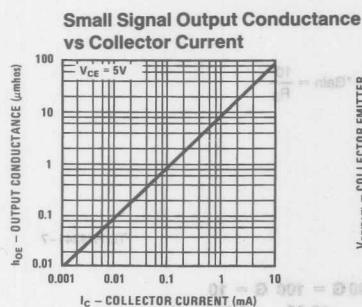
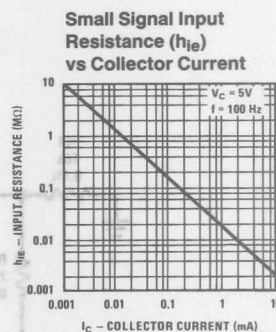
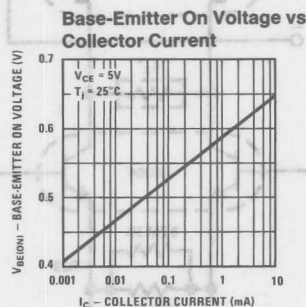
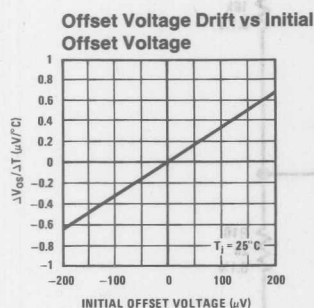
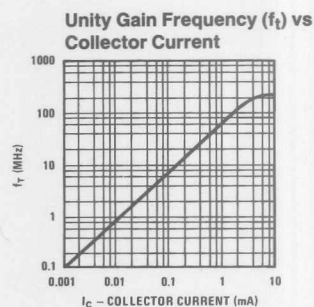
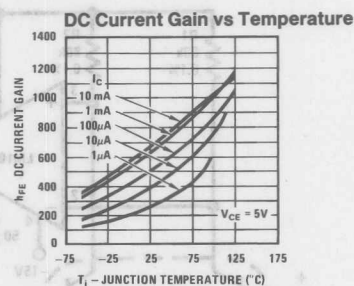
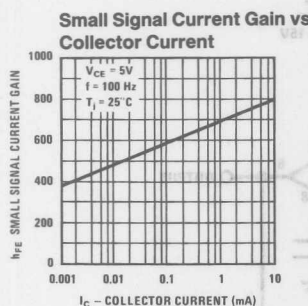


Performance Characteristics

| | $G = 10,000$ | $G = 1,000$ | $G = 100$ | $G = 10$ |
|--|-------------------|-------------------|-------------------|-------------------|
| Linearity of Gain ($\pm 10V$ Output) | ≤ 0.01 | ≤ 0.01 | ≤ 0.02 | ≤ 0.05 |
| Common-Mode Rejection Ratio (60 Hz) | ≥ 120 | ≥ 120 | ≥ 110 | ≥ 90 |
| Common-Mode Rejection Ratio (1 kHz) | ≥ 110 | ≥ 110 | ≥ 90 | ≥ 70 |
| Power Supply Rejection Ratio | | | | |
| + Supply | > 110 | > 110 | > 110 | > 110 |
| - Supply | > 110 | > 110 | > 90 | > 70 |
| Bandwidth (-3 dB) | 50 | 50 | 50 | 50 |
| Slew Rate | 0.3 | 0.3 | 0.3 | 0.3 |
| Offset Voltage Drift** | ≤ 0.25 | ≤ 0.4 | 2 | ≤ 10 |
| Common-Mode Input Resistance | $> 10^9$ | $> 10^9$ | $> 10^9$ | $> 10^9$ |
| Differential Input Resistance | $> 3 \times 10^8$ | $> 3 \times 10^8$ | $> 3 \times 10^8$ | $> 3 \times 10^8$ |
| Input Referred Noise ($100 \text{ Hz} \leq f \leq 10 \text{ kHz}$) | 5 | 6 | 12 | 70 |
| Input Bias Current | 75 | 75 | 75 | 75 |
| Input Offset Current | 1.5 | 1.5 | 1.5 | 1.5 |
| Common-Mode Range | ± 11 | ± 11 | ± 11 | ± 10 |
| Output Swing ($R_L = 10 \text{ k}\Omega$) | ± 13 | ± 13 | ± 13 | ± 13 |

**Assumes $\leq 5 \text{ ppm}/^\circ\text{C}$ tracking of resistors

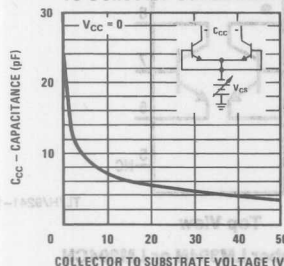
Typical Performance Characteristics



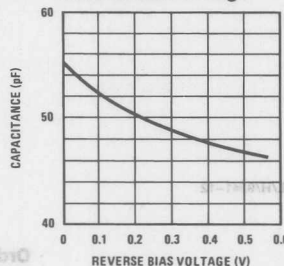
Typical Performance Characteristics (Continued)

LM194/LM394

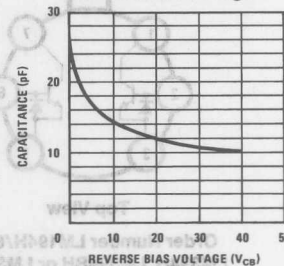
Collector to Collector Capacitance vs Collector-Substrate Voltage



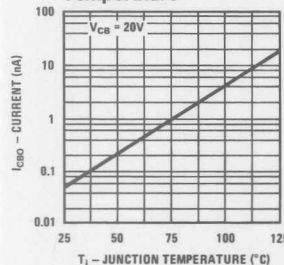
Emitter-Base Capacitance vs Reverse Bias Voltage



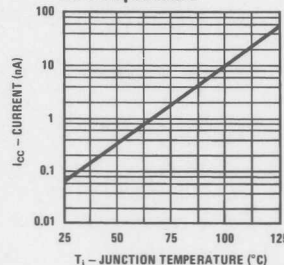
Collector-Base Capacitance vs Reverse Bias Voltage



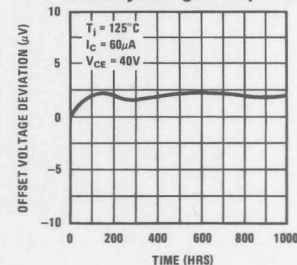
Collector-Base Leakage vs Temperature



Collector to Collector Leakage vs Temperature

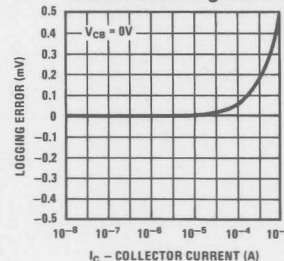


Offset Voltage Long Term Stability at High Temperature



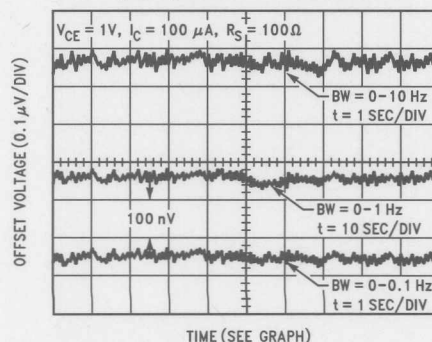
TL/H/9241-9

Emitter-Base Log Conformity



TL/H/9241-10

Low Frequency Noise of Differential Pair*



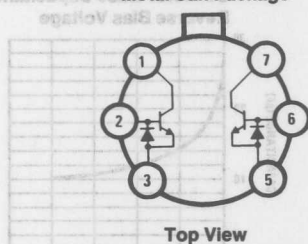
TL/H/9241-11

*Unit must be in still air environment so that differential lead temperature is held to less than 0.0003°C.

Connection Diagrams

Typical Performance Characteristics (Continued)

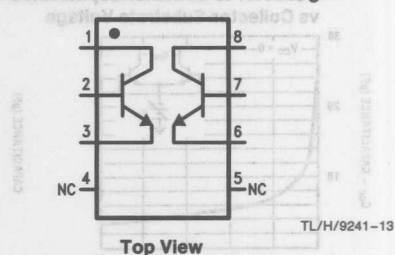
Metal Can Package



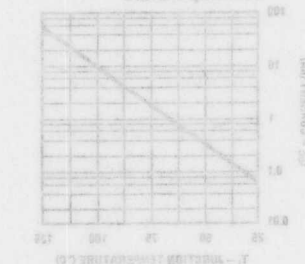
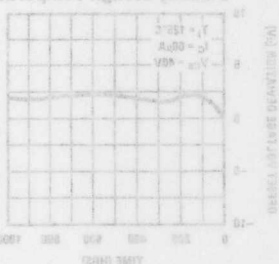
Order Number LM194H/883*,
LM394H, LM394BH or LM394CH
See NS Package Number H06C

Emitter-Bias Capacitance vs
Reverse Bias Voltage

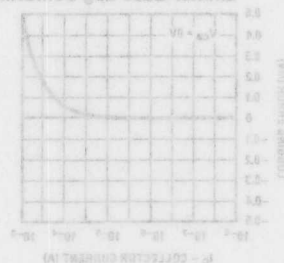
Dual-In-Line and Small Outline Packages



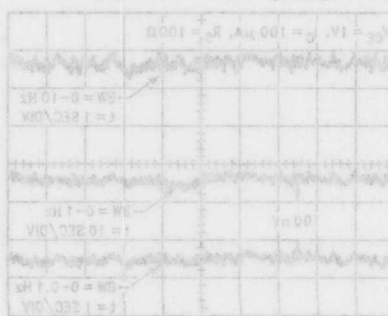
Order Number LM394N or LM394CN
See NS Package Number N08E

Collector to Collector Leakage
vs Temperature

Emitter-Bias Log Continuity



Low Frequency Noise at Differential Pair*



*Available per SMD #5962-8777701

LM195/LM395 Ultra Reliable Power Transistors

General Description

The LM195/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscilla-

tions. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply bypassing is recommended.

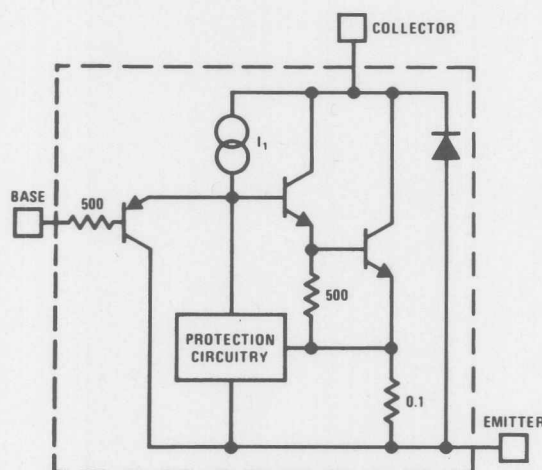
For low-power applications (under 100 mA), refer to the LM395 Ultra Reliable Power Transistor.

The LM195/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from -55°C to $+150^{\circ}\text{C}$ and the LM395 from 0°C to $+125^{\circ}\text{C}$.

Features

- Internal thermal limiting
- Greater than 1.0A output current
- 3.0 μA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL
- 100% electrical burn-in

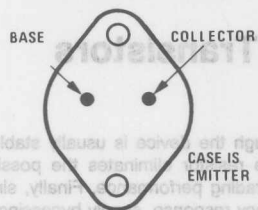
Simplified Circuit



TL/H/6009-1

Connection Diagrams

TO-3 Metal Can Package

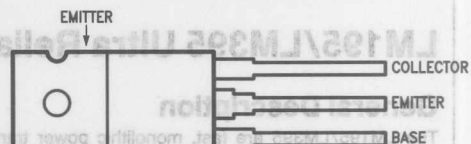


Bottom View

Order Number LM195K/883
See NS Package Number K02A

TL/H/6009-2

TO-220 Plastic Package

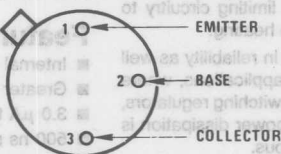


Top View

Order Number LM395T
See NS Package Number T03B

TL/H/6009-3

TO-5 Metal Can Package

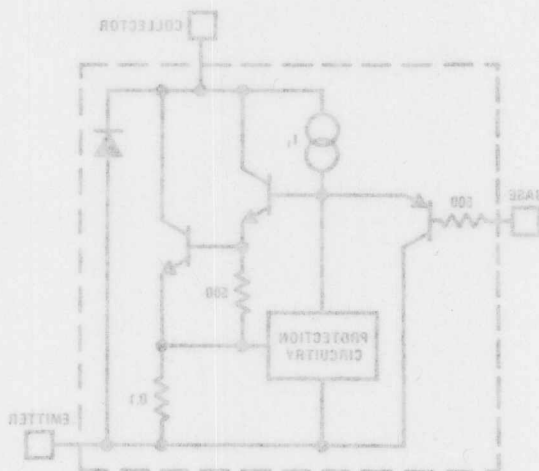


CASE IS EMITTER

Bottom View

Order Number LM195H/883
See NS Package Number H03B

TL/H/6009-4



TL/H/6009-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Collector to Emitter Voltage

LM195
LM395

Collector to Base Voltage

LM195
LM395

Base to Emitter Voltage (Forward)

LM195
LM395

Base to Emitter Voltage (Reverse)

20V

Collector Current

Internally Limited

Power Dissipation

Internally Limited

Operating Temperature Range

LM195
LM395

–55°C to +150°C
0°C to +125°C

Storage Temperature Range

–65°C to +150°C

Lead Temperature (Soldering, 10 sec.)

260°C

Preconditioning

100% Burn-In in Thermal Limit

Electrical Characteristics (Note 1)

| Parameter | Conditions | LM195 | | | LM395 | | | Units |
|--|---|-------|-----|-----|-------|-----|-----|--------------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Collector-Emitter Operating Voltage (Note 3) | $I_Q \leq I_C \leq I_{MAX}$ | | | 42 | | | 36 | V |
| Base to Emitter Breakdown Voltage | $0 \leq V_{CE} \leq V_{CEMAX}$ | 42 | | | 36 | 60 | | V |
| Collector Current TO-3, TO-220 TO-5 | $V_{CE} \leq 15V$ | 1.2 | 2.2 | | 1.0 | 2.2 | | A |
| | $V_{CE} \leq 7.0V$ | 1.2 | 1.8 | | 1.0 | 1.8 | | A |
| Saturation Voltage | $I_C \leq 1.0A, T_A = 25^\circ C$ | | 1.8 | 2.0 | | 1.8 | 2.2 | V |
| Base Current | $0 \leq I_C \leq I_{MAX}$ $0 \leq V_{CE} \leq V_{CEMAX}$ | | 3.0 | 5.0 | | 3.0 | 10 | μA |
| Quiescent Current (I_Q) | $V_{be} = 0$ $0 \leq V_{CE} \leq V_{CEMAX}$ | | 2.0 | 5.0 | | 2.0 | 10 | mA |
| Base to Emitter Voltage | $I_C = 1.0A, T_A = +25^\circ C$ | | 0.9 | | | 0.9 | | V |
| Switching Time | $V_{CE} = 36V, R_L = 36\Omega$, $T_A = 25^\circ C$ | | 500 | | | 500 | | ns |
| Thermal Resistance Junction to Case (Note 2) | TO-3 Package (K) | | 2.3 | 3.0 | | 2.3 | 3.0 | $^\circ C/W$ |
| | TO-5 Package (H) | | 12 | 15 | | 12 | 15 | $^\circ C/W$ |
| | TO-220 Package (T) | | | | | 4 | 6 | $^\circ C/W$ |

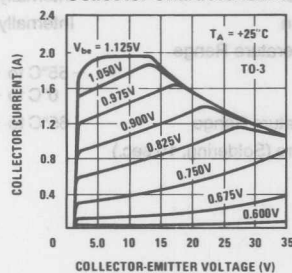
Note 1: Unless otherwise specified, these specifications apply for $-55^\circ C \leq T_J \leq +150^\circ C$ for the LM195 and $0^\circ C \leq +125^\circ C$ for the LM395.

Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about $+150^\circ C/W$, while that of the TO-3 package is $+35^\circ C/W$.

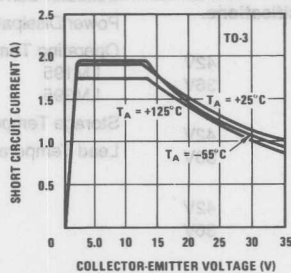
Note 3: Selected devices with higher breakdown available.

Note 4: Refer to RETS195H and RETS195K drawings of military LM195H and LM195K versions for specifications.

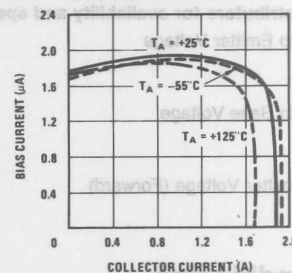
Collector Characteristics



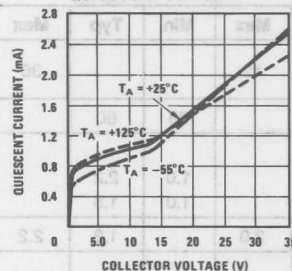
Short Circuit Current



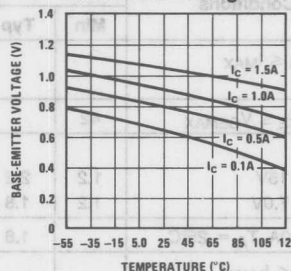
Bias Current



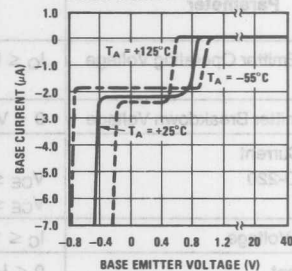
Quiescent Current



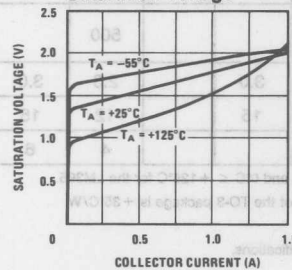
Base-Emitter Voltage



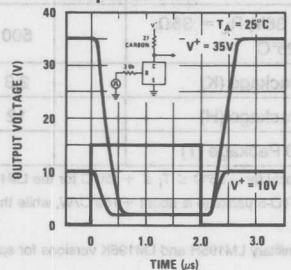
Base Current



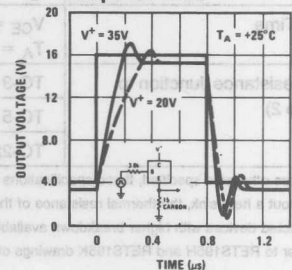
Saturation Voltage



Response Time

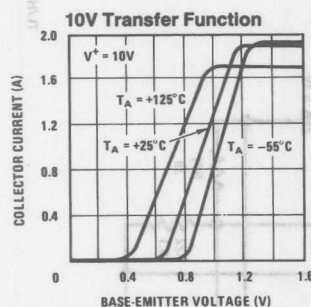


Response Time

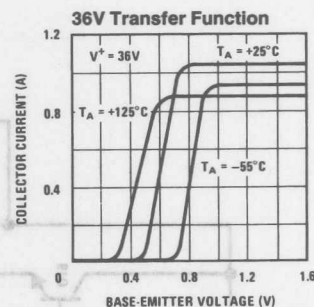


TL/H/6009-6

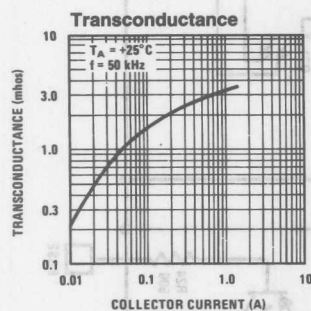
Typical Performance Characteristics (for K and T Packages) (Continued)



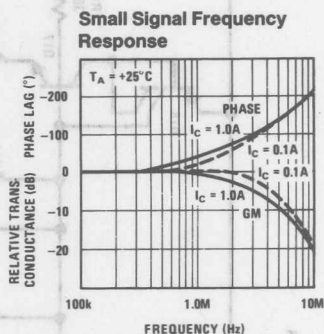
TL/H/6009-7



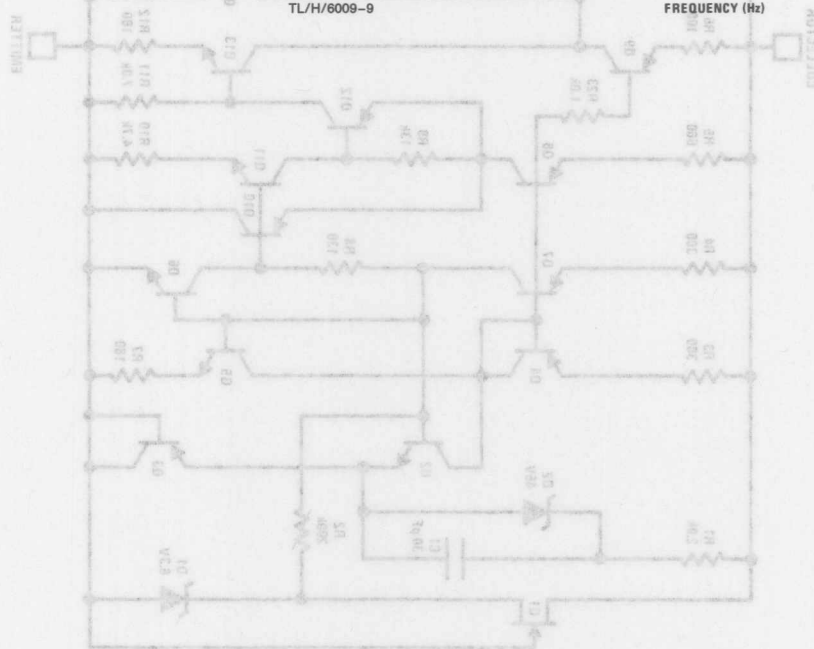
TL/H/6009-8



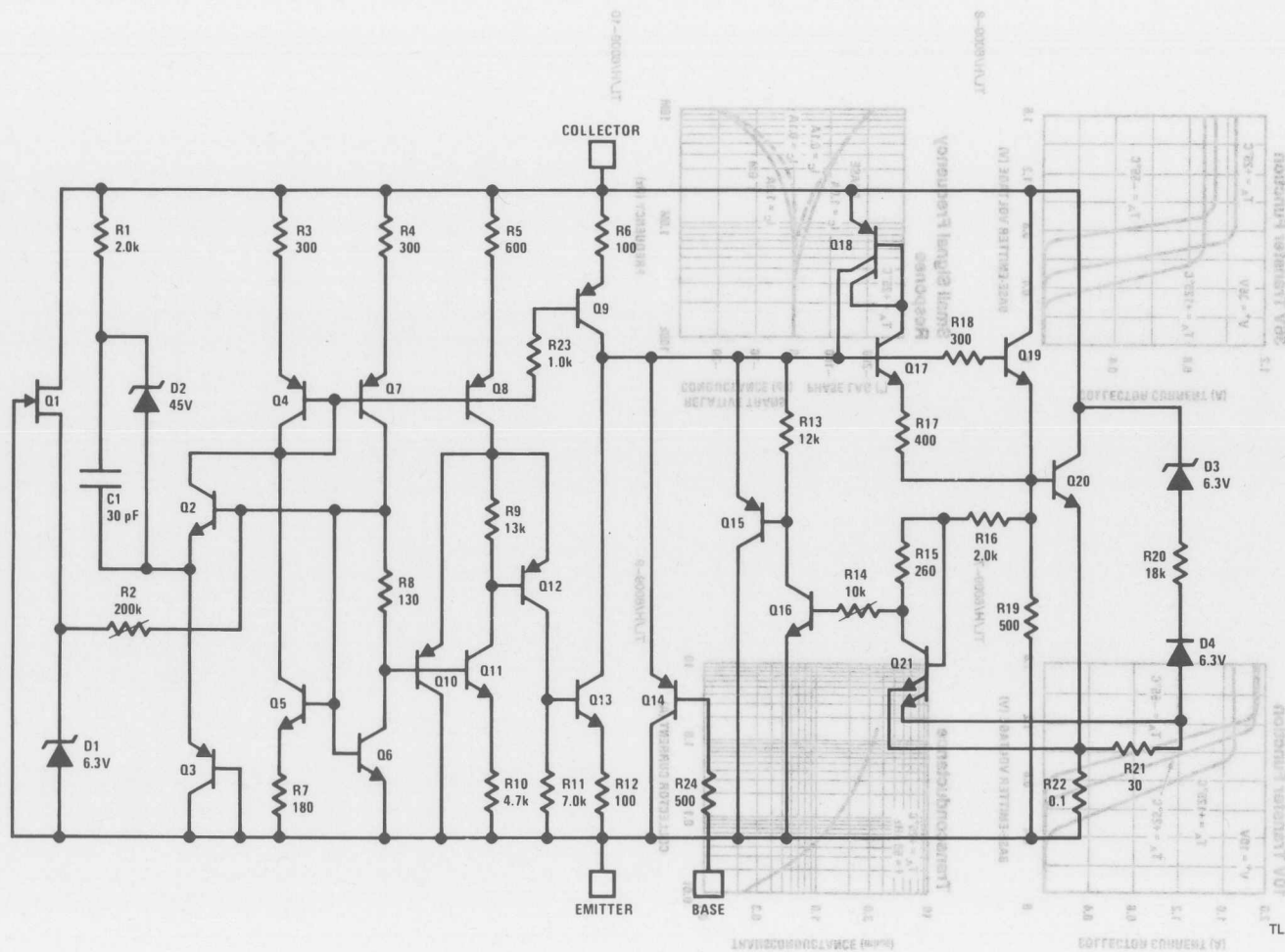
TL/H/6009-9



TL/H/6009-10



Schematic Diagram

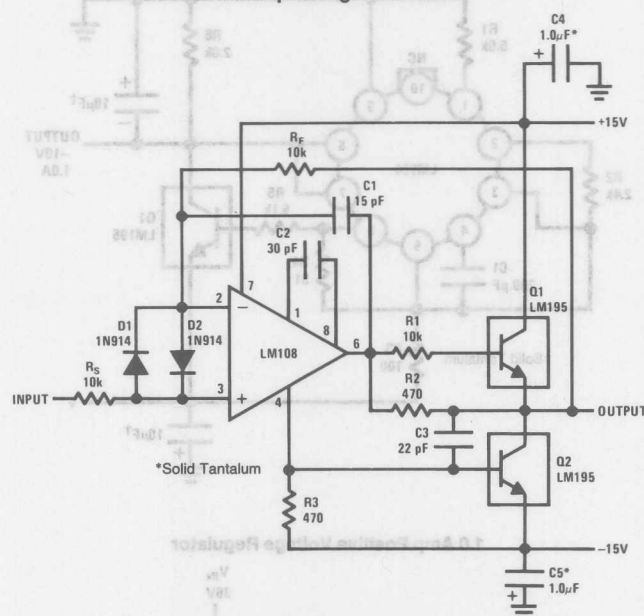


TL/H/6009-11

Typical Applications

Typical Applications (Continued)

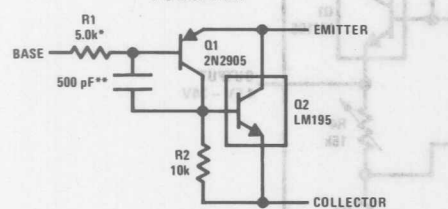
1.0 Amp Voltage Follower



*Solid Tantalum

TL/H/6009-12

Power PNP

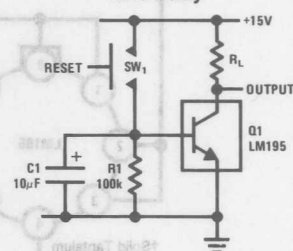


*Protects against excessive base drive

**Needed for stability

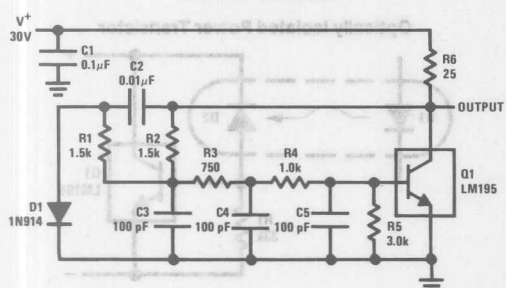
TL/H/6009-13

Time Delay



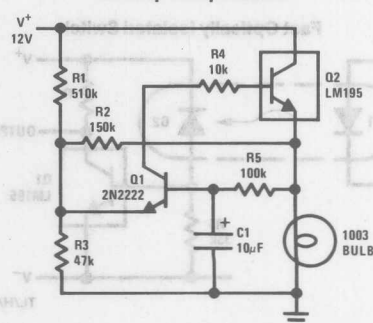
TL/H/6009-14

1.0 MHz Oscillator



TL/H/6009-15

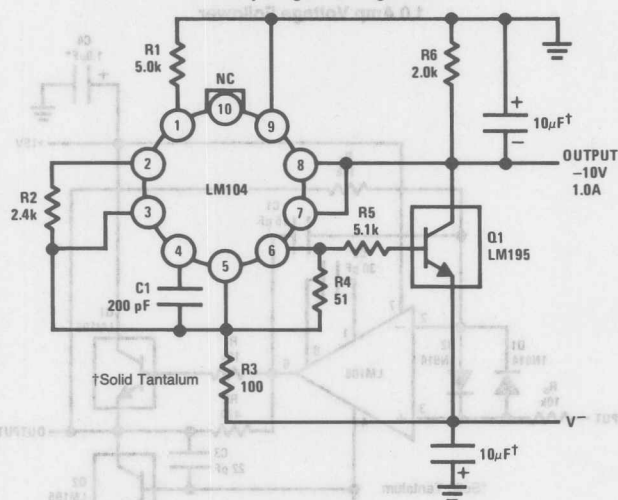
1.0 Amp Lamp Flasher



TL/H/6009-16

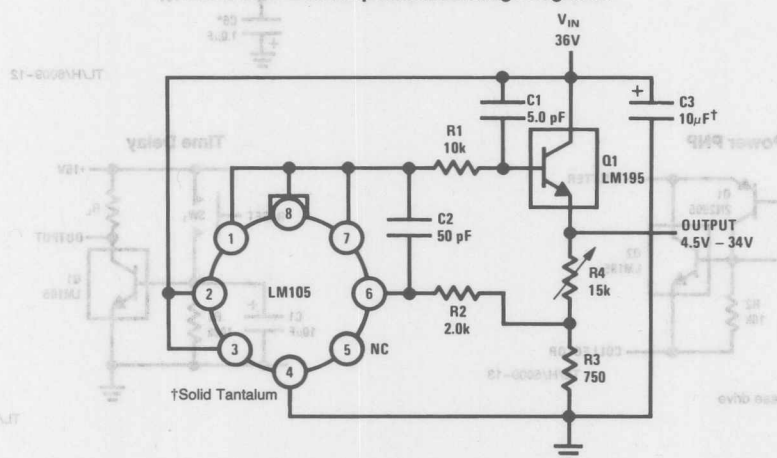
Typical Applications (Continued)

1.0 Amp Negative Regulator



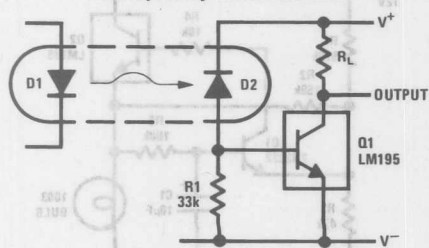
TL/H/6009-17

1.0 Amp Positive Voltage Regulator



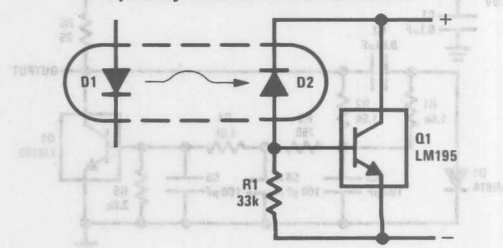
TL/H/6009-18

Fast Optically Isolated Switch



TL/H/6009-19

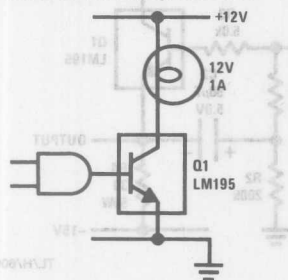
Optically Isolated Power Transistor



TL/H/6009-20

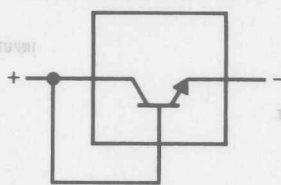
Typical Applications (Continued)

CMOS or TTL Lamp Interface



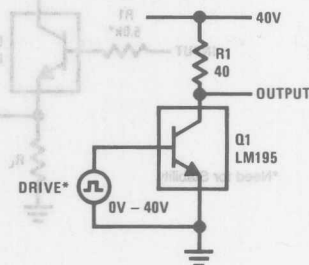
TL/H/6009-21

Two Terminal Current Limiter



TL/H/6009-22

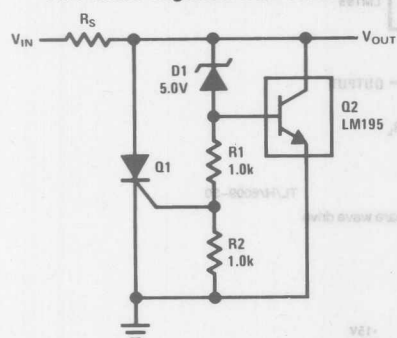
40V Switch



TL/H/6009-23

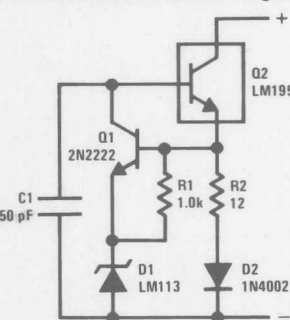
*Drive Voltage 0V to $\geq 10V \leq 42V$

6.0V Shunt Regulator with Crowbar



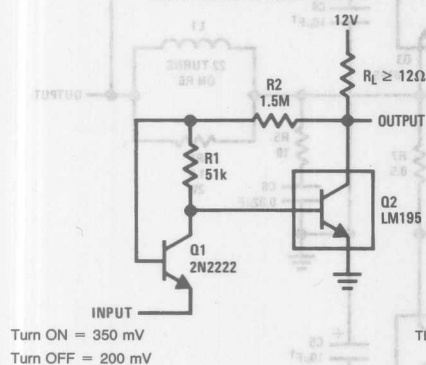
TL/H/6009-24

Two Terminal 100 mA Current Regulator



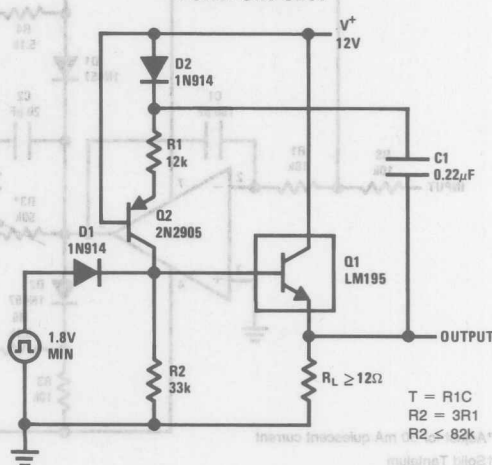
TL/H/6009-25

Low Level Power Switch

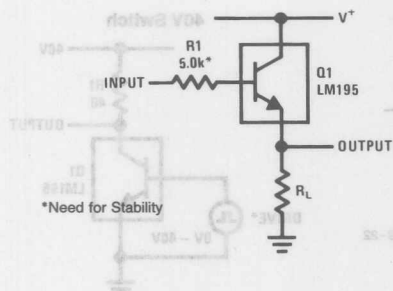
Turn ON = 350 mV
Turn OFF = 200 mV

TL/H/6009-26

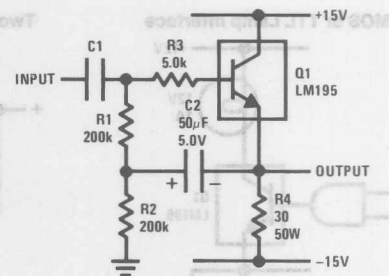
Power One-Shot

T = R1C
R2 = 3R1
R2 $\leq 82k\Omega$

TL/H/6009-27

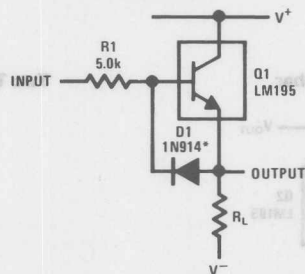


TL/H/6009-28



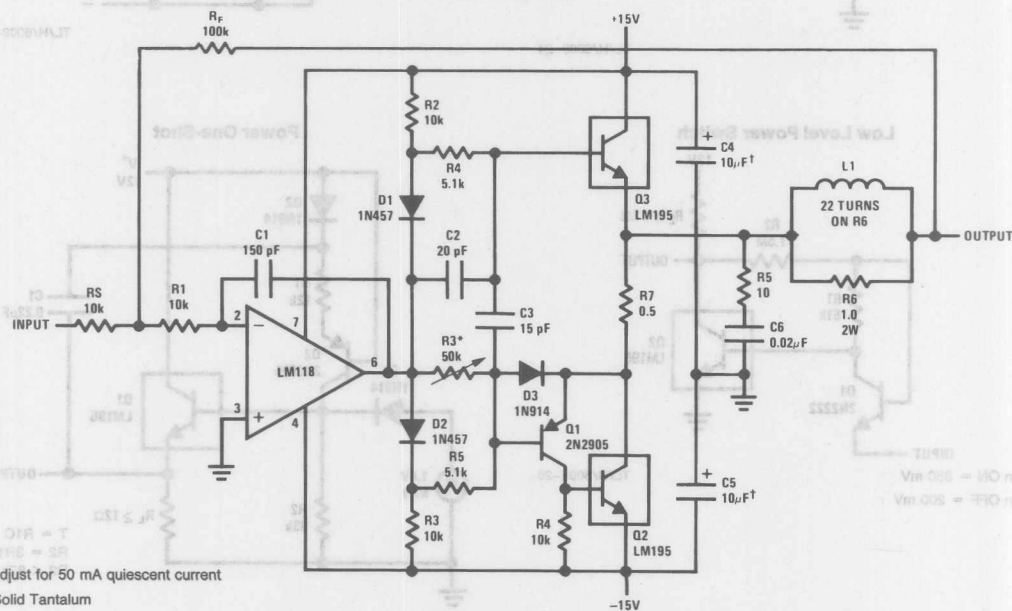
TL/H/6009-29

Fast Follower



TL/H/6009-30

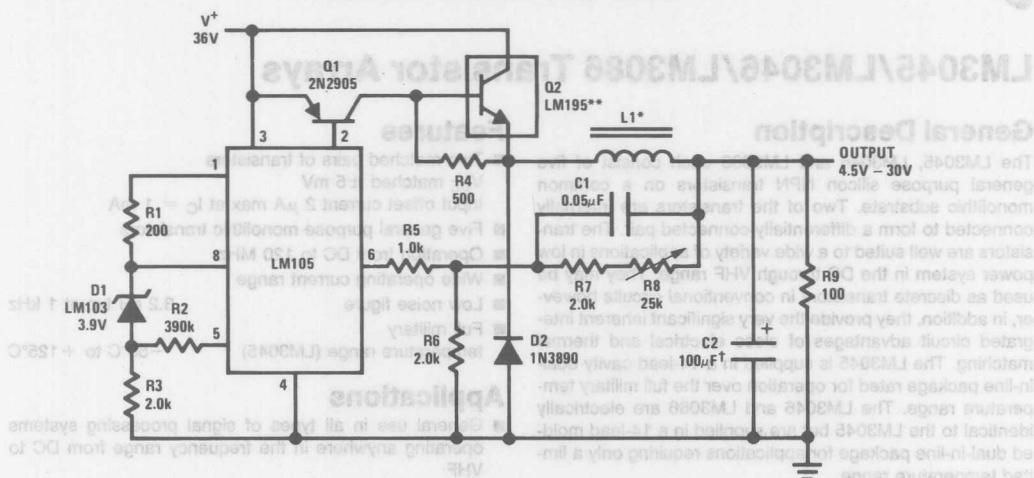
Power Op Amp



TL/H/6009-31

Typical Applications (Continued)

6.0 Amp Variable Output Switching Regulator



*Sixty turns wound on Arnold Type A-083081-2 core.

**Four devices in parallel

†Solid tantalum

TL/H/6009-32



LM3045/LM3046/LM3086 Transistor Arrays

General Description

The LM3045, LM3046 and LM3086 each consist of five general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the DC through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3045 is supplied in a 14-lead cavity dual-in-line package rated for operation over the full military temperature range. The LM3046 and LM3086 are electrically identical to the LM3045 but are supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

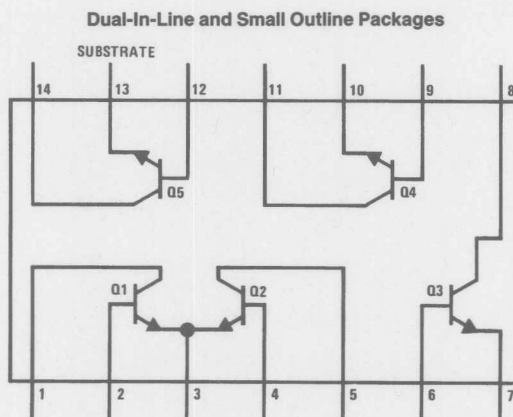
Features

- Two matched pairs of transistors
V_{BE} matched ± 5 mV
Input offset current $2 \mu\text{A}$ max at $I_C = 1 \text{ mA}$
- Five general purpose monolithic transistors
- Operation from DC to 120 MHz
- Wide operating current range
- Low noise figure
3.2 dB typ at 1 kHz
- Full military temperature range (LM3045)
 -55°C to $+125^\circ\text{C}$

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from DC to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Schematic and Connection Diagram



Top View

TL/H/7950-1

Order Number LM3045J, LM3046M, LM3046N or LM3086N
See NS Package Number J14A, M14A or N14A

| | Each Transistor | Total Package | Each Transistor | Total Package | Units |
|---|--|------------------|---|------------------|------------------------|
| Power Dissipation: | | | | | |
| $T_A = 25^{\circ}\text{C}$ | 300 | 750 | 300 | 750 | mW |
| $T_A = 25^{\circ}\text{C to } 55^{\circ}\text{C}$ | | | 300 | 750 | mW |
| $T_A > 55^{\circ}\text{C}$ | | | Derate at 6.67 | | mW/ $^{\circ}\text{C}$ |
| $T_A = 25^{\circ}\text{C to } 75^{\circ}\text{C}$ | 300 | 750 | | | mW |
| $T_A > 75^{\circ}\text{C}$ | Derate at 8 | | | | mW/ $^{\circ}\text{C}$ |
| Collector to Emitter Voltage, V_{CEO} | 15 | | 15 | | V |
| Collector to Base Voltage, V_{CBO} | 20 | | 20 | | V |
| Collector to Substrate Voltage, V_{CIO} (Note 1) | 20 | | 20 | | V |
| Emitter to Base Voltage, V_{EBO} | 5 | | 5 | | V |
| Collector Current, I_{C} | 50 | | 50 | | mA |
| Operating Temperature Range | $-55^{\circ}\text{C to } +125^{\circ}\text{C}$ | | $-40^{\circ}\text{C to } +85^{\circ}\text{C}$ | | |
| Storage Temperature Range | $-65^{\circ}\text{C to } +150^{\circ}\text{C}$ | | $-65^{\circ}\text{C to } +85^{\circ}\text{C}$ | | |
| Soldering Information | | | | | |
| Dual-In-Line Package Soldering (10 Sec.) | 260 $^{\circ}\text{C}$ | | 260 $^{\circ}\text{C}$ | | |
| Small Outline Package | | | | | |
| Vapor Phase (60 Seconds) | | | 215 $^{\circ}\text{C}$ | | |
| Infrared (15 Seconds) | | | 220 $^{\circ}\text{C}$ | | |
| See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices. | | | | | |

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Conditions | Limits | | | Limits | | | Units |
|--|--|----------------|-------|-----|--------|-------|-----|-------------------|
| | | LM3045, LM3046 | | | LM3086 | | | |
| | | Min | Typ | Max | Min | Typ | Max | |
| Collector to Base Breakdown Voltage ($V_{(BR)CBO}$) | $I_C = 10 \mu A, I_E = 0$ | 20 | 60 | | 20 | 60 | | V |
| Collector to Emitter Breakdown Voltage ($V_{(BR)CEO}$) | $I_C = 1 \text{ mA}, I_B = 0$ | 15 | 24 | | 15 | 24 | | V |
| Collector to Substrate Breakdown Voltage ($V_{(BR)CIO}$) | $I_C = 10 \mu A, I_{CI} = 0$ | 20 | 60 | | 20 | 60 | | V |
| Emitter to Base Breakdown Voltage ($V_{(BR)EBO}$) | $I_E 10 \mu A, I_C = 0$ | 5 | 7 | | 5 | 7 | | V |
| Collector Cutoff Current (I_{CBO}) | $V_{CB} = 10V, I_E = 0$ | | 0.002 | 40 | | 0.002 | 100 | nA |
| Collector Cutoff Current (I_{CEO}) | $V_{CE} = 10V, I_B = 0$ | | | 0.5 | | | 5 | μA |
| Static Forward Current Transfer Ratio (Static Beta) (h_{FE}) | $V_{CE} = 3V$ $\begin{cases} I_C = 10 \text{ mA} \\ I_C = 1 \text{ mA} \\ I_C = 10 \mu A \end{cases}$ | | 100 | | | 100 | | |
| | | 40 | 100 | | 40 | 100 | | |
| | | | 54 | | | 54 | | |
| Input Offset Current for Matched Pair Q_1 and Q_2 $ I_{O1} - I_{O2} $ | $V_{CE} = 3V, I_C = 1 \text{ mA}$ | | 0.3 | 2 | | | | μA |
| Base to Emitter Voltage (V_{BE}) | $V_{CE} = 3V$ $\begin{cases} I_E = 1 \text{ mA} \\ I_E = 10 \text{ mA} \end{cases}$ | | 0.715 | | | 0.715 | | V |
| | | | 0.800 | | | 0.800 | | |
| Magnitude of Input Offset Voltage for Differential Pair $ V_{BE1} - V_{BE2} $ | $V_{CE} = 3V, I_C = 1 \text{ mA}$ | | 0.45 | 5 | | | | mV |
| Magnitude of Input Offset Voltage for Isolated Transistors $ V_{BE3} - V_{BE4} , V_{BE4} - V_{BE5} , V_{BE5} - V_{BE3} $ | $V_{CE} = 3V, I_C = 1 \text{ mA}$ | | 0.45 | 5 | | | | mV |
| Temperature Coefficient of Base to Emitter Voltage $\left(\frac{\Delta V_{BE}}{\Delta T}\right)$ | $V_{CE} = 3V, I_C = 1 \text{ mA}$ | | -1.9 | | | -1.9 | | mV/ $^{\circ}C$ |
| Collector to Emitter Saturation Voltage ($V_{CE(SAT)}$) | $I_B = 1 \text{ mA}, I_C = 10 \text{ mA}$ | | 0.23 | | | 0.23 | | V |
| Temperature Coefficient of Input Offset Voltage $\left(\frac{\Delta V_{I0}}{\Delta T}\right)$ | $V_{CE} = 3V, I_C = 1 \text{ mA}$ | | 1.1 | | | | | $\mu V/^{\circ}C$ |

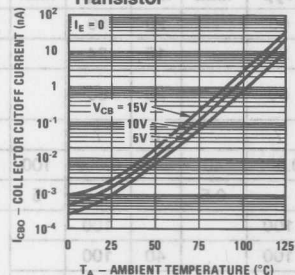
Note 1: The collector of each transistor of the LM3045, LM3046, and LM3086 is isolated from the substrate by an integral diode. The substrate (terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.

Electrical Characteristics (Continued)

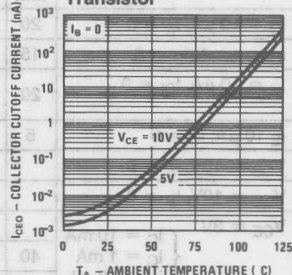
| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|-----|----------------------------------|-----|------------------|
| Low Frequency Noise Figure (NF) | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 100 \mu\text{A}, R_S = 1 \text{ k}\Omega$ | | 3.25 | | dB |
| LOW FREQUENCY, SMALL SIGNAL EQUIVALENT CIRCUIT CHARACTERISTICS | | | | | |
| Forward Current Transfer Ratio (h_{fe}) | $f = 1 \text{ kHz}, V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$ | | 110 (LM3045, LM3046) (LM3086) | | |
| Short Circuit Input Impedance (h_{ie}) | | | 3.5 | | $\text{k}\Omega$ |
| Open Circuit Output Impedance (h_{oe}) | | | 15.6 | | μmho |
| Open Circuit Reverse Voltage Transfer Ratio (h_{re}) | | | 1.8×10^{-4} | | |
| ADMITTANCE CHARACTERISTICS | | | | | |
| Forward Transfer Admittance (Y_{fe}) | $f = 1 \text{ MHz}, V_{CE} = 3 \text{ V}, I_C = 1 \text{ mA}$ | | $31 - j1.5$ | | |
| Input Admittance (Y_{ie}) | | | $0.3 + j0.04$ | | |
| Output Admittance (Y_{oe}) | | | $0.001 + j0.03$ | | |
| Reverse Transfer Admittance (Y_{re}) | | | See Curve | | |
| Gain Bandwidth Product (f_T) | $V_{CE} = 3 \text{ V}, I_C = 3 \text{ mA}$ | 300 | 550 | | |
| Emitter to Base Capacitance (C_{EB}) | $V_{EB} = 3 \text{ V}, I_E = 0$ | | 0.6 | | pF |
| Collector to Base Capacitance (C_{CB}) | $V_{CB} = 3 \text{ V}, I_C = 0$ | | 0.58 | | pF |
| Collector to Substrate Capacitance (C_{CI}) | $V_{CS} = 3 \text{ V}, I_C = 0$ | | 2.8 | | pF |

Typical Performance Characteristics

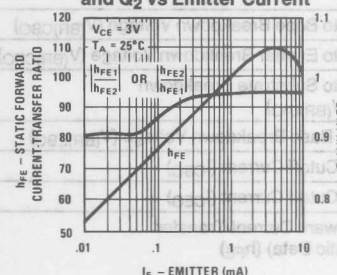
Typical Collector To Base Cutoff Current vs Ambient Temperature for Each Transistor



Typical Collector To Emitter Cutoff Current vs Ambient Temperature for Each Transistor

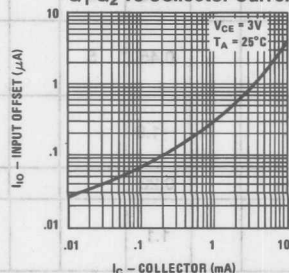


Typical Static Forward Current-Transfer Ratio and Beta Ratio for Transistors Q₁ and Q₂ vs Emitter Current

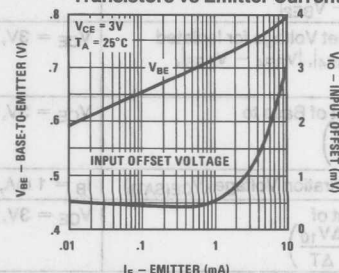


TL/H/7950-2

Typical Input Offset Current for Matched Transistor Pair Q₁ Q₂ vs Collector Current



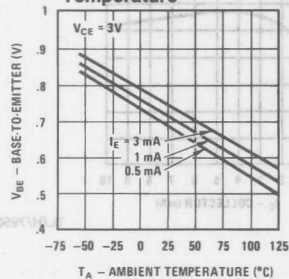
Typical Static Base To Emitter Voltage Characteristic and Input Offset Voltage for Differential Pair and Paired Isolated Transistors vs Emitter Current



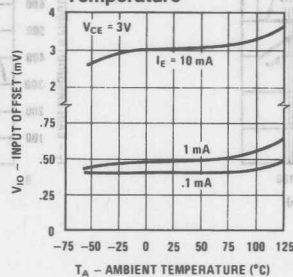
TL/H/7950-3

Typical Performance Characteristics (Continued)

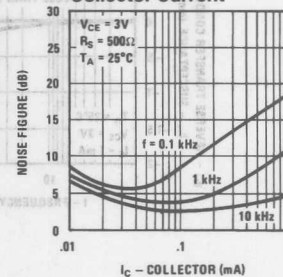
Typical Base To Emitter Voltage Characteristic for Each Transistor vs Ambient Temperature



Typical Input Offset Voltage Characteristics for Differential Pair and Paired Isolated Transistors vs Ambient Temperature

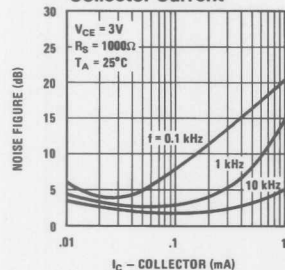


Typical Noise Figure vs Collector Current

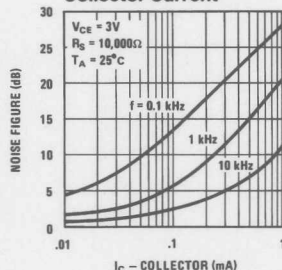


TL/H/7950-4

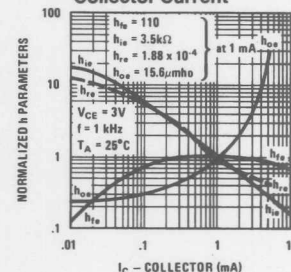
Typical Noise Figure vs Collector Current



Typical Noise Figure vs Collector Current

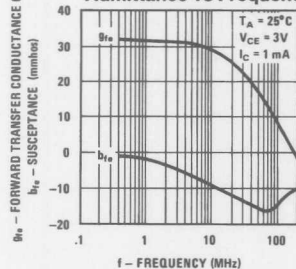


Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current

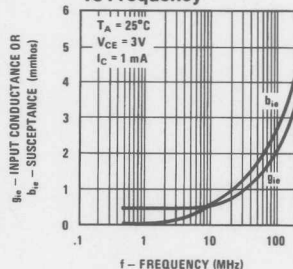


TL/H/7950-5

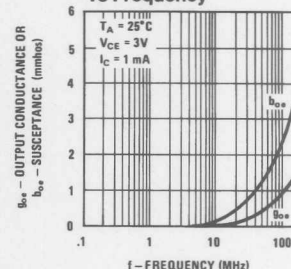
Typical Forward Transfer Admittance vs Frequency



Typical Input Admittance vs Frequency



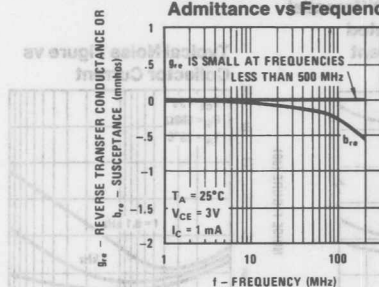
Typical Output Admittance vs Frequency



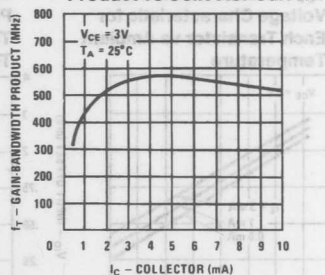
TL/H/7950-6

Typical Performance Characteristics (Continued)

Typical Reverse Transfer Admittance vs Frequency



Typical Gain-Bandwidth Product vs Collector Current



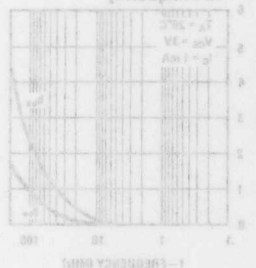
TL/H/7950-7

Typical Normalized Forward Current Transfer Ratio, Short Circuit Input Impedance, Open Circuit Output Impedance, and Open Circuit Reverse Voltage Transfer Ratio vs Collector Current



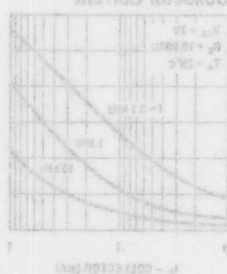
TL/H/7950-8

Typical Output Admittance vs Frequency

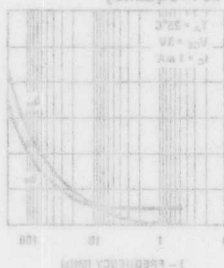


TL/H/7950-9

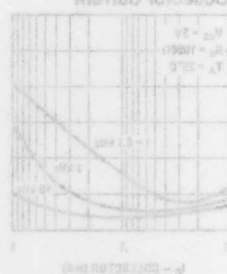
Typical Noise Figure vs Collector Current



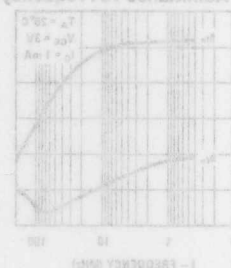
Typical Input Admittance vs Frequency



Typical Noise Figure vs Collector Current



Typical Forward Transfer Admittance vs Frequency



General Description

The LM3146 consists of five high voltage general purpose silicon NPN transistors on a common monolithic substrate. Two of the transistors are internally connected to form a differentially-connected pair. The transistors are well suited to a wide variety of applications in low power system in the dc through VHF range. They may be used as discrete transistors in conventional circuits however, in addition, they provide the very significant inherent integrated circuit advantages of close electrical and thermal matching. The LM3146 is supplied in a 14-lead molded dual-in-line package for applications requiring only a limited temperature range.

Features

- High voltage matched pairs of transistors, V_{BE} matched ± 5 mV, input offset current $2 \mu\text{A}$ max at $I_C = 1$ mA
- Five general purpose monolithic transistors
- Operation from dc to 120 MHz
- Wide operating current range
- Low noise figure 3.2 dB typ at 1 kHz

Applications

- General use in all types of signal processing systems operating anywhere in the frequency range from dc to VHF
- Custom designed differential amplifiers
- Temperature compensated amplifiers

Connection Diagram

Top View

Order Number LM3146M or LM3146N
See NS Package Number M14A or N14A

TL/H/7959-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | LM3146 | Units |
|--|----------------|----------------------|
| Power Dissipation: Each transistor | | |
| $T_A = 25^\circ\text{C}$ to 55°C | 300 | mW |
| $T_A > 55^\circ\text{C}$ | Derate at 6.67 | mW/ $^\circ\text{C}$ |
| Power Dissipation: Total Package | | |
| $T_A = 25^\circ\text{C}$ | 500 | mW |
| $T_A > 25^\circ\text{C}$ | Derate at 6.67 | mW/ $^\circ\text{C}$ |
| Collector to Emitter Voltage, V_{CEO} | 30 | V |
| Collector to Base Voltage, V_{CBO} | 40 | V |
| Collector to Substrate Voltage, V_{CIO} (Note 1) | 40 | V |
| Emitter to Base Voltage, V_{EBO} (Note 2) | 5 | V |
| Collector to Current, I_C | 50 | mA |
| Operating Temperature Range | -40 to +85 | $^\circ\text{C}$ |
| Storage Temperature Range | -65 to +150 | $^\circ\text{C}$ |

Soldering Information

| | |
|--------------------------|----------------------|
| Dual-In-Line Package | |
| Soldering (10 seconds) | 260 $^\circ\text{C}$ |
| Small Outline Package | |
| Vapor Phase (60 seconds) | 215 $^\circ\text{C}$ |
| Infrared (15 seconds) | 220 $^\circ\text{C}$ |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

DC Electrical Characteristics $T_A = 25^\circ\text{C}$

| Symbol | Parameter | Conditions | Limits | | | Units |
|--------------------------|---|--|--------|-----------------|------|------------------------------|
| | | | Min | Typ | Max | |
| $V_{(BR)CBO}$ | Collector to Base Breakdown Voltage | $I_C = 10\text{ }\mu\text{A}$, $I_E = 0$ | 40 | 72 | | V |
| $V_{(BR)CEO}$ | Collector to Emitter Breakdown Voltage | $I_C = 1\text{ mA}$, $I_B = 0$ | 30 | 56 | | V |
| $V_{(BR)CIO}$ | Collector to Substrate Breakdown Voltage | $I_{C1} = 10\text{ }\mu\text{A}$, $I_B = 0$, $I_E = 0$ | 40 | 72 | | V |
| $V_{(BR)EBO}$ | Emitter to Base Breakdown Voltage (Note 2) | $I_C = 0$, $I_E = 10\text{ }\mu\text{A}$ | 5 | 7 | | V |
| I_{CBO} | Collector Cutoff Current | $V_{CB} = 10\text{ V}$, $I_E = 0$ | | 0.002 | 100 | nA |
| I_{CEO} | Collector Cutoff Current | $V_{CE} = 10\text{ V}$, $I_B = 0$ | | (Note 3) | 5 | μA |
| h_{FE} | Static Forward Current Transfer Ratio (Static Beta) | $I_C = 10\text{ mA}$, $V_{CE} = 5\text{ V}$ $I_C = 1\text{ mA}$, $V_{CE} = 5\text{ V}$ $I_C = 10\text{ }\mu\text{A}$, $V_{CE} = 5\text{ V}$ | 30 | 85 100 90 | | |
| $I_{B1} - I_{B2}$ | Input Offset Current for Matched Pair Q1 and Q2 | $I_{C1} = I_{C2} = 1\text{ mA}$, $V_{CE} = 5\text{ V}$ | | 0.3 | 2 | μA |
| V_{BE} | Base to Emitter Voltage | $I_C = 1\text{ mA}$, $V_{CE} = 3\text{ V}$ | 0.63 | 0.73 | 0.83 | V |
| $V_{BE1} - V_{BE2}$ | Magnitude of Input Offset Voltage for Differential Pair | $V_{CE} = 5\text{ V}$, $I_E = 1\text{ mA}$ | | 0.48 | 5 | mV |
| $\Delta V_{BE}/\Delta T$ | Temperature Coefficient of Base to Emitter Voltage | $V_{CE} = 5\text{ V}$, $I_E = 1\text{ mA}$ | | -1.9 | | mV/ $^\circ\text{C}$ |
| $V_{CE(SAT)}$ | Collector to Emitter Saturation Voltage | $I_C = 10\text{ mA}$, $I_B = 1\text{ mA}$ | | 0.33 | | V |
| $\Delta V_{10}/\Delta T$ | Temperature Coefficient of Input Offset Voltage | $I_C = 1\text{ mA}$, $V_{CE} = 5\text{ V}$ | | 1.1 | | $\mu\text{V}/^\circ\text{C}$ |

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

Note 2: If the transistors are forced into zener breakdown ($V_{(BR)EBO}$), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.

AC Electrical Characteristics

| Symbol | Parameter | Conditions | Limits | | | Units |
|----------|------------------------------------|---|--------|------|-----|-------|
| | | | Min | Typ | Max | |
| NF | Low Frequency Noise Figure | $f = 1 \text{ kHz}$, $V_{CE} = 5 \text{ V}$, $I_C = 100 \mu\text{A}$, $R_S = 1 \text{ k}\Omega$ | | 3.25 | | dB |
| f_T | Gain Bandwidth Product | $V_{CE} = 5 \text{ V}$, $I_C = 3 \text{ mA}$ | 300 | 500 | | MHz |
| C_{EB} | Emitter to Base Capacitance | $V_{EB} = 5 \text{ V}$, $I_E = 0$ | | 0.70 | | pF |
| C_{CB} | Collector to Base Capacitance | $V_{CB} = 5 \text{ V}$, $I_C = 0$ | | 0.37 | | pF |
| C_{CI} | Collector to Substrate Capacitance | $V_{CI} = 5 \text{ V}$, $I_C = 0$ | | 2.2 | | pF |

Low Frequency, Small Signal Equivalent Circuit Characteristics

| | | | | | | |
|----------|---|--|--|----------------------|--|------------------|
| h_{fe} | Forward Current Transfer Ratio | $f = 1 \text{ kHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | 100 | | |
| h_{ie} | Short Circuit Input Impedance | $f = 1 \text{ kHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | 3.5 | | $\text{k}\Omega$ |
| h_{oe} | Open Circuit Output Impedance | $f = 1 \text{ kHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | 15.6 | | μmho |
| h_{re} | Open Circuit Reverse Voltage Transfer Ratio | $f = 1 \text{ kHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | 1.8×10^{-4} | | |

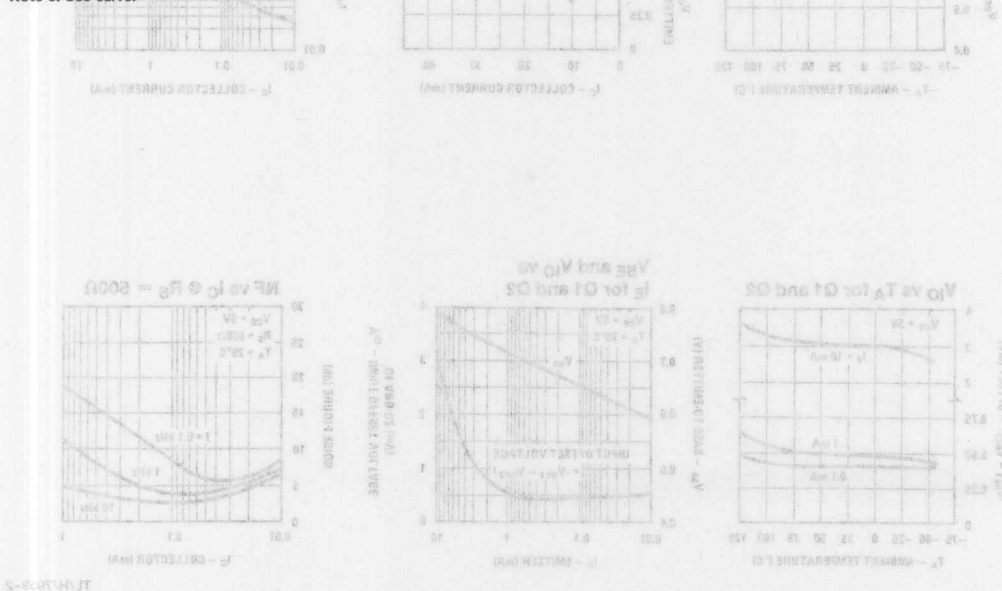
Admittance Characteristics

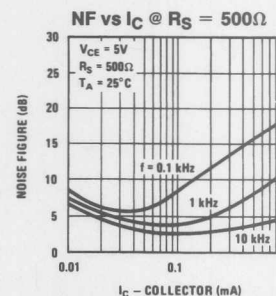
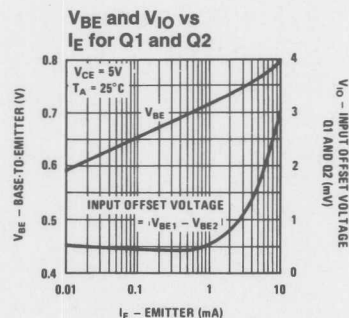
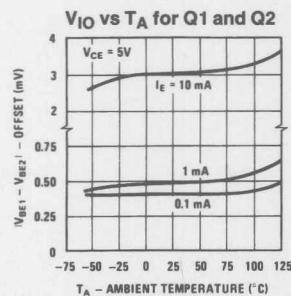
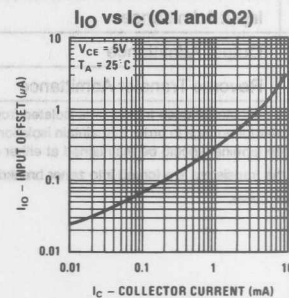
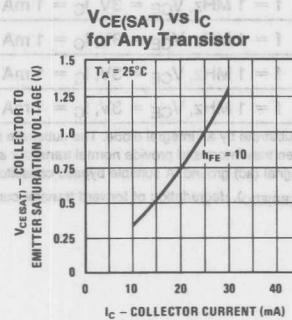
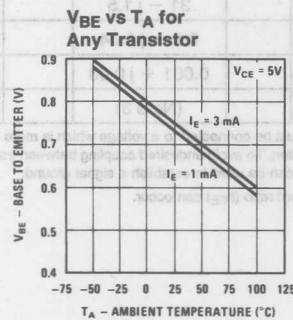
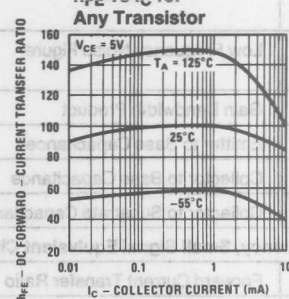
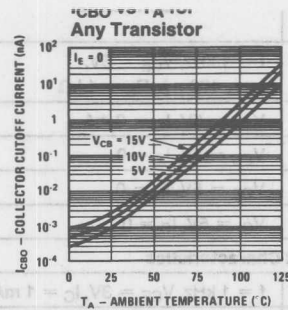
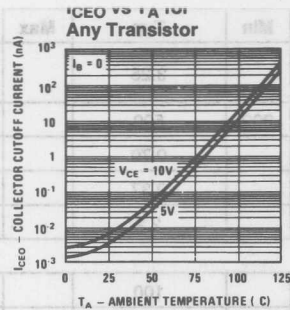
| | | | | | | |
|----------|-----------------------------|---|--|------------------|--|---------------|
| Y_{fe} | Forward Transfer Admittance | $f = 1 \text{ MHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | $31 - j 1.5$ | | mmho |
| Y_{ie} | Input Admittance | $f = 1 \text{ MHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | $0.3 + j 0.04$ | | mmho |
| Y_{oe} | Output Admittance | $f = 1 \text{ MHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | $0.001 + j 0.03$ | | mmho |
| Y_{re} | Reverse Transfer Admittance | $f = 1 \text{ MHz}$, $V_{CE} = 3 \text{ V}$, $I_C = 1 \text{ mA}$ | | (Note 3) | | mmho |

Note 1: The collector of each transistor is isolated from the substrate by an integral diode. The substrate must be connected to a voltage which is more negative than any collector voltage in order to maintain isolation between transistors and provide normal transistor action. To avoid undesired coupling between transistors, the substrate terminal should be maintained at either dc or signal (ac) ground. A suitable bypass capacitor can be used to establish a signal ground.

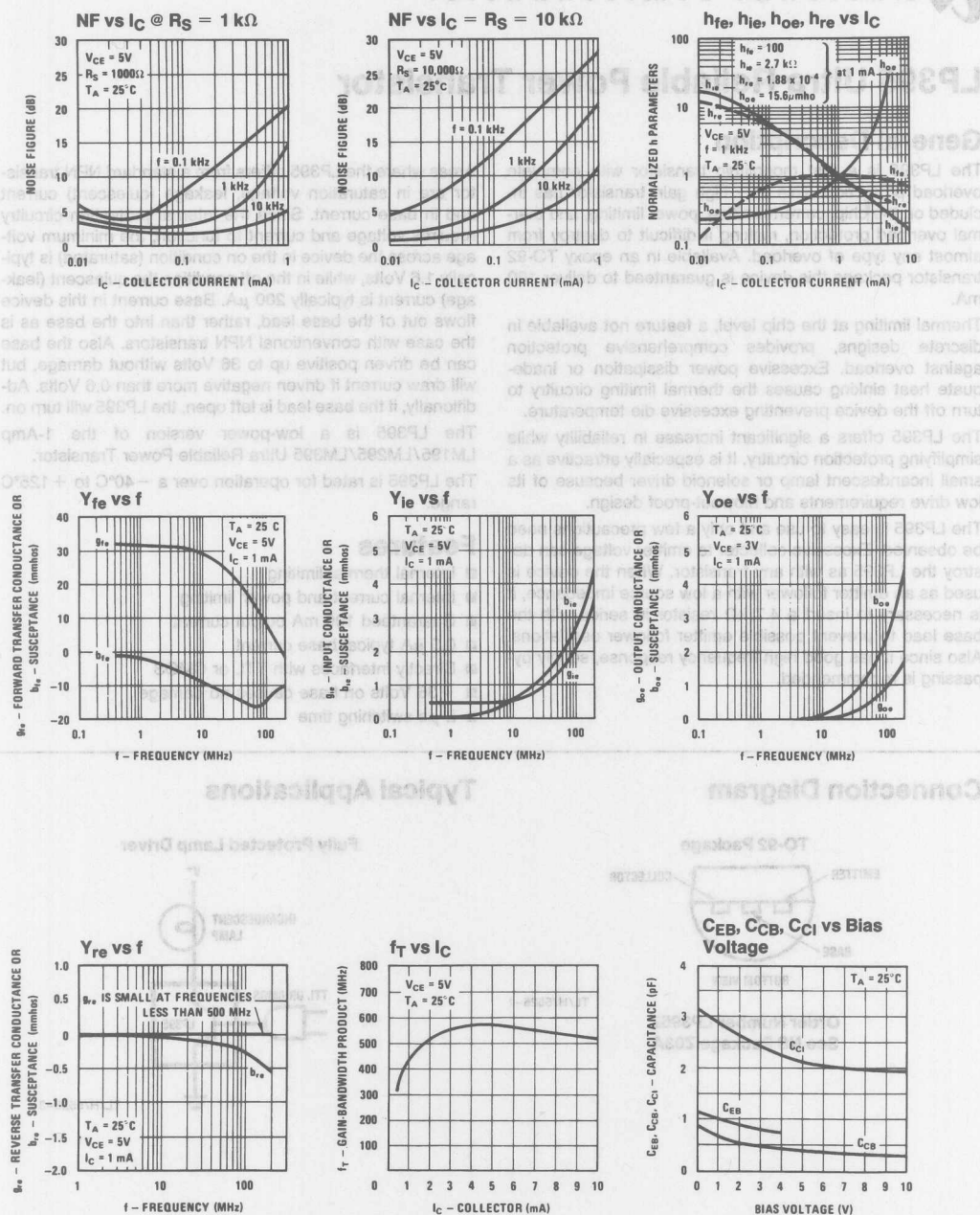
Note 2: If the transistors are forced into zener breakdown (V_{BER}), degradation of forward transfer current ratio (h_{FE}) can occur.

Note 3: See curve.





Typical Performance Characteristics (Continued)



TL/H/7959-3



LP395 Ultra Reliable Power Transistor

General Description

The LP395 is a fast monolithic transistor with complete overload protection. This very high gain transistor has included on the chip, current limiting, power limiting, and thermal overload protection, making it difficult to destroy from almost any type of overload. Available in an epoxy TO-92 transistor package this device is guaranteed to deliver 100 mA.

Thermal limiting at the chip level, a feature not available in discrete designs, provides comprehensive protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive die temperature.

The LP395 offers a significant increase in reliability while simplifying protection circuitry. It is especially attractive as a small incandescent lamp or solenoid driver because of its low drive requirements and blowout-proof design.

The LP395 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LP395 as with any transistor. When the device is used as an emitter follower with a low source impedance, it is necessary to insert a 4.7 kΩ resistor in series with the base lead to prevent possible emitter follower oscillations. Also since it has good high frequency response, supply bypassing is recommended.

Areas where the LP395 differs from a standard NPN transistor are in saturation voltage, leakage (quiescent) current and in base current. Since the internal protection circuitry requires voltage and current to function, the minimum voltage across the device in the on condition (saturated) is typically 1.6 Volts, while in the off condition the quiescent (leakage) current is typically 200 μA. Base current in this device flows out of the base lead, rather than into the base as is the case with conventional NPN transistors. Also the base can be driven positive up to 36 Volts without damage, but will draw current if driven negative more than 0.6 Volts. Additionally, if the base lead is left open, the LP395 will turn on.

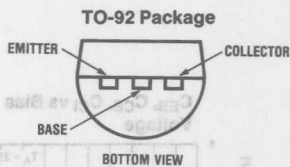
The LP395 is a low-power version of the 1-Amp LM195/LM295/LM395 Ultra Reliable Power Transistor.

The LP395 is rated for operation over a -40°C to +125°C range.

Features

- Internal thermal limiting
- Internal current and power limiting
- Guaranteed 100 mA output current
- 0.5 μA typical base current
- Directly interfaces with TTL or CMOS
- +36 Volts on base causes no damage
- 2 μs switching time

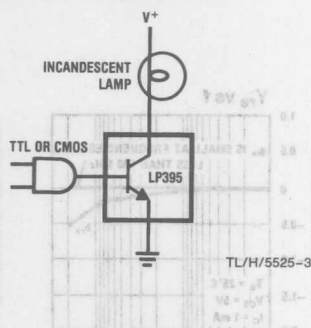
Connection Diagram



Order Number LP395Z
See NS Package Z03A

Typical Applications

Fully Protected Lamp Driver



Absolute Maximum Ratings

| | | | |
|-----------------------------------|-------|------------------------------------|--------------------|
| Collector to Emitter Voltage | 36V | Collector Current Limit | Internally Limited |
| Collector to Base Voltage | 36V | Power Dissipation | Internally Limited |
| Base to Emitter Voltage (Forward) | 36V | Operating Temperature Range | -40°C to +125°C |
| Base to Emitter Voltage (Reverse) | 10V | Storage Temperature Range | -65°C to +150°C |
| Base to Emitter Current (Reverse) | 20 mA | Lead Temp. (Soldering, 10 seconds) | 260°C |

Electrical Characteristics

| Symbol | Parameter | Conditions | Typical | Tested Limit (Note 2) | Design Limit (Note 3) | Units (Limit) |
|----------------------|---|---|-----------------|-----------------------|-----------------------|-------------------------------|
| V_{CE} | Collector to Emitter Operating Voltage | $0.5 \text{ mA} \leq I_C \leq 100 \text{ mA}$ | | 36 | 36 (Note 1) | V(Max) |
| I_{CL} | Collector Current Limit (Note 4) | $V_{BE} = 2V, V_{CE} = 36V$ $V_{BE} = 2V, V_{CE} = 15V$ $V_{BE} = 2V, 2V \leq V_{CE} \leq 6V$ | 45 90 130 | 25 60 100 | 20 50 100 | mA(Min) mA(Min) mA(Min) |
| I_B | Base Current | $0 \leq I_C \leq 100 \text{ mA}$ | -0.3 | -2.0 | -2.5 | $\mu\text{A}(\text{Max})$ |
| I_Q | Quiescent Current | $V_{BE} = 0V, 0 \leq V_{CE} \leq 36V$ | 0.24 | 0.50 | 0.60 | mA(Max) |
| $V_{CE(\text{SAT})}$ | Saturation Voltage | $V_{BE} = 2V, I_C = 100 \text{ mA}$ | 1.82 | 2.00 | 2.10 | V(Max) |
| BV_{BE} | Base to Emitter Break-down Voltage (Note 4) | $0 \leq V_{CE} \leq 36V, I_B = 2 \mu\text{A}$ | | 36 | 36 | V(Min) |
| V_{BE} | Base to Emitter Voltage (Note 5) | $I_C = 5 \text{ mA}$ | 0.69 | 0.79 | 0.90 | V(Max) |
| | | $I_C = 100 \text{ mA}$ (Note 4) | 1.02 | | 1.40 | V(Max) |
| t_S | Switching Time | $V_{CE} = 20V, R_L = 200\Omega$ $V_{BE} = 0V, +2V, 0V$ | 2 | | | μs |
| θ_{JA} | Thermal Resistance Junction to Ambient | 0.4" leads soldered to printed circuit board | 150 | | 180 | °C/W (Max) |
| | | 0.125" leads soldered to printed circuit board | 130 | | 160 | °C/W (Max) |

Note 1: Parameters identified with **boldface type** apply at temp. extremes. All other numbers, unless noted apply at +25°C.

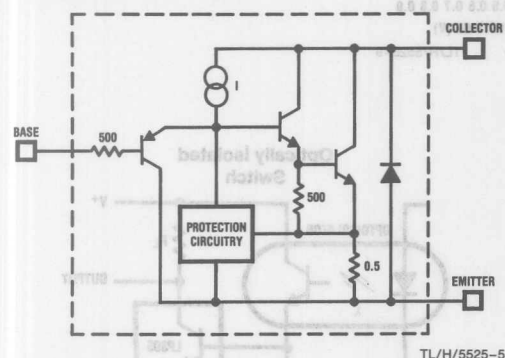
Note 2: Guaranteed and 100% production tested.

Note 3: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 4: These numbers apply for pulse testing with a low duty cycle.

Note 5: Base positive with respect to emitter.

Simplified Circuit

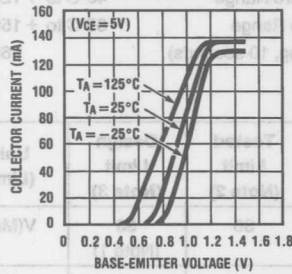


Applications Information

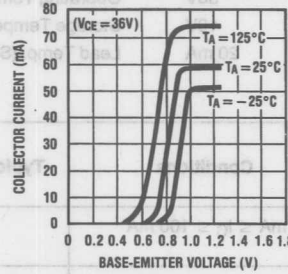
One failure mode incandescent lamps may experience is one in which the filament resistance drops to a very low value before it actually blows out. This is especially rough on most solid-state lamp drivers and in most cases a lamp failure of this type will also cause the lamp driver to fail. Because of its high gain and blowout-proof design, the LP395 is an ideal candidate for reliably driving small incandescent lamps. Additionally, the current limiting characteristics of the LP395 are advantageous as it serves to limit the cold filament inrush current, thus increasing lamp life.

Typical Performance Characteristics

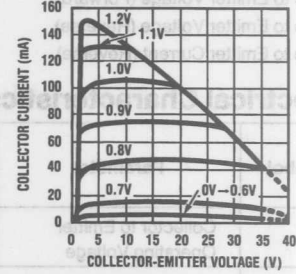
5 Volt Transfer Function



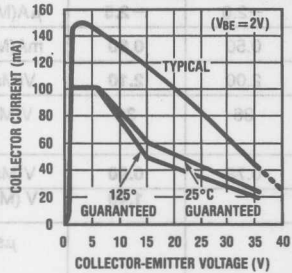
36 Volt Transfer Function



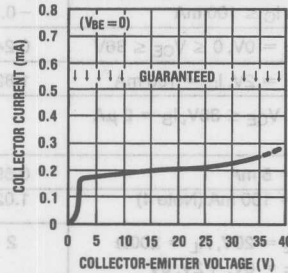
Collector Characteristics



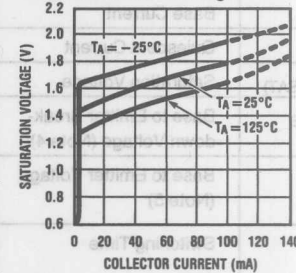
Available Collector Current



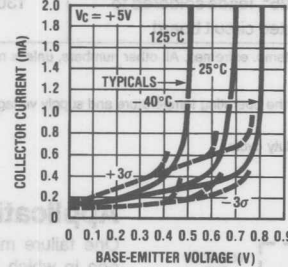
Quiescent Collector Current



Saturation Voltage

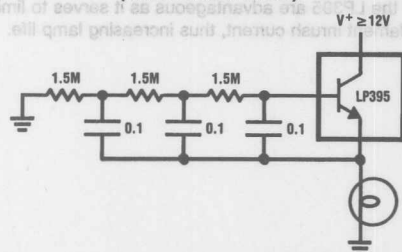


Collector Current Threshold



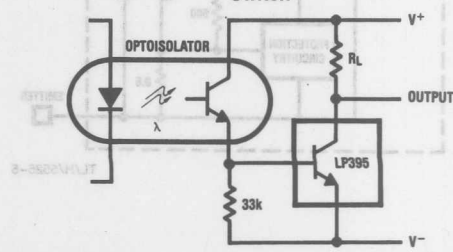
Typical Applications (Continued)

Lamp Flasher
(Short Circuit Proof)



TL/H/5525-6

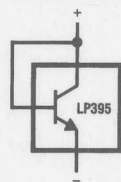
Optically Isolated Switch



TL/H/5525-7

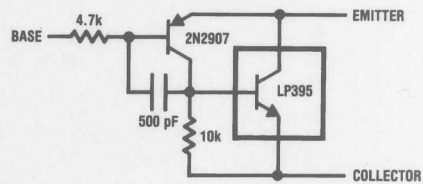
Typical Applications (Continued)

Two Terminal Current Limiter



TL/H/5525-8

Composite PNP



TL/H/5525-2



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Section 6 Surface Mount



Section 6 Contents

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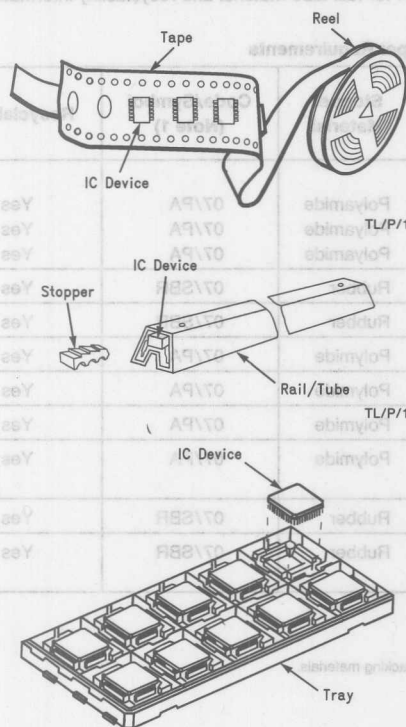
Section 6
Surface Mount

Packing Considerations (Methods, Materials and Recycling)

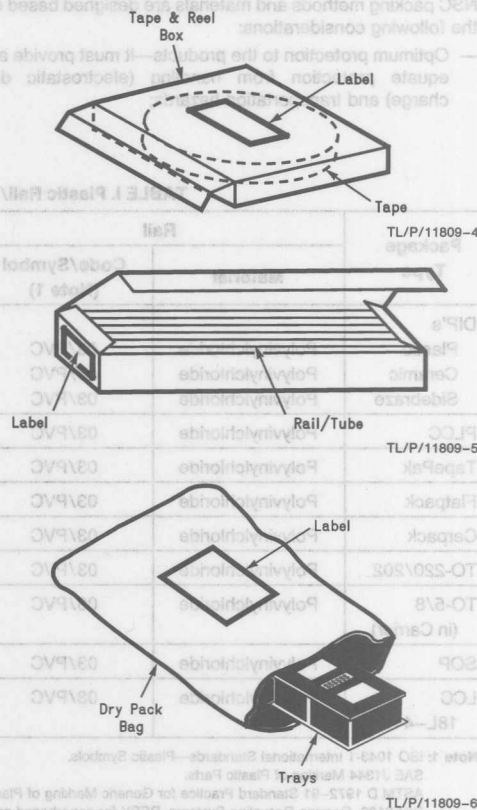
Transport Media

All NSC devices are prepared, inspected and packed to insure proper physical support and to protect during transport and shipment. All assembled devices are packed in one or more of the following container forms—immediate containers, intermediate containers and outer/shipping containers. An example of each container form is illustrated below.

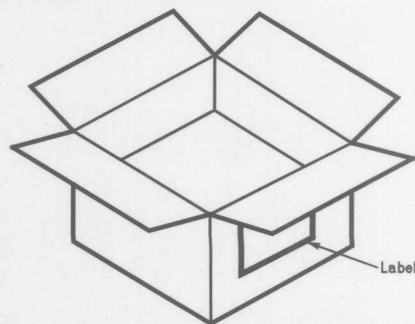
IMMEDIATE CONTAINER



INTERMEDIATE CONTAINER



OUTER/SHIPPING CONTAINER



Methods of immediate carrier packing include insertion of components into molded trays and rails/tubes, mounting of components onto tape and reel or placement in corrugated cartons. The immediate containers are then packed into intermediate containers (bags or boxes) which specify quantities of trays, rails/tubes or tape and reels. Outer/shipping containers are then filled or partially filled with intermediate containers to meet order quantity requirements and to further insure protection from transportation hazards. Additional dunnage filler material is required to fill voids within the intermediate and outer/shipping containers.

General Packing Requirements

NSC packing methods and materials are designed based on the following considerations:

- Optimum protection to the products—it must provide adequate protection from handling (electrostatic discharge) and transportation hazards;

- Ease of handling—it should be easy to assemble, load and unload products in and from it; and
- Impacts to the environment—it shall be reusable and recyclable.

Levels of Product Packing

IMMEDIATE CONTAINER

The first level of product packing is the immediate container. The immediate container type varies with the product or package being packed. In addition, the materials used in the immediate container depend on the fragility, size and profile of the product. The four types of immediate containers used by NSC are rails/tubes, trays, tape and reel, and corrugated and chipboard containers.

Rails/tubes are generally made of acrylic or polyvinyl chloride (PVC) plastics. The electrical characteristics of the material are altered by either intrinsically adding carbon fillers, and/or topically coating it with antistatic solution. Refer to Table I for rail/tube material and recyclability information.

TABLE I. Plastic Rail/Tube and Stopper Requirements

| Package Type | Rail | | Type | Stopper Material | Code/Symbol (Note 1) | Recyclability |
|------------------------|-------------------|----------------------|------|------------------|----------------------|---------------|
| | Material | Code/Symbol (Note 1) | | | | |
| DIP's | | | | | | |
| Plastic | Polyvinylchloride | 03/PVC | Pin | Polyamide | 07/PA | Yes |
| Ceramic | Polyvinylchloride | 03/PVC | Pin | Polyamide | 07/PA | Yes |
| Sidebrazed | Polyvinylchloride | 03/PVC | Pin | Polyamide | 07/PA | Yes |
| PLCC | Polyvinylchloride | 03/PVC | Plug | Rubber | 07/SBR | Yes |
| TapePak | Polyvinylchloride | 03/PVC | Plug | Rubber | 07/SBR | Yes |
| Flatpack | Polyvinylchloride | 03/PVC | Pin | Polymide | 07/PA | Yes |
| Cerpack | Polyvinylchloride | 03/PVC | Pin | Polymide | 07/PA | Yes |
| TO-220/202 | Polyvinylchloride | 03/PVC | Pin | Polymide | 07/PA | Yes |
| TO-5/8 (in Carrier) | Polyvinylchloride | 03/PVC | Pin | Polymide | 07/PA | Yes |
| SOP | Polyvinylchloride | 03/PVC | Plug | Rubber | 07/SBR | Yes |
| LCC 18L-44L | Polyvinylchloride | 03/PVC | Plug | Rubber | 07/SBR | Yes |

Note 1: ISO 1043-1 International Standards—Plastic Symbols.

SAE J1344 Marking of Plastic Parts.

ASTM D 1972-91 Standard Practice for Generic Marking of Plastic Products.

DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Molded injection and vacuum formed trays can be either conductive or static dissipative. Molded injection trays are classified as either low-temperature or high-temperature

depending on the material type. Vacuum formed trays are only used in ambient room temperature conditions. Refer to Table II for tray material and recyclability information.

TABLE II. Tray Requirements

| Package Type | Class | Material | Tray | | Binding Type |
|---|----------------------|--------------------------------|------------------------|----------------------|-------------------------|
| | | | Recyclability (Note 1) | Code/Symbol (Note 1) | |
| PQFP (All) | High Temperature | Polyethersulfone | Yes | 07/PES | Wire Tie or Nylon Strap |
| | Low Temperature | Acrylonitrilebutadiene Styrene | Yes | 07/ABS | Wire Tie or Nylon Strap |
| PGA, LDCC CERQUADs and LCC (48 leads–125 leads) | Low Temperature Only | ABS/PVC | Yes | 07/ABS-PVC | Wire Tie |
| PPGA | Low Temperature Only | Polyarylsulfone | Yes | 07/PAS | Wire Tie |

Tape and reel is a multi-part immediate container system. The reel is made of either polystyrene (PS) material coated with antistatic solution or chipboard. The embossed or cavity tape is made of either PVC or PS material. The cover tape

is made of polyester (PET) and polyethylene (PE) materials. Refer to Table III for tape and reel material and recyclability information.

TABLE III. Tape and Reel Requirements

| Package Type | Reel | | Cover Type | | Carrier Tape | | Recyclability (Note 1) |
|--------------------|--------------------------|----------------------|-------------|----------------------|--------------|----------------------|------------------------|
| | Material | Code/Symbol (Note 1) | Material | Code/Symbol (Note 1) | Material | Code/Symbol (Note 1) | |
| TO-92 | Chipboard | Resy | N/A | | Paper Tape | | Yes |
| SOP-23 | Polystyrene Chipboard | 06/PS Resy | Polystyrene | 06/PS | PVC | 03/PVC | Yes |
| SOP, SSOP and PLCC | Polystyrene Polyethylene | 06/PS | Polyester | 07/PET-PE | PVC | 03/PVC | Yes |

Note 1: 150 1043-1 International Standards—Plastic Symbols.

SAE J1344 Marking of Plastic Parts.

ASTM D 1972–91 Standard Practice for Generic Marking of Plastic Products.

DIN 6120, German Recycling Systems, RESY for paperbased and VGG for plastic packing materials.

TABLE IV. Fibreboard Container Requirements

| Package Type | Pack Method | | Container Type | | Recyclability |
|---|--------------------------|----------------------|--|--|---------------|
| | Material | Code/Symbol (Note 1) | Immediate (IMM) Intermediate (INT) Outer or Shipping (SHP) | | |
| TO-92/18, TO-46/5, TO-39, 220, TO-202/126, TO-237 | Corrugated (E070 BOX) | Resy | IMM | | Yes |
| All Products | Corrugated | Resy | INT and SHIP | | Yes |
| All Products | 3-Ply Paper (Padpak) | Resy | Dunnage | | Yes |
| All Products PLCC | Plastic Bubble Sheet | 04/PE | Dunnage | | Yes |

Note 1: ISO 1043-1 International Standards—Plastic Symbols.

SAE J1344 Marking of Plastic Parts.

ASTM D1972-91 Standard Practice for Generic Marking of Plastic Products.

DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

INTERMEDIATE CONTAINERS

The second level of product packing is the intermediate container. Three types on intermediate containers are used by NSC. They are plastic bags, moisture barrier bags and corrugated cartons/boxes.

Two types of plastic bags are used and usage of each type depends on the product or package being packed. Conductive bags are made of polyvinylchloride plastic material. The electrical characteristics of the bag are altered by adding

carbon fillers which make the bag black (opaque) in color. Conductive bags are used on products or packages that are packed in static dissipative (SD) rails/tubes. Static shielding bags are made of two layers of SD polyethylene sheets with a metallized film separating the sheets. Refer to Table V for material and recyclability information.

Moisture barrier bags are used on rail/tube, tape and reel, and tray packs for moisture sensitive products. NSC uses National Metallizing's Stratoguard™ 4.6.

| | | | | | | | |
|-----|--------|-----|-----------|--------------|-------|--------------|-------------------|
| Yes | 03/PVC | PVC | 06/PS | Polyethylene | 06/PS | Polyethylene | SOP-23 |
| Yes | 03/PVC | PVC | 07/PET/PE | Polyester | 06/PS | Polyethylene | SOP, SOP and PLCC |

Note 1: ISO 1043-1 International Standards—Plastic Symbols.

SAE J1344 Marking of Plastic Parts.

ASTM D 1972-91 Standard Practice for Generic Marking of Plastic Products.

DIN 6120, German Recycling Systems, RESY for paperbased and VGK for plastic packing materials.

Immediate Container Pack Methods

The following table identifies the primary immediate container pack method for all hermetic and plastic packages offered by National Semiconductor. A secondary immediate container pack method is identified where applicable.

Immediate Packing Method for Ceramic Packages

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|--|---------------------------|-----------------------------|----------|-------------------------------|----------|
| | | Method | Quantity | Method | Quantity |
| Ceramic Sidebrazed Dual-In-Line Package (SB) | D08C | Rail/Tube | 35 | | |
| | D14D | Rail/Tube | 25 | | |
| | D16C | Rail/Tube | 20 | | |
| | D18A | Rail/Tube | 20 | | |
| | D20A | Rail/Tube | 18 | | |
| | D20B | Rail/Tube | 18 | | |
| | D24C | Rail/Tube | 15 | | |
| | D24H | Rail/Tube | 15 | | |
| | D24K | Rail/Tube | 15 | | |
| | D28D | Rail/Tube | 13 | | |
| | D28G | Rail/Tube | 13 | | |
| | D28H | Rail/Tube | 13 | | |
| | D40C | Rail/Tube | 9 | | |
| | D40J | Rail/Tube | 9 | | |
| Ceramic Leadless Chip Carrier (LCC) | D48A | Rail/Tube | 7 | | |
| | D52A | Rail/Tube | 7 | | |
| | E20A | Rail/Tube | 50 | | |
| | EA20B | Rail/Tube | 50 | | |
| | E24B | Tray | 25 | | |
| | E28A | Tray | 28 | | |
| | EA028C | Tray | 100 | | |
| | E32A | Rail/Tube | 35 | | |
| | E32B | Rail/Tube | 35 | | |
| | E32C | Rail/Tube | 35 | | |
| | E40A | Rail/Tube | 35 | | |
| | E44A | Rail/Tube | 25 | | |
| | E48A | Tray | 25 | | |
| | E68B | Tray | 48 | | |
| | E68C | Tray | 48 | | |
| | E84A | Tray | 42 | | |
| | E84B | Tray | 42 | | |

Packing Considerations

6

Immediate Packing Method for Ceramic Packages (Continued)

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|---------------------------------------|---------------------------|-----------------------------|----------|-------------------------------|----------|
| | | Method | Quantity | Method | Quantity |
| Ceramic Dual-In-Line Package (Cerdip) | J08A | Rail/Tube | 40 | | |
| | J14A | Rail/Tube | 25 | | |
| | J16A | Rail/Tube | 25 | | |
| | J18A | Rail/Tube | 20 | | |
| | J20A | Rail/Tube | 20 | | |
| | J22A | Rail/Tube | 17 | | |
| | J24A | Rail/Tube | 15 | | |
| | J24AQ | Rail/Tube | 15 | | |
| | J24B-Q | Rail/Tube | 15 | | |
| | J24CQ | Rail/Tube | 15 | | |
| | J24E | Rail/Tube | 16 | | |
| | J24F | Rail/Tube | 15 | | |
| | J28A | Rail/Tube | 12 | | |
| | J28AQ | Rail/Tube | 12 | | |
| | J28B | Rail/Tube | 12 | | |
| | J28BQ | Rail/Tube | 12 | | |
| | J28CQ | Rail/Tube | 13 | | |
| | J32B | Rail/Tube | 11 | | |
| | J32AQ | Rail/Tube | 11 | | |
| | J40A | Rail/Tube | 9 | | |
| | J40AQ | Rail/Tube | 9 | | |
| | J40BQ | Rail/Tube | 9 | | |
| Ceramic Small Outline Package, Wide | MC16A | Rail/Tube | 45 | | |
| | MC20A | Rail/Tube | 36 | | |
| | MC20B | Rail/Tube | 36 | | |
| | MC24A | Rail/Tube | 30 | | |
| | MC28A | Rail/Tube | 26 | | |
| | MC28B | Rail/Tube | 26 | | |

Immediate Packing Method for Ceramic Packages (Continued)

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|----------------------------------|---------------------------------|-----------------------------------|----------|-------------------------------------|----------|
| | | Method | Quantity | Method | Quantity |
| Ceramic Pin Grid Array (CPGA) | U44A | Tray | 80 | | |
| | U68B | Tray | 42 | | |
| | U68C | Tray | 42 | | |
| | U68D | Tray | 42 | | |
| | U68E | Tray | 42 | | |
| | U75A | Tray | 35 | | |
| | U84A | Tray | 42 | | |
| | U84B | Tray | 42 | | |
| | U84C | Tray | 42 | | |
| | U99A | Tray | 25 | | |
| | U100A | Tray | 30 | | |
| | U109A | Tray | 25 | | |
| | U120A | Tray | 30 | | |
| | U120C | Tray | 30 | | |
| | U124A | Tray | 30 | | |
| | U132A | Tray | 30 | | |
| | U132B | Tray | 30 | | |
| | U144A | Tray | 20 | | |
| | U156A | Tray | 20 | | |
| | U156B | Tray | 20 | | |
| | U169A | Tray | 20 | | |
| | U173A | Tray | 20 | | |
| | U175A | Tray | 20 | | |
| | U180A | Tray | 20 | | |
| | U223A | Tray | 20 | | |
| | U224A | Tray | 20 | | |
| | U257A | Tray | 12 | | |
| | U259A | Tray | 12 | | |
| | U299A | Tray | 12 | | |
| | U301A | Tray | 12 | | |
| | U303A | Tray | 12 | | |
| | U323A | Tray | 12 | | |

6-12

Immediate Packing Method for Metal Cans

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|------------------------|------------------------------|-----------------------------|----------|-------------------------------|------------------------------------|
| | | Method | Quantity | Method | Quantity |
| TO-5 | H06C | Tray | 100 | Carrier/Rail | 18 |
| | H08A | Tray | 100 | Carrier/Rail | 18 |
| | H08C | Tray | 100 | Carrier/Rail | 18 |
| | H10C | Tray | 100 | Carrier/Rail | 18 |
| TO-18 | H03C | Box | 1800 | Tray | 100 |
| TO-39 | H03A | Tray | 100 | Carrier/Rail | 18 |
| | H03B | Tray | 100 | Carrier/Rail | 18 |
| | HA04E | Tray | 100 | Carrier/Rail | 18 |
| TO-46 | H02A | Box | 1800 | Tray | 100 |
| | H03H | Box | 1800 | Tray | 100 |
| | H04A | Box | 1800 | Tray | 100 |
| | H04D | Box | 1800 | Tray | 100 |
| TO-52 | H03J | Box | 1800 | Tray | 100 |
| TO-72 | H04C | Box | 1800 | Tray | 100 |
| | | | | MOA20 | Shrink Small Outline Package (SOP) |
| | | | | MOA24 | Shrink Small Outline Package (SOP) |
| | | | | MSBA | Shrink Small Outline Package (SOP) |
| | | | | MSBA | Shrink Small Outline Package (SOP) |
| | | | | MSA20 | Shrink Small Outline Package (SOP) |
| | | | | MSA24 | Shrink Small Outline Package (SOP) |
| | | | | MSA40 | Shrink Small Outline Package (SOP) |
| | | | | MSA40 | Shrink Small Outline Package (SOP) |
| | | | | MOA | Very Small Outline Package (VSO) |
| | | | | MOA | Very Small Outline Package (VSO) |
| | | | | MSH2A | Thin Small Outline Package (TSOP) |
| | | | | MSH2A | Thin Small Outline Package (TSOP) |
| | | | | MTA20 | Thin Small Outline Package (TSOP) |
| | | | | MTA20 | Thin Small Outline Package (TSOP) |

Immediate Packing Method for Plastic Packages

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|---|---------------------------|-----------------------------|----------------|-------------------------------|----------|
| | | Method | Quantity | Method | Quantity |
| Small Outline Transistor (SOT-23) | M03A | Tape and Reel | 3000/ 10000 | Bulk/Bag | 500 |
| | M03B | Tape and Reel | 3000/ 10000 | Bulk/Bag | 500 |
| Small Outline Package, JEDEC (SOP) | M08A | Rail/Tube | 95 | Tape and Reel | 2500 |
| | M14A | Rail/Tube | 55 | Tape and Reel | 2500 |
| | M14B | Rail/Tube | 50 | Tape and Reel | 1000 |
| | M16A | Rail/Tube | 48 | Tape and Reel | 2500 |
| | M16B | Rail/Tube | 45 | Tape and Reel | 1000 |
| | M20B | Rail/Tube | 36 | Tape and Reel | 1000 |
| | M24B | Rail/Tube | 30 | Tape and Reel | 1000 |
| | M28B | Rail/Tube | 26 | Tape and Reel | 1000 |
| Small Outline Package, EIAJ (SOP) | M14D | Rail/Tube | 47 | Tape and Reel | 1000 |
| | M16D | Rail/Tube | 47 | Tape and Reel | 1000 |
| | M20D | Rail/Tube | 37 | Tape and Reel | 1000 |
| Shrink Small Outline Package, JEDEC (SSOP) | MQA20 | Rail/Tube | 54 | Tape and Reel | 2500 |
| | MQA24 | Rail/Tube | 54 | Tape and Reel | 2500 |
| | MS48A | Rail/Tube | 29 | Tape and Reel | 1000 |
| | MS56A | Rail/Tube | 25 | Tape and Reel | 1000 |
| Shrink Small Outline Package, EIAJ (SSOP) | MSA20 | Rail/Tube | 65 | Tape and Reel | 1000 |
| | MSA24 | Rail/Tube | 58 | Tape and Reel | 1000 |
| | MS40A | Rail/Tube | 34 | Tape and Reel | 1000 |
| Very Small Outline Package (VSOP) | M40A | Rail/Tube | 34 | Tape and Reel | 1000 |
| Thin Small Outline Package, EIAJ (TSOP) | MBH32A | Tray | 156 | | |
| Thin Shrink Small Outline Package, EIAJ (TSSOP) | MTA20 | Tape and Reel | 2500 | | |

Immediate Packing Method for Plastic Packages (Continued)

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|------------------------------------|---------------------------|-----------------------------|----------|-------------------------------|----------|
| | | Method | Quantity | Method | Quantity |
| Molded Dual-In-Line Package (MDIP) | N08E | Rail/Tube | 40 | | |
| | N14A | Rail/Tube | 25 | | |
| | N16A | Rail/Tube | 20 | | |
| | N16E | Rail/Tube | 25 | | |
| | N16G | Rail/Tube | 20 | | |
| | N18A | Rail/Tube | 20 | | |
| | N20A | Rail/Tube | 18 | | |
| | N22A | Rail/Tube | 15 | | |
| | N22B | Rail/Tube | 15 | | |
| | N24A | Rail/Tube | 15 | | |
| | N24C | Rail/Tube | 15 | | |
| | N24D | Rail/Tube | 15 | | |
| | N24E | Rail/Tube | 15 | | |
| | N28B | Rail/Tube | 13 | | |
| | N40A | Rail/Tube | 9 | | |
| | N48A | Rail/Tube | 7 | | |
| TO-202 | P03A | Rail/Tube | 45 | Box | 300 |
| | P03B | Rail/Tube | 45 | Box | 300 |
| | P03C | Rail/Tube | 45 | Box | 300 |
| | P03D | Rail/Tube | 45 | Box | 300 |
| | P03E | Rail/Tube | 45 | Box | 300 |
| | P03F | Rail/Tube | 45 | Box | 300 |
| | P03G | Rail/Tube | 45 | Box | 300 |
| | P03H | Rail/Tube | 45 | Box | 300 |
| | P03J | Rail/Tube | 45 | Box | 300 |
| | P04A | Rail/Tube | 45 | Box | 300 |
| | P11A | Rail/Tube | 15 | | |
| TO-237 | R03A | Box | 1500 | Tape and Reel | 2000 |
| | R03B | Box | 1500 | Tape and Reel | 2000 |
| | R03C | Box | 1500 | Tape and Reel | 2000 |
| | R03D | Box | 1500 | Tape and Reel | 2000 |
| TO-226 | RC03A | Box | 1500 | Tape and Reel | 2000 |
| | RC03B | Box | 1500 | Tape and Reel | 2000 |
| | RC03C | Box | 1500 | Tape and Reel | 2000 |
| | RC03D | Box | 1500 | Tape and Reel | 2000 |

| Package Type (Code) | Package Marketing Drawing | Immediate Container | | Immediate Container | |
|------------------------------------|---------------------------|---------------------|----------|---------------------|----------|
| | | Method | Quantity | Method | Quantity |
| TO-220 | TA02A | Rail/Tube | 45 | Box | 300 |
| | T02D | Rail/Tube | 45 | Box | 300 |
| | TA03A | Rail/Tube | 45 | Box | 300 |
| | TA03B | Rail/Tube | 45 | Box | 300 |
| | TA03D | Rail/Tube | 45 | Box | 300 |
| | T03A | Rail/Tube | 45 | Box | 300 |
| | T03B | Rail/Tube | 45 | Box | 300 |
| | T03D | Rail/Tube | 45 | Box | 300 |
| | T03F | Rail/Tube | 45 | Box | 300 |
| | T05A | Rail/Tube | 45 | Box | 300 |
| | T05B | Rail/Tube | 45 | Box | 300 |
| | T05C | Rail/Tube | 45 | Box | 300 |
| | T05D | Rail/Tube | 45 | Box | 300 |
| | T05E | Rail/Tube | 45 | Box | 300 |
| | T05F | Rail/Tube | 45 | Box | 300 |
| | TA05A | Rail/Tube | 45 | Box | 300 |
| | TA05B | Rail/Tube | 45 | Box | 300 |
| | TA11A | Rail/Tube | 20 | Box | 300 |
| | TA11B | Rail/Tube | 20 | Box | 300 |
| | TA11C | Rail/Tube | 20 | Box | 300 |
| | TA11D | Rail/Tube | 20 | Box | 300 |
| | TA11E | Rail/Tube | 20 | Box | 300 |
| | TA12A | Rail/Tube | 20 | Box | 300 |
| | TA15A | Rail/Tube | 20 | Box | 300 |
| | TA23A | Rail/Tube | 15 | Box | 300 |
| TapePak® | TP40A | Coinstack Tube | 100 | Flat Rail | 25 |
| Plastic Pin Grid Array (PPGA) | UP124A | Tray | 30 | | |
| | UP159A | Tray | 20 | | |
| | UP175A | Tray | 20 | | |
| Plastic Leaded Chip Carrier (PLCC) | V20A | Rail/Tube | 40 | Tape and Reel | 1000 |
| | V28A | Rail/Tube | 35 | Tape and Reel | 750 |
| | V32A | Rail/Tube | 30 | | |
| | V44A | Rail/Tube | 25 | Tape and Reel | 500 |
| | V52A | Rail/Tube | 22 | Tape and Reel | 500 |
| | V68A | Rail/Tube | 18 | Tape and Reel | 250 |
| | V84A | Rail/Tube | 15 | Tape and Reel | 250 |

Immediate Packing Method for Plastic Packages (Continued)

| Package Type (Code) | Package Marketing Drawing | Primary Immediate Container | | Secondary Immediate Container | |
|------------------------------|---------------------------|-----------------------------|----------|-------------------------------|----------|
| | | Method | Quantity | Method | Quantity |
| Plastic Quad Flatpack (PQFP) | VEF44A | Tray | 96 | | |
| | VBG48A | Tray | 60 | | |
| | VHG80A | Tray | 60 | | |
| | VJE80A | Tray | 84 | | |
| | VCC80A | Tray | 50/66 | | |
| | VCE100A | Tray | 84 | | |
| | VLJ100A | Tray | 50 | | |
| | VJG100A | Tray | 60 | | |
| | VNG144A | Tray | 60 | | |
| | VUL160A | Tray | 24 | | |
| | VQL160A | Tray | 24 | | |
| | VUW208A | Tray | 24 | | |
| | VF132A | Tray | 36 | | |
| | VF196A | Tray | 21 | | |
| TO-92 | Z03A | Box | 1800 | Tape and Reel | 2000 |
| | Z03B | Box | 1800 | Tape and Reel | 2000 |
| | Z03C | Box | 1800 | Tape and Reel | 2000 |
| | Z03D | Box | 1800 | Tape and Reel | 2000 |
| | Z03E | Box | 1800 | Tape and Reel | 2000 |
| | Z03G | Box | 1800 | Tape and Reel | 2000 |
| | Z03H | Box | 1800 | Tape and Reel | 2000 |
| | Z03J | Box | 1800 | Tape and Reel | 2000 |

Labeling

National Semiconductor offers 3 standard bar code labels; reel and intermediate container labels for Tape and Reel; intermediate container label other than for Tape and Reel;

and outer/shipping container labels. The tape and reel, and intermediate container labels are National's own format while the outer/shipping container label is based on the EIA-556-A label standard.

NSC Standard Tape and Reel Label

(P) CPN: CPN 123456789012

XYZ COMPANY



PD #: PD 123456789012

(Q) QTY: 1000

(D) D/C: P9236

NSID: DM74ALS253WM



SPEC: SPEC1234

LOT : LOT 12345678912

This label is placed on the reel (immediate container) as well as on the intermediate box.

TL/P/11809-8

NSC Standard Intermediate Container Label

XYZ COMPANY
(P) CPN CPN 1234567890



(Q) QTY 1000



(D) D.C. P9236



(A) P.O. PO 123456789012



NSID : DM74PLS253WM
FIN OPT : SPEC1234
LOT : LOT 123456789

P.L. : PL1234
REQA : RV1234
BOX 01 OF 03

NATIONAL SEMICONDUCTOR

TL/P/11809-9

NSC Standard Outer/Shipping Container Label

(CS) PKG ID: EIR14+EP123456



FROM: N S C

SANTA CLARA, CA 95051

TO: XYZ COMPANY

(Z) SPECIAL:

SHIP TO ADDRESS 1
SHIP TO ADDRESS 2
SHIP TO ADDRESS 3
SHIP TO ADDRESS 4
SHIP TO ADDRESS 5

(Q) QUANTITY



10000 EA

PACKAGE COUNT

02 OF 05

(K) TRANS. ID: P01234567890123456789



PACKAGE WEIGHT

1000 KG 2540 LB

(P) CUSTOMER

PROD ID: CPN12345678901234567890



TL/P/11809-10

Board Mount of Surface Mount Components

Abstract

In facing the challenges of "Surface Mount Technology", many manufacturers of printed circuit boards have taken steps to convert some portions of their boards to this process. However, as the availability of all products as surface mount components is still limited, many have had to mix lead-inserted components with surface mount devices (SMD's). Furthermore, to take advantage of using both sides of the board, some surface mounted components are adhered to the bottom side of the board while the top side is reserved for the conventional lead-insert packages and fine pitch surface mount packages.

There are three surface mount processes in hi-volume use today:

1. **WAVE SOLDER**; the surface mounted components are adhered to the bottom side of the board while the top side is reserved for the lead-inserted packages. The surface mount components are subjected to severe thermal stress when they are immersed into the molten solder.
2. **INFRA-RED** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, the solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment.
3. **VAPOR PHASE** mass reflow; the surface mount components are placed on the solder paste which has been applied to the board, the solder joints are formed when the board is passed thru the reflow media. The surface mount devices are subjected to a controlled thermal environment, more severe than Infra-red but much less than wavesolder.

A discussion of the effect of these processes on the reliability of plastic semiconductor packages follows.

Role of Wave Soldering in Application of SMDs

The generally acceptable methods of soldering SMDs are vapor phase reflow soldering and IR reflow soldering, both requiring application of solder paste on PW boards prior to placement of the components. However, sentiment still exists for retaining the use of the old wave soldering machine. The reasons being:

Most PC Board Assembly houses already possess wave soldering equipment. Switching to another technology such as vapor phase soldering requires substantial investment in equipment and people.

Due to the limited number of devices that are surface mount components, it is necessary to mix both lead inserted components and surface mount components on the same board.

Some components such as relays and switches are made of materials which would not be able to survive the temperature exposure in a vapor phase or IR furnace.

PW Board Assembly Procedures

There are two considerations in which through-hole ICs may be combined with surface mount components on the PW Board:

- a) Whether to mount ICs on one or both sides of the board.
- b) The sequence of soldering using Vapor Phase, IR or Wave Soldering singly or a combination of two or more methods.

The various processes that may be employed are:

A) WAVE SOLDER BEFORE VAPOR/IR REFLOW SOLDER

1. Components on the same side of PW Board. Lead insert standard DIPs onto PW Board Wave solder (conventional). Wash and lead trim. Dispense solder paste on SEM pads. Pick and place SMDs onto PW Board. Bake Vapor phase/IR reflow. Clean.
2. Components on opposite side of PW Board. Lead insert standard DIPs onto PW Board Wave Solder (conventional). Clean and lead trim. Invert PW Board. Dispense drop of adhesive on SMD sites (optional for smaller components). Pick and place SMDs onto board. Bake/Cure. Invert board to rest on raised fixture. Vapor/IR reflow soldering. Clean.

B) VAPOR/IR REFLOW SOLDER THEN WAVE SOLDER

1. Components on the same side of PW Board. Solder paste screened on SMD side of Printed Wire Board. Pick and place SMDs. Bake Vapor/IR reflow. Lead insert on same side as SMD's. Wave solder. Clean and trim underside of PCB.

C) VAPOR/IR REFLOW ONLY

1. Components on the same side of PW Board Trim and form standard DIPs in "gull wing" configuration. Solder paste screened on PW Board. Pick and place SMDs and DIPs. Bake Vapor/IR reflow. Clean.
2. Components on opposite sides of PW Board. Solder paste screened on SMD-side of Printed Wire Board. Adhesive dispensed at central location of each component. Pick and place SMDs. Bake. Solder paste screened on all pads on DIP-side or alternatively apply solder rings (performs) on leads. Lead insert DIPs. Vapor/IR reflow. Clean and lead trim.

- Components on opposite sides of PW board. Adhesive dispense on SMD side of PW Board. Pick and place SMDs. Cure adhesive. Lead insert top side with DIPs. Wave solder with SMDs down and into solder bath. Clean and lead trim.

All of the above assembly procedures can be divided into three categories for IC. Reliability considerations:

- Components are subjected to both a vapor phase/IR heat cycle then followed by a wave-solder heat cycle or vice versa.
- Components are subjected to only a vapor phase/IR heat cycle.
- Components are subjected to wave-soldering only and SMDs are subjected to heat by immersion into a solder pot.

Of these three categories, the last is the most severe regarding heat treatment to a semiconductor device. However, note that semiconductor molded packages generally possess a coating of solder on their leads as a final finish for solderability and protection of base leadframe material. Most semiconductor manufacturers solder-plate the component leads, while others perform hot solder dip. In the latter case the packages may be subjected to total immersion into a hot solder bath under controlled conditions (manual operation) or be partially immersed while in a "pallet" where automatic wave or DIP soldering processes are used. It is, therefore, possible to subject SMDs to solder heat under certain conditions and not cause catastrophic failures.

Thermal Characteristics of Molded Integrated Circuits

Since Plastic DIPs and SMDs are encapsulated with a thermoset epoxy, the thermal characteristics of the material generally correspond to a TMA (Thermo-Mechanical Analysis) graph. The critical parameters are (a) its Linear thermal expansion characteristics and (b) its glass transition temperature after the epoxy has been fully cured. A typical TMA graph is illustrated in *Figure 1*. Note that the epoxy changes to a higher thermal expansion once it is subjected to temperatures exceeding its glass transition temperature. Metals (as used on leadframes, for example) do not have this characteristic and generally will have a consistent Linear thermal expansion over the same temperature range.

In any good reliable plastic package, the choice of leadframe material should be such to match its thermal expansion properties to that of the encapsulating epoxy. In the event that there is a mismatch between the two, stresses can build up at the interface of the epoxy and metal. There now exists a tendency for the epoxy to separate from the metal leadframe in a manner similar to that observed on bimetallic thermal range.

In most cases when the packages are kept at temperatures below their glass transition, there is a small possibility of separation at the epoxy-metal interface. However, if the package is subjected to temperature above its glass-transition temperature, the epoxy will expand much faster than the metal and the probability of separation is greatly increased.

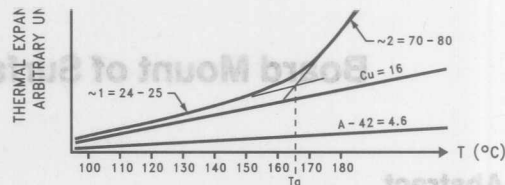


FIGURE 1. Thermal Expansion and Glass

Conventional Wave Soldering

Most wave soldering operations occur at temperatures between 240°C–260°C. Conventional epoxies for encapsulation have glass-transition temperatures between 140°C–170°C. An I.C. directly exposed to these temperatures risks its long term functionality due to epoxy/metal separation.

Fortunately, there are factors that can reduce that element of risk:

- The PW board has a certain amount of heat-sink effort and tends to shield the components from the temperature of the solder (if they were placed on the top side of the board). In actual measurements, DIPs achieve a temperature between 120°C–150°C in a 5-second pass over the solder. This accounts for the fact that DIPs mounted in the conventional manner are reliable.
- In conventional soldering, only the tip of each lead in DIP would experience the solder temperature because the epoxy and die are standing above the PW board and out of the solder bath.

Effect on Package Performance by Epoxy-Metal Separation

In wave soldering, it is necessary to use fluxes to assist the solderability of the components and PW boards. Some facilities may even process the boards and components through some form of acid cleaning prior to the soldering temperature. If separation occurs, the flux residues and acid residues (which may be present owing to inadequate cleaning) will be forced into the package mainly by capillary action as the residues move away from the solder heat source. Once the package is cooled, these contaminants are now trapped within the package and are available to diffuse with moisture from the epoxy over time. It should be noted that electrical tests performed immediately after soldering generally will give no indication of this potential problem. In any case, the end result will be corrosion of the chip metalization over time and premature failure of the device in the field.

Vapor Phase/IR Reflow Soldering

In both vapor phase and IR reflow soldering, the risk of separation between epoxy/metal can also be high. Maximum operating temperatures are 219°C (vapor phase) or 240°C (IR) and duration may also be longer (30 sec-60 sec). On the same theoretical basis, there should also be separation. However, in both these methods, solder paste is applied to the pads of the boards; no fluxes are used. Also, the devices are not immersed into the hot solder. This reduces the possibility of solder forcing itself into the epoxy-leadframe interface. Furthermore, in the vapor phase system, the soldering environment is "oxygen-free" and considered "contaminant free". Being so, it could be visualized that as far as reliability with respect to corrosion, both of these methods are advantageous over wave soldering.

Bias Moisture Test

A bias moisture test was designed to determine the effect on package performance. In this test, the packages are pressured in a steam chamber to accelerate penetration of moisture into the package. An electrical bias is applied on the device. Should there be any contaminants trapped within the package, the moisture will quickly form an electrolyte and cause the electrodes (which are the lead fingers), the gold wire and the aluminum bond-pads of the silicon device to corrode. The aluminum bond-pads, being the weakest link of the system, will generally be the first to fail.

This proprietary accelerated bias/moisture pressure-test is significant in relation to the life test condition at 85°C and 85% relative humidity. One cycle of approximately 100 hours has been shown to be equivalent to 2,000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 2,000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the workmanship or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

Test Results

The comparison of vapor phase and wave-soldering upon the reliability of molded Small-Outline packages was performed using the bias moisture test (see Table IV). It is clearly seen that vapor phase reflow soldering gave more consistent results. Wave soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

TABLE IV. Vapor Phase vs. Wave Solder

1. Vapor phase (60 sec, exposure @ 217°C)
= 9 failures/1723 samples
= 0.5% (average over 32 sample lots)

2. Wave solder (2 sec total immersion @ 260°C)
= 16 failures/1201 samples
= 1.3% (average over 27 sample lots)

Package: SO-14 lead

Test: Bias moisture test 85% R.H.

85°C for 2,000 hours

Device: LM324M

In Table V we examine the tolerance of the Small-Outlined (SOIC) package to varying immersion time in a hot solder pot. SO-14 lead molded packages were subjected to the bias moisture test after being treated to the various soldering conditions and repeated four (4) times. End point was an electrical test after an equivalent of 4,000 hours 85/85 test. Results were compared for packages by themselves against packages which were surface-mounted onto a FR-4 printed wire board.

TABLE V. Summary of Wave Solder Results

| | Unmounted | Mounted |
|---------------------------------------|----------------|-------------|
| Control/Vapor Phase 15 sec @ 215°C | 0/114 | 0/84 |
| Solder Dip 4 Sec @ 260°C | 2/144 (1.4%) | 0/85 |
| Solder Dip 4 Sec @ 260°C | — | 0/83 |
| Solder Dip 6 Sec @ 260°C | 13/248 (5.2%) | 1/76 (1.3%) |
| Solder Dip 10 Sec @ 260°C | 14/127 (11.0%) | 3/79 (3.8%) |
| Package: SO-14 lead | | |
| Device: LM324M | | |

Since the package is of very small mass and experiences a rather sharp thermal shock followed by stresses created by the mismatch in expansion, the results show the packages being susceptible to failures after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursion was reduced. In any case, because of the repeated treatment, the package had failures when subjected in excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even though the immediate electrical test data could be acceptable.

Finally, Table VI examines the bias moisture test performed on surface mount (SOIC) components manufactured by various semiconductor houses. End point was an electrical test after an equivalent of 6,000 hours in an 85/85 test. Failures were analyzed and corrosion was checked for in each case to detect flaws in package integrity.

TABLE VI. U.S. Manufacturing Integrated Circuits Reliability in Various Solder Environments (# Failure/Total Environment)

| Package SO-8 | Vapor Phase 30 sec | Wave Solder 2 sec | Wave Solder 4 sec | Wave Solder 6 sec | Wave Solder 10 sec |
|--------------|--------------------|-------------------|-------------------|-------------------|--------------------|
| Manuf A | 8/30* | 1/30* | 0/30 | 12/30* | 16/30* |
| Manuf B | 2/30* | 8/30* | 2/30* | 22/30* | 20/30* |
| Manuf C | 0/30 | 0/29 | 0/29 | 0/30 | 0/30 |
| Manuf D | 1/30* | 12/30* | 14/30* | 2/30* | 0/30 |
| Manuf E | 1/30** | 0/30 | 0/30 | 0/30 | 0/30 |
| Manuf F | 0/30 | 0/30 | 0/30 | 0/30 | 0/30 |
| NSC | 0/30 | 0/30 | 0/30 | 0/30 | 0/30 |

*Corrosion failures

**No Visual Defects-Non-corrosion failures

Test Accelerated Bias Moisture Test: 85% R.H./85°C. 6,000 equivalent hours

| Mounted | Unmounted | Control/Vapor Phase |
|---------------------|--------------|------------------------------|
| 0/85 | 0/14 | 15 sec @ 215°C |
| 0/85 | 2/144 (1.4%) | Solder Dip 4 Sec @ 280°C |
| 0/85 | — | Solder Dip 4 Sec @ 280°C |
| 1/75 (1.3%) | 1/148 (0.7%) | Solder Dip 6 Sec @ 280°C |
| 3/70 (4.3%) | 1/172 (1.0%) | Solder Dip 10 Sec @ 280°C |
| Package: SO-14 lead | | Device: LM323M |

Since the package is of very small mass and experiences rather sharp thermal shock followed by stresses caused by the mismatch in expansion, the results show the packages being susceptible to failure after being immersed in excess of 6 seconds in a solder pot. In the second case where the packages were mounted, the effect of severe temperature excursions was reduced. In any case, because of the repeat of treatment, the packages had failures when subjected to excess of 6 seconds immersion in hot solder. The safety margin is therefore recommended as maximum 4 seconds immersion. If packages were immersed longer than 4 seconds, there is a probable chance of finding some long term reliability failures even through the immediate electrical test data could be acceptable.

Summary

Based on the results presented, it is noted that surface-mounted components are as reliable as standard molded DIP packages. Whereas DIPs were never processed by being totally immersed in hot solder wave during printed circuit board soldering, surface mounted components such as SOICs (Small Outline) are expected to survive a total immersion in the hot solder in order to capitalize on maximum population on boards. Being constructed from a thermoset plastic of relatively low T_g compared to the soldering temperature, the ability of the package to survive is dependent on the time of immersion and also the cleanliness of material. The results indicate that one should limit the immersion time of the package in the solder wave to a maximum of 4 seconds in order to truly duplicate the reliability of a DIP. As the package size is reduced, as in a SO-8 lead, the requirement becomes even more critical. This is shown by the various manufacturers' performance. Results indicate there is room for improvement since not all survived the hot solder immersion without compromise to lower reliability.

This proprietary accelerated bias/moisture pressure test is significant in relation to the test condition at 85°C and 85% relative humidity. One cycle of approximately 100 hours has been shown to be equivalent to 5,000 hours in the 85/85 condition. Should the packages start to fail within the first cycle in the test, it is anticipated that the boards with these components in the harsh operating environment (85°C/85% RH) will experience corrosion and eventual electrical failures within its first 5,000 hours of operation.

Whether this is significant to a circuit board manufacturer will obviously be dependent on the products being manufactured and the working or reliability standards. Generally in systems with a long warranty and containing many components, it is advisable both on a reputation and cost basis to have the most reliable parts available.

Test Results

The comparison of vapor phase and wave soldering upon the reliability of molded Small Outline packages was performed using the bias moisture test (see Table IV). It is noted that vapor phase reflow soldering gave more consistent results. Wave soldering results were based on manual operation giving variations in soldering parameters such as temperature and duration.

Note: Temperature in degrees celcius. N/A = Not Applicable.

*Will vary depending on board density, geometry, and package type.

**Will vary depending on package types, and board density.

***For plastic packages; ceramic packages maximum may be 250°C.

Small Outline (SO) Package Surface Mounting Methods-Parameters and Their Effect on Product Reliability

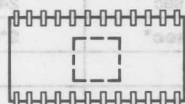
National Semiconductor
Application Note 450
Josip Huljev
W. K. Boey



The SO (small outline) package has been developed to meet customer demand for ever-increasing miniaturization and component density.

COMPONENT SIZE COMPARISON

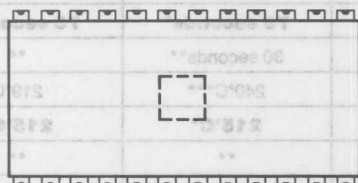
S.O. Package



← TYPICALLY 0.050" LEADSPACING

TL/F/8766-1

Standard DIP Package



← TYPICALLY 0.100" LEADSPACING

TL/F/8766-2

Because of its small size, reliability of the product assembled in SO packages needs to be carefully evaluated.

SO packages at National were internally qualified for production under the condition that they be of comparable reliability performance to a standard dual in line package under all accelerated environmental tests. Figure A is a summary of accelerated bias moisture test performance on 30V bipolar and 15V CMOS product assembled in SO and DIP (control) packages.

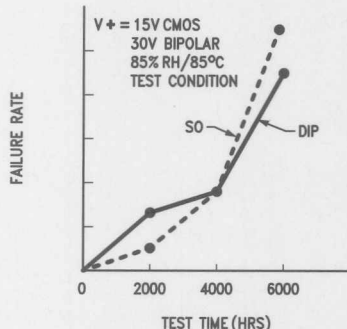


FIGURE A

TL/F/8766-3

In order to achieve reliability performance comparable to DIPs—SO packages are designed and built with materials and processes that effectively compensate for their small size.

All SO packages tested on 85%RA, 85°C were assembled on PC conversion boards using vapor-phase reflow soldering. With this approach we are able to measure the effect of surface mounting methods on reliability of the process. As illustrated in Figure A no significant difference was detected between the long term reliability performance of surface mounted S.O. packages and the DIP control product for up to 6000 hours of accelerated 85%/85°C testing.

SURFACE-MOUNT PROCESS FLOW

The standard process flowcharts for basic surface-mount operation and mixed-lead insertion/surface-mount operations, are illustrated on the following pages.

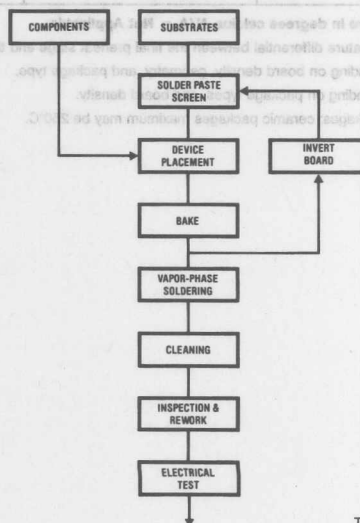
Usual variations encountered by users of SO packages are:

- Single-sided boards, surface-mounted components only.
- Single-sided boards, mixed-lead inserted and surface-mounted components.
- Double-sided boards, surface-mounted components only.
- Double-sided boards, mixed-lead inserted and surface-mounted components.

In consideration of these variations, it became necessary for users to utilize techniques involving wave soldering and adhesive applications, along with the commonly-used vapor-phase solder reflow soldering technique.

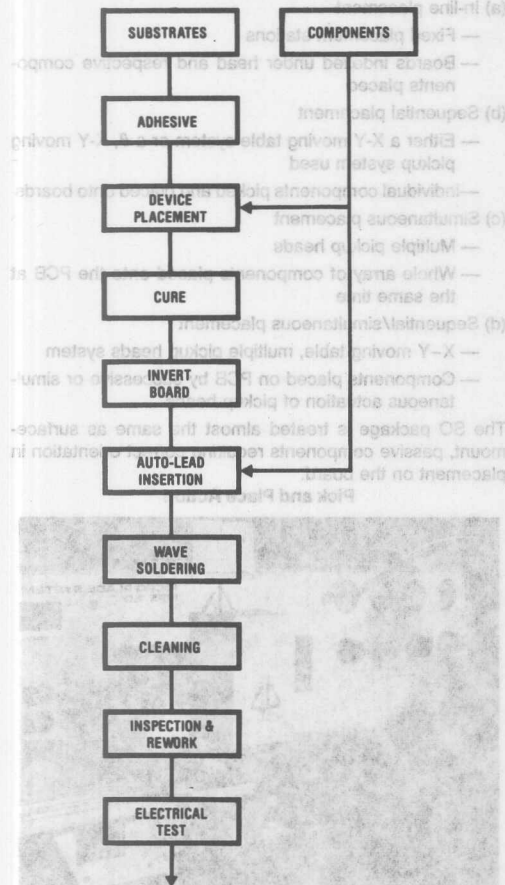
PRODUCTION FLOW

Basic Surface-Mount Production Flow



TL/F/8766-4

Mixed Surface-Mount and Axial-Leaded Insertion Components Production Flow



TL/F/8766-5

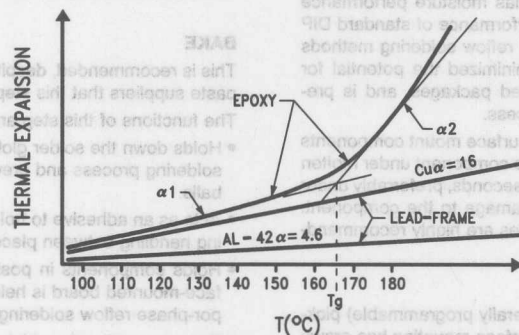
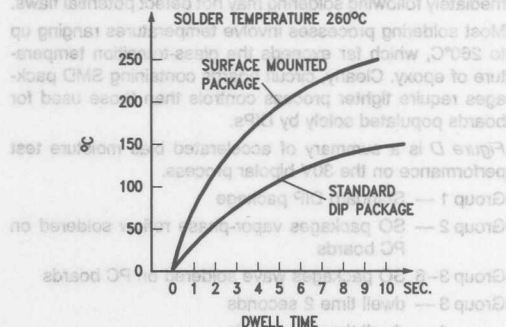


FIGURE C

TL/F/8766-26

Thermal stress of the packages during surface-mounting processing is more severe than during standard DIP-PC board mounting processes. Figure B illustrates package temperature versus wave soldering dwell time for surface mounted packages (components are immersed into the molten solder) and the standard DIP wave soldering process. (Only leads of the package are immersed into the molten solder).



TL/F/8766-6

FIGURE B

For an ideal package, the thermal expansion rate of the encapsulant should match that of the leadframe material in order for the package to maintain mechanical integrity during the soldering process. Unfortunately, a perfect match of thermal expansion rates with most presently used packaging materials is scarce. The problem lies primarily with the epoxy compound.

Normally, thermal expansion rates for epoxy encapsulant and metal lead frame materials are linear and remain fairly close at temperatures approaching 160 $^{\circ}\text{C}$, Figure C. At lower temperatures the difference in expansion rate of the two materials is not great enough to cause interface separation. However, when the package reaches the glass-transition temperature (T_g) of epoxy (typically 160–165 $^{\circ}\text{C}$), the thermal expansion rate of the encapsulant increases sharply, and the material undergoes a transition into a plastic state. The epoxy begins to expand at a rate three times or more greater than the metal leadframe, causing a separation at the interface.

even solder can enter the cavity created by the separation and become entrapped when the material cools. These contaminants can eventually diffuse into the interior of the package, especially in the presence of moisture. The result is die contamination, excessive leakage, and even catastrophic failure. Unfortunately, electrical tests performed immediately following soldering may not detect potential flaws. Most soldering processes involve temperatures ranging up to 260°C, which far exceeds the glass-transition temperature of epoxy. Clearly, circuit boards containing SMD packages require tighter process controls than those used for boards populated solely by DIPs.

Figure D is a summary of accelerated bias moisture test performance on the 30V bipolar process.

Group 1 — Standard DIP package

Group 2 — SO packages vapor-phase reflow soldered on PC boards

Group 3–6 SO packages wave soldered on PC boards

Group 3 — dwell time 2 seconds

4 — dwell time 4 seconds

5 — dwell time 6 seconds

6 — dwell time 10 seconds

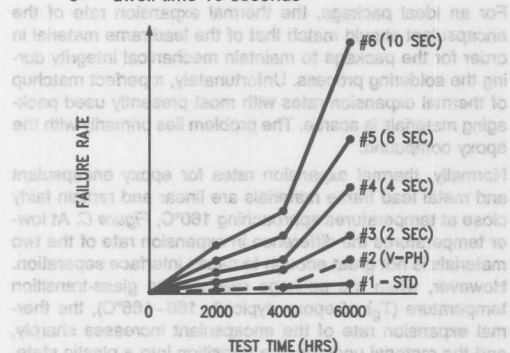


FIGURE D
TL/F/8766-7

It is clear based on the data presented that SO packages soldered onto PC boards with the vapor phase reflow process have the best long term bias moisture performance and this is comparable to the performance of standard DIP packages. The key advantage of reflow soldering methods is the clean environment that minimized the potential for contamination of surface mounted packages, and is preferred for the surface-mount process.

When wave soldering is used to surface mount components on the board, the dwell time of the component under molten solder should be no more than 4 seconds, preferably under 2 seconds in order to prevent damage to the component. Non-Halide, or (organic acid) fluxes are highly recommended.

PICK AND PLACE

The choice of automatic (all generally programmable) pick-and-place machines to handle surface mounting has grown considerably, and their selection is based on individual needs and degree of sophistication.

(a) In-line placement

- Fixed placement stations
- Boards indexed under head and respective components placed

(b) Sequential placement

- Either a X-Y moving table system or a θ , X-Y moving pickup system used
- Individual components picked and placed onto boards

(c) Simultaneous placement

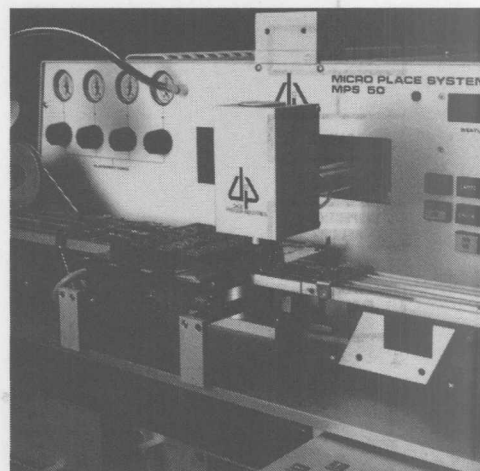
- Multiple pickup heads
- Whole array of components placed onto the PCB at the same time

(d) Sequential/simultaneous placement

- X-Y moving table, multiple pickup heads system
- Components placed on PCB by successive or simultaneous actuation of pickup heads

The SO package is treated almost the same as surface-mount, passive components requiring correct orientation in placement on the board.

Pick and Place Action



TL/F/8766-8

BAKE

This is recommended, despite claims made by some solder paste suppliers that this step be omitted.

The functions of this step are:

- Holds down the solder globules during subsequent reflow soldering process and prevents expulsion of small solder balls.
- Acts as an adhesive to hold the components in place during handling between placement to reflow soldering.
- Holds components in position when a double-sided surface-mounted board is held upside down going into a vapor-phase reflow soldering operation.
- Removes solvents which might otherwise contaminate other equipment.
- Initiates activator cleaning of surfaces to be soldered.
- Prevents moisture absorption.

The process is moreover very simple. The usual schedule is about 20 minutes in a 65°C–95°C (dependent on solvent system of solder paste) oven with adequate venting. Longer bake time is not recommended due to the following reasons:

- The flux will degrade and affect the characteristics of the paste.
- Solder globules will begin to oxidize and cause solderability problems.
- The paste will creep and after reflow, may leave behind residues between traces which are difficult to remove and vulnerable to electro-migration problems.

REFLOW SOLDERING

There are various methods for reflowing the solder paste, namely:

- Hot air reflow
- Infrared heating (furnaces)
- Convectional oven heating
- Vapor-phase reflow soldering
- Laser soldering

For SO applications, hot air reflow/infrared furnace may be used for low-volume production or prototype work, but vapor-phase soldering reflow is more efficient for consistency and speed. Oven heating is not recommended because of "hot spots" in the oven and uneven melting may result. Laser soldering is more for specialized applications and requires a great amount of investment.

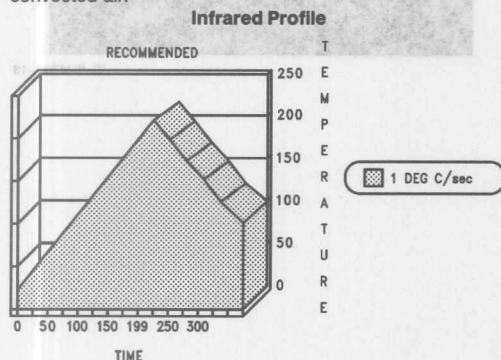
HOT GAS REFLOW/INFRARED HEATING

A hand-held or table-mount air blower (with appropriate orifice mask) can be used.

The boards are preheated to about 100°C and then subjected to an air jet at about 260°C. This is a slow process and results may be inconsistent due to various heat-sink properties of passive components.

INFRARED REFLOW SOLDERING

Use of an infrared furnace is currently the most popular method to automate mass reflow, the heating is promoted by use of IR lamps or panels. Early objections to this method were that certain materials may heat up at different rates under IR radiation and could result in damage to those components (usually sockets and connectors). This has been minimized by using far-infrared (non-focused) systems and convected air.



VAPOR-PHASE REFLOW SOLDERING

Currently the most popular and consistent method, vapor-phase soldering utilizes a fluoroinert fluid with excellent heat-transfer properties to heat up components until the solder paste reflows. The maximum temperature is limited by the vapor temperature of the fluid.

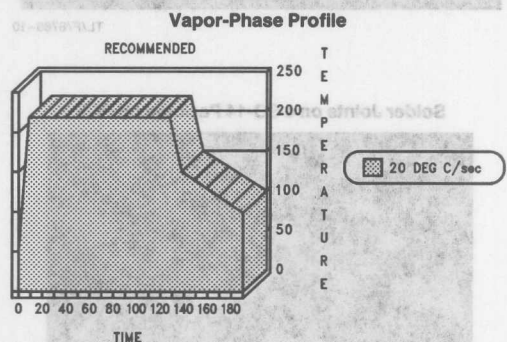
The commonly used fluids (supplied by 3M Corp) are:

- FC-70, 215°C vapor (most applications) or FX-38
- FC-71, 253°C vapor (low-lead or tin-plate)

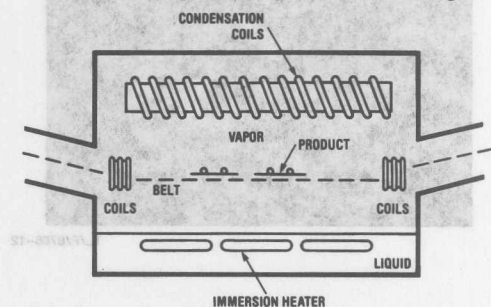
HTC, Concord, CA, manufactures equipment that utilizes this technique, with two options:

- Batch systems, where boards are lowered in a basket and subjected to the vapor from a tank of boiling fluid.
- In-line conveyORIZED systems, where boards are placed onto a continuous belt which transports them into a concealed tank where they are subjected to an environment of hot vapor.

Dwell time in the vapor is generally on the order of 15–30 seconds (depending on the mass of the boards and the loading density of boards on the belt).



In-Line Conveyorized Vapor-Phase Soldering



The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as cerdips, metal cans and TO-5 cans with glass seals, have also been tested.

Vapor-Phase Furnace



TL/F/8766-10

Solder Joints on a SO-14 Package on PCB

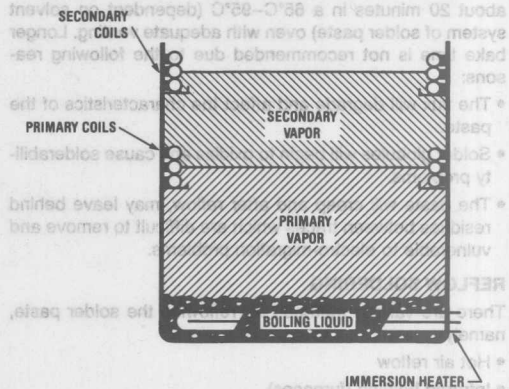


TL/F/8766-12

TL/F/8766-8

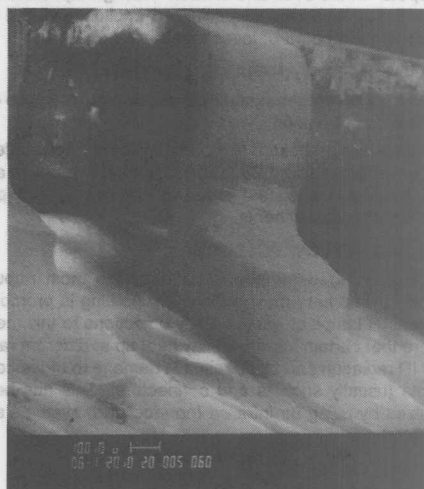
The question of thermal shock is asked frequently because of the relatively sharp increase in component temperature from room temperature to 215°C. SO packages mounted on representative boards have been tested and have shown little effect on the integrity of the packages. Various packages, such as ceramic, metal cans and TO-8 cans with glass seals, have also been tested.

Batch-Fed Production Vapor-Phase Soldering Unit

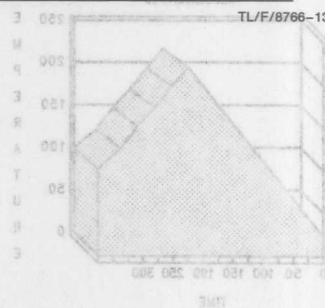


TL/F/8766-11

Solder Joints on a SO-14 Package on PCB



TL/F/8766-13



TL/F/8766-14

PRINTED CIRCUIT BOARD

The SO package is molded out of clean, thermoset plastic compound and has no particular compatibility problems with most printed circuit board substrates.

The package can be reliably mounted onto substrates such as:

- G10 or FR4 glass/resin
- FR5 glass/resin systems for high-temperature applications
- Polyimide boards, also high-temperature applications
- Ceramic substrates

General requirements for printed circuit boards are:

- Mounting pads should be solder-plated whenever applicable.
- Solder masks are commonly used to prevent solder bridging of fine lines during soldering.

The mask also protects circuits from processing chemical contamination and corrosion.

If coated over pre-tinned traces, residues may accumulate at the mask/trace interface during subsequent reflow, leading to possible reliability failures.

Recommended application of solder resist on bare, clean traces prior to coating exposed areas with solder.

General requirements for solder mask:

- Good pattern resolution.
- Complete coverage of circuit lines and resistance to flaking during soldering.
- Adhesion should be excellent on substrate material to keep off moisture and chemicals.
- Compatible with soldering and cleaning requirements.

SOLDER PASTE SCREEN PRINTING

With the initial choice of printed circuit lithographic design and substrate material, the first step in surface mounting is the application of solder paste.

The typical lithographic "footprints" for SO packages are illustrated below. Note that the 0.050" lead center-center spacing is not easily managed by commercially-available air pressure, hand-held dispensers.

Using a stainless-steel, wire-mesh screen stencilled with an emulsion image of the substrate pads is by far the most

common and well-tried method. The paste is forced through the screen by a V-shaped plastic squeegee in a sweeping manner onto the board placed beneath the screen.

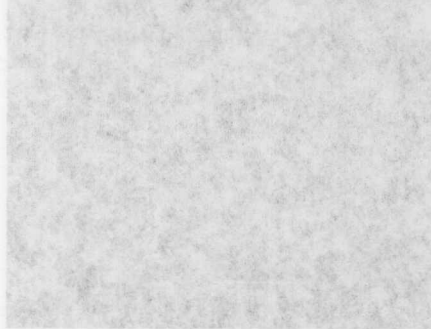
The setup for SO packages has no special requirement from that required by other surface-mounted, passive components. Recommended working specifications are:

- Use stainless-steel, wire-mesh screens, #80 or #120, wire diameter 2.6 mils. Rule of thumb: mesh opening should be approximately 2.5–5 times larger than the average particle size of paste material.
- Use squeegee of Durometer 70.
- Experimentation with squeegee travel speed is recommended, if available on machine used.
- Use solder paste of mesh 200–325.
- Emulsion thickness of 0.005" usually used to achieve a solder paste thickness (wet) of about 0.008" typical.
- Mesh pattern should be 90 degrees, square grid.
- Snap-off height of screen should not exceed $\frac{1}{8}$ ", to avoid damage to screens and minimize distortion.

SOLDER PASTE

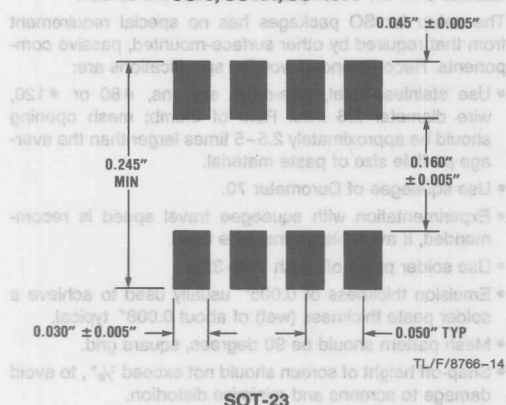
Selection of solder paste tends to be confusing, due to numerous formulations available from various manufacturers. In general, the following guidelines are sufficient to qualify a particular paste for production:

- Particle sizes (see following photographs). Mesh 325 (approximately 45 microns) should be used for general purposes, while larger (solder globules) particles are preferred for leadless components (LCC). The larger particles can easily be used for SO packages.
- Uniform particle distribution. Solder globules should be spherical in shape with uniform diameters and minimum amount of elongation (visual under 100/200 \times magnification). Uneven distribution causes uneven melting and subsequent expulsion of smaller solder balls away from their proper sites.
- Composition, generally 60/40 or 63/37 Sn/Pb. Use 62/36 Sn/Pb with 2% Ag in the presence of Au on the soldering area. This formulation reduces problems of metal leaching from soldering pads.
- RMA flux system usually used.
- Use paste with approximately 88–90% solids.

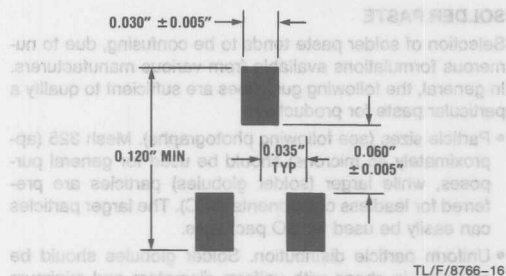


RECOMMENDED SOLDER PADS FOR SO PACKAGES

SO-8, SO-14, SO-16

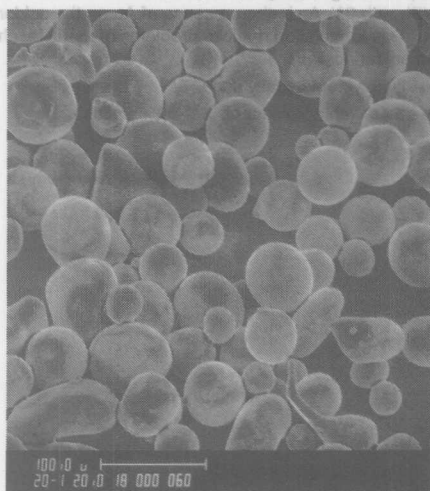


SOT-23



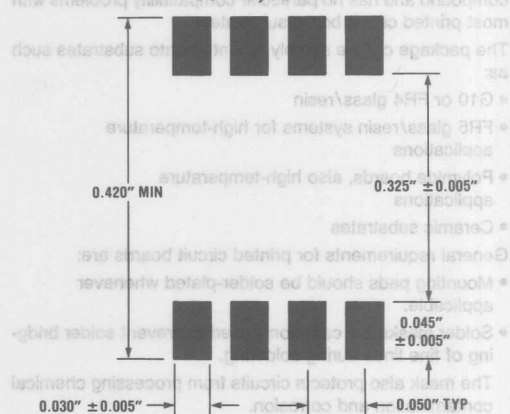
Comparison of Particle Size/Shape of Various Solder Pastes

200 × Alpha (62/36/2)

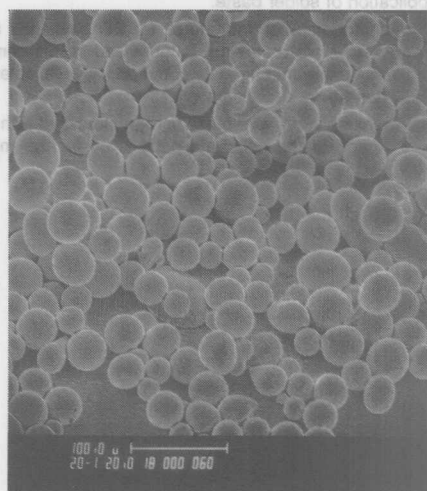


TL/F/8766-17

SO-16L, SO-20



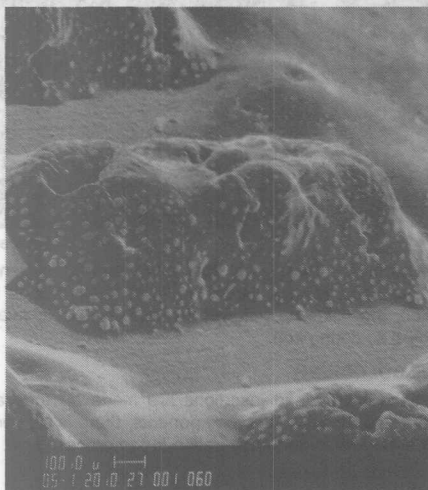
200 × Kester (63/37)



TL/E/8766-18

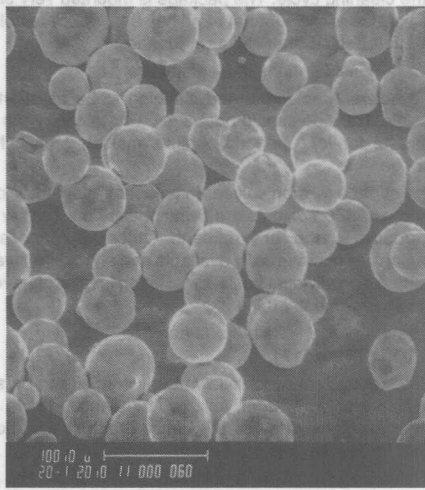
Comparison of Particle Size/Shape of Various Solder Pastes (Continued)

Solder Paste Screen on Pads



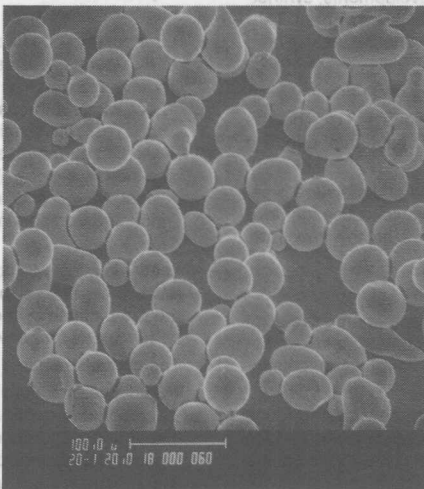
TL/F/8766-19

200 × Fry Metal (63/37)

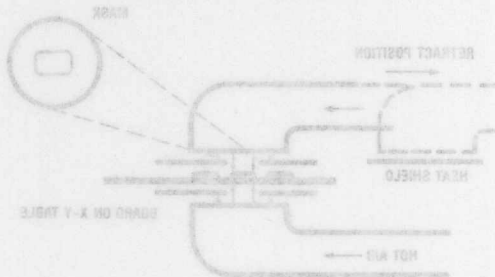


TL/F/8766-20

200 ESL (63/37)



TL/F/8766-21



TL/F/8766-22

components are placed in position, but not soldered. Instead, a top of adhesive about 0.005 inch high with diameter not exceeding 0.010 inch is used to hold down the package and then proceed to solder. The assembly is then passed over a hot air gun. Note that the solder is not applied to the underside of the component.

There is a problem after soldering in the lead of the reaction components. A board specially designed to localize access to the thin blade.

for wave soldering are: to be 240-260°C. The dwell time of molten solder to be short (preferably less than 10 seconds) to prevent damage to most components.

(Organic Acid) flux or more aggressive OA fluxes are applied by either dipping or spraying on boards prior to preheat and soldering. Cleaning procedures are also more difficult. When OA flux is used, as the entire board has been treated by flux (flux like solder paste, which is more or less localized). Non-oxidative OA fluxes are highly recommended.

* Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.

* Due to the close lead spacing (0.050" vs 0.100" for dual-in-line packages), bridging or traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual wave soldering.

form

to the surface of the substrate and has a tendency to collect residue left behind after reflow soldering.

Important considerations in cleaning are:

- Time between soldering and cleaning to be as short as possible. Residue should not be allowed to solidify on the substrate for long periods of time, making it difficult to dislodge.
- A low surface tension solvent (high penetration) should be employed. CFC solvents are being phased out as they are hazardous to the environment. Other approaches to cleaning are commercially available and should be investigated on an individual basis considering local and government environmental rules.

Preleto or 1,1,1-Trichloroethane
Kester 5120/5121

- A defluxer system which allows the workpiece to be subjected to a solvent vapor, followed by a rinse in pure solvent and a high-pressure spray lance are the basic requirements for low-volume production.
- For volume production, a conveyORIZED, multiple hot solvent spray/jet system is recommended.
- Rosin, being a natural occurring material, is not readily soluble in solvents, and has long been a stumbling block to the cleaning process. In recent developments, synthetic flux (SA flux), which is readily soluble in Freon TMS solvent, has been developed. This should be explored where permissible.

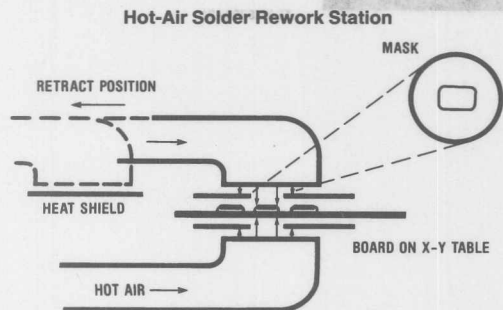
The dangers of an inadequate cleaning cycle are:

- Ion contamination, where ionic residue left on boards would cause corrosion to metallic components, affecting the performance of the board.
- Electro-migration, where ionic residue and moisture present on electrically-biased boards would cause dendritic growth between close spacing traces on the substrate, resulting in failures (shorts).

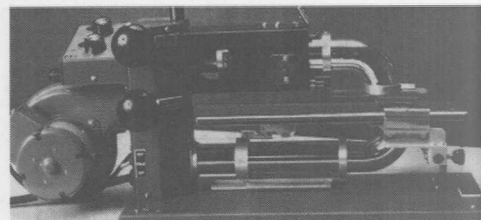
REWORK

Should there be a need to replace a component or re-align a previously disturbed component, a hot air system with appropriate orifice masking to protect surrounding components may be used.

When rework is necessary in the field, specially-designed tweezers that thermally heat the component may be used to remove it from its site. The replacement can be fluxed at the



TL/F/8766-22



TL/F/8766-23

lead tips or, if necessary, solder paste can be dispensed onto the pads using a varimeter. After being placed into position, the solder is reflowed by a hot-air jet or even a standard soldering iron.

WAVE SOLDERING

In a case where lead insertions are made on the same board as surface-mounted components, there is a need to include a wave-soldering operation in the process flow.

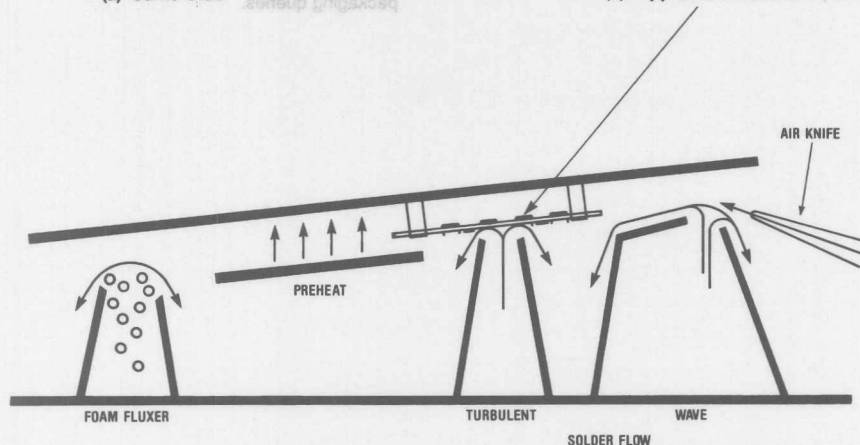
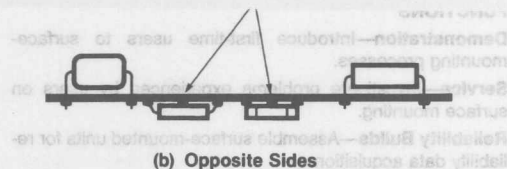
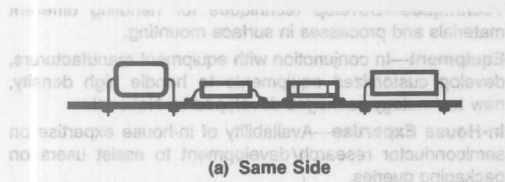
Two options are used:

- Surface mounted components are placed and vapor phase reflowed before auto-insertion of remaining components. The board is carried over a standard wave-solder system and the underside of the board (only lead-inserted leads) soldered.
- Surface-mounted components are placed in position, but no solder paste is used. Instead, a drop of adhesive about 5 mils maximum in height with diameter not exceeding 25% width of the package is used to hold down the package. The adhesive is cured and then proceeded to auto-insertion on the reverse side of the board (surface-mounted side facing down). The assembly is then passed over a "dual wave" soldering system. Note that the surface-mounted components are immersed into the molten solder.

Lead trimming will pose a problem after soldering in the latter case, unless the leads of the insertion components are pre-trimmed or the board specially designed to localize certain areas for easy access to the trim blade.

The controls required for wave soldering are:

- Solder temperature to be 240–260°C. The dwell time of components under molten solder to be short (preferably kept under 2 seconds), to prevent damage to most components and semiconductor devices.
- RMA (Rosin Mildly Activated) flux or more aggressive OA (Organic Acid) flux are applied by either dipping or foam fluxing on boards prior to preheat and soldering. Cleaning procedures are also more difficult (aqueous, when OA flux is used), as the entire board has been treated by flux (unlike solder paste, which is more or less localized). Non-halide OA fluxes are highly recommended.
- Preheating of boards is essential to reduce thermal shock on components. Board should reach a temperature of about 100°C just before entering the solder wave.
- Due to the closer lead spacings (0.050" vs 0.100" for dual-in-line packages), bridging of traces by solder could occur. The reduced clearance between packages also causes "shadowing" of some areas, resulting in poor solder coverage. This is minimized by dual-wave solder systems.



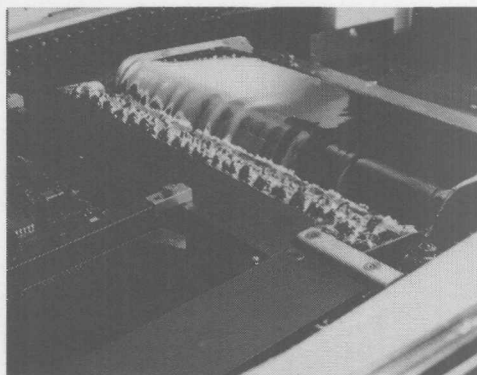
TL/F/8766-24

A typical dual-wave system is illustrated below, showing the various stages employed. The first wave typically is in turbulence and given a transverse motion (across the motion of the board). This covers areas where "shadowing" occurs. A second wave (usually a broad wave) then proceeds to perform the standard soldering. The departing edge from the solder is such to reduce "icicles," and is still further reduced by an air knife placed close to the final soldering step. This air knife will blow off excess solder (still in the fluid stage) which would otherwise cause shorts (bridging) and solder bumps.

AQUEOUS CLEANING

- For volume production, a conveyORIZED system is often used with a heated recirculating spray wash (water temperature 130°C), a final spray rinse (water temperature 45–55°C), and a hot (120°C) air/air-knife drying section.
- For low-volume production, the above cleaning can be done manually, using several water rinses/tanks. Fast-drying solvents, like alcohols that are miscible with water, are sometimes used to help the drying process.
- Neutralizing agents which will react with the corrosive materials in the flux and produce material readily soluble in water may be used; the choice depends on the type of flux used.
- Final rinse water should be free from chemicals which are introduced to maintain the biological purity of the water. These materials, mostly chlorides, are detrimental to the assemblies cleaned because they introduce a fresh amount of ionizable material.

Dual Wave



TL/F/8766-25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

- Complete coating over components and solder joints.
- Thixotropic material which will not flow under the packages or fill voids, otherwise will introduce stress on solder joints on expansion.
- Compatibility and possess excellent adhesion with PCB material/components.
- Silicones are recommended where permissible in application.

SMD Lab Support

FUNCTIONS

Demonstration—Introduce first-time users to surface-mounting processes.

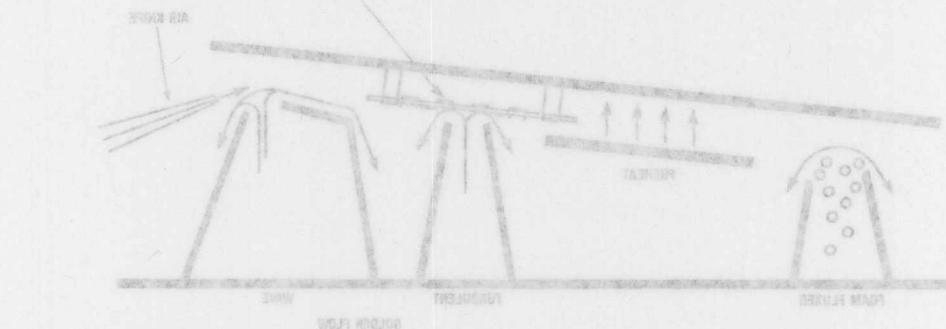
Service—Investigate problems experienced by users on surface mounting.

Reliability Builds—Assemble surface-mounted units for reliability data acquisition.

Techniques—Develop techniques for handling different materials and processes in surface mounting.

Equipment—In conjunction with equipment manufacturers, develop customized equipments to handle high density, new technology packages developed by National.

In-House Expertise—Availability of in-house expertise on semiconductor research/development to assist users on packaging queries.



T/LP/3708-24

Dual Wave



T/LP/3708-25

CONFORMAL COATING

Conformal coating is recommended for high-reliability PCBs to provide insulation resistance, as well as protection against contamination and degradation by moisture.

Requirements:

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- Compatibility and possess excellent adhesion with PCB materials/components.
- Silicones are recommended where permissible in application.

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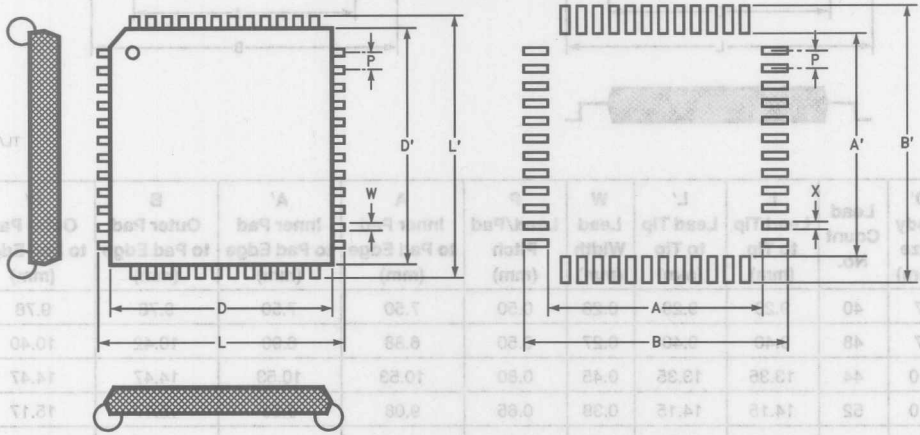
Land Pattern Recommendations

The following land pattern recommendations are provided as guidelines for board layout and assembly purposes.

These recommendations cover the following National Semiconductor packages: PLCC, PQFP, SOP, SSOP and TSOP.

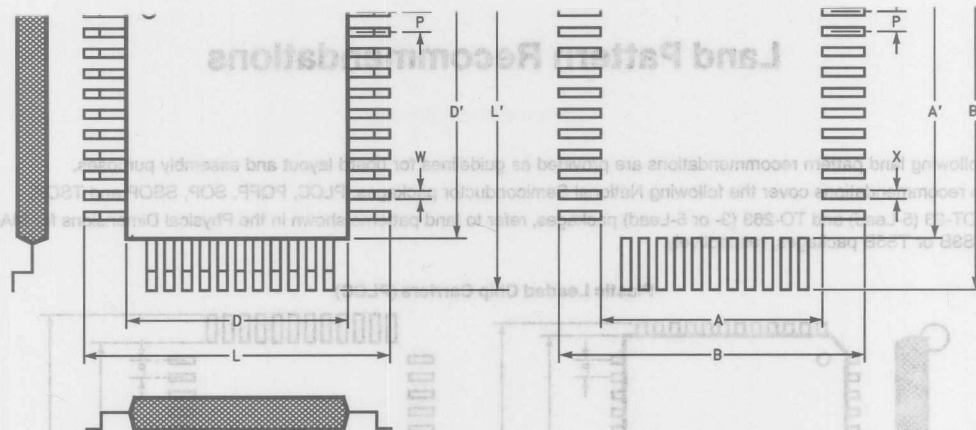
For SOT-23 (5-Lead) and TO-263 (3- or 5-Lead) packages, refer to land patterns shown in the Physical Dimensions for MA05A and TS3B or TS5B packages, respectively.

Plastic Leaded Chip Carriers (PLCC)



| D Body Size (mm) | D' Body Size (mm) | Lead Count No. | L Lead Tip to Tip (mm) | L' Lead Tip to Tip (mm) | W Lead Width (mm) | P Lead/Pad Pitch (mm) | A Inner Pad to Pad Edge (mm) | A' Inner Pad to Pad Edge (mm) | B Outer Pad to Pad Edge (mm) | B' Outer Pad to Pad Edge (mm) | X Land Width (mm) |
|---------------------------|----------------------------|----------------------|---------------------------------|----------------------------------|----------------------------|--------------------------------|---------------------------------------|--|---------------------------------------|--|----------------------------|
| 8.89 | 8.89 | 20 | 10.03 | 10.03 | 0.53 | 1.27 | 6.73 | 6.73 | 10.80 | 10.80 | 0.63 |
| 11.43 | 11.43 | 28 | 12.57 | 12.57 | 0.53 | 1.27 | 9.27 | 9.27 | 13.34 | 13.34 | 0.63 |
| 11.43 | 14.05 | 32 | 12.57 | 15.11 | 0.53 | 1.27 | 9.27 | 12.00 | 13.34 | 16.00 | 0.63 |
| 16.51 | 16.51 | 44 | 17.65 | 17.65 | 0.53 | 1.27 | 14.35 | 14.35 | 18.42 | 18.42 | 0.63 |
| 19.05 | 19.05 | 52 | 20.19 | 20.19 | 0.53 | 1.27 | 16.89 | 16.89 | 20.96 | 20.96 | 0.63 |
| 24.13 | 24.13 | 68 | 25.27 | 25.27 | 0.53 | 1.27 | 21.97 | 21.97 | 26.04 | 26.04 | 0.63 |
| 29.21 | 29.21 | 84 | 30.35 | 30.35 | 0.53 | 1.27 | 27.05 | 27.05 | 31.12 | 31.12 | 0.63 |

Land Pattern Recommendation

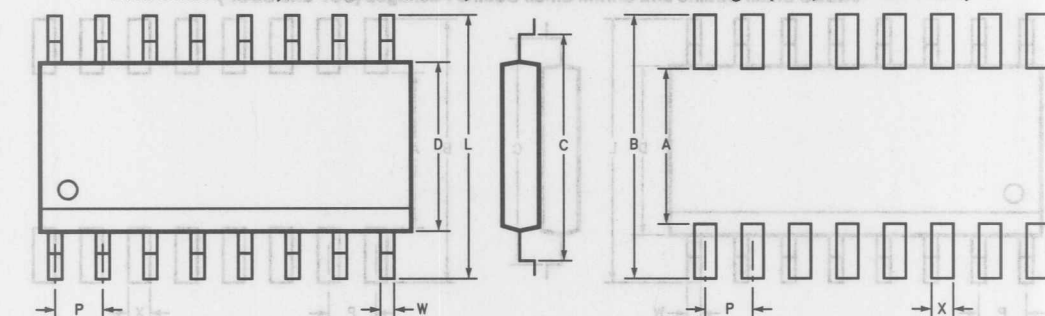


TL/P/11811-2

| D Body Size (mm) | D' Body Size (mm) | Lead Count No. | L Lead Tip to Tip (mm) | L' Lead Tip to Tip (mm) | W Lead Width (mm) | P Lead/Pad Pitch (mm) | A Inner Pad to Pad Edge (mm) | A' Inner Pad to Pad Edge (mm) | B Outer Pad to Pad Edge (mm) | B' Outer Pad to Pad Edge (mm) | X Land Width (mm) |
|---------------------------|----------------------------|----------------------|---------------------------------|----------------------------------|----------------------------|--------------------------------|---------------------------------------|--|---------------------------------------|--|----------------------------|
| 7 | 7 | 40 | 9.29 | 9.29 | 0.26 | 0.50 | 7.50 | 7.50 | 9.78 | 9.78 | 0.30 |
| 7 | 7 | 48 | 9.40 | 9.40 | 0.27 | 0.50 | 6.88 | 6.90 | 10.42 | 10.40 | 0.32 |
| 10 | 10 | 44 | 13.35 | 13.35 | 0.45 | 0.80 | 10.53 | 10.53 | 14.47 | 14.47 | 0.55 |
| 10 | 10 | 52 | 14.15 | 14.15 | 0.38 | 0.65 | 9.08 | 9.08 | 15.17 | 15.17 | 0.43 |
| 12 | 12 | 64 | 14.00 | 14.00 | 0.38 | 0.65 | 11.48 | 11.48 | 15.02 | 15.02 | 0.43 |
| 14 | 14 | 80 | 18.15 | 18.15 | 0.38 | 0.65 | 13.08 | 13.08 | 19.17 | 19.17 | 0.43 |
| 14 | 20 | 80 | 17.80 | 23.80 | 0.35 | 0.80 | 13.50 | 19.50 | 18.50 | 24.50 | 0.40 |
| 14 | 14 | 100 | 17.45 | 17.45 | 0.30 | 0.50 | 13.08 | 13.08 | 18.47 | 18.47 | 0.35 |
| 14 | 20 | 100 | 17.80 | 23.80 | 0.30 | 0.65 | 13.50 | 19.50 | 18.50 | 24.50 | 0.35 |
| 20 | 20 | 100 | 24.30 | 18.30 | 0.40 | 0.65 | 21.28 | 15.28 | 25.32 | 19.32 | 0.45 |
| 24 | 24 | 132 | 24.21 | 24.21 | 0.30 | 0.64 | 21.67 | 21.67 | 25.23 | 25.23 | 0.40 |
| 28 | 28 | 120 | 32.15 | 32.15 | 0.45 | 0.80 | 27.88 | 27.88 | 33.17 | 33.17 | 0.55 |
| 28 | 28 | 128 | 31.45 | 31.45 | 0.45 | 0.80 | 28.03 | 28.03 | 32.47 | 32.47 | 0.55 |
| 28 | 28 | 144 | 32.15 | 32.15 | 0.38 | 0.65 | 28.03 | 28.03 | 33.17 | 33.17 | 0.43 |
| 28 | 28 | 160 | 32.40 | 32.40 | 0.38 | 0.65 | 29.48 | 29.48 | 33.42 | 33.42 | 0.43 |
| 28 | 28 | 208 | 30.60 | 30.60 | 0.30 | 0.50 | 28.08 | 28.08 | 31.62 | 31.62 | 0.35 |

| JEDEC Small Outline and Shrink Small Outline Packages (SOP and SSOP) | | | | | | | | | |
|--|----------------------|--------------------------------------|---------------------------------|----------------------------|--------------------------------|---------------------------------------|---------------------------------------|---------------------------|--|
| | | | | | | | | | |
| D Body Size (in) | Lead Count No. | C Shoulder to Shoulder (in) | L Lead Tip to Tip (in) | W Lead Width (in) | P Lead/Pad Pitch (in) | A Inner Pad to Pad Edge (in) | B Outer Pad to Pad Edge (in) | X Pad Width (in) | |
| SOP | | | | | | | | | |
| 0.150 | 8 | 0.144 | 0.244 | 0.020 | 0.050 | 0.094 | 0.294 | 0.028 | |
| 0.150 | 14 | 0.144 | 0.244 | 0.020 | 0.050 | 0.094 | 0.294 | 0.028 | |
| 0.150 | 16 | 0.144 | 0.244 | 0.020 | 0.050 | 0.094 | 0.294 | 0.028 | |
| 0.300 | 14 | 0.3300 | 0.4100 | 0.0190 | 0.0500 | 0.2800 | 0.4600 | 0.0270 | |
| 0.300 | 16 | 0.3300 | 0.4100 | 0.0190 | 0.0500 | 0.2800 | 0.4600 | 0.0270 | |
| 0.300 | 20 | 0.3300 | 0.4100 | 0.0190 | 0.0500 | 0.2800 | 0.4600 | 0.0270 | |
| 0.300 | 24 | 0.3300 | 0.4100 | 0.0190 | 0.0500 | 0.2800 | 0.4600 | 0.0270 | |
| 0.300 | 28 | 0.3300 | 0.4100 | 0.0190 | 0.0500 | 0.2800 | 0.4600 | 0.0270 | |
| SSOP | | | | | | | | | |
| 0.150 | 20 | 0.185 | 0.241 | 0.010 | 0.025 | 0.145 | 0.281 | 0.014 | |
| 0.150 | 24 | 0.185 | 0.241 | 0.010 | 0.025 | 0.145 | 0.281 | 0.014 | |
| 0.300 | 48 | 0.340 | 0.420 | 0.012 | 0.025 | 0.300 | 0.460 | 0.016 | |
| 0.300 | 56 | 0.340 | 0.420 | 0.012 | 0.025 | 0.300 | 0.460 | 0.016 | |

EIAJ Small Outline, Shrink Small Outline, and Thin Small Outline Packages (SOP, SSOP and TSOP)



6-11811-1

TL/P/11811-4

| D Body Size (mm) | Lead Count No. | C Shoulder to Shoulder (mm) | L Lead Tip to Tip (mm) | W Lead Width (mm) | P Lead/Pad Pitch (mm) | A Inner Pad to Pad Edge (mm) | B Outer Pad to Pad Edge (mm) | X Pad Width (mm) |
|---------------------------|----------------------|--------------------------------------|---------------------------------|----------------------------|--------------------------------|---------------------------------------|---------------------------------------|---------------------------|
| SOP TYPE II | | | | | | | | |
| 5.300 | 14 | 6.280 | 8.000 | 0.400 | 1.270 | 5.010 | 9.270 | 0.600 |
| 5.300 | 16 | 6.280 | 8.000 | 0.400 | 1.270 | 5.010 | 9.270 | 0.600 |
| 5.300 | 20 | 6.280 | 8.000 | 0.400 | 1.270 | 5.010 | 9.270 | 0.600 |
| SSOP TYPE II | | | | | | | | |
| 5.300 | 20 | 6.600 | 8.100 | 0.400 | 0.650 | 5.584 | 9.116 | 0.451 |
| 5.300 | 24 | 6.600 | 8.100 | 0.400 | 0.650 | 5.584 | 9.116 | 0.451 |
| SSOP TYPE III | | | | | | | | |
| 7.500 | 40 | 8.900 | 10.500 | 0.350 | 0.650 | 7.884 | 11.516 | 0.452 |
| TSOP TYPE I | | | | | | | | |
| 18.500 | 32 | 19.000 | 20.200 | 0.250 | 0.500 | 17.984 | 21.216 | 0.301 |



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Bookshelf
Distributors

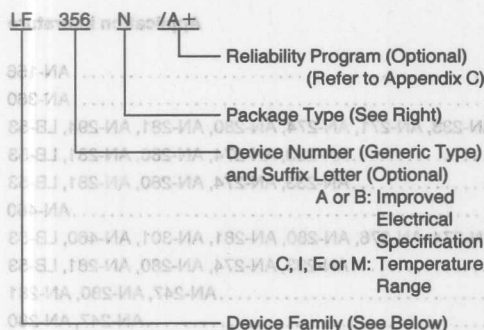
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Appendix A General Product Marking & Code Explanation



Device Family

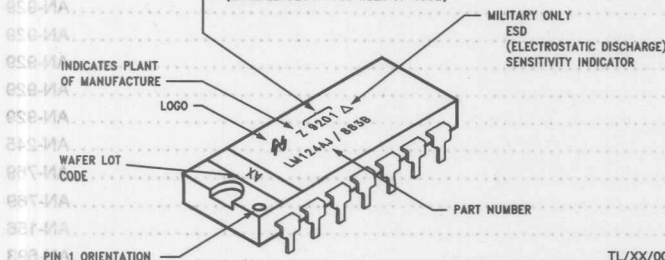
| | |
|-----|----------------------------|
| ADC | Data Conversion |
| AF | Active Filter |
| AH | Analog Switch (Hybrid) |
| DAC | Data Conversion |
| DMS | Digital (Monolithic) |
| HS | Hybrid |
| LF | Linear (BI-FET™) |
| LH | Linear (Hybrid) |
| LM | Linear (Monolithic) |
| LMC | Linear CMOS |
| LMD | Linear DMOS |
| LP | Linear (Low Power) |
| LPC | Linear CMOS (Low Power) |
| MF | Linear (Monolithic Filter) |
| LMF | Linear Monolithic Filter |

Package Type

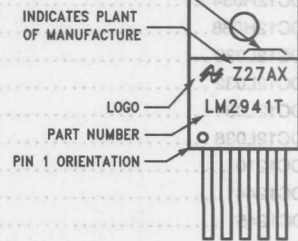
| | |
|---------|--|
| D | Glass/Metal DIP |
| E | Ceramic Leadless Chip Carrier (LCC) |
| F | Glass/Metal Flat Pak (1/4" x 1/4") |
| G | 12 Lead TO-8 Metal Can (M/C) |
| H | Multi-Lead Metal Can (M/C) |
| H-05 | 4 Lead M/C (TO-5) } Shipped with |
| H-46 | 4 Lead M/C (TO-46) } Thermal Shield |
| J | Lo-Temp Ceramic DIP |
| J-8 | 8 Lead Ceramic DIP ("MiniDIP") |
| J-14 | 14 Lead Ceramic DIP (-14 used only when product is also available in -8 pkg). |
| K | TO-3 M/C in Steel, except LM309K which is shipped in Aluminum |
| KC | TO-3 M/C (Aluminum) |
| K Steel | TO-3 M/C (Steel) |
| M | Small Outline Package |
| M3 | 3-Lead Small Outline Package |
| M5 | 5-Lead Small Outline Package |
| N | Molded DIP (EPOXY B) |
| N-01 | Molded DIP (Epoxy B) with Staggered Leads |
| N-8 | 8 Lead Molded DIP (Epoxy B) ("Mini-DIP") |
| N-14 | 14 Lead Molded DIP (Epoxy B) (-14 used only when product is also available in -8 pkg). |
| P | 3 Lead TO-202 Power Pkg |
| Q | Cerdip with UV Window |
| S | 3,5,11, & 15 Lead TO-263 Surf. Mt. Power Pkg |
| T | 3,5,11,15 & 23 Lead TO-220 PWR Pkg (Epoxy B) |
| V | Multi-lead Plastic Chip Carrier (PCC) |
| W | Lo-Temp Ceramic Flat Pak |
| WM | Wide Body Small Outline Package |

DATE CODE
NON-MILITARY
2ND DIGIT - CALENDAR YEAR
3RD & 4TH DIGITS - CALENDAR WORK WEEK

MILITARY - 883 & M38510
1ST & 2ND DIGITS - CALENDAR YEAR
3RD & 4TH DIGITS - CALENDAR WORK WEEK
(EXAMPLE: 9201 = 1ST WEEK OF 1992)



DATE CODE
1ST DIGIT - CALENDAR YEAR
2ND DIGIT - 6-WEEK PERIOD
IN CALENDAR YEAR
3RD & 4TH DIGITS - WAFER LOT CODE



TL/XX/0027-2

TL/XX/0027-3

Appendix B Device/Application Literature Cross-Reference

| Device Number | Package Type | Application Literature |
|---------------|-------------------------------|---|
| ADCXXXX | Glass/Metal DIP | AN-156 |
| ADC80 | Plastic/Metal Flat Pack (QFN) | AN-360 |
| ADC0801 | Plastic/Metal Flat Pack (QFN) | AN-233, AN-271, AN-274, AN-280, AN-281, AN-294, LB-53 |
| ADC0802 | Plastic/Metal Flat Pack (QFN) | AN-233, AN-274, AN-280, AN-281, LB-53 |
| ADC0803 | Plastic/Metal Flat Pack (QFN) | AN-233, AN-274, AN-280, AN-281, LB-53 |
| ADC08031 | Plastic/Metal Flat Pack (QFN) | AN-460 |
| ADC0804 | Plastic/Metal Flat Pack (QFN) | AN-233, AN-274, AN-276, AN-280, AN-281, AN-301, AN-460, LB-53 |
| ADC0805 | Plastic/Metal Flat Pack (QFN) | AN-233, AN-274, AN-280, AN-281, LB-53 |
| ADC0808 | Plastic/Metal Flat Pack (QFN) | AN-247, AN-280, AN-281 |
| ADC0809 | Plastic/Metal Flat Pack (QFN) | AN-247, AN-280 |
| ADC0816 | Plastic/Metal Flat Pack (QFN) | AN-193, AN-247, AN-258, AN-280 |
| ADC0817 | Plastic/Metal Flat Pack (QFN) | AN-247, AN-258, AN-280 |
| ADC0820 | Plastic/Metal Flat Pack (QFN) | AN-237 |
| ADC0831 | Plastic/Metal Flat Pack (QFN) | AN-280, AN-281 |
| ADC0832 | Plastic/Metal Flat Pack (QFN) | AN-280, AN-281 |
| ADC0833 | Plastic/Metal Flat Pack (QFN) | AN-280, AN-281 |
| ADC0834 | Plastic/Metal Flat Pack (QFN) | AN-280, AN-281 |
| ADC0838 | Plastic/Metal Flat Pack (QFN) | AN-280, AN-281 |
| ADC1001 | Plastic/Metal Flat Pack (QFN) | AN-276, AN-280, AN-281 |
| ADC1005 | Plastic/Metal Flat Pack (QFN) | AN-280 |
| ADC10461 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| ADC10462 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| ADC10464 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| ADC10662 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| ADC10664 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| ADC12030 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12032 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12034 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12038 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12H030 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12H032 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12H034 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12H038 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12L030 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12L032 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12L034 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC12L038 | Plastic/Metal Flat Pack (QFN) | AN-929 |
| ADC1210 | Plastic/Metal Flat Pack (QFN) | AN-245 |
| ADC12441 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| ADC12451 | Plastic/Metal Flat Pack (QFN) | AN-769 |
| DACXXXX | Plastic/Metal Flat Pack (QFN) | AN-156 |
| DAC0800 | Plastic/Metal Flat Pack (QFN) | AN-693 |
| DAC0830 | Plastic/Metal Flat Pack (QFN) | AN-284 |

Device/Application Literature Cross-Reference (Continued)

| Device Number | Application Literature |
|---------------|--|
| DAC0831 | AN-271, AN-284 |
| DAC0832 | AN-271, AN-284 |
| DAC1006 | AN-271, AN-275, AN-277, AN-284 |
| DAC1007 | AN-271, AN-275, AN-277, AN-284 |
| DAC1008 | AN-271, AN-275, AN-277, AN-284 |
| DAC1020 | AN-263, AN-269, AN-2293, AN-294, AN-299 |
| DAC1021 | AN-269 |
| DAC1022 | AN-269 |
| DAC1208 | AN-271, AN-284 |
| DAC1209 | AN-271, AN-284 |
| DAC1210 | AN-271, AN-284 |
| DAC1218 | AN-293 |
| DAC1219 | AN-693 |
| DAC1220 | AN-253, AN-269 |
| DAC1221 | AN-269 |
| DAC1222 | AN-269 |
| DAC1230 | AN-284 |
| DAC1231 | AN-271, AN-284 |
| DAC1232 | AN-271, AN-284 |
| DAC1280 | AN-261, AN-263 |
| DH0034 | AN-253 |
| DH0035 | AN-49 |
| INS0070 | AN-260 |
| LF111 | LB-39 |
| LF155 | AN-263, AN-447 |
| LF198 | AN-245, AN-294 |
| LF311 | AN-301 |
| LF347 | AN-256, AN-262, AN-263, AN-265, AN-266, AN-301, AN-344, AN-447, LB-44 |
| LF351 | AN-242, AN-263, AN-266, AN-271, AN-275, AN-293, AN-447, Appendix C |
| LF351A | AN-240 |
| LF351B | Appendix D |
| LF353 | AN-256, AN-258, AN-262, AN-263, AN-266, AN-271, AN-285, AN-293, AN-447, LB-44, Appendix D |
| LF356 | AN-253, AN-258, AN-260, AN-263, AN-266, AN-271, AN-272, AN-275, AN-293, AN-294, AN-295, AN-301, AN-447, AN-693 |
| LF357 | AN-263, AN-447, LB-42 |
| LF398 | AN-247, AN-258, AN-266, AN-294, AN-298, LB-45 |
| LF411 | AN-294, AN-301, AN-344, AN-447 |
| LF412 | AN-272, AN-299, AN-301, AN-344, AN-447 |
| LF441 | AN-301, AN-447 |
| LF13006 | AN-344 |
| LF13007 | AN-344 |
| LF13331 | AN-294, AN-447 |
| LH0002 | AN-13, AN-227, AN-263, AN-272, AN-301 |
| LH0024 | AN-253 |
| LH0032 | AN-242, AN-253 |
| LH0033 | AN-48, AN-227, AN-253 |
| LH0063 | AN-227 |
| LH0070 | AN-301 |
| LH0071 | AN-245 |
| LH0094 | AN-301 |
| LH0101 | AN-261 |

Device/Application Literature Cross-Reference (Continued)

| Device Number | Application Literature |
|---------------|--|
| LH1605 | AN-343 |
| LH2424 | AN-867 |
| LM10 | AN-211, AN-247, AN-258, AN-271, AN-288, AN-299, AN-300, AN-460, AN-693 |
| LM11 | AN-241, AN-242, AN-260, AN-266, AN-271 |
| LM12 | AN-446, AN-693, AN-706 |
| LM101 | AN-4, AN-13, AN-20, AN-24, LB-42, Appendix A |
| LM101A | AN-29, AN-30, AN-31, AN-79, AN-241, AN-711, LB-1, LB-2, LB-4, LB-8, LB-14, LB-16, LB-19, LB-28 |
| LM102 | AN-4, AN-13, AN-30, LB-1, LB-5, LB-6, LB-11 |
| LM103 | AN-110, LB-41 |
| LM105 | AN-23, AN-110, LB-3 |
| LM106 | AN-41, LB-6, LB-12 |
| LM107 | AN-20, AN-31, LB-1, LB-12, LB-19, Appendix A |
| LM108 | AN-29, AN-30, AN-31, AN-79, AN-211, AN-241, LB-14, LB-15, LB-21 |
| LM108A | AN-260, LB-15, LB-19 |
| LM109 | AN-42, LB-15 |
| LM109A | LB-15 |
| LM110 | LB-11, LB-42 |
| LM111 | AN-41, AN-103, LB-12, LB-16, LB-32, LB-39 |
| LM112 | LB-19 |
| LM113 | AN-56, AN-110, LB-21, LB-24, LB-28, LB-37 |
| LM117 | AN-178, AN-181, AN-182, LB-46, LB-47 |
| LM117HV | LB-46, LB-47 |
| LM118 | LB-17, LB-19, LB-21, LB-23, Appendix A |
| LM119 | LB-23 |
| LM120 | AN-182 |
| LM121 | AN-79, AN-104, AN-184, AN-260, LB-22 |
| LM121A | LB-32 |
| LM122 | AN-97, LB-38 |
| LM125 | AN-82 |
| LM126 | AN-82 |
| LM129 | AN-173, AN-178, AN-262, AN-266 |
| LM131 | AN-210, AN-460, Appendix D |
| LM131A | AN-210 |
| LM134 | LB-41, AN-460 |
| LM135 | AN-225, AN-262, AN-292, AN-298, AN-460 |
| LM137 | LB-46 |
| LM137HV | LB-46 |
| LM138 | LB-46 |
| LM139 | AN-74 |
| LM143 | AN-127, AN-271 |
| LM148 | AN-260 |
| LM150 | LB-46 |
| LM158 | AN-116 |
| LM160 | AN-87 |
| LM161 | AN-87, AN-266 |
| LM163 | AN-295 |
| LM194 | AN-222, LB-21 |
| LM195 | AN-110 |
| LM199 | AN-161, AN-260 |
| LM199A | AN-161 |
| LM211 | LB-39 |

Device/Application Literature Cross-Reference (Continued)

| Device Number | Application Literature |
|---------------|---|
| LM231 | AN-210 |
| LM231A | AN-210 |
| LM235 | AN-225 |
| LM239 | AN-74 |
| LM258 | AN-116 |
| LM260 | AN-87 |
| LM261 | AN-87 |
| LM34 | AN-460 |
| LM35 | AN-460 |
| LM301A | AN-178, AN-181, AN-222 |
| LM308 | AN-88, AN-184, AN-272, LB-22, LB-28, Appendix D |
| LM308A | AN-225, LB-24 |
| LM309 | AN-178, AN-182 |
| LM311 | AN-41, AN-103, AN-260, AN-263, AN-288, AN-294, AN-295, AN-307, LB-12, LB-16, LB-18, LB-39 |
| LM313 | AN-263 |
| LM316 | AN-258 |
| LM317 | AN-178, LB-35, LB-46 |
| LM317H | LB-47 |
| LM318 | AN-299, LB-21 |
| LM319 | AN-828, AN-271, AN-293 |
| LM320 | AN-288 |
| LM321 | LB-24 |
| LM324 | AN-88, AN-258, AN-274, AN-284, AN-301, LB-44, AB-25, Appendix C |
| LM329 | AN-256, AN-263, AN-284, AN-295, AN-301 |
| LM329B | AN-225 |
| LM330 | AN-301 |
| LM331 | AN-210, AN-240, AN-265, AN-278, AN-285, AN-311, LB-45, Appendix C, Appendix D |
| LM331A | AN-210, Appendix C |
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| LM335 | AN-225, AN-263, AN-295 |
| LM336 | AN-202, AN-247, AN-258 |
| LM337 | LB-46 |
| LM338 | LB-49, LB-51 |
| LM339 | AN-74, AN-245, AN-274 |
| LM340 | AN-103, AN-182 |
| LM340L | AN-256 |
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| LM348 | AN-202, LB-42 |
| LM349 | LB-42 |
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| LM358A | Appendix D |
| LM359 | AN-278, AB-24 |
| LM360 | AN-87 |
| LM361 | AN-87, AN-294 |
| LM363 | AN-271 |
| LM380 | AN-69, AN-146 |
| LM385 | AN-242, AN-256, AN-301, AN-344, AN-460, AN-693, AN-777 |
| LM386 | LB-54 |
| LM391 | AN-272 |
| LM392 | AN-274, AN-286 |

Device/Application Literature Cross-Reference (Continued)

| Device Number | Application Literature |
|---------------|---|
| LM393 | AN-271, AN-274, AN-293, AN-694 |
| LM394 | AN-262, AN-263, AN-271, AN-293, AN-299, AN-311, LB-52 |
| LM395 | AN-178, AN-181, AN-262, AN-263, AN-266, AN-301, AN-460, LB-28 |
| LM399 | AN-184 |
| LM555 | AN-694, AB-7 |
| LM556 | AB-7 |
| LM565 | AN-46, AN-146 |
| LM566 | AN-146 |
| LM604 | AN-460 |
| LM628 | AN-693, AN-706 |
| LM629 | AN-693, AN-694, AN-706 |
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| LM725 | LB-22 |
| LM741 | AN-79, LB-19, LB-22 |
| LM833 | AN-346 |
| LM1036 | AN-390 |
| LM1202 | AN-867 |
| LM1203 | AN-861 |
| LM1204 | AN-934 |
| LM1458 | AN-116 |
| LM1524 | AN-272, AN-288, AN-292, AN-293 |
| LM1558 | AN-116 |
| LM1578A | AB-30 |
| LM1823 | AN-391 |
| LM1830 | AB-10 |
| LM1865 | AN-390 |
| LM1886 | AN-402 |
| LM1889 | AN-402 |
| LM1894 | AN-384, AN-386, AN-390 |
| LM2419 | AN-861 |
| LM2577 | AN-776, AN-777 |
| LM2876 | AN-898 |
| LM2889 | AN-391, AN-402 |
| LM2907 | AN-162 |
| LM2917 | AN-162 |
| LM2931 | AB-12 |
| LM2931CT | AB-11 |
| LM3045 | AN-286 |
| LM3046 | AN-146, AN-299 |
| LM3089 | AN-147 |
| LM3524 | AN-272, AN-288, AN-292, AN-293 |
| LM3525A | AN-694 |
| LM3578A | AB-30 |
| LM3875 | AN-898 |
| LM3876 | AN-898 |
| LM3886 | AN-898 |
| LM3900 | AN-72, AN-263, AN-274, AN-278, LB-20, AB-24 |
| LM3909 | AN-154 |
| LM3914 | AN-460, LB-48, AB-25 |
| LM3915 | AN-386 |
| LM3999 | AN-161 |

Device/Application Literature Cross-Reference (Continued)

| Device Number | Application Literature |
|---------------|------------------------|
| LM4250 | AN-88, LB-34 |
| LM6181 | AN-813, AN-840 |
| LM7800 | AN-178 |
| LM12454 | AN-906, AN-947, AN-949 |
| LM12458 | AN-906, AN-947, AN-949 |
| LM12H454 | AN-906, AN-947, AN-949 |
| LM12H458 | AN-906, AN-947, AN-949 |
| LM12L458 | AN-906, AN-947, AN-949 |
| LM18293 | AN-706 |
| LM78L12 | AN-146 |
| LM78S40 | AN-711 |
| LMC555 | AN-460, AN-828 |
| LMC660 | AN-856 |
| LMC835 | AN-435 |
| LMC6044 | AN-856 |
| LMC6062 | AN-856 |
| LMC6082 | AN-856 |
| LMC6484 | AN-856 |
| LM18200 | AN-694, AN-828 |
| LMF40 | AN-779 |
| LMF60 | AN-779 |
| LMF90 | AN-779 |
| LMF100 | AN-779 |
| LMF380 | AN-779 |
| LMF390 | AN-779 |
| LP324 | AN-284 |
| LP395 | AN-460 |
| LPC660 | AN-856 |
| MF4 | AN-779 |
| MF5 | AN-779 |
| MF6 | AN-779 |
| MF8 | AN-779 |
| MF10 | AN-307, AN-779 |
| MM2716 | LB-54 |
| MM54104 | AN-252, AN-287, LB-54 |
| MM57110 | AN-382 |
| MM74C00 | AN-88 |
| MM74C02 | AN-88 |
| MM74C04 | AN-88 |
| MM74C948 | AN-193 |
| MM74HC86 | AN-861, AN-867 |
| MM74LS138 | LB-54 |
| MM53200 | AN-290 |
| 2N4339 | AN-32 |

Appendix C

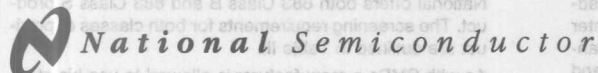
Summary of Commercial Reliability Programs

P + Product Enhancement

The P+ product enhancement program involves dynamic tests that screen out assembly related and silicon defects that can lead to infant mortality and/or reduce the survival

ability of the device under high stress conditions. This program includes but is not limited to the following power devices:

| Device | Package Types | | | | | |
|------------------|-----------------|--------------|---------------|------------|-----------|---------------|
| | TO-3 K STEEL | TO-39 (H) | TO-220 (T) | DIP (N) | SO (M) | TO-263 (S) |
| LM12 | X | | | | | |
| LM109/309 | X | X | | | | |
| LM117/317 | X | X | X | | | X |
| LM117HV/317HV | X | X | | | | |
| LM120/320 | X | X | X | | | |
| LM123/323 | X | | | | | |
| LM133/333 | X | | X | | | |
| LM137/337 | X | X | X | | | |
| LM137HV/337HV | X | X | | | | |
| LM138/338 | X | | X | | | |
| LM140/340 | X | | X | | | |
| LM145/345 | X | | | | | |
| LM150/350 | X | | X | | | |
| LM195/395 | X | X | X | | | |
| LM2930/2935/2984 | | | X | | | X |
| LM2937 | | | X | | | X |
| LM2940/2941 | | | X | | | X |
| LM2990/2991 | | | X | | | X |
| LM2575/2575HV | | | X | X | X | X |
| LM2576 | | | X | | | X |
| LM2577 | | | X | X | X | X |
| LMD18200/18201 | | | X | | | |



National offers both 883 Class B and 883 Class C products. The screening requirements for both classes are identical. As with SMDs a manufacturer is allowed to use his own test methods. Also, the electrical test parameters and electrical tests provided that all critical parameters are tested. Test limits and test temperatures must be clearly defined. At National Semiconductor, this information is provided in the form of a test plan (formerly RETS, Reliability Test Specification Program). The Table I (continued) is controlled by our QA department. Individual copies are available upon request.

Some of National's products are produced on a flow basis. This appendix is intended to provide a brief overview of military products available from National Semiconductor. The process flows and categories shown below are for general reference only. For further information and availability, please contact the Customer Response Center at 1-800-272-9959, Military/Aerospace Marketing group or your local sales office.

National Semiconductor's Military/Aerospace Program is founded on dedication to excellence. National offers complete support across the broadest range of products with the widest selection of qualification levels and screening flows. These flows include:

"on-site" monitoring of production, "on-line" program management, monitored line for test, generally do not allow "customizing," and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company. Military Screening Program (MSP): National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly. Through this program, screened product is made available for prototype and preproduction prior to running the QML screening. MSP products receive the 100% screening of Table I, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

Appendix D Military Aerospace Programs from National Semiconductor

| Process Flows (Integrated Circuits) | Description |
|--|--|
| JAN S | QML products processed to MIL-I-38535 Level S or V for Space level applications. |
| JAN B | QML products processed to MIL-I-38535 Level B or Q for Military applications. |
| SMD | QML products processed to a Standard Microcircuit Drawing with Table I Electricals controlled by DESC. |
| 883 | QML products processed to MIL-STD-883 Level B for Military applications. |
| MLP | Products processed on the Monitored Line (Program) developed by the Air Force for Space level applications. |
| -MIL | Similar to MIL-STD-883 with exceptions noted on the Certificate of Conformance. |
| MSP | Military Screening Products for initial release of advanced products. |
| MCP | Commercial products processed in a military assembly. Electrical testing performed at 25°C, plus minimum and maximum operating temperature to commercial limits. |
| MCR | Commercial products processed in a military assembly. Electrical testing performed at 25°C to commercial limits. |
| MRP | Military Ruggedized Plastic products processed to avionics requirements. |
| MRR | Commercial Ruggedized plastic product processed in a commercial assembly with electrical testing at 25°C. |
| MPC | Commercial plastic products processed in a commercial assembly with electrical testing at 25°C. |

■ **QML:** The purpose of the QML program, which is administered by the Defense Electronics Supply Center (DESC), is to provide the military community with standardized products that have been manufactured and screened to the highest quality and reliability standards in facilities that have been certified by the government. To achieve QML status, manufacturers must submit their facilities, quality procedures and design philosophies to a thorough audit aimed at confirming their ability to produce product to the highest design and quality standards. They must be listed on DESC's Qualified Manufacturer List (QML) before devices can be marked and shipped as QML product.

Two processing levels are specified within MIL-I-38535, the QML standard: Class S (typically specified for space and strategic applications) and Class B (used for tactical missile, airborne, naval and ground systems). The requirements for both classes are defined within MIL-STD-883. National is one of the industry's leading suppliers of both classes.

■ **Standard Microcircuit Drawings (SMD).** SMDs are issued to provide standardized versions of devices offered under QML. MIL-STD-883 screening is coupled with tightly controlled electrical test specifications that allow a manufacturer to use his standard electrical tests. Table I explains the marking of JAN devices, and Table II outlines current marking requirements for QML/SMD devices. Copies of MIL-I-38535 and the QML can be obtained from the Naval Publications and Forms Center (5801 Tabor Avenue, Philadelphia, PA 19120, 212/697-2179. A current listing of National's SMD offerings can be obtained from our authorized distributors, our sales offices, our Customer Response Center (Arlington, Texas, 817/468-6300), or from DESC.

■ **MIL-STD-883.** Originally intended to establish uniform test methods and procedures, MIL-STD-883 has also become the general specification for non-SMD military product. MIL-STD-883 defines the minimum requirements for a device to be marked and advertised as 883-compliant. Design and construction criteria, documentation controls, electrical and mechanical screening requirements, and quality control procedures are outlined in paragraph 1.1.2 of MIL-STD-883.

National offers both 883 Class B and 883 Class S product. The screening requirements for both classes of product are outlined in Table III.

As with SMDs a manufacturer is allowed to use his standard electrical tests provided that all critical parameters are tested. Also, the electrical test parameters, test conditions, test limits and test temperatures must be clearly documented. At National Semiconductor, this information is available via our Table I (formerly RETS, Reliability Electrical Test Specification Program). The Table I document is a complete description of the electrical tests performed and is controlled by our QA department. Individual copies are available upon request.

Some of National's products are produced on a flow similar to MIL-STD-883. These devices are screened to the same stringent requirements as 883 product, but are marked as **-MIL**; specific reasons for prevention of conformance are clearly defined in the Certificate of Conformance (C of C) shipped with the product.

■ **Monitored Line Program (MLP):** is a non JAN Level S program developed by the Air Force. Monitored Line product usually provides the shortest cycle time, and is acceptable for application in several space level programs. Lockheed Missiles and Space Company in Sunnyvale, California, under an Air Force contract, provides "on-site" monitoring of product processing, and as appropriate, program management. Monitored Line orders generally do not allow "customizing", and most flows do not include quality conformance inspection. Drawing control is maintained by the Lockheed Company.

■ **Military Screening Program (MSP):** National's Military Screening Program was developed to make screened versions of advanced products such as gate arrays and microprocessors available more quickly. Through this program, screened product is made available for prototypes and breadboards prior to or during the QML activities. MSP products receive the 100% screening of Table III, but are not subjected to Group C and D quality conformance testing. Other criteria such as electrical testing and temperature range will vary depending upon individual device status and capability.

| | |
|--|-----|
| Commercial plastic products processed in a commercial assembly with electrical testing at 25°C. | MPC |
| Commercial ruggedized plastic product processed in a commercial assembly with electrical testing at 25°C. | MPR |
| Military ruggedized plastic products processed to avionics requirements. | MRP |
| Commercial products processed in a military assembly. Electrical testing performed at 25°C to commercial limits. | MCR |
| Commercial products processed in a military assembly. Electrical testing performed at 25°C plus minimum and maximum operating temperatures to commercial limits. | MCP |

TABLE I. JAN S or B Part Marking

| JM38510/XXXXXXYY | |
|---|--|
| Lead Finish | |
| A = Solder Dipped | |
| B = Tin Plate | |
| C = Gold Plate | |
| X = Any lead finish above is acceptable | |
| Device Package (see Table II) | |
| Screening Level S or B | |
| Device Number on Slash Sheet | |
| Slash Sheet Number | |
| For radiation hard devices this slash is replaced by the Radiation Hardness Assurance Designator (M, D, R, or H of MIL-I-38535) | |
| MIL-M-38510 | |
| JAN Prefix | |

TABLE I-A. JAN Package Codes

| JAN Package Designation | Microcircuit Industry Description |
|-------------------------|---|
| A | 14-pin $\frac{1}{4}$ " x $\frac{1}{4}$ " (Metal) Flatpak |
| B | 14-pin $\frac{3}{16}$ " x $\frac{1}{4}$ " (Metal) Flatpak |
| C | 14-pin $\frac{1}{4}$ " x $\frac{3}{4}$ " Dual-In-Line |
| D | 14-pin $\frac{1}{4}$ " x $\frac{3}{8}$ " (Ceramic) Flatpak |
| E | 16-pin $\frac{1}{4}$ " x $\frac{7}{8}$ " Dual-In-Line |
| F | 16-pin $\frac{1}{4}$ " x $\frac{3}{8}$ " (Metal or Ceramic) Flatpak |
| G | 8-pin TO-99 Can or Header |
| H | 10-pin $\frac{1}{4}$ " x $\frac{1}{4}$ " (Metal) Flatpak |
| I | 10-pin TO-100 Can or Header |
| J | 24-pin $\frac{1}{2}$ " x $1\frac{1}{4}$ " Dual-In-Line |
| K | 24-pin $\frac{3}{8}$ " x $\frac{5}{8}$ " Flatpak |
| L | 24-pin $\frac{1}{4}$ " x $1\frac{1}{4}$ " Dual-In-Line |
| M | 12-pin TO-101 Can or Header |
| N | (Note 1) |
| P | 8-pin $\frac{1}{4}$ " x $\frac{3}{8}$ " Dual-In-Line |
| Q | 40-pin $\frac{3}{16}$ " x $2\frac{1}{16}$ " Dual-In-Line |
| R | 20-pin $\frac{1}{4}$ " x $1\frac{1}{16}$ " Dual-In-Line |
| S | 20-pin $\frac{1}{4}$ " x $\frac{1}{2}$ " Flatpak |
| T | (Note 1) |
| U | (Note 1) |
| V | 18-pin $\frac{3}{8}$ " x $1\frac{5}{16}$ " Dual-In-Line |
| W | 22-pin $\frac{3}{8}$ " x $1\frac{1}{8}$ " Dual-In-Line |
| X | (Note 1) |
| Y | (Note 1) |
| Z | (Note 1) |
| 2 | 20-terminal 0.350" x 0.350" Chip Carrier |
| 3 | 28-terminal 0.450" x 0.450" Chip Carrier |

Note 1: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

**TABLE II. Standard Military Drawing
(SMD) Marking**

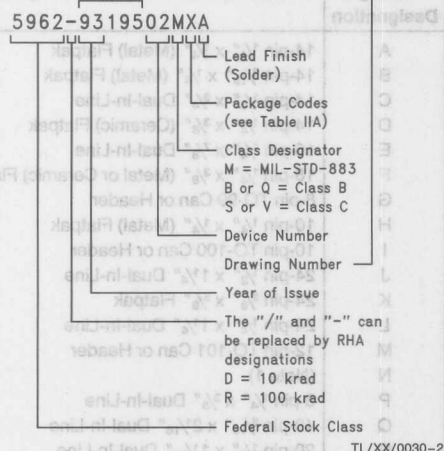


TABLE II-A. SMD Package Codes

| SMD Package Designation | Microcircuit Industry Description |
|-------------------------|-----------------------------------|
| C | 14-pin Flatpak |
| D | 14-pin C DIP |
| E | 16-pin C DIP |
| F | 16-pin Flatpak |
| G | 8-pin TO-99 Can |
| H | 10-pin (Metal) Flatpak |
| I | 10-pin TO-100 Can |
| X | (Note 2) |
| Y | (Note 2) |
| P | 8-pin C DIP |
| 2 | 20-pin LCC |
| R | 20-Pin DIP |

Note 2: These letters are assigned to packages by individual detail specifications and may be assigned to different packages in different specifications.

TABLE III. 100% Screening Requirements

| | Screen | Class S | | Class B | |
|-----|--|---|----------|---|-------|
| | | Method | Reqmt | Method | Reqmt |
| 1. | Wafer Lot Acceptance | 5007 | All Lots | | |
| 2. | Nondestructive Bond Pull (Note 14) | 2023 | 100% | | |
| 3. | Internal Visual (Note 1) | 2020, Condition A | 100% | 2010, Condition B | 100% |
| 4. | Stabilization Bake (Note 16) | 1008, Condition C, Min 24 Hrs. Min | 100% | 1008, Condition C, Min 24 Hrs. Min | 100% |
| 5. | Temperature Cycling (Note 2) | 1010, Condition C | 100% | 1010, Condition C | 100% |
| 6. | Constant Acceleration | 2001, Condition E Min Y ₁ Orientation Only | 100% | 2001, Condition E Min Y ₁ Orientation Only | 100% |
| 7. | Visual Inspection (Note 3) | | 100% | | 100% |
| 8. | Particle Impact Noise Detection (PIND) | 2010, Condition A (Note 4) | 100% | | |
| 9. | Serialization | (Note 5) | 100% | | |
| 10. | Interim (Pre-Burn-In) Electrical Parameters | Per Applicable Device Specification (Note 13) | 100% | Per Applicable Device Specification (Note 6) | |
| 11. | Burn-In Test | 1015 240 Hrs. @ 125°C Min (Cond. F Not Allowed) | 100% | 1015 160 Hrs. @ 125°C Min | 100% |
| 12. | Interim (Post Burn-In) Electrical Parameters | Per Applicable Device Specification (Note 3) | 100% | | |

TABLE III. 100% Screening Requirements (Continued)

| | Screen | Class S | | Class B | |
|-----|--|--|------------------|-------------------------------------|------------------|
| | | Method | Reqmt | Method | Reqmt |
| 13. | Reverse Bias Burn-In (Note 7) | 1015; Test Condition A, C, 72 Hrs. @ 150°C Min (Cond. F Not Allowed) | 100% | | |
| 14. | Interim (Post-Burn-In) Electrical Parameters | Per Applicable Device Specification (Note 13) | 100% | Per Applicable Device Specification | 100% |
| 15. | PDA Calculation | 5% Parametric (Note 14), 3% Functional | All Lots | 5% Parametric (Note 14) | All Lots |
| 16. | Final Electrical Test (Note 15) a) Static Tests 1) 25°C (Subgroup 1, Table I, 5005) 2) Max & Min Rated Operating Temp. (Subgroups 2, 3, Table I, 5005) b) Dynamic Tests or Functional Tests 1) 25°C (Subgroup 4 or 7) 2) Max and Min Rated Operating Temp. (Subgroups 5 and 6 or 8, Table I, 5005) c) Switching Tests 25°C (Subgroup 9, Table I, 5005) | Per Applicable Device Specification | | Per Applicable Device Specification | |
| | | | 100% | | 100% |
| | | | 100% | | 100% |
| | | | 100% | | 100% |
| | | | 100% | | 100% |
| | | | 100% | | 100% |
| 17. | Seal Fine, Gross | 1014 | 100% (Note 8) | 1014 | 100% (Note 9) |
| 18. | Radiographic (Note 10) | 2012 Two Views | 100% | | |
| 19. | Qualification or Quality Conformance Inspection Test Sample Selection | (Note 11) | Samp. | (Note 11) | Samp. |
| 20. | External Visual (Note 12) | 2009 | 100% | | 100% |

Note 1: Unless otherwise specified, at the manufacturer's option, test samples for Group B, bond strength (Method 5005) may be randomly selected prior to or following internal visual (Method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual).

Note 2: For Class B devices, this test may be replaced with thermal shock Method 1011, Test Condition A, minimum.

Note 3: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

Note 4: The PIND test may be performed in any sequence after step 6 and prior to step 16. See MIL-I-38585 paragraph 40.6.3.

Note 5: Class S devices shall be serialized prior to interim electrical parameter measurements.

Note 6: When specified, all devices shall be tested for those parameters requiring delta calculations.

Note 7: Reverse bias burn-in is a requirement only when specified in the applicable device specification. The order of performing burn-in and reverse bias burn-in may be inverted.

Note 8: For Class S devices, the seal test may be performed in any sequence between step 16 and step 19, but it shall be performed after all shearing and forming operations on the terminals.

Note 9: For Class B devices, the fine and gross seal tests shall be performed separately or together in any sequence and order between step 6 and step 20 except that they shall be performed after all shearing and forming operations on the terminals. When 100% seal screen cannot be performed after shearing and forming (e.g., flatpaks and chip carriers) the seal screen shall be done 100% prior to these operations and a sample test (LTPD = 5) shall be performed on each inspection lot following these operations. If the sample fails, 100% rescreening shall be required.

Note 10: The radiographic screen may be performed in any sequence after step 9.

Note 11: Samples shall be selected for testing in accordance with the specific device class and lot requirements of Method 5005.

Note 12: External Visual shall be performed on the lot any time after step 19 and prior to shipment.

Note 13: Read and record is required at steps 10 and 12 only for those parameters for which post-burn-in delta measurements are specified. All parameters shall be read and recorded at step 14.

Note 14: The PDA shall apply to all subgroup 1 parameters at 25°C and all delta parameters.

Note 15: Only one view is required for flat packages and leadless chip carriers with leads on all four sides.

Note 16: May be performed at any time prior to step 10.

Appendix D—Military Aerospace Programs from National Sem

| HIGH PERFORMANCE AMPLIFIERS AND BUFFERS | | | | |
|---|---------|---------------------------------------|---------|--------------|
| LF147 | D, J | Wide BW Quad JFET Op Amp | SMD/JAN | /11906 |
| LF155A | H | JFET Input Op Amp | 883 | — |
| LF156 | H | JFET Input Op Amp | 883 | — |
| LF156A | H | JFET Input Op Amp | 883 | — |
| LF157 | H | JFET Input Op Amp | 883 | — |
| LF157A | H | JFET Input Op Amp | 883 | — |
| LF411M | H | Low Offset, Low Drift JFET Input | 883/JAN | /11904 |
| LF412M | H, J | Low Offset, Low Drift JFET Input-Dual | 883/JAN | /11905 |
| LF441M | H | Low Power JFET Input | 883 | — |
| LF442M | H | Low Power JFET Input-Dual | 883 | — |
| LF444M | D | Low Power JFET Input-Quad | 883 | — |
| LH0002 | H | Buffer Amp | “MIL” | — |
| LH0021 | K | 1.0 Amp Power Op Amp | “MIL” | — |
| LH0024 | H | High Slew Rate Op Amp | “MIL” | — |
| LH0032 | G | Ultra Fast FET-Input Op Amp | “MIL” | — |
| LH0041 | G | 0.2 Amp Power Op Amp | “MIL” | — |
| LH0101 | K | Power Op Amp | “MIL” | — |
| LM10 | H | Super-Block™ Micropower Op Amp/Ref | 883/SMD | 5962-87604 |
| LM101A | J, H, W | General Purpose Op Amp | 883/JAN | /10103 |
| LM108A | J, H, W | Precision Op Amp | 883/JAN | /10104 |
| LM118 | J, H | Fast Op Amp | 883/JAN | /10107 |
| LM124 | J, E, W | Low Power Quad Op Amp | 883/JAN | /11005 |
| LM124A | J, E, W | Low Power Quad | 883/JAN | /11006 |
| LM146 | J | Quad Programmable Op Amp | 883 | — |
| LM148 | J, E | Quad 741 Op amp | 883/JAN | /11001 |
| LM158A | J, H | Low Power Dual Op Amp | 883/SMD | 5962-8771002 |
| LM158 | J, H | Low Power Dual Op Amp | 883/SMD | 5962-8771001 |
| LM611AM | J | Super-Block Op Amp/Reference | 883/SMD | — |
| LM613AM | J, E | Super-Block Dual Op Amp/Dual Comp/Ref | 883/SMD | — |
| LM614AM | J | Super-Block Quad Op Amp/Ref | 883/SMD | — |
| LM709A | H, J, W | General Purpose Op Amp | 883/SMD | 7800701 |
| LM741 | J, H, W | General Purpose Op Amp | 883/JAN | /10101 |
| LM747 | J, H | General Purpose Dual Op Amp | 883/JAN | /10102 |
| LM6118 | J, E | VIP Dual Op Amp | 883/SMD | 5962-91565 |
| LM6121 | H, J | VIP Buffer | 883/SMD | 5962-90812 |
| LM6125 | H | VIP Buffer with Error Flag | 883/SMD | 5962-90815 |
| LM6161 | J, E, W | VIP Op Amp (Unity Gain) | 883/SMD | 5962-89621 |
| LM6162 | J, E, W | VIP Op Amp ($A_V > 2, -1$) | 883/SMD | 5962-92165 |
| LM6164 | J, E, W | VIP Op Amp ($A_V > 5$) | 883/SMD | 5962-89624 |
| LM6165 | J, E, W | VIP Op Amp ($A_V > 25$) | 883/SMD | 5962-89625 |
| LM6181AM | J | VIP Current Feedback Op Amp | 883/SMD | 5962-9081802 |
| LM6182AM | J | VIP Current Feedback Dual Op Amp | 883/SMD | 5962-9460301 |
| LMC660AM | J | Low Power CMOS Quad Op Amp | 883/SMD | 5962-9209301 |
| LMC662AM | J | Low Power CMOS Dual Op Amp | 883/SMD | 5962-9209401 |
| LPC660AM | J | Micropower CMOS Quad Op Amp | 883/SMD | 5962-9209302 |
| LPC662AM | J | Micropower CMOS Dual Op Amp | 883/SMD | 5962-9209402 |
| LMC6482AM | J | Rail to Rail CMOS Dual Op Amp | 883/SMD | 5962-9453401 |
| LMC6484AM | J | Rail to Rail CMOS Quad Op Amp | 883/SMD | 5962-9453402 |
| OP07 | H | Precision Op Amp | 883 | — |

| Military Analog Products Available from National Semiconductor (Continued) | | | | |
|--|-------------------------------|---------------------------------------|------------------------------|---------------------|
| Device (Note 3) | Package Styles (Note 1) | Description | Process Flows (Note 2) | SMD/JAN (Note 3) |
| COMPARATORS | | | | |
| LF111 | H | Voltage Comparator | "-MIL" | — |
| LH2111 | J, W | Dual Voltage Comparator | 883/JAN | /10305 |
| LM106 | H, W | Voltage Comparator | 883/SMD | 8003701 |
| LM111 | J, H, E, W | Voltage Comparator | 883/JAN | /10304 |
| LM119 | J, H, E, W | High Speed Dual Comparator | 883/JAN | /10306 |
| LM139 | J, E, W | Quad Comparator | 883/JAN | /11201 |
| LM139A | J, E, W | Precision Quad Comparator | 883/SMD | 5962-87739 |
| LM160 | J, H | High Speed Differential Comparator | 883/SMD | 8767401 |
| LM161 | J, H, W | High Speed Differential Comparator | 883/SMD | 5962-87572 |
| LM193 | J, H | Dual Comparator | 883 | — |
| LM193A | J, H | Dual Comparator | 883/JAN | /11202 |
| LM612AM | J | Dual-Channel Comparator/Reference | 883/SMD | 5962-93002 |
| LM613AM | J, E | Super-Block Dual Comparator/Reference | 883/SMD | 5962-93003 |
| LM615AM | J | Dual Op Amp/Adj Reference | 883 | — |
| LM710A* | J, H, W | Quad Comparator/Adjustable Reference | 883 | — |
| LM711A* | J, H, W | Voltage Comparator | 883/JAN | /10301 |
| LM760 | J, H | Dual LM710 | 883/JAN | /10302 |
| LM760 | J, H | High Speed Differential Comparator | 883/SMD | 5962-87545 |
| *Formerly manufactured by Fairchild Semiconductor as part numbers μ A710 and μ A711. | | | | |
| LINEAR REGULATORS | | | | |
| Positive Voltage Regulators | | | | |
| LM105 | H | Adjustable Voltage Regulator | 883/SMD | 5962-89588 |
| LM109 | H | 5V Regulator, $I_o = 20$ mA | 883/JAN | /10701BXA |
| LM109 | K | 5V Regulator, $I_o = 1$ A | 883/JAN | /10701BYA |
| LM117 | H, E, K | Adjustable Regulator | 883/JAN | /11703, /11704 |
| LM117HV | H | Adjustable Regulator, $I_o = 0.5$ A | 883/SMD | 7703402XA |
| LM117HV | K | Adjustable Regulator, $I_o = 1.5$ A | 883/SMD | 7703402YA |
| LM123 | K | 3A Voltage Regulator | 883 | — |
| LM138 | K | 5A Adjustable Regulator | "-MIL" K | — |
| LM140-5.0 | H | 0.5A Fixed 5V Regulator | 883/JAN | /10702 |
| LM140-6.0 | H | 0.5A Fixed 6V Regulator | 883 | — |
| LM140-8.0 | H | 0.5A Fixed 8V Regulator | 883 | — |
| LM140-12 | H | 0.5A Fixed 12V Regulator | 883/JAN | /10703 |
| LM140-15 | H | 0.5A Fixed 15V Regulator | 883/JAN | /10704 |
| LM140-24 | H | 0.5A Fixed 24V Regulator | 883 | — |
| LM140A-5.0 | K | 1.0A Fixed 5V Regulator | 883 | — |
| LM140A-12 | K | 1.0A Fixed 12V Regulator | 883 | — |
| LM140A-15 | K | 1.0A Fixed 15V Regulator | 883 | — |
| LM140K-5.0 | K | 1.0A Fixed 5V Regulator | 883/JAN | /10706 |
| LM140K-12 | K | 1.0A Fixed 12V Regulator | 883/JAN | /10707 |
| LM140K-15 | K | 1.0A Fixed 15V Regulator | 883/JAN | /10708 |
| LM140LAH-5.0 | H | 100 mA Fixed 5V Regulator | 883 | — |
| LM140LAH-12 | H | 100 mA Fixed 12V Regulator | 883 | — |
| LM140LAH-15 | H | 100 mA Fixed 15V Regulator | 883 | — |
| LM150 | K | 3A Adjustable Power Regulator | 883 | — |
| LM2940-5.0 | K | 5V Low Dropout Regulator | 883/SMD | 5962-89587 |
| LM2940-8.0 | K | 8V Low Dropout Regulator | 883/SMD | 5962-90883 |
| LM2940-12 | K | 12V Low Dropout Regulator | 883/SMD | 5962-90884 |
| LM2940-15 | K | 15V Low Dropout Regulator | 883/SMD | 5962-90885 |
| LM2941 | K | Adjustable Low Dropout Regulator | 883/SMD | TBD |
| LM431 | H, K | Adjustable Shunt Regulator | 883 | — |
| LM723 | H, J, E | Precision Adjustable Regulator | 883/JAN | /10201 |
| LP2951 | H, E, J | Adjustable Micropower LDO | 883/SMD | 5962-38705 |
| LP2953AM | J | 250 mA Adj. Micropower LDO | 883/SMD | 5962-9233601 |

| Military Analog Products Available from National Semiconductor (Continued) | | | | |
|---|----------------------------|--|---------------------------|---------------------|
| Device | Package Styles (Note 1) | Description | Process Flows (Note 2) | SMD/JAN (Note 3) |
| LINEAR REGULATORS (Continued) | | | | |
| Negative Voltage Regulators | | | | |
| LM120-5.0 | H | Fixed 0.5A Regulator, $V_{OUT} = -5V$ | 883/JAN | /11501 |
| LM120-8.0 | H | Fixed 0.5A Regulator, $V_{OUT} = -8V$ | 883 | — |
| LM120-12 | H | Fixed 0.5A Regulator, $V_{OUT} = -12V$ | 883/JAN | /11502 |
| LM120-15 | H | Fixed 0.5A Regulator, $V_{OUT} = -15V$ | 883/JAN | /11503 |
| LM120-5.0 | K | Fixed 1.0A Regulator, $V_{OUT} = -5V$ | 883/JAN | /11505 |
| LM120-12 | K | Fixed 1.0A Regulator, $V_{OUT} = -12V$ | 883/JAN | /11506 |
| LM120-15 | K | Fixed 1.0A Regulator, $V_{OUT} = -15V$ | 883/JAN | /11507 |
| LM137A | H | Precision Adjustable Regulator | 883/SMD | 7703406XA |
| LM137A | K | Precision Adjustable Regulator | 883/SMD | 7703406YA |
| LM137 | H, K | Adjustable Regulator | 883/JAN | /11803, /11804 |
| LM137HV | H | Adjustable (High Voltage) Regulator | 883/SMD | 7703404XA |
| LM137HV | K | Adjustable (High Voltage) Regulator | 883/SMD | 7703404YA |
| LM145-5.0 | K | Negative 3 Amp Regulator | 883/SMD | 5962-90645 |
| LM145-5.2 | K | Negative 3 Amp Regulator | 883 | — |
| SWITCHING REGULATORS | | | | |
| LM1575-5 | J, K | Simple Switcher™ Step-Down, $V_{OUT} = 5V$ | 883/SMD | 5962-9167201 |
| LM1575-12 | J, K | Simple Switcher Step-Down, $V_{OUT} = 12V$ | 883/SMD | 5962-9167301 |
| LM1575-15 | J, K | Simple Switcher Step-Down, $V_{OUT} = 15V$ | 883/SMD | 5962-9167401 |
| LM1575-ADJ | J, K | Simple Switcher Step-Down, Adj V_{OUT} | 883/SMD | 5962-9167101 |
| LM1575HV-5 | K | Simple Switcher Step-Down, $V_{OUT} = 5V$ | 883 | — |
| LM1575HV-12 | K | Simple Switcher Step-Down, $V_{OUT} = 12V$ | 883 | — |
| LM1575HV-15 | K | Simple Switcher Step-Down, $V_{OUT} = 15V$ | 883 | — |
| LM1575HV-ADJ | K | Simple Switcher Step-Down, Adj V_{OUT} | 883 | — |
| LM1577-12 | K | Simple Switcher Step-Up, $V_{OUT} = 12V$ | 883/SMD | 5962-9216701 |
| LM1577-15 | K | Simple Switcher Step-Up, $V_{OUT} = 15V$ | 883/SMD | 5962-9216801 |
| LM1577-ADJ | K | Simple Switcher Step-Up, Adj V_{OUT} | 883/SMD | 5962-9216601 |
| LM1578 | H | 750 mA Switching Regulator | 883/SMD | 5962-89586 |
| LM78S40* | J | Universal Switching Regulator Subsystem | 883/SMD | 5962-88761 |
| *Formerly manufactured by Fairchild Semiconductor as the $\mu A78S40DMQB$. | | | | |
| VOLTAGE REFERENCES | | | | |
| LM103-3.0 | H | Reference Diode, $BV = 3.0V$ | 883/SMD | 7702806 |
| LM103-3.3 | H | Reference Diode, $BV = 3.3V$ | 883/SMD | 7702807 |
| LM103-3.6 | H | Reference Diode, $BV = 3.6V$ | 883/SMD | 7702808 |
| LM103-3.9 | H | Reference Diode, $BV = 3.9V$ | 883/SMD | 7702809 |
| LM113 | H | Reference Diode with 5% Tolerance | 883/SMD | 5962-8671101 |
| LM113-1 | H | Reference Diode with 1% Tolerance | 883/SMD | 5962-8671102 |
| LM113-2 | H | Reference Diode with 2% Tolerance | 883/SMD | 5962-8671103 |
| LM129A | H | Precision Reference, 10 ppm/°C Drift | 883/SMD | 5962-8992101XA |
| LM129B | H | Precision Reference, 20 ppm/°C Drift | 883/SMD | 5962-8992102XA |
| LM136A-2.5 | H | 2.5V Reference Diode, 1% V_{OUT} Tolerance | 883 | — |
| LM136A-5.0 | H | 5V Reference Diode, 1% V_{OUT} Tolerance | 883/SMD | 8418001 |
| LM136-2.5 | H | 2.5V Reference Diode, 2% V_{OUT} Tolerance | 883 | — |
| LM136-5.0 | H | 5V Reference Diode, 2% V_{OUT} Tolerance | 883 | — |

| Military Analog Products Available from National Semiconductor (Continued) | | | | |
|--|----------------------------|---|---------------------------|---------------------|
| Device | Package Styles (Note 1) | Description | Process Flows (Note 2) | SMD/JAN (Note 3) |
| VOLTAGE REFERENCES (Continued) | | | | |
| LM169 | H | 10V Precision Reference, Low Tempco 0.05% Tolerance | 883 | — |
| LM185B | H, E | Adjustable Micropower Voltage Reference | 883/SMD | 5962-9041401 |
| LM185BX2.5 | H | 2.5V Micropower Reference Diode, Ultralow Drift | 883/SMD | 5962-8759404 |
| LM185BY | H | Adjustable Micropower Voltage Reference | 883 | — |
| LM185BY1.2 | H | 1.2V Micropower Reference Diode, Low Drift | 883/SMD | 5962-8759405 |
| LM185BY2.5 | H | 2.5V Micropower Reference Diode, Low Drift | 883/SMD | 5962-8759406 |
| LM185-1.2 | H, E | 1.2V Micropower Reference Diode, Low Drift | 883/SMD | 5962-8759401 |
| LM185-2.5 | H, E | 2.5V Micropower Reference Diode, Low Drift | 883/SMD | 5962-8759402 |
| LM199 | H | Precision Reference, Low Tempco | 883/SMD | 5962-8856102 |
| LM199A | H | Precision Reference, Ultralow Tempco | 883/SMD | 5962-8856101 |
| LM199A-20 | H | Precision Reference, Ultralow Tempco | 883 | — |
| LM611AM | J | Super-Block Op Amp/Reference | 883 | — |
| LM612AM | J | Super-Block Dual-Channel Comparator/Reference | 883/SMD | 5962-9300201 |
| LM613AM | J, E | Super-Block Dual Op Amp/DualComp/Dual Ref | 883/SMD | 5962-9300301 |
| LM614AM | J | Super-Block Quad Op Amp/Reference | 883/SMD | 5962-9300401 |
| LM615AM | J | Super-Block Quad Comparator/Reference | 883/SMD | TBD |
| LH0070-0 | H | Precision BCD Buffered Reference | "-MIL" | — |
| LH0070-1 | H | Precision BCD Buffered Reference | "-MIL" | — |
| LH0070-2 | H | Precision BCD Buffered Reference | "-MIL" | — |
| DATA ACQUISITION | | | | |
| ADC08020L | J | 8-Bit μ P-Compatible | 883/SMD | 5962-90966 |
| ADC0851 | J | 8-Bit Analog Data Acquisition & Monitoring System | 883/SMD | TBD |
| ADC0858 | J | 8-Bit Analog Data Acquisition & Monitoring System | 883/SMD | TBD |
| ADC08061CM | J | 8-Bit Multistep ADC | 883/SMD | TBD |
| ADC10061CM | J | 10-Bit Multistep ADC | 883/SMD | TBD |
| ADC10062CM | J | 10-Bit Multistep ADC w/Dual Input Multiplexer | 883/SMD | TBD |
| ADC10064CM | J | 10-Bit Multistep ADC w/Quad Input Multiplexer | 883/SMD | TBD |
| ADC1241CM | J | 12-Bit Plus Sign Self-Calibrating with Sample/Hold Function | 883/SMD | 5962-9157801 |
| ADC12441CM | J | Dynamically-Tested ADC1241 | 883/SMD | 5962-9157802 |
| ADC1251CM | J | 12-Bit Plus Sign Self-Calibrating with Sample/Hold Function | 883/SMD | 5962-9157801 |
| ADC12451CM | J | Dynamically-Tested ADC1251 | 883/SMD | TBD |
| DAC0854CM | J | Quad 8-Bit D/A Converter with Read Back | 883/SMD | TBD |
| DAC1054CM | J | Quad 10-Bit D/A Converter with Read Back | 883/SMD | TBD |
| LM12458M | EL, W | 12-Bit Data Acquisition System | 883/SMD | 5962-9319501 |
| LM12H458M | EL, W | 12-Bit Data Acquisition System | 883/SMD | 5962-9319502 |

| Military Analog Products Available from National Semiconductor (Continued) | | | | |
|---|-------------------------------|---|------------------------------|----------------------|
| Device (Note 1) | Package Styles (Note 1) | Description | Process Flows (Note 2) | SMD/JAN (Note 3) |
| DATA ACQUISITION SUPPORT | | | | |
| Switched Capacitor Filters | | | | |
| LMF60CMJ50 | J | 6th Order Butterworth Lowpass | 883/SMD | 5962-90967 |
| LMF60CMJ100 | J | 6th Order Butterworth Lowpass | 883/SMD | 5962-90967 |
| LMF90CM | J | 4th Order Elliptic Notch | 883/SMD | 5962-90968 |
| LMF100A | J, E | Dual 2nd Order General Purpose | 883/SMD | 5962-9153301 |
| Sample and Hold | | | | |
| LF198 | H | Monolithic Sample and Hold | SMD/JA | 5962-87608 /12501 |
| Motion Control | | | | |
| LMD18200-2 | D | Dual 3A, 55V H-Bridge | 883/JAN | 5962-9232501 |
| <p>Note 1: D: Side-Brazed DIP E: Leadless Ceramic Chip Carrier G: Metal Can (TO-8) H: Metal Can (TO-39, TO-5, TO-99, TO-100) J: Ceramic DIP K: Metal Can (TO-3) W: Flatpak</p> <p>Note 2: Process Flows JAN = JM38510, Level B SMD = Standard Military Drawing 883 = MIL-STD-883 Rev C -MIL = Exceptions to 883C noted on Certificate of Conformance</p> <p>Note 3: Please call your local sales office to determine price and availability of space-level products. All "LM" prefix products in this guide are available with space-level processing.</p> | | | | |
| DATA ACQUISITION | | | | |
| ADC08020L | J | 8-Bit A/D Converter | J | 5962-90969 |
| ADC0881 | J | 8-Bit Analog Data Acquisition & Monitoring System | J | 5962-90970 |
| ADC0888 | J | 8-Bit Analog Data Acquisition & Monitoring System | J | 5962-90971 |
| ADC0881CM | J | 8-Bit Multistep A/D | J | 5962-90972 |
| ADC10081CM | J | 10-Bit Multistep A/D | J | 5962-90973 |
| ADC10082CM | J | 10-Bit Multistep A/D w/ Dual Input Multiplexer | J | 5962-90974 |
| ADC10084CM | J | 10-Bit Multistep A/D w/ Quad Input Multiplexer | J | 5962-90975 |
| ADC1241CM | J | 12-Bit Plus Sign Self-Calibrating with Sample/Hold Function | J | 5962-90976 |
| ADC12441CM | J | Dynamically-Tested ADC1241 | J | 5962-90977 |
| ADC1241CM | J | 12-Bit Plus Sign Self-Calibrating with Sample/Hold Function | J | 5962-90978 |
| ADC1242CM | J | Dynamically-Tested ADC1242 | J | 5962-90979 |
| DAC084CM | J | Quad 8-Bit D/A Converter with Feed Back | J | 5962-90980 |
| DAC104CM | J | Quad 10-Bit D/A Converter with Feed Back | J | 5962-90981 |
| LM1248M | EL, W | 12-Bit Data Acquisition System | EL, W | 5962-90982 |
| LM1248M | EL, W | 12-Bit Data Acquisition System | EL, W | 5962-90983 |

Appendix E Understanding Integrated Circuit Package Power Capabilities

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

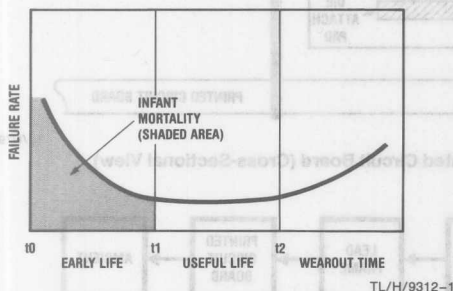


FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t_0 to t_1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$MTBF = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t_1 and t_2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X_1}{X_2} = \exp \left[\frac{E}{K} \left(\frac{1}{T_2} - \frac{1}{T_1} \right) \right]$$

Where: X_1 = Failure rate at junction temperature T_1

X_2 = Failure rate at junction temperature T_2

T = Junction temperature in degrees Kelvin

E = Thermal activation energy in electron volts (ev)

K = Boltzman's constant

plot of the above equation for three different activation energies in Figure 2. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 eV line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

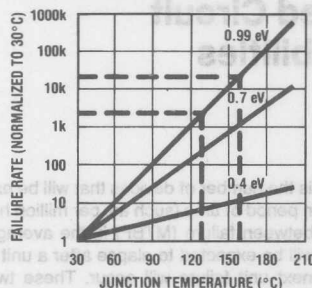


FIGURE 2. Failure Rate as a Function of Junction Temperature

TL/H/9312-2

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by Figures 3 and 4.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit

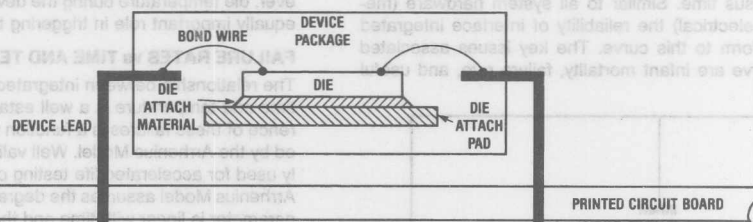


FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

TL/H/9312-3

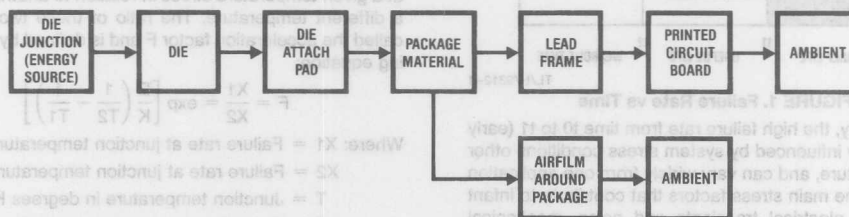


FIGURE 4. Thermal Flow (Predominant Paths)

TL/H/9312-4

from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of Figure 4 will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity of device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA} , the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA} .

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using IC components.

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA} , worst-case ambient operating temperature, $T_A(\max)$, the only unknown parameter is device power dissipation, P_D . In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70^\circ\text{C} + (63^\circ\text{C/W}) \times (0.6\text{W}) = 108^\circ\text{C}$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. Figure 5 is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D \text{ @ } 25^\circ\text{C} = \frac{T_J(\max) - T_A}{\theta_{JA}} = \frac{150^\circ\text{C} - 25^\circ\text{C}}{63^\circ\text{C/W}} = 1.98\text{W}$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, Figure 5 is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

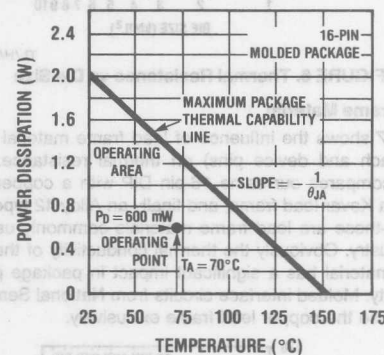


FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all integrated circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

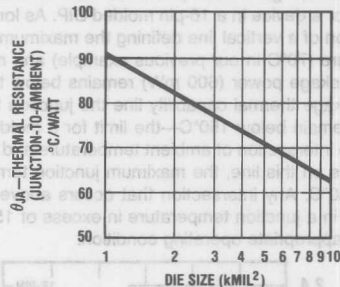


FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 42 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

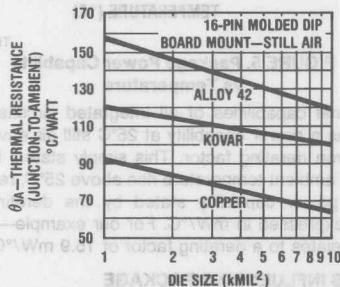


FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of Figure 8 comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

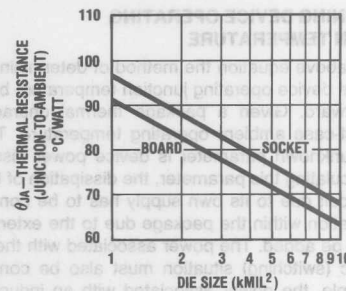


FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of Figure 9 illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

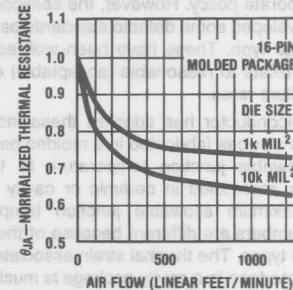


FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

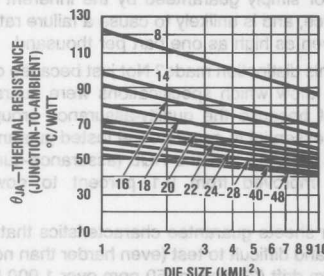
Figures 10 and 11 show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Linear Circuits product family. Figure 10 is a composite of the copper lead frame molded

package. Figure 11 is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTEGRATED CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Linear Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from $\pm 10\%$ to $\pm 15\%$ due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the linear data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount— Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Surface Mount (M, MW Packages), Board Mount, Still Air

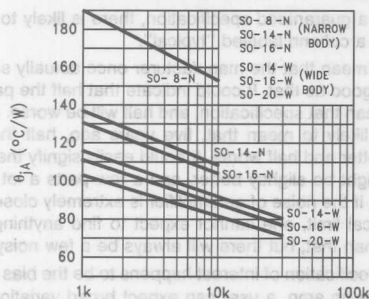


FIGURE 12. Thermal Resistance for "SO" Packages (Board Mount)

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

Maximum Power Dissipation* at 25°C

Cavity Package 1509 mW

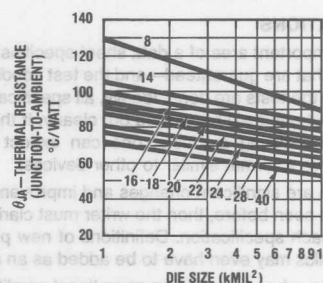
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D @ 70^\circ\text{C} = 1476 \text{ mW} - (11.8 \text{ mW}/^\circ\text{C}) \times (70^\circ\text{C} - 25^\circ\text{C}) = 945 \text{ mW}$$

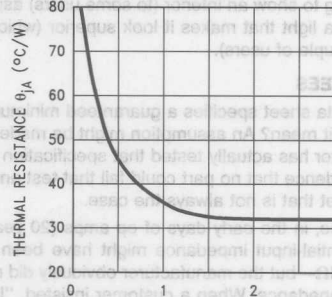
Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

TO-263 (S Package) Board Mount, Still Air



*For products with high current ratings ($> 3\text{A}$), thermal resistance may be lower. Consult product datasheet for more information.

FIGURE 13. Thermal Resistance (typ.) for 3-, 5-, and 7-L TO-263 packages mounted on 1 oz. (0.036mm) PC board foil

By Robert A. Reese

When a new product arrives in the marketplace, it hopefully will have a good, clear data sheet with it.

SPECIFICATIONS

The most important area of a data sheet specifies the characteristics that are guaranteed—and the test conditions that apply when the tests are done. Ideally, all specifications that the users will need will be spelled out clearly. If the product is similar to existing products, one can expect the data sheet to have a format similar to other devices.

However, the reader ought to be on the alert. In a few cases, the data-sheet writer is playing a specsman's game, and is trying to show an inferior (to some users) aspect of a product in a light that makes it look superior (which it may be, to a couple of users).

When a data sheet specifies a guaranteed minimum value, what does it mean? An assumption might be made that the manufacturer has actually tested that specification and has great confidence that no part could fail that test and still be shipped. Yet that is not always the case.

In other cases, the manufacturer may specify a test that can be made only on the die as it is probed on the wafer, but cannot be tested after the die is packaged because that signal is not accessible any longer. To avoid frustrating and confusing the customer, some manufacturers are establishing two classes of guaranteed specifications:

- Why was this distinction made? Not just because customers wanted to know which specifications were guaranteed by testing, but because the quality-assurance group insisted that it was essential to separate the tested guarantees from the design limits so that the AQL (assurance-quality level) could be improved from 0.1 percent to down below 100 ppm.

The data sheet may not tell the reader if it is measured, tested or estimated. One manufacturer may perform a 100-percent test, while another states, "Guaranteed by sample testing." This is not a very comforting assurance that a part is good, especially in a critical case where only a long-term test can prove if the device did meet the manufacturer's specification. If in doubt, question the manufacturer.

Next to a guaranteed specification, there is likely to be another in a column labeled "typical".

If the specification of interest happens to be the bias current (I_b) of an op amp, a user can expect broad variations. For example, if the specification is 200 nA maximum, there might be many parts where I_b is 40 nA on one batch (where the beta is high), and a month later, many parts where the I_b is 140 nA when the beta is low.

Absolute Maximum Ratings (Note 11)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|----------------------|-----------------|
| Supply Voltage | +35V to -0.2V |
| Output Voltage | +6V to -1.0V |
| Output Current | 10 mA |
| Storage Temperature, | |
| TO-46 Package | -76°F to +356°F |
| TO-92 Package | -76°F to +300°F |

Lead Temp. (Soldering, 4 seconds) *

| | |
|--|---|
| TO-46 Package | +300°C |
| TO-92 Package | +260°C |
| Specified Operating Temp. Range (Note 2) | |
| | T_{MIN} to T_{MAX} |
| LM34, LM34A | -50°F to +300°F |
| LM34C, LM34CA | -40°F to +230°F |
| LM34D | +32°F to +212°F |

DC Electrical Characteristics (Note 1, Note 6)

| Parameter | Conditions | LM34A | | | LM34CA | | | Units (Max) |
|---|---|---------|-----------------------------|-----------------------------|---------|-----------------------------|-----------------------------|--------------------------|
| | | Typical | Tested Limit (Note 4) | Design Limit (Note 5) | Typical | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Accuracy (Note 7) | T _A = +77°F | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | °F |
| | T _A = 0°F | ±0.6 | | | ±0.6 | | ±2.0 | °F |
| | T _A = T _{MAX} | ±0.8 | ±2.0 | | ±0.8 | ±2.0 | | °F |
| | T _A = T _{MIN} | ±0.8 | ±2.0 | | ±0.8 | | ±3.0 | °F |
| Nonlinearity (Note 8) | T _{MIN} ≤ T _A ≤ T _{MAX} | ±0.35 | | ±0.7 | ±0.30 | | ±0.6 | °F |
| Sensor Gain (Average Slope) | T _{MIN} ≤ T _A ≤ T _{MAX} | +10.0 | +9.9, +10.1 | | +10.0 | | +9.9, +10.1 | mV/°F, min mV/°F, max |
| Load Regulation (Note 3) | T _A = +77°F | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | mV/mA |
| | T _{MIN} ≤ T _A ≤ T _{MAX} 0 ≤ I _L ≤ 1 mA | ±0.5 | | ±3.0 | ±0.5 | | ±3.0 | mV/mA |
| Line Regulation (Note 3) | T _A = +77°F | ±0.01 | ±0.05 | | ±0.01 | ±0.05 | | mV/V |
| | 5V ≤ V _S ≤ 30V | ±0.02 | | ±0.1 | ±0.02 | | ±0.1 | mV/V |
| Quiescent Current (Note 9) | V _S = +5V, +77°F | 75 | 90 | | 75 | 90 | | μA |
| | V _S = +5V | 131 | | 160 | 116 | | 139 | μA |
| | V _S = +30V, +77°F | 76 | 92 | | 76 | 92 | | μA |
| | V _S = +30V | 132 | | 163 | 117 | | 142 | μA |
| Change of Quiescent Current (Note 3) | 4V ≤ V _S ≤ 30V, +77°F | +0.5 | 2.0 | | 0.5 | 2.0 | | μA |
| | 5V ≤ V _S ≤ 30V | +1.0 | | 3.0 | 1.0 | | 3.0 | μA |
| Temperature Coefficient of Quiescent Current | | +0.30 | | +0.5 | +0.30 | | +0.5 | μA/°F |
| Minimum Temperature for Rated Accuracy | In circuit of Figure 1, I _L = 0 | +3.0 | | +5.0 | +3.0 | | +5.0 | °F |
| Long-Term Stability | T _J = T _{MAX} for 1000 hours | ±0.16 | | | ±0.16 | | | °F |

Note 1: Unless otherwise noted, these specifications apply: -50°F ≤ T_J ≤ +300°F for the LM34 and LM34A; -40°F ≤ T_J ≤ +230°F for the LM34C and LM34CA; and +32°F ≤ T_J ≤ +212°F for the LM34D. V_S = +5 Vdc and I_{LOAD} = 50 μA in the circuit of Figure 2; +6 Vdc for LM34 and LM34A for 230°F ≤ T_J ≤ 300°F. These specifications also apply from +5°F to T_{MAX} in the circuit of Figure 1.

Note 2: Thermal resistance of the TO-46 package is 292°F/W junction to ambient and 43°F/W junction to case. Thermal resistance of the TO-92 package is 324°F/W junction to ambient.

Note 3: Regulation is measured at constant junction temperature using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

Note 4: Tested limits are guaranteed and 100% tested in production.

Note 5: Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

Note 6: Specification in **BOLDFACE TYPE** apply over the full rated temperature range.

Note 7: Accuracy is defined as the error between the output voltage and 10 mV/°F times the device's case temperature at specified conditions of voltage, current, and temperature (expressed in °F).

Note 8: Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line over the device's rated temperature range.

Note 9: Quiescent current is defined in the circuit of Figure 1.

Note 10: Contact factory for availability of LM34CAZ.

* **Note 11:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions (see Note 1).

A Point-By-Point Look

Let's look a little more closely at the data sheet of the National Semiconductor LM34, which happens to be a temperature sensor.

Note 1 lists the nominal test conditions and test circuits in which all the characteristics are defined. Some additional test conditions are listed in the column "Conditions", but Note 1 helps minimize the clutter.

Note 2 gives the thermal impedance, (which may also be shown in a chart or table).

Note 3 warns that an output impedance test, if done with a long pulse, could cause significant self-heating and thus, error.

Note 6 is intended to show which specs apply at all rated temperatures.

Note 7 is the definition of the "Accuracy" spec, and Note 8 the definition for non-linearity. Note 9 states in what test circuit the quiescent current is defined. Note 10 indicates that one model of the family may not be available at the time of printing (but happens to be available now), and Note 11 is the definition of Absolute Max Ratings.

* Note—the "4 seconds" soldering time is a new standard for plastic packages.

** Note—the wording of Note 11 has been revised—this is the best wording we can devise, and we will use it on all future datasheets.

APPLICATIONS

Another important part of the data sheet is the applications section. It indicates the novel and conventional ways to use a device. Sometimes these applications are just little ideas to tweak a reader's mind. After looking at a couple of applications, one can invent other ideas that are useful. Some applications may be of no real interest or use.

In other cases, an application circuit may be the complete definition of the system's performance; it can be the test circuit in which the specification limits are defined, tested and guaranteed. But, in all other instances, the performance of a typical application circuit is not guaranteed, it is only typical. In many circumstances, the performance may depend on external components and their precision and matching. Some manufacturers have added a phrase to their data sheets:

"Applications for any circuits contained in this document are for illustration purposes only and the manufacturer makes no representation or warranty that such applications will be suitable for the use indicated without further testing or modification."

In the future, manufacturers may find it necessary to add disclaimers of this kind to avoid disappointing users with circuits that work well, much of the time, but cannot be easily guaranteed.

The applications section is also a good place to look for advice on quirks—potential drawbacks or little details that may not be so little when a user wants to know if a device will actually deliver the expected performance.

For example, if a buffer can drive heavy loads and can handle fast signals cleanly (at no load), the maker isn't doing anybody any favors if there is no mention that the distortion goes sky-high if the rated load is applied.

Another example is the application hint for the LF156 family:

"Exceeding the negative common-mode limit on either input will cause a reversal of the phase to output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur, since raising the input back within the common-mode range again puts the input stage and, thus the amplifier, in a normal operating mode."

That's the kind of information a manufacturer should really give to a data-sheet reader because no one could ever guess it.

Sometimes, a writer slips a quirk into a characteristic curve, but it's wiser to draw attention to it with a line of text. This is because it's better to make the user sad before one gets started, rather than when one goes into production. Conversely, if a user is going to spend more than 10 minutes using a new product, one ought to spend a full five minutes reading the entire data sheet.

FINE PRINT

What other fine print can be found on a data sheet? Sometimes the front page may be marked "advance" or "preliminary." Then on the back page, the fine print may say something such as:

"This data sheet contains preliminary limits and design specifications. Supplemental information will be published at a later date. The manufacturer reserves the right to make changes in the products contained in this document in order to improve design or performance and to supply the best possible products. We also assume no responsibility for the use of any circuits described herein, convey no license under any patent or other right and make no representation that the circuits are free from patent infringement."

In fact, after a device is released to the marketplace in a preliminary status, the engineers love to make small improvements and upgrades in specifications and characteristics, and hate to degrade a specification from its first published value—but occasionally that is necessary.

Another item in the fine print is the manufacturer's telephone number. Usually it is best to refer questions to the local sales representative or field-applications engineer, because they may know the answer or they may be best able to put a questioner in touch with the right person at the factory.

Occasionally, the factory's applications engineers have all the information. Other times, they have to bring in product engineers, test engineers or marketing people. And sometimes the answer can't be generated quickly—data have to be gathered, opinions solidified or policies formulated before the manufacturer can answer the question. Still, the telephone number is the key to getting the factory to help.

ORIGINS OF DATA SHEETS

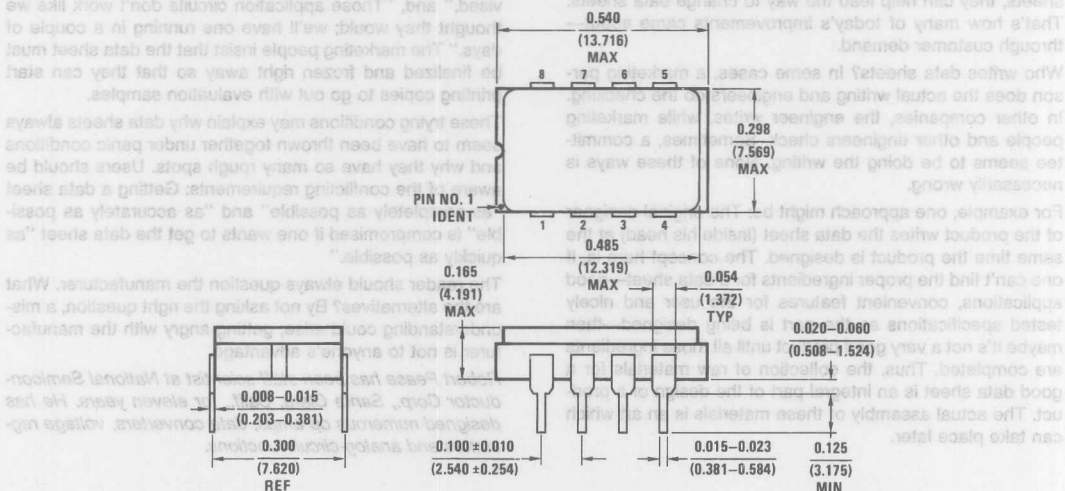
Of course, historically, most data sheets for a class of products have been closely modeled on the data sheet of the forerunner of that class. The first data sheet was copied to make new versions.

That's the way it happened with the UA709 (the first monolithic op amp) and all its copies, as well as many other similar families of circuits.

8 Lead Ceramic Sidebrazed Dual-in-Line Package

NS Package Number D08C

All dimensions are in inches (millimeters)

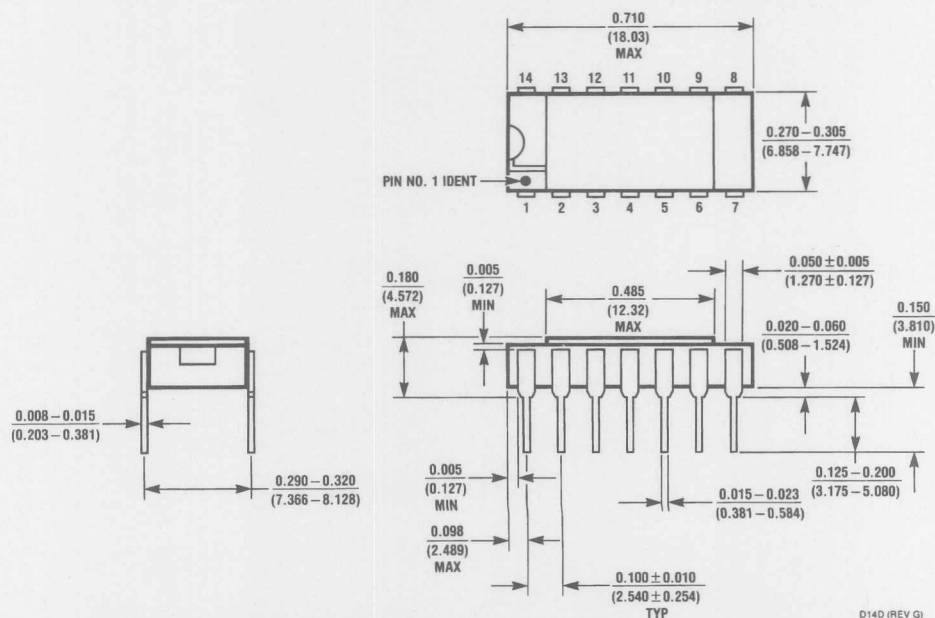


D08C (REV C)

14 Lead Ceramic Sidebrazed Dual-in-Line Package

NS Package Number D14D

All dimensions are in inches (millimeters)



D14D (REV G)

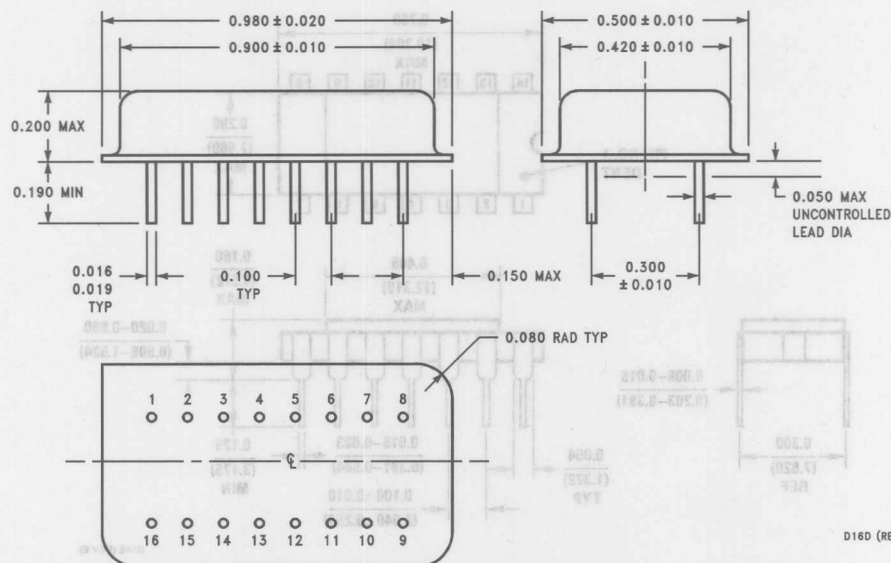
Dimensions



16 Lead Hybrid Metal Can Dual-in-Line Package NS Package Number D16D

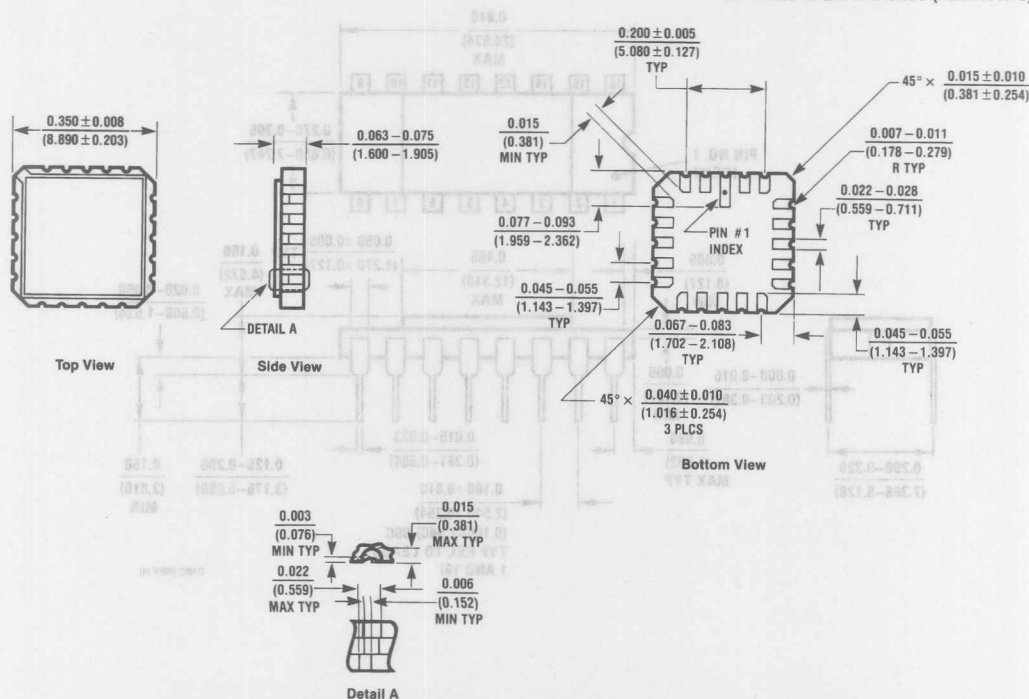
(All dimensions are in inches (millimeters))

All dimensions are in inches



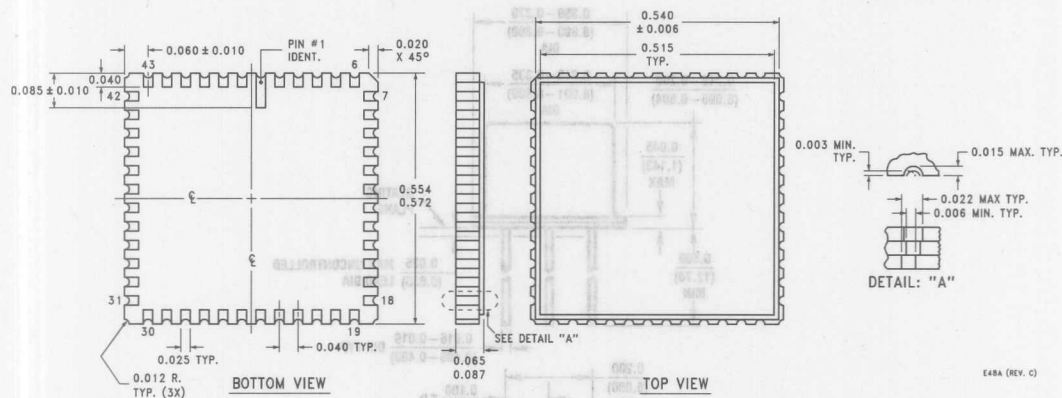
20 Lead Ceramic Leadless Chip Carrier, Type C NS Package Number E20A

All dimensions are in inches (millimeters)



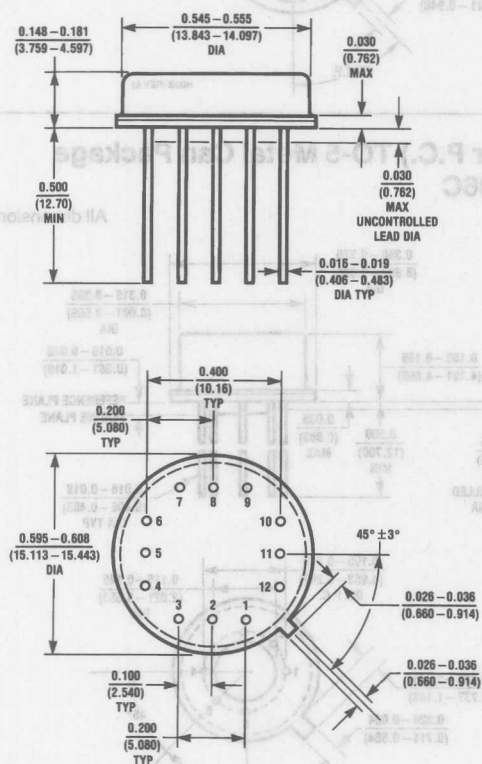
48 Lead Ceramic Leadless Chip Carrier, Type C NS Package Number E48A

All dimensions are in inches



12 Lead (0.400" Square Pattern) TO-8 Metal Can Package NS Package Number G12B

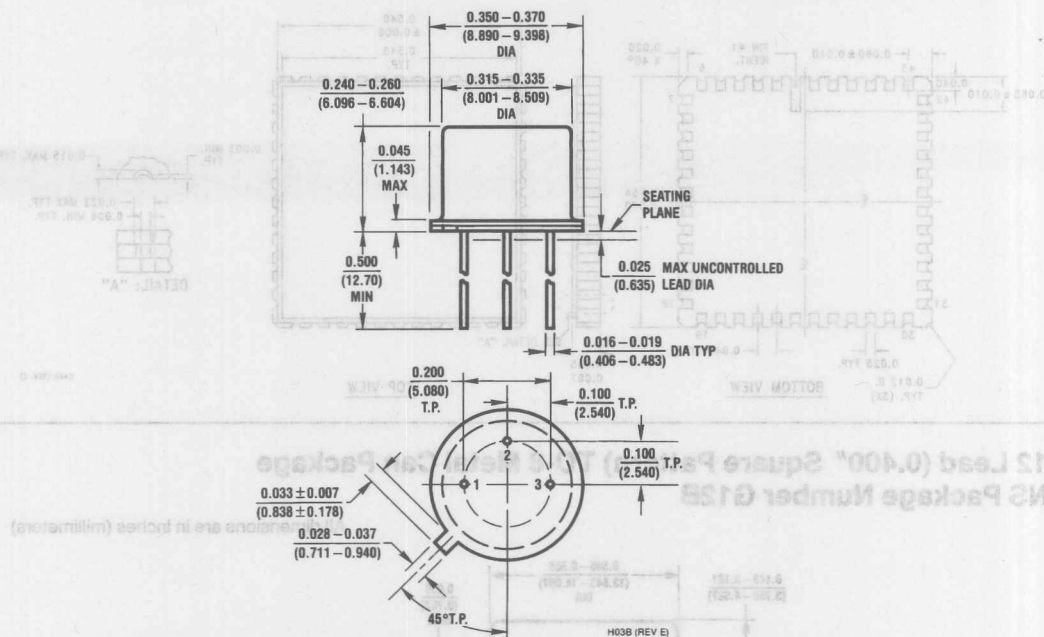
All dimensions are in inches (millimeters)



3 Lead (0.200" Diameter P.C.) TO-39 Metal Can Package, High Profile NS Package Number H03B

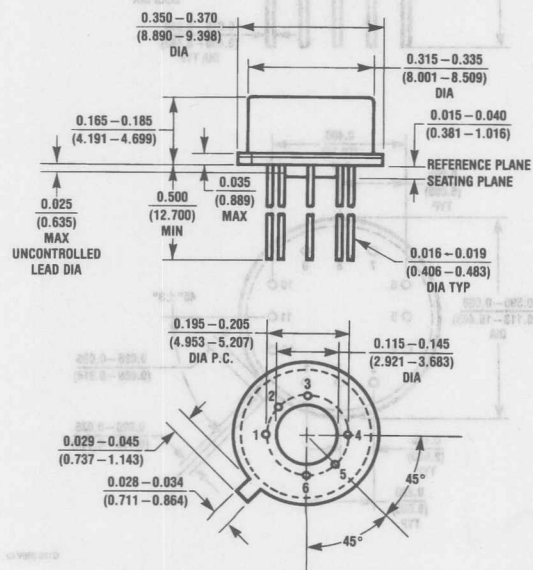
All dimensions are in inches (millimeters)

All dimensions are in inches (millimeters)



6 Lead (0.200" Diameter P.C.) TO-5 Metal Can Package NS Package Number H06C

All dimensions are in inches (millimeters)

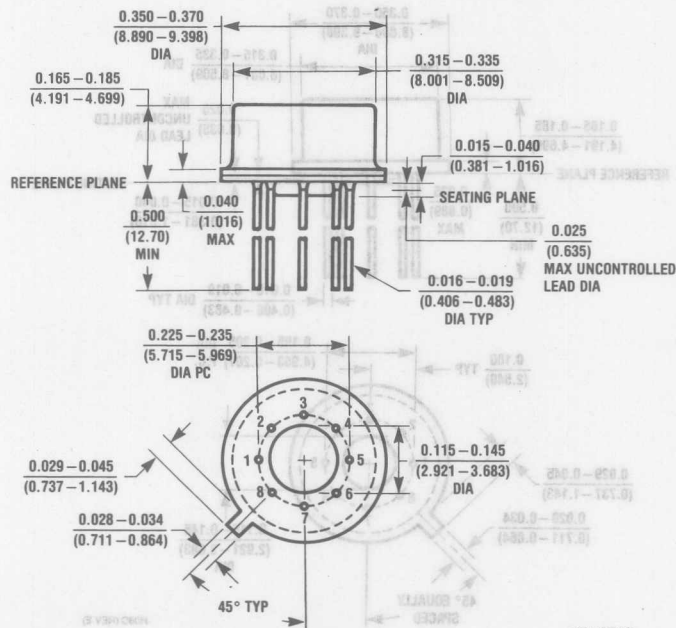


8 Lead (0.230" Diameter P.C.) TO-5 Metal Can Package

NS Package Number H08A

All dimensions are in inches (millimeters)

All dimensions are in inches (millimeters)



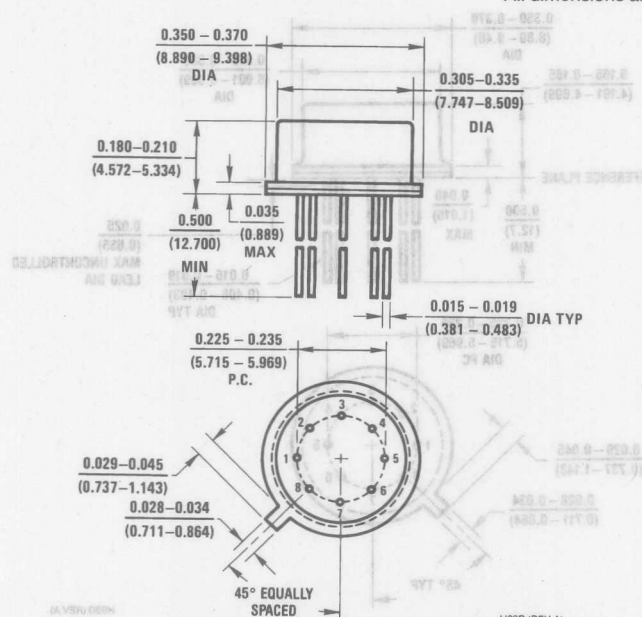
H08A (REV C)

8 Lead (0.230" Diameter P.C.) Metal Can Package

NS Package Number H08B

All dimensions are in inches (millimeters)

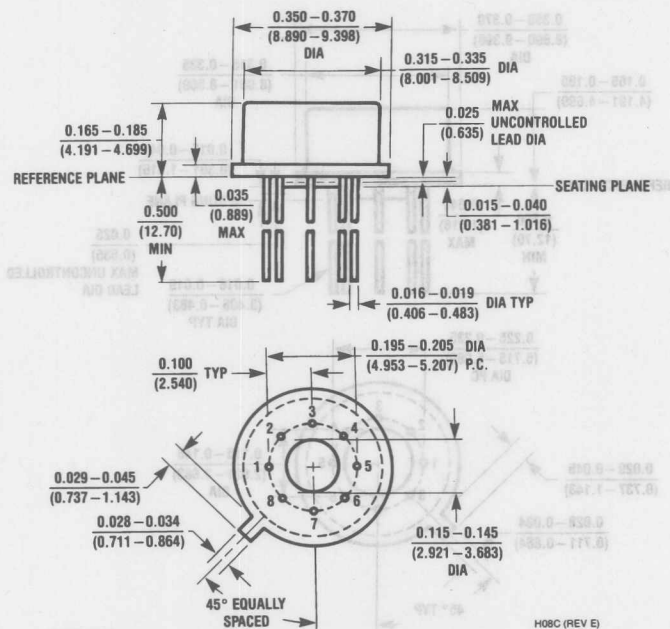
All dimensions are in inches (millimeters)



H08B (REV A)

(All dimensions are in inches (millimeters))

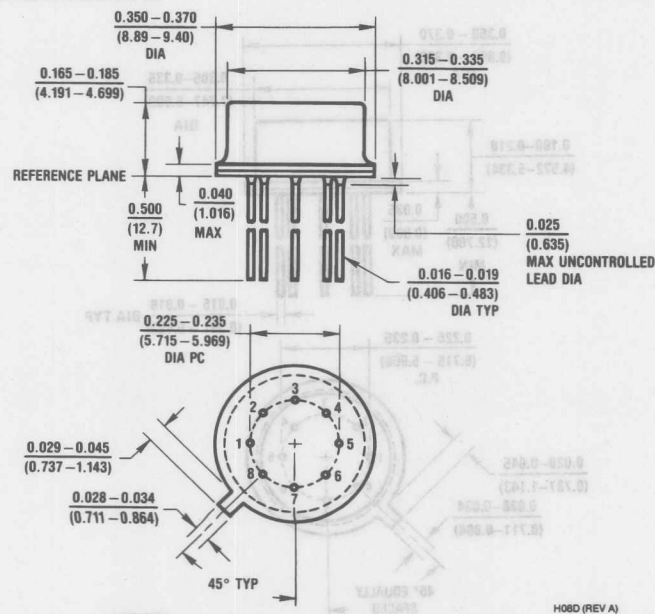
All dimensions are in inches (millimeters)



8 Lead (0.230" Diameter P.C.) Metal Can Package NS Package Number H08D

(All dimensions are in inches (millimeters))

All dimensions are in inches (millimeters)



Package

All dimensions are in inches (millimeters)

Physical Dimensions



NS Package Number H12B
12 Lead (0.400" Square Pad)

All dimensions are in inches (millimeters)

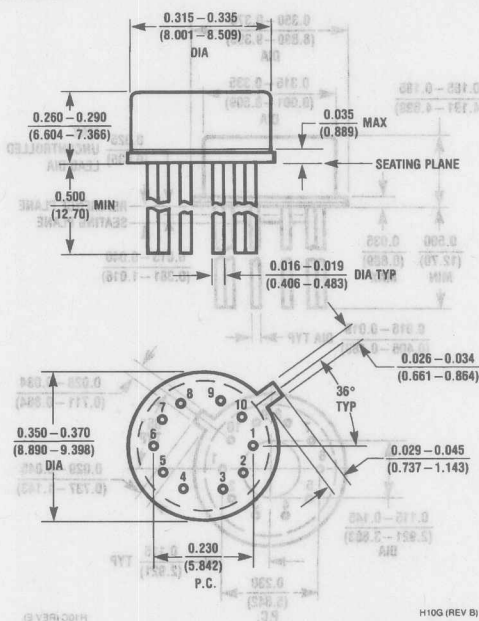


10 Lead (0.230" Diameter P.C.) Metal Can Package

NS Package Number H10G

All dimensions are in inches (millimeters)

All dimensions are in inches (millimeters)

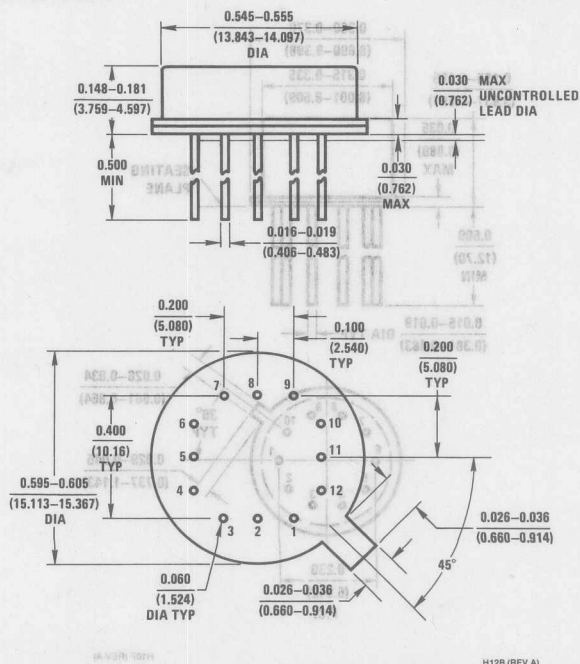


12 Lead (0.400" Square Pattern) Metal Can Package

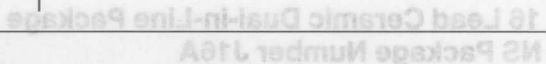
NS Package Number H12B

All dimensions are in inches (millimeters)

All dimensions are in inches (millimeters)



All dimensions are in inches



NS Package Number J16A

All dimensions are in inches

Technical drawing of a 4-pin connector assembly. The top view shows a rectangular body with a width of 0.400 MAX and a height of 0.220 to 0.291. It has four pins numbered 1 to 4. The side view shows a height of 0.310 MAX GLASS and a pin diameter of 0.045 TYP. The bottom view shows a pin pitch of 0.005 MIN and a pin diameter of 0.055 MAX BOTH ENDS. The drawing also includes a 90° ± 4° TYP angle and a 0.100 ± 0.010 TYP dimension.

0.400 MAX

0.220
0.291

0.310 MAX
GLASS

0.045 TYP
0.065 TYP

GLASS
SEALANT

0.005 MIN

0.055 MAX
BOTH ENDS

0.020
0.060

0.125
0.200

0.150 MIN

90° ± 4° TYP

0.018 ± 0.003 TYP

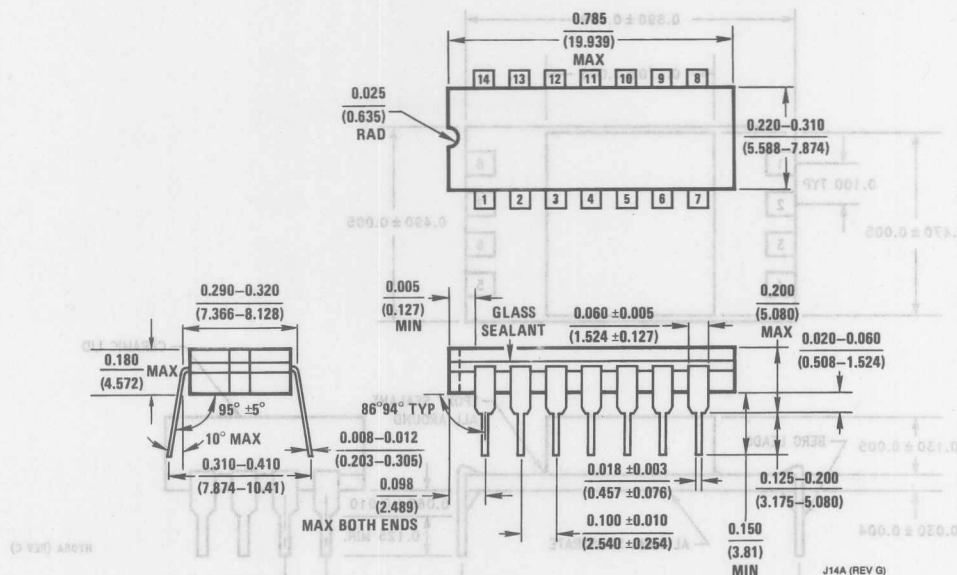
0.100 ± 0.010 TYP

JOBA (REV K)

14 Lead Ceramic Dual-in-Line Package NS Package Number J14A

All dimensions are in inches

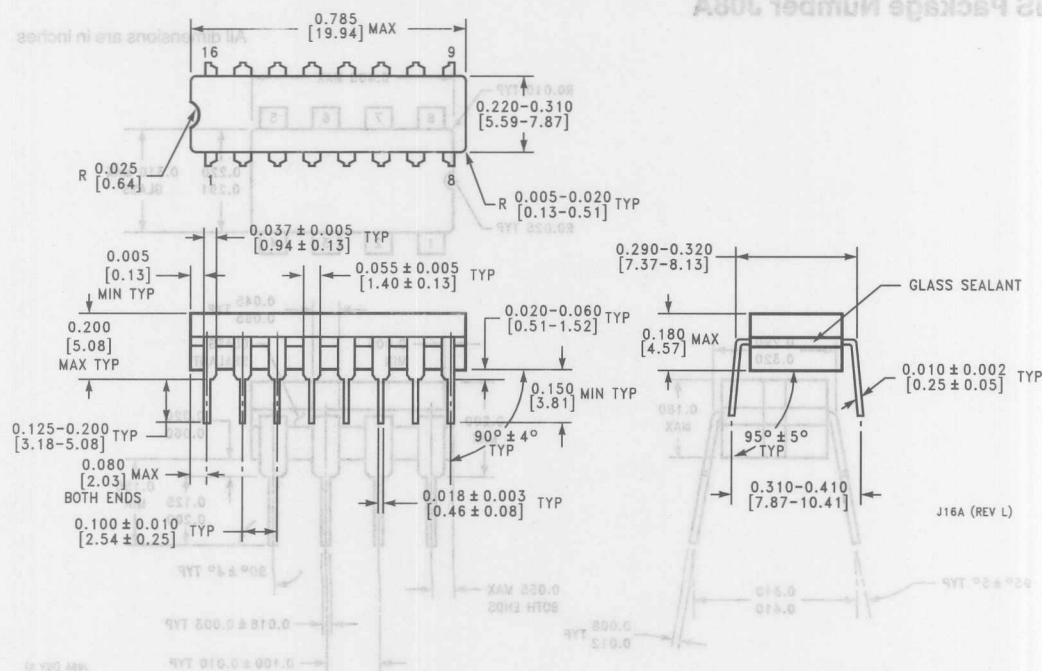
All dimensions are in inches (millimeters)



16 Lead Ceramic Dual-in-Line Package NS Package Number J16A

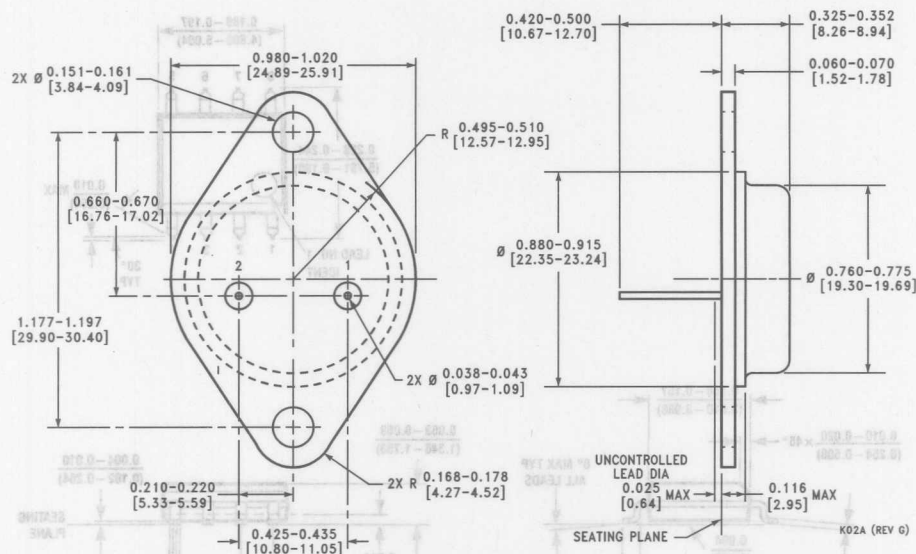
All dimensions are in inches

All dimensions are in inches [millimeters]



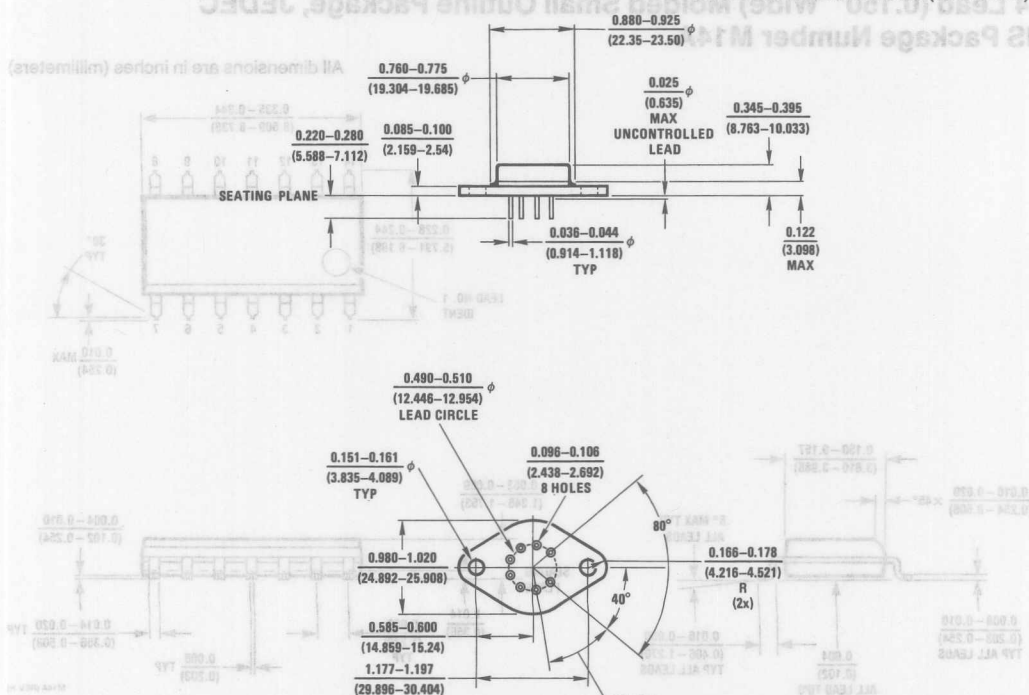
2 Lead TO-3 Metal Can Package NS Package Number K02A

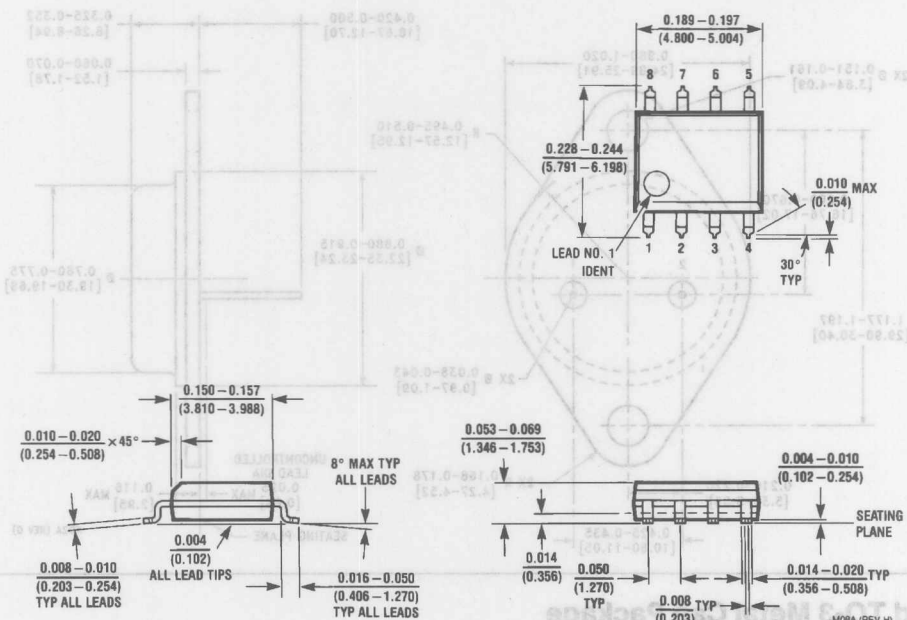
All dimensions are in inches (millimeters)



8 Lead TO-3 Metal Can Package NS Package Number K08A

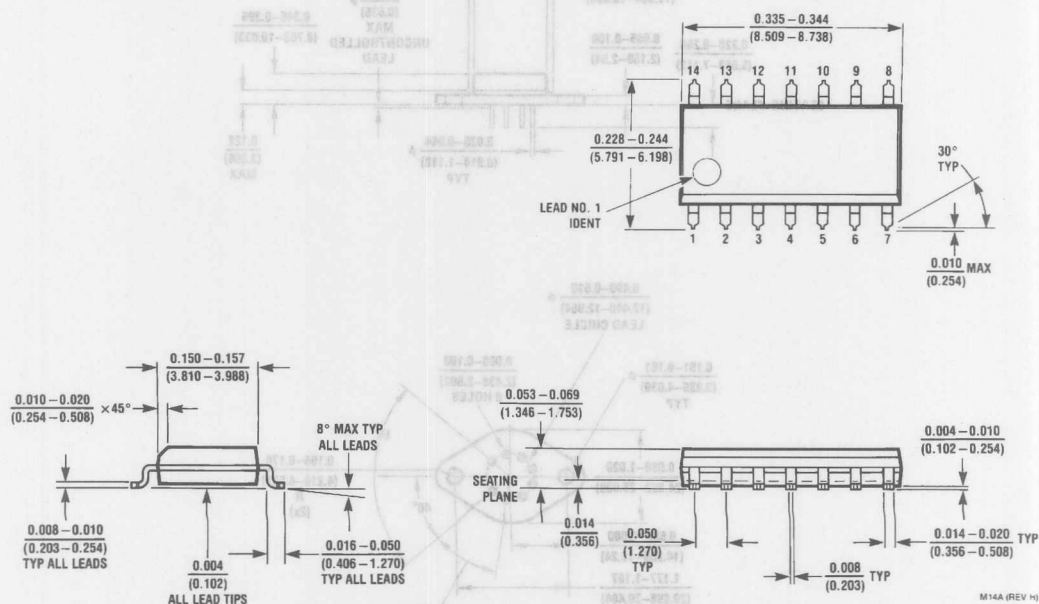
All dimensions are in inches (millimeters)





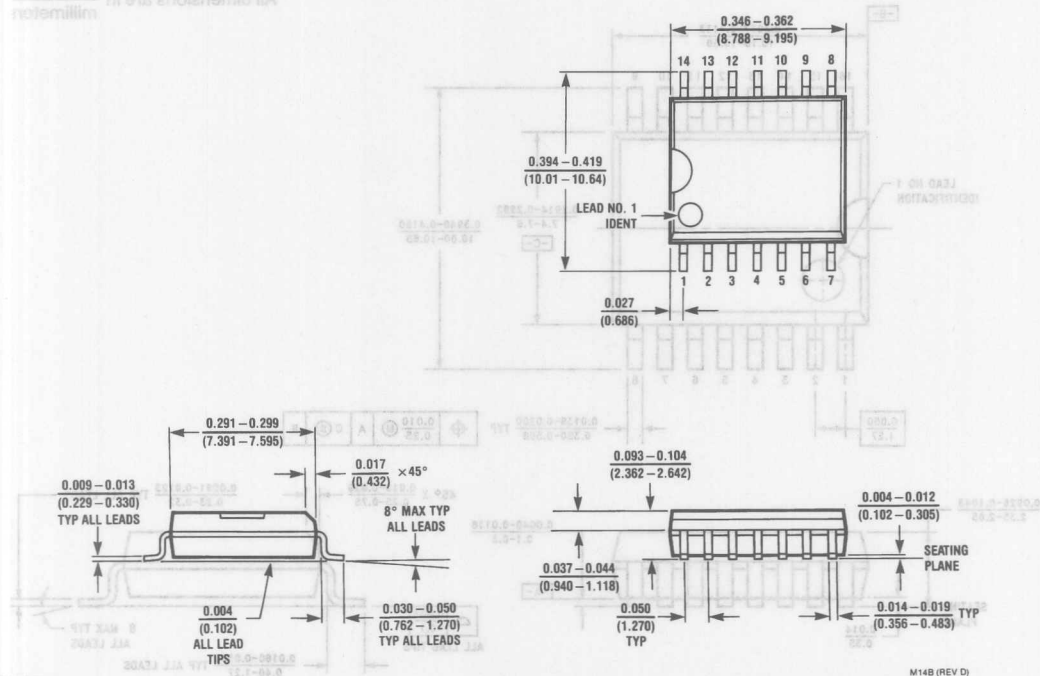
14 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M14A

All dimensions are in inches (millimeters)



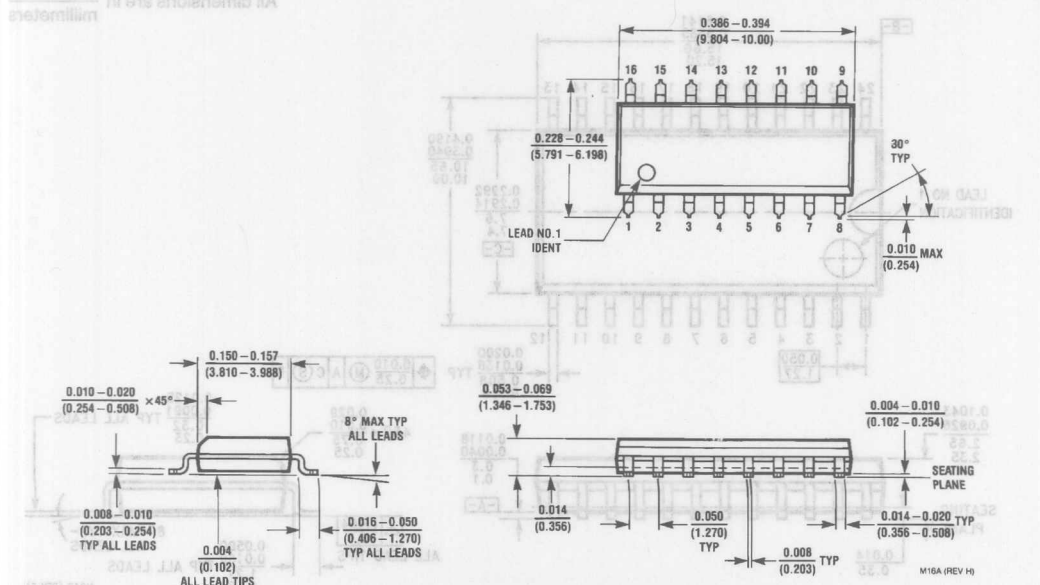
14 Lead (0.300" Wide) Molded Small Outline Package, JEDEC NS Package Number M14B

All dimensions are in inches (millimeters)

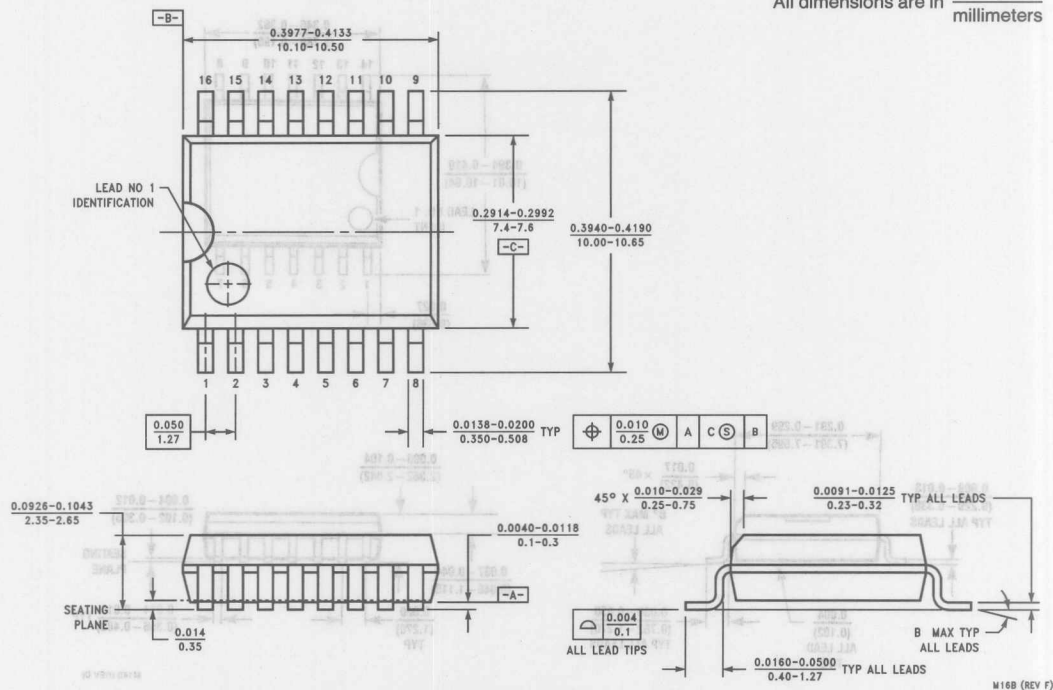


16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC NS Package Number M16A

All dimensions are in inches (millimeters)



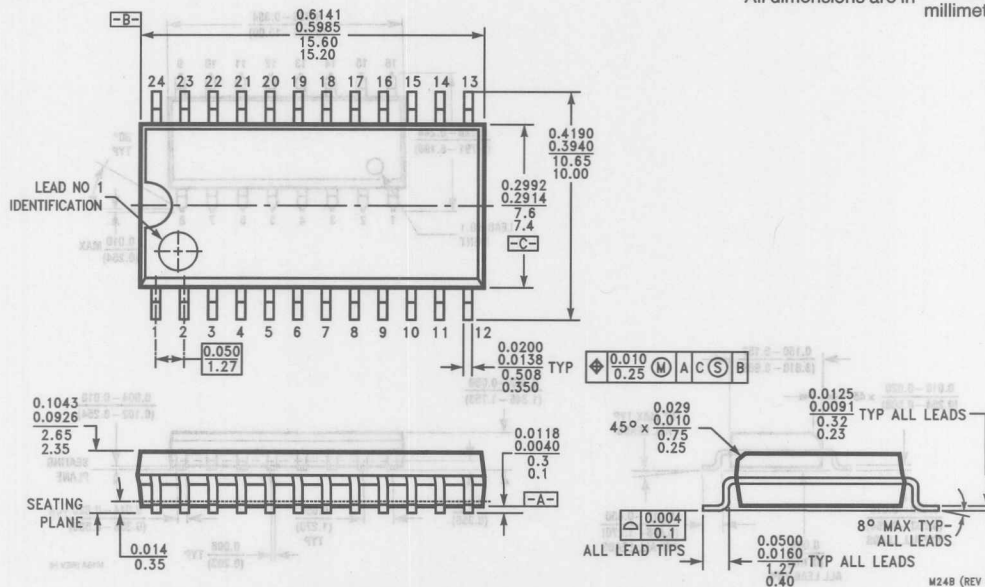
All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



M16B (REV F)

**24 Lead (0.300" Wide) Molded Small Outline Package, JEDEC
NS Package Number M24B**

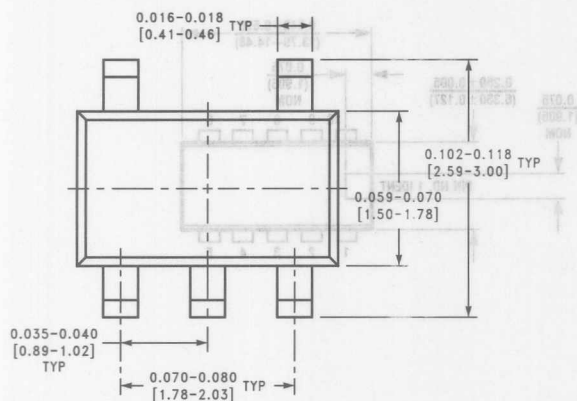
All dimensions are in $\frac{\text{inches}}{\text{millimeters}}$



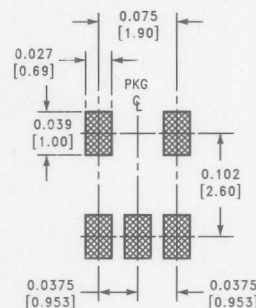
M24B (REV F

5 Lead Molded SOT-23-5 NS Package Number MA05A

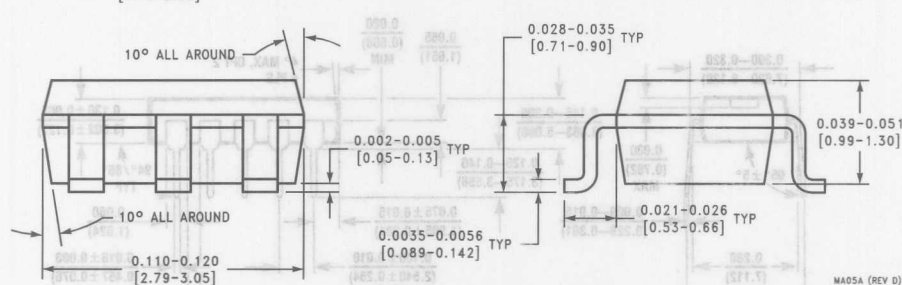
All dimensions are in inches [millimeters]



All dimensions are in inches [millimeters]



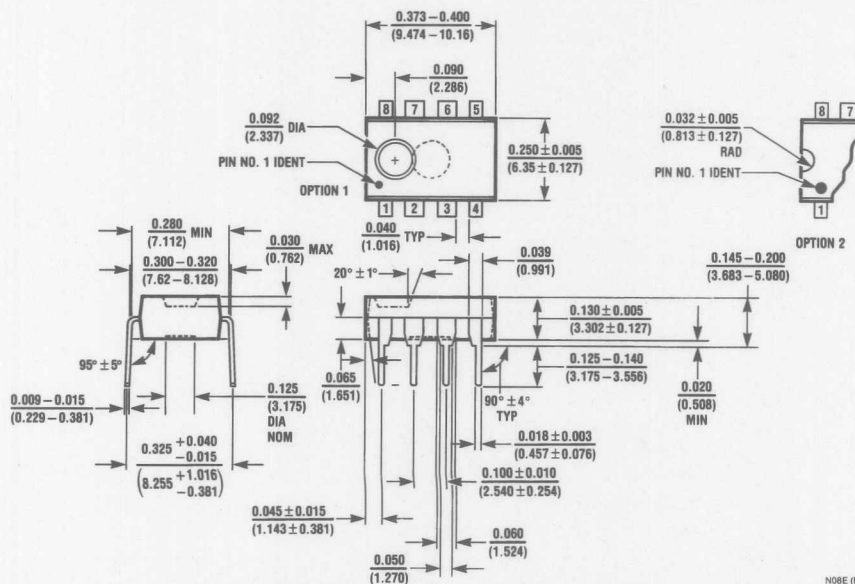
LAND PATTERN RECOMMENDATION



MA05A (REV D)

8 Lead (0.300" Wide) Molded Dual-in-Line Package NS Package Number N08E

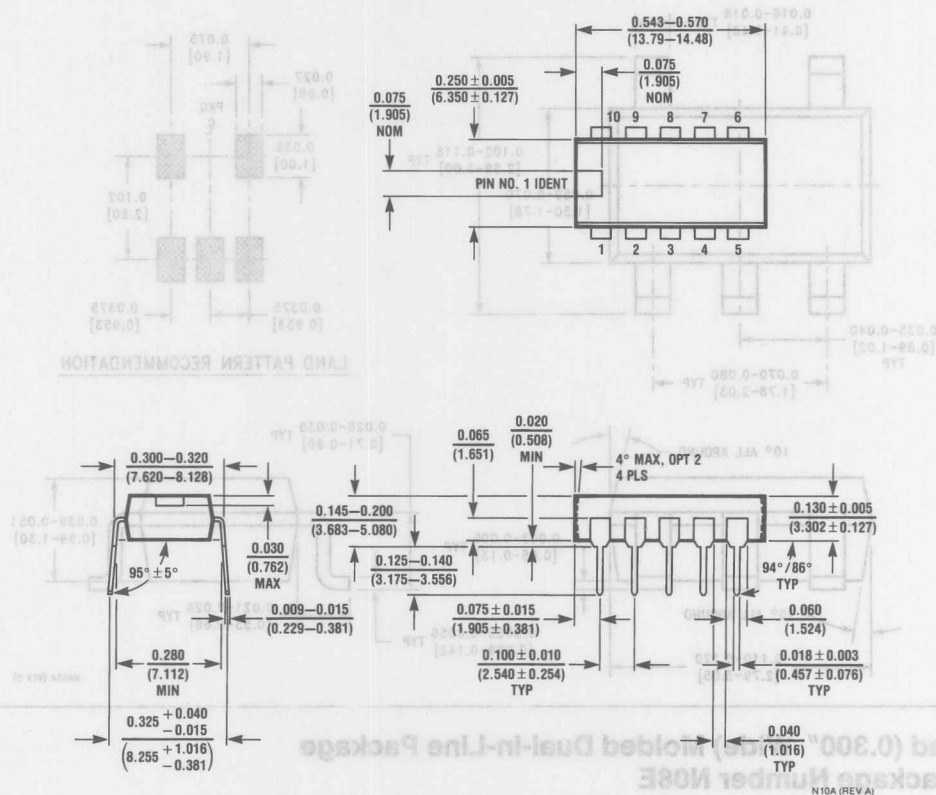
All dimensions are in inches (millimeters)



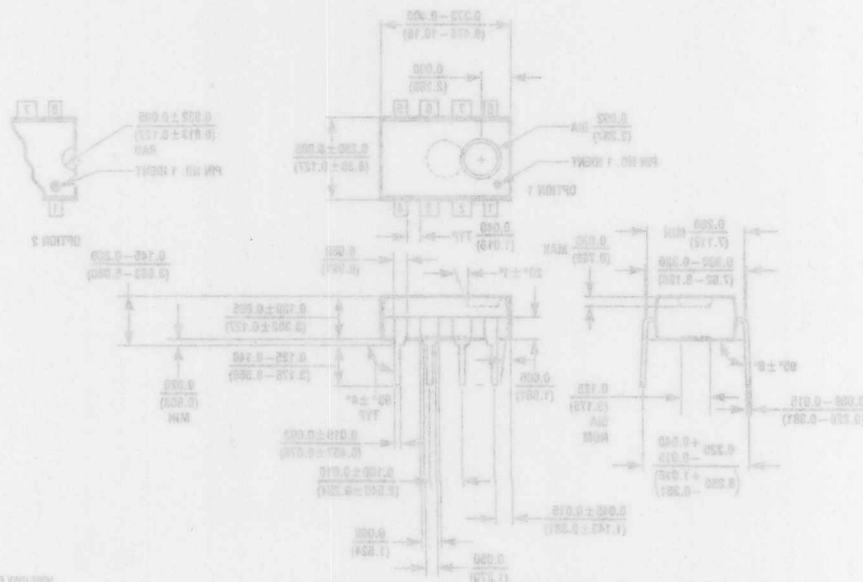
N08E (REV F)

All dimensions are in inches (millimeters)

All dimensions are in inches (millimeters)



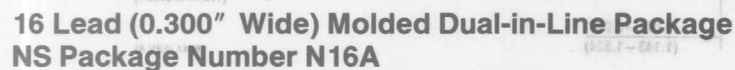
All dimensions are in inches (millimeters)



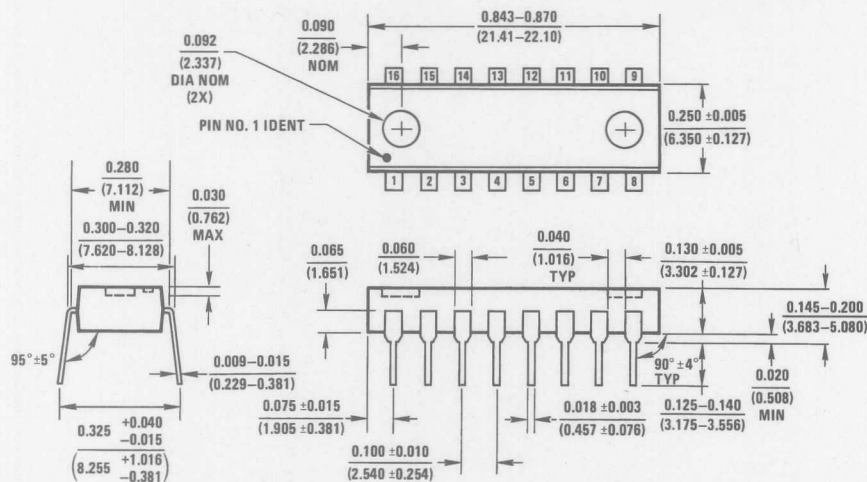
4 Lead Molded TO-202
NS Package Number P04A

All dimensions are in inches (millimeters)

7



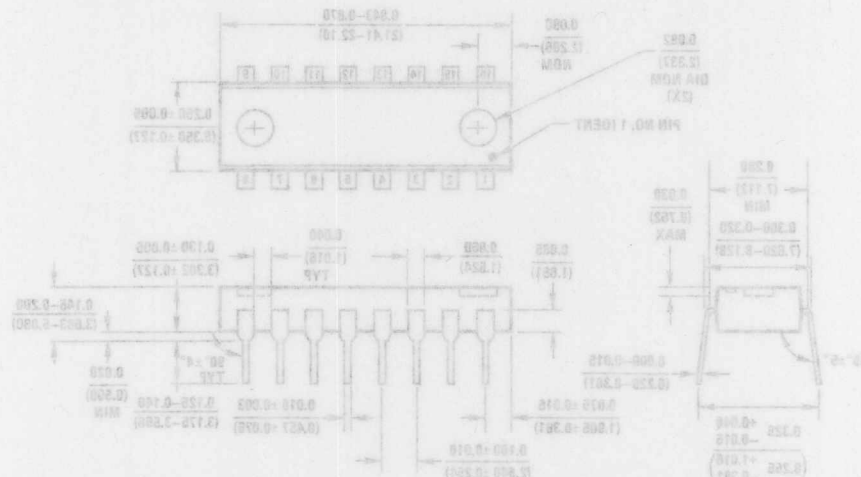
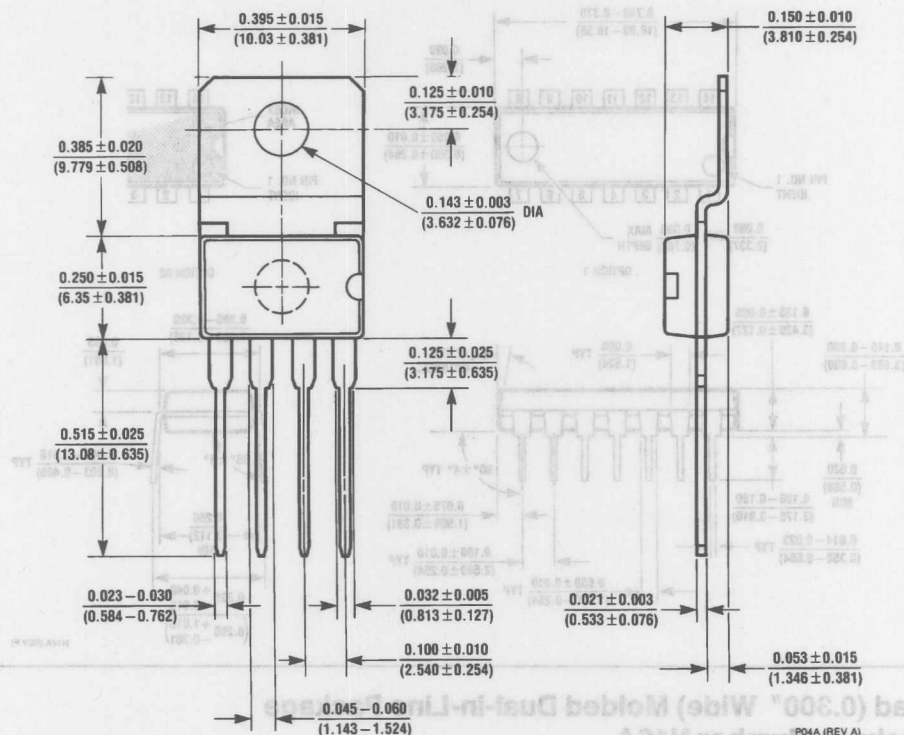
All dimensions are in inches (millimeters)



N16A (REV E)

4 Lead Molded TO-202 NS Package Number P04A

All dimensions are in inches (millimeters)



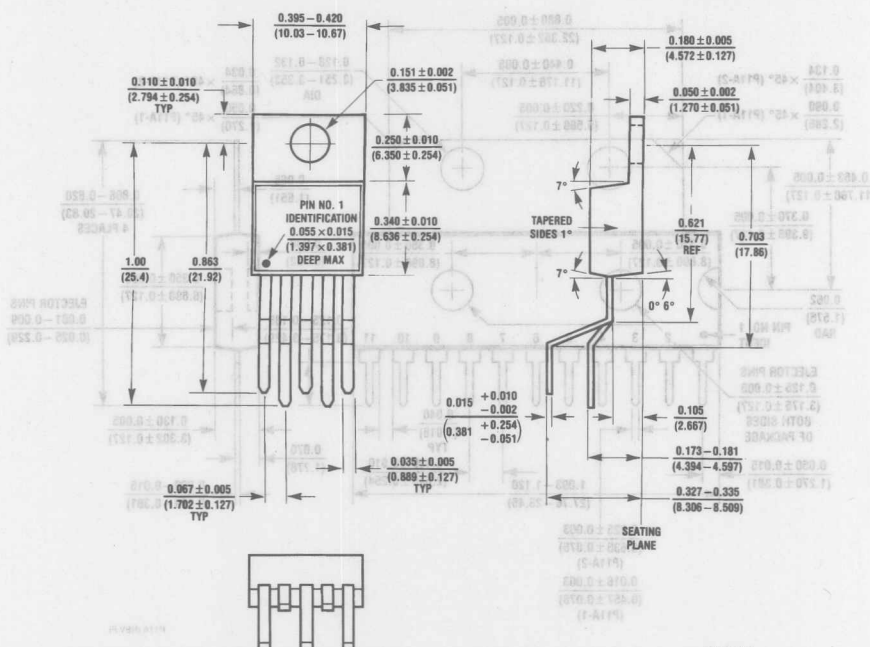
All dimensions are in inches (millimeters)



All dimensions are in inches [millimeters]



**5 Lead Molded TO-220
NS Package Number T05B**

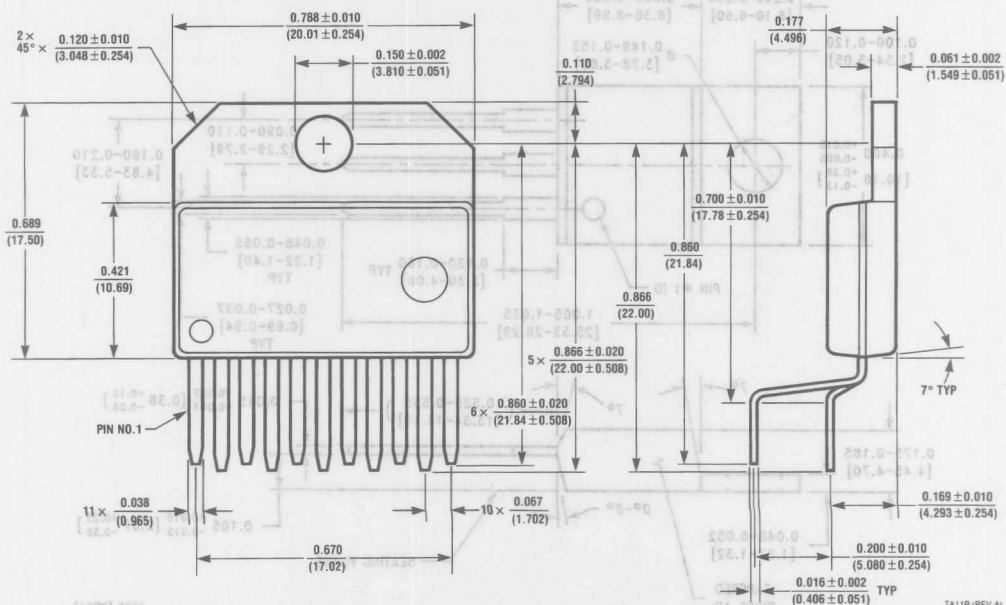


T058 (REV F)

**11 Lead Molded TO-220
NS Package Number TA11B**

101 Package Number 1A1

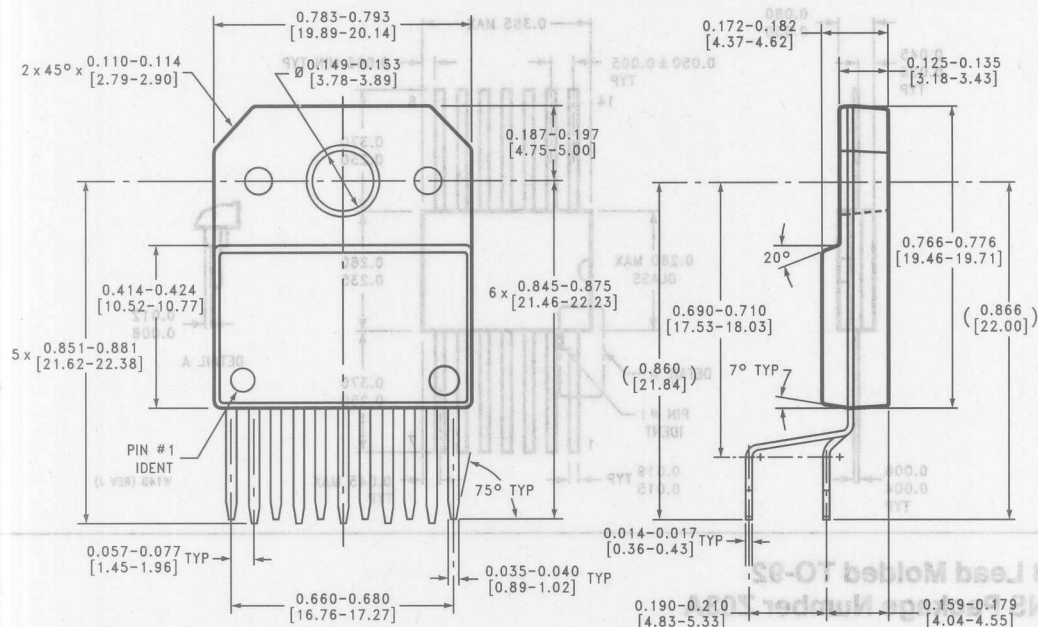
All dimensions are in inches (millimeters)



TA11B (REV. A)

11 Lead Molded TO-220 NS Package Number TF11B

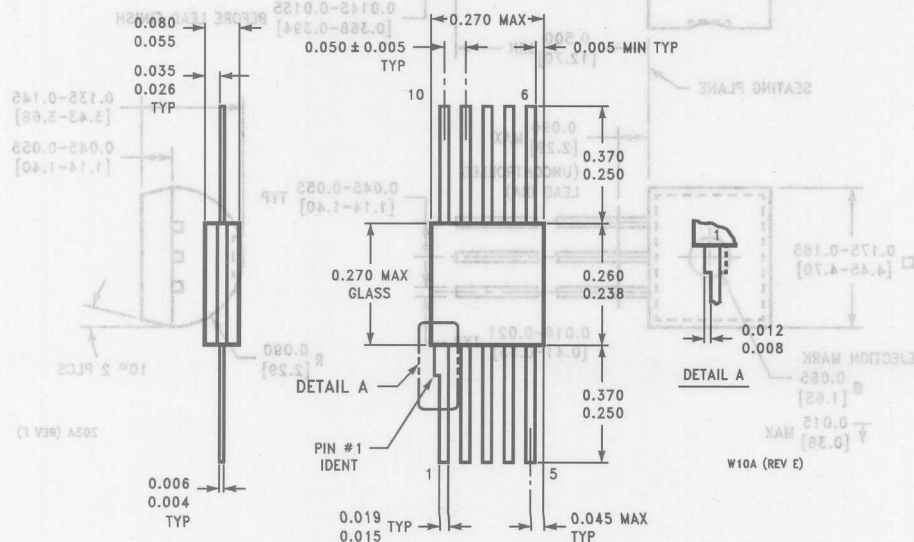
All dimensions are in inches



TF11B (REV C)

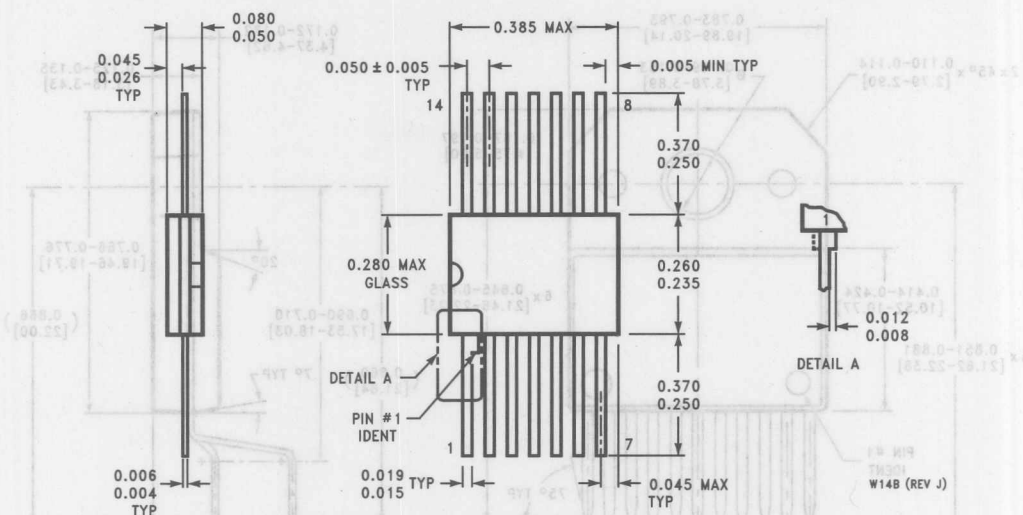
10 Lead Cerpack NS Package Number W10A

All dimensions are in inches



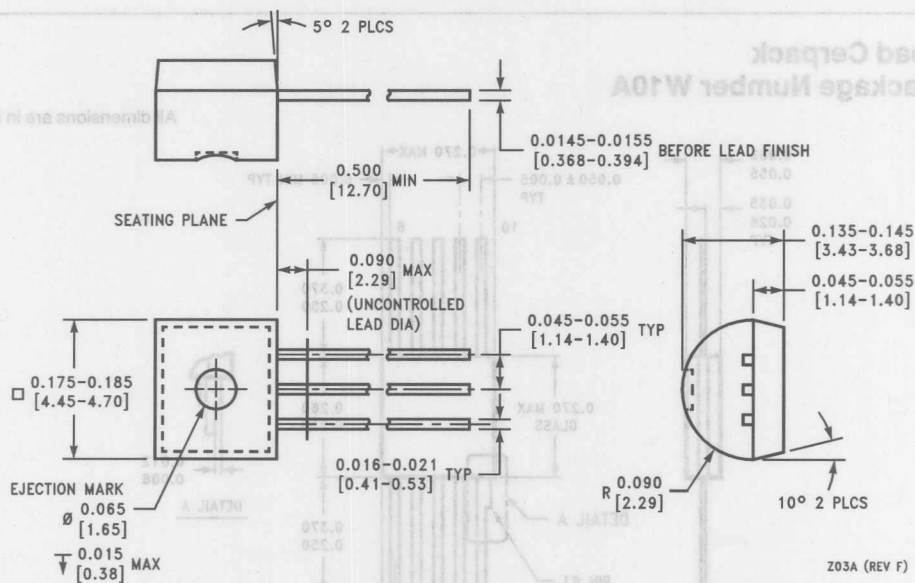
**14 Lead Ceramic Flatpack
NS Package Number W14B**

All dimensions are in inches



**3 Lead Molded TO-92
NS Package Number Z03A**

All dimensions are in inches [millimeters]





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ADVANCED BiCMOS LOGIC (ABTC, IBF, BiCMOS SCAN, LOW VOLTAGE BiCMOS, EXTENDED TTL TECHNOLOGY) DATABOOK—1994

ABTC/BCT Description and Family Characteristics • ABTC/BCT Ratings, Specifications and Waveforms
ABTC Applications and Design Considerations • Quality and Reliability • Integrated Bus Function (IBF) Introduction
54/74ABT3283 Synchronous Datapath Multiplexer • 74FR900/25900 9-Bit 3-Port Latchable Datapath Multiplexer
54/74ACTQ3283 32-Bit Latchable Transceiver with Parity Generator/Checker and Byte Multiplexing
SCAN18xxxA BiCMOS 5V Logic with Boundary Scan • 74LVT Low Voltage BiCMOS Logic
VME Extended TTL Technology for Backplanes

ALS/AS LOGIC DATABOOK—1990

Introduction to Advanced Bipolar Logic • Advanced Low Power Schottky • Advanced Schottky

APPLICATION SPECIFIC ANALOG PRODUCTS DATABOOK—1995

Audio Circuits • Video Circuits • Automotive • Special Functions • Surface Mount

ASIC DESIGN MANUAL/GATE ARRAYS & STANDARD CELLS—1987

SSI/MSI Functions • Peripheral Functions • LSI/VLSI Functions • Design Guidelines • Packaging

CMOS LOGIC DATABOOK—1988

CMOS AC Switching Test Circuits and Timing Waveforms • CMOS Application Notes • MM54HC/MM74HC
MM54HCT/MM74HCT • CD4XXX • MM54CXXX/MM74CXXX • Surface Mount

CLOCK GENERATION AND SUPPORT (CGS) DESIGN DATABOOK—1994

Low Skew Clock Buffers/Drivers • Video Clock Generators • Low Skew PLL Clock Generators
Crystal Clock Generators

COP8™ DATABOOK—1994

COP8 Family • COP8 Applications • MICROWIRE/PLUS Peripherals • COP8 Development Support

CROSSVOLT™ LOW VOLTAGE LOGIC SERIES DATABOOK—1994

LCX Family • LVX Translator Family • LVX Bus Switch Family • LVX Family • LVQ Family • LVT Family

DATA ACQUISITION DATABOOK—1995

Data Acquisition Systems • Analog-to-Digital Converters • Digital-to-Analog Converters • Voltage References
Temperature Sensors • Active Filters • Analog Switches/Multiplexers • Surface Mount

DATA ACQUISITION DATABOOK SUPPLEMENT—1992

New devices released since the printing of the 1989 Data Acquisition Linear Devices Databook.

DRAM MANAGEMENT HANDBOOK—1993

Dynamic Memory Control • CPU Specific System Solutions • Error Detection and Correction
Microprocessor Applications

EMBEDDED CONTROLLERS DATABOOK—1992

COP400 Family • COP800 Family • COPS Applications • HPC Family • HPC Applications
MICROWIRE and MICROWIRE/PLUS Peripherals • Microcontroller Development Tools

FDDI DATABOOK—1994

Datasheets • Application Notes

F100K ECL LOGIC DATABOOK & DESIGN GUIDE—1992

Family Overview • 300 Series (Low-Power) Datasheets • 100 Series Datasheets • 11C Datasheets
Design Guide • Circuit Basics • Logic Design • Transmission Line Concepts • System Considerations
Power Distribution and Thermal Considerations • Testing Techniques • 300 Series Package Qualification
Quality Assurance and Reliability • Application Notes

FACT™ ADVANCED CMOS LOGIC DATABOOK—1993

Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations • 54AC/74ACXXX • 54ACT/74ACTXXX • Quiet Series: 54ACQ/74ACQXXX
Quiet Series: 54ACTQ/74ACTQXXX • 54FCT/74FCTXXX • FCTA: 54FCTXXXA/74FCTXXXA/B

FAST® ADVANCED SCHOTTKY TTL LOGIC DATABOOK—1990

Circuit Characteristics • Ratings, Specifications and Waveforms • Design Considerations • 54F/74FXXX

FAST® APPLICATIONS HANDBOOK—1990

Reprint of 1987 Fairchild FAST Applications Handbook

Contains application information on the FAST family: Introduction • Multiplexers • Decoders • Encoders
Operators • FIFOs • Counters • TTL Small Scale Integration • Line Driving and System Design
FAST Characteristics and Testing • Packaging Characteristics

HIGH-PERFORMANCE BUS INTERFACE DATABOOK—1994

QuickRing • Futurebus+ /BTL Devices • BTL Transceiver Application Notes • Futurebus+ Application Notes
High Performance TTL Bus Drivers • PI-Bus • Futurebus+ /BTL Reference

IBM DATA COMMUNICATIONS HANDBOOK—1992

IBM Data Communications • Application Notes

INTERFACE: DATA TRANSMISSION DATABOOK—1994

TIA/EIA-232 (RS-232) • TIA/EIA-422/423 • TIA/EIA-485 • Line Drivers • Receivers • Repeaters
Transceivers • Low Voltage Differential Signaling • Special Interface • Application Notes

LINEAR APPLICATIONS HANDBOOK—1994

The purpose of this handbook is to provide a fully indexed and cross-referenced collection of linear integrated circuit applications using both monolithic and hybrid circuits from National Semiconductor.

Individual application notes are normally written to explain the operation and use of one particular device or to detail various methods of accomplishing a given function. The organization of this handbook takes advantage of this innate coherence by keeping each application note intact, arranging them in numerical order, and providing a detailed Subject Index.

LOCAL AREA NETWORKS DATABOOK—1993 SECOND EDITION

Integrated Ethernet Network Interface Controller Products • Ethernet Physical Layer Transceivers
Ethernet Repeater Interface Controller Products • Token-Ring Interface Controller (TROPIC)
Hardware and Software Support Products • FDDI Products • Glossary and Acronyms

LOW VOLTAGE DATABOOK—1992

This databook contains information on National's expanding portfolio of low and extended voltage products. Product datasheets included for: Low Voltage Logic (LVQ), Linear, EPROM, EEPROM, SRAM, Interface, ASIC, Embedded Controllers, Real Time Clocks, and Clock Generation and Support (CGS).

MASS STORAGE HANDBOOK—1989

Rigid Disk Pulse Detectors • Rigid Disk Data Separators/Synchronizers and ENDECs
Rigid Disk Data Controller • SCSI Bus Interface Circuits • Floppy Disk Controllers • Disk Drive Interface Circuits
Rigid Disk Preamplifiers and Servo Control Circuits • Rigid Disk Microcontroller Circuits • Disk Interface Design Guide

MEMORY DATABOOK—1994

FLASH • CMOS EPROMs • CMOS EEPROMs • PROMs • Application Notes

MEMORY APPLICATIONS HANDBOOK—1994

FLASH • EEPROMs • EPROMs • Application Notes

OPERATIONAL AMPLIFIERS DATABOOK—1995

Operational Amplifiers • Buffers • Voltage Comparators • Active Matrix/LCD Display Drivers
Special Functions • Surface Mount

PACKAGING DATABOOK—1993

Introduction to Packaging • Hermetic Packages • Plastic Packages • Advanced Packaging Technology
Package Reliability Considerations • Packing Considerations • Surface Mount Considerations

POWER IC's DATABOOK—1995

Linear Voltage Regulators • Low Dropout Voltage Regulators • Switching Voltage Regulators
Motion Control • Surface Mount

PROGRAMMABLE LOGIC DEVICE DATABOOK AND DESIGN GUIDE—1993

Product Line Overview • Datasheets • Design Guide: Designing with PLDs • PLD Design Methodology
PLD Design Development Tools • Fabrication of Programmable Logic • Application Examples

REAL TIME CLOCK HANDBOOK—1993

3-Volt Low Voltage Real Time Clocks • Real Time Clocks and Timer Clock Peripherals • Application Notes

RELIABILITY HANDBOOK—1987

Reliability and the Die • Internal Construction • Finished Package • MIL-STD-883 • MIL-M-38510
The Specification Development Process • Reliability and the Hybrid Device • VLSI/VHSIC Devices
Radiation Environment • Electrostatic Discharge • Discrete Device • Standardization
Quality Assurance and Reliability Engineering • Reliability and Documentation • Commercial Grade Device
European Reliability Programs • Reliability and the Cost of Semiconductor Ownership
Reliability Testing at National Semiconductor • The Total Military/Aerospace Standardization Program
883B/RETSM Products • MILS/RETSM Products • 883/RETSM Hybrids • MIL-M-38510 Class B Products
Radiation Hardened Technology • Wafer Fabrication • Semiconductor Assembly and Packaging
Semiconductor Packages • Glossary of Terms • Key Government Agencies • AN/ Numbers and Acronyms
Bibliography • MIL-M-38510 and DESC Drawing Cross Listing

SCANTM DATABOOK—1994

Evolution of IEEE 1149.1 Standard • SCAN BiCMOS Products • SCAN CMOS Products • System Test Products
Other IEEE 1149.1 Devices

TELECOMMUNICATIONS—1994

COMBO and SLIC Devices • ISDN • Digital Loop Devices • Analog Telephone Components • Software • Application Notes

VHC/VHCT ADVANCED CMOS LOGIC DATABOOK—1993

This databook introduces National's Very High Speed CMOS (VHC) and Very High Speed TTL Compatible CMOS (VHCT) designs. The databook includes Description and Family Characteristics • Ratings, Specifications and Waveforms
Design Considerations and Product Datasheets. The topics discussed are the advantages of VHC/VHCT AC Performance, Low Noise Characteristics and Improved Interface Capabilities.

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